



# FDMS86350

## N-Channel PowerTrench<sup>®</sup> MOSFET

80 V, 130 A, 2.4 mΩ

### Features

- Max  $r_{DS(on)}$  = 2.4 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 25\text{ A}$
- Max  $r_{DS(on)}$  = 3.2 mΩ at  $V_{GS} = 8\text{ V}$ ,  $I_D = 22\text{ A}$
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

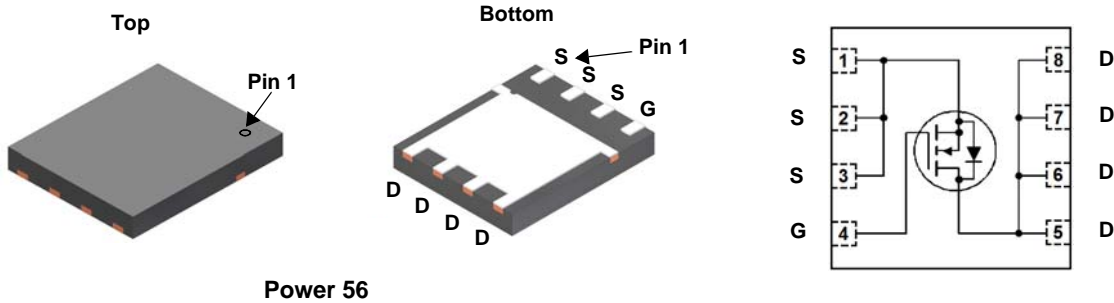


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench<sup>®</sup> process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Applications

- Primary MOSFET
- Synchronous Rectifier
- Load Switch
- Motor Control Switch



Power 56

### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	80	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	$T_C = 25\text{ °C}$	130
	-Continuous	$T_A = 25\text{ °C}$ (Note 1a)	25
	-Pulsed	(Note 4)	300
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	864
$P_D$	Power Dissipation	$T_C = 25\text{ °C}$	156
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1a)	2.7
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	45	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86350	FDMS86350	Power 56	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		45		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 64\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.5	3.8	4.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-12		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$		2.0	2.4	m $\Omega$
		$V_{GS} = 8\text{ V}, I_D = 22\text{ A}$		2.5	3.2	
		$V_{GS} = 10\text{ V}, I_D = 25\text{ A}, T_J = 125\text{ }^\circ\text{C}$		3.1	3.8	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 25\text{ A}$		70		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		8030	10680	pF
$C_{oss}$	Output Capacitance			1370	1825	pF
$C_{rss}$	Reverse Transfer Capacitance			31	50	pF
$R_g$	Gate Resistance		0.1	1.1	3	$\Omega$

### Switching Characteristics

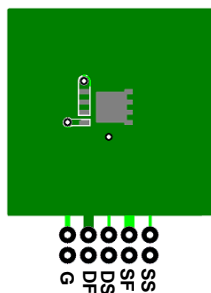
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{ V}, I_D = 25\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		50	80	ns	
$t_r$	Rise Time			34	55	ns	
$t_{d(off)}$	Turn-Off Delay Time			40	65	ns	
$t_f$	Fall Time			11	20	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		110	155	nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } 8\text{ V}$	$V_{DD} = 40\text{ V},$ $I_D = 25\text{ A}$		90	127
$Q_{gs}$	Gate to Source Charge				46		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				23		nC

### Drain-Source Diode Characteristics

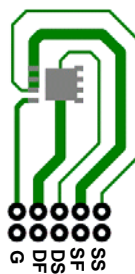
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.71	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 25\text{ A}$ (Note 2)		0.79	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 25\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		63	101	ns
$Q_{rr}$	Reverse Recovery Charge			62	100	nC

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 45  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



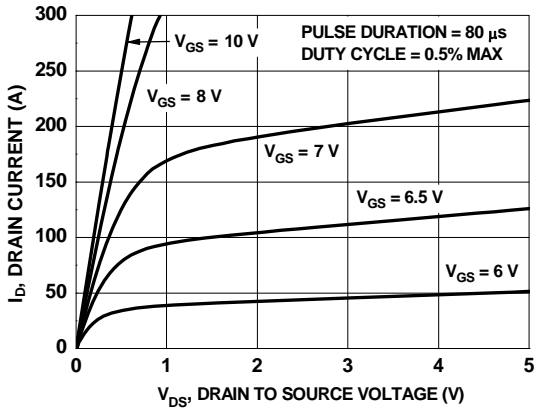
b. 115  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

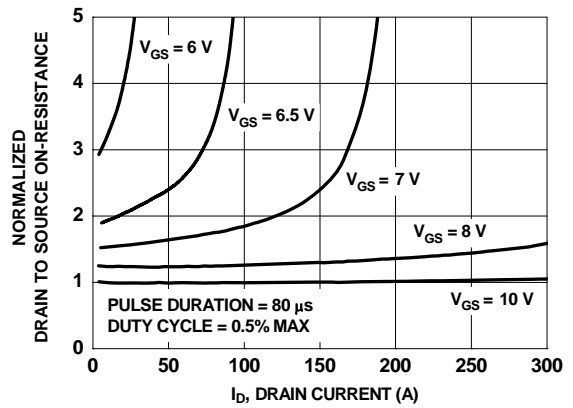
3.  $E_{AS}$  of 864 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 24\text{ A}$ ,  $V_{DD} = 80\text{ V}$ ,  $V_{GS} = 10\text{ V}$ , 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 74\text{ A}$ .

4. Pulse Id limited by junction temperature,  $t_d \leq 100\text{ }\mu\text{s}$ , please refer to SOA curve for more details.

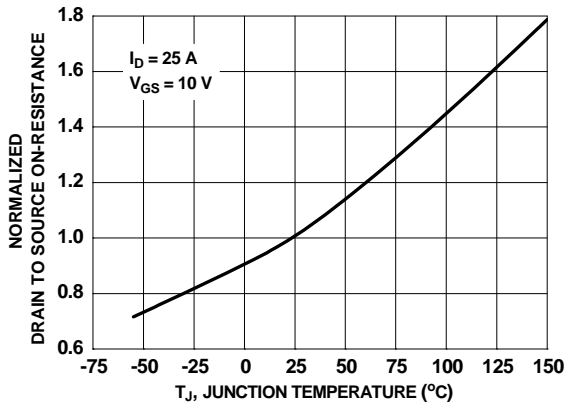
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



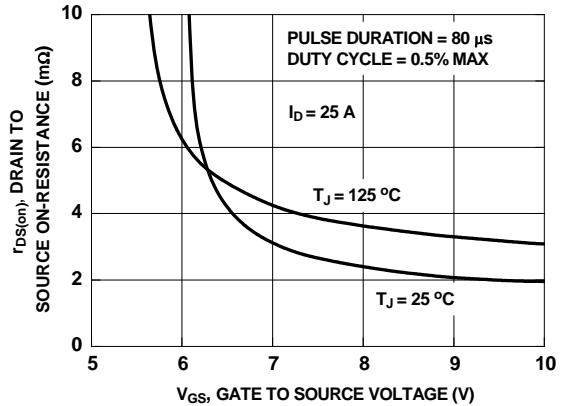
**Figure 1. On-Region Characteristics**



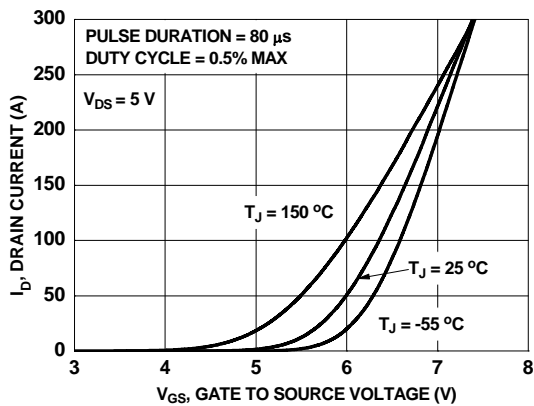
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



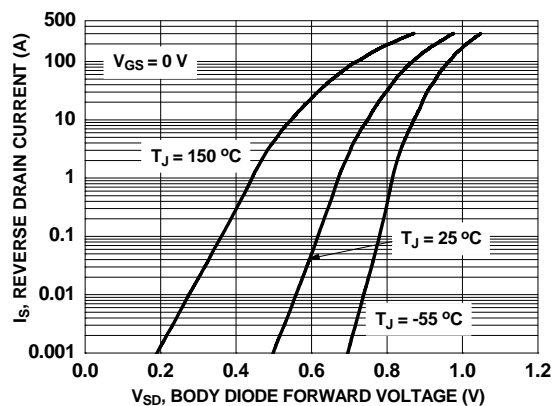
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

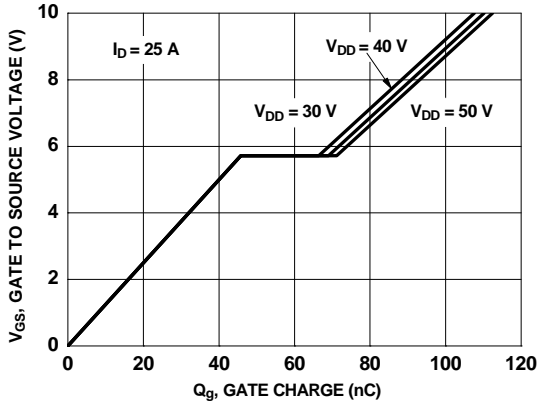


**Figure 5. Transfer Characteristics**

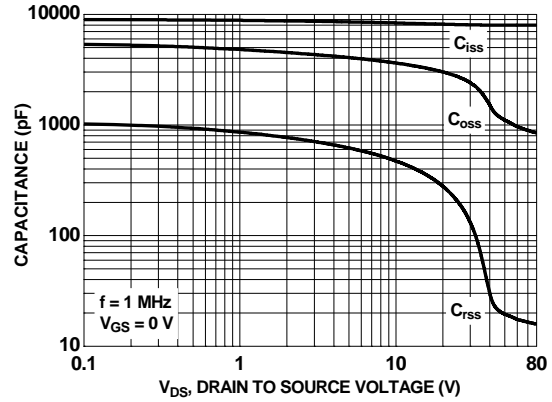


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

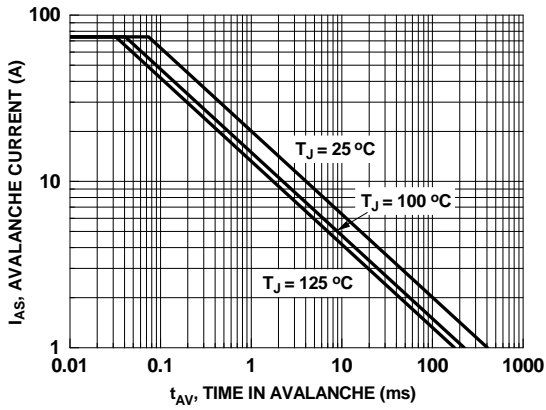
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



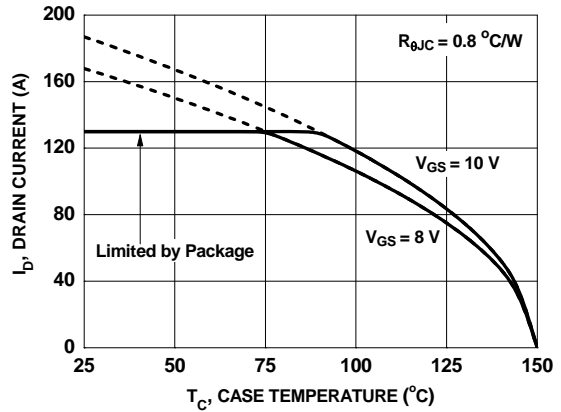
**Figure 7. Gate Charge Characteristics**



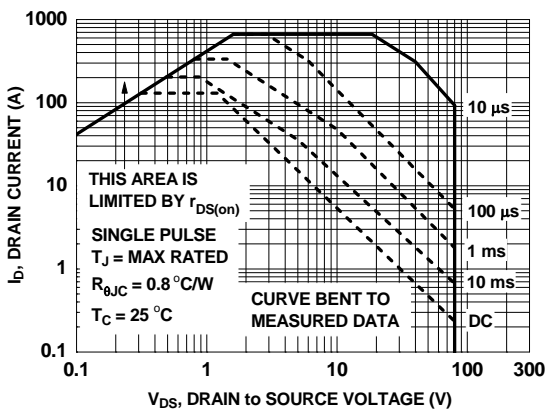
**Figure 8. Capacitance vs Drain to Source Voltage**



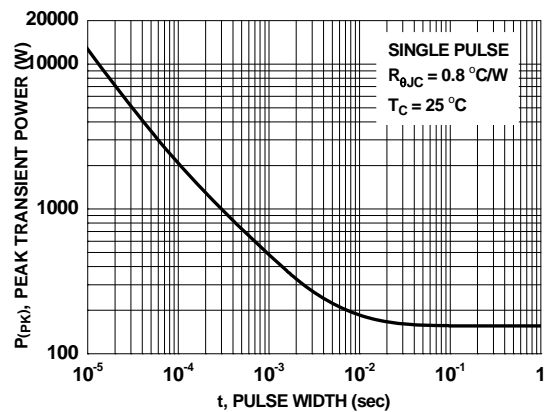
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

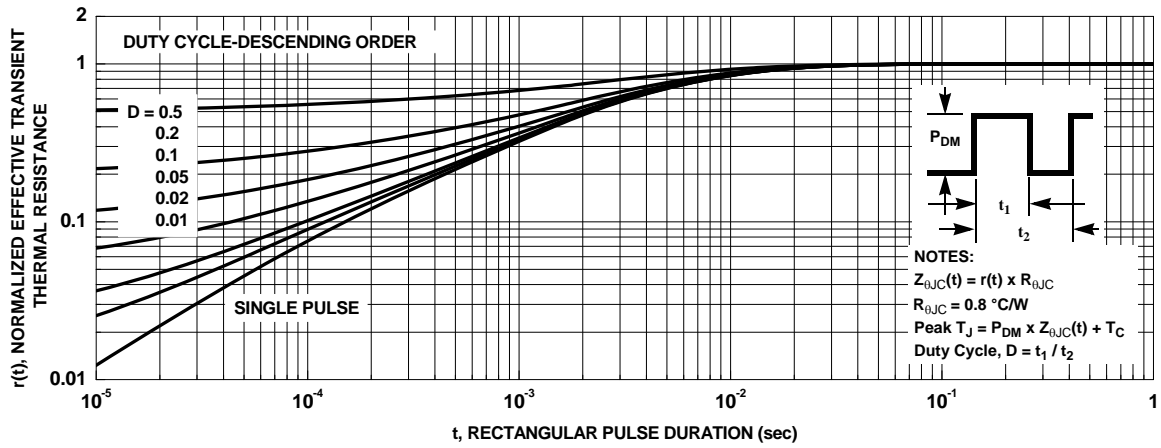


**Figure 11. Forward Bias Safe Operating Area**

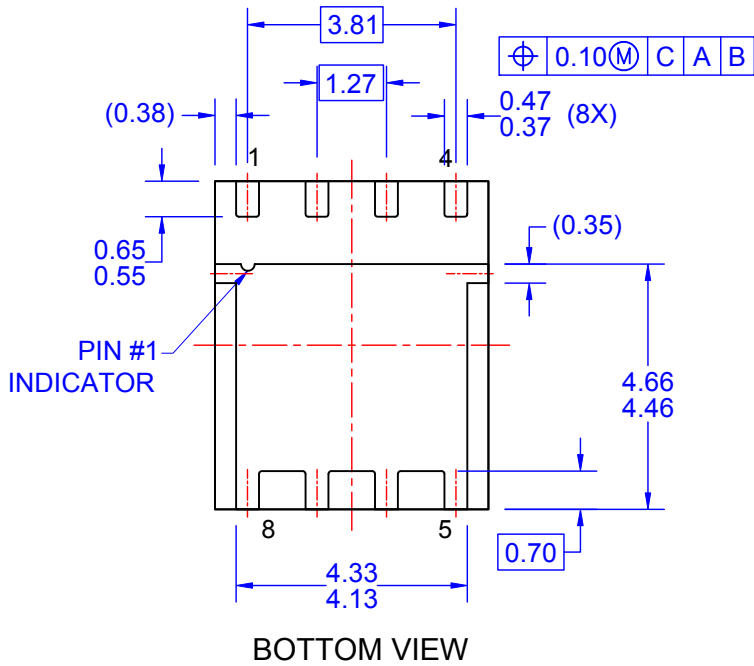
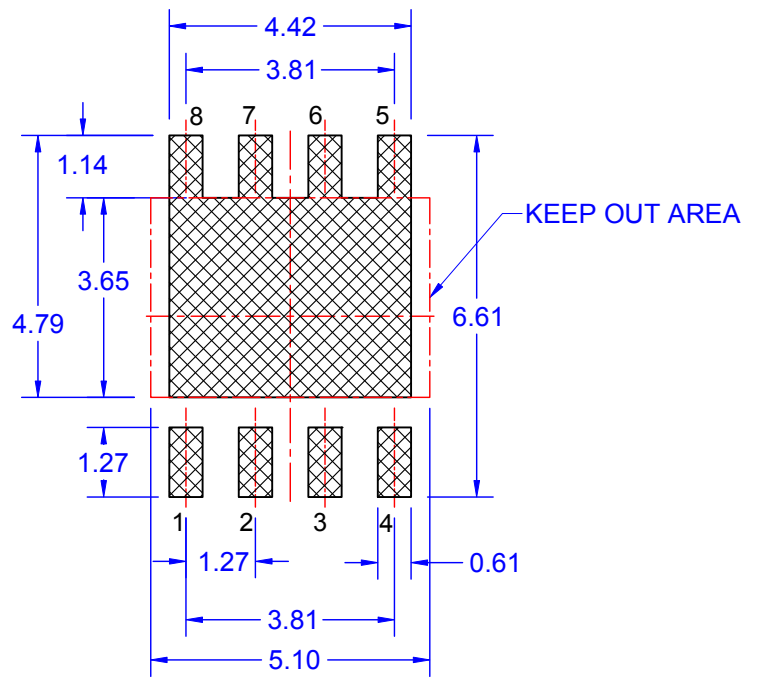
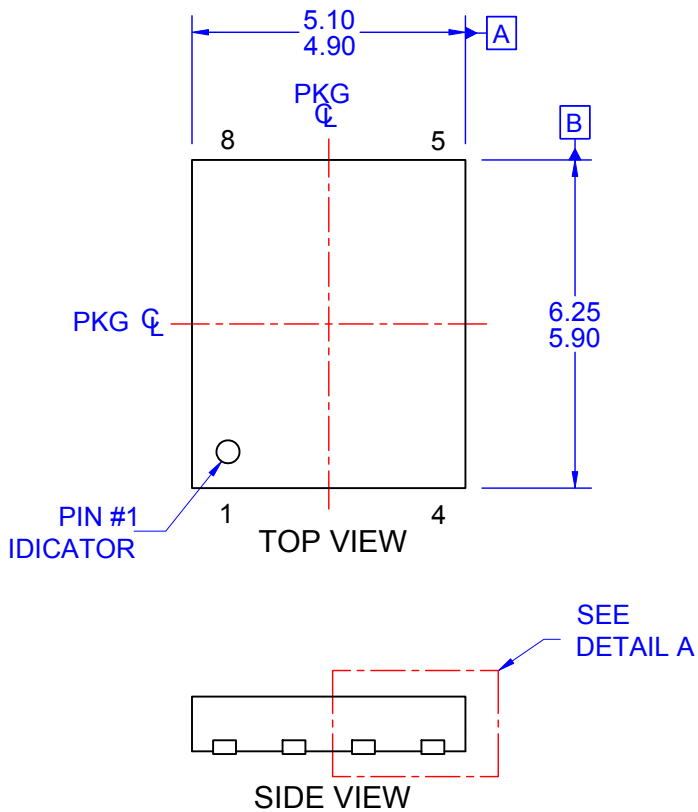


**Figure 12. Single Pulse Maximum Power Dissipation**

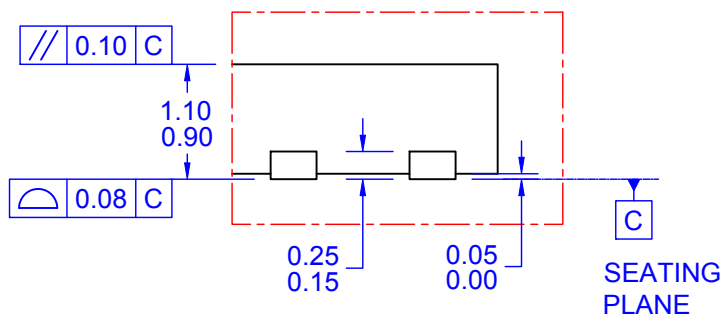
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Case Transient Thermal Response Curve**



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
  - F) DRAWING FILE NAME: PQFN08JREV3.



**DETAIL A**  
SCALE: 2:1







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#### Definition of Terms

Datasheet Identification	Product Status	Definition
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I74

# AMEYA360

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➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd  
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692

Email [amall@ameya360.com](mailto:amall@ameya360.com)

QQ 800077892

Skype [ameyasales1](#) [ameyasales2](#)

➤ Customer Service :

Email [service@ameya360.com](mailto:service@ameya360.com)

➤ Partnership :

Tel +86 (21) 64016692-8333

Email [mkt@ameya360.com](mailto:mkt@ameya360.com)