

HIGH-SPEED CMOS LOGIC 16-CHANNEL ANALOG MULTIPLEXER and DEMULTIPLEXER

 Check for Samples: [CD74HCT4067-Q1](#)

FEATURES

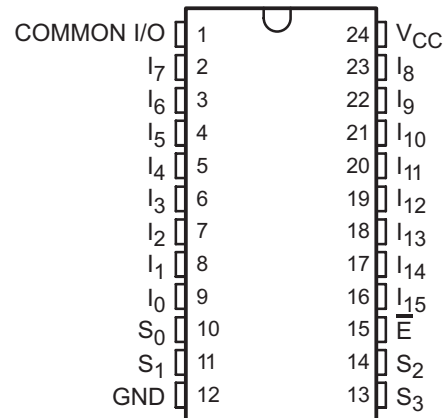
- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following Results:
 - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H1A
 - Device CDM ESD Classification Level C2
- Wide Analog Input Voltage Range
- Low ON Resistance
 - 70 Ω Typical ($V_{CC} = 4.5\text{ V}$)
- Fast Switching and Propagation Speeds
- Break-Before-Make Switching
 - 6 ns Typical ($V_{CC} = 4.5\text{ V}$)
- Fanout (Over Temperature Range)
 - Standard Outputs: 10 LSTTL Loads
 - Bus Driver Outputs: 15 LSTTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- 4.5-V to 5.5-V Operation
- Direct LSTTL Input Logic Compatibility: $V_{IL} =$

 0.8 V Max, $V_{IH} = 2\text{ V Min}$

- CMOS Input Compatibility: $I_I \leq 1\ \mu\text{A}$ at V_{OL}, V_{OH}

APPLICATIONS

- Automotive
- Analog Switch
- Analog Multiplexer and Demultiplexer

**M PACKAGE
(TOP VIEW)**


DESCRIPTION

The CD74HCT4067-Q1 device is a digitally controlled analog switch that utilizes silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

This analog multiplexer and demultiplexer controls analog voltages that may vary across the voltage supply range. It is a bidirectional switch, thus allowing any analog input to be used as an output and vice-versa. The switch has low (on) resistance and low (off) leakages. In addition, the device has an enable control that, when high, disables all switches to their off state.

ORDERING INFORMATION⁽¹⁾

| T_A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER ⁽³⁾ | TOP-SIDE MARKING |
|----------------|------------------------|--------------|--------------------------------------|------------------|
| –40°C to 125°C | DW-SOIC-M | Reel of 2000 | CD74HCT4067QM96Q1 | HCT4067I |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) The suffix 96 denotes tape and reel.



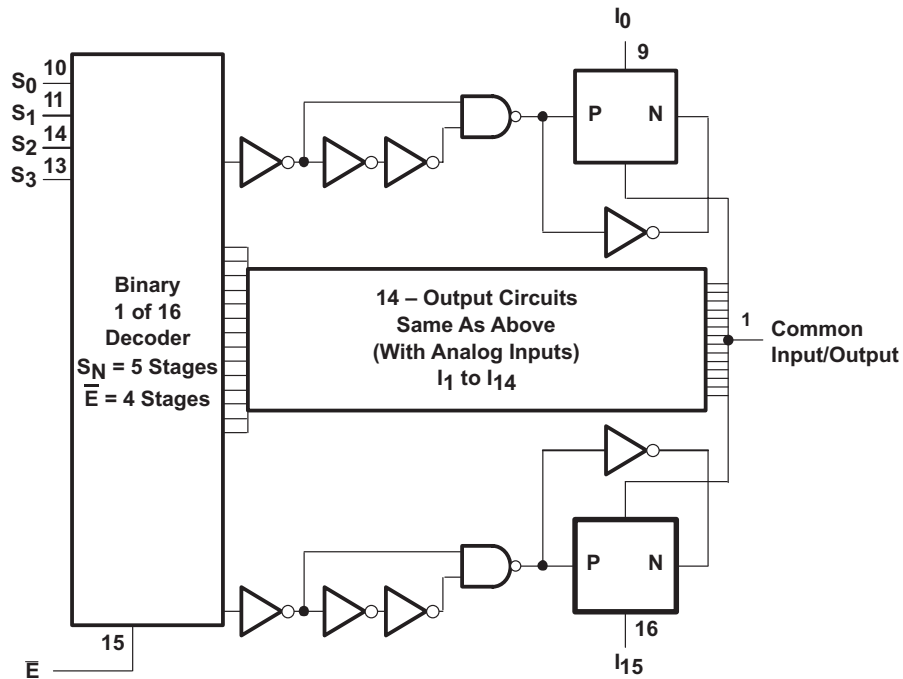
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Table 1. FUNCTION TABLE⁽¹⁾

| S0 | S1 | S2 | S3 | \bar{E} | SELECTED CHANNEL |
|----|----|----|----|-----------|------------------|
| X | X | X | X | H | None |
| L | L | L | L | L | 0 |
| H | L | L | L | L | 1 |
| L | H | L | L | L | 2 |
| H | H | L | L | L | 3 |
| L | L | H | L | L | 4 |
| H | L | H | L | L | 5 |
| L | H | H | L | L | 6 |
| H | H | H | L | L | 7 |
| L | L | L | H | L | 8 |
| H | L | L | H | L | 9 |
| L | H | L | H | L | 10 |
| H | H | L | H | L | 11 |
| L | L | H | H | L | 12 |
| H | L | H | H | L | 13 |
| L | H | H | H | L | 14 |
| H | H | H | H | L | 15 |

(1) H = High level
 L = Low level
 X = Don't care

Logic Diagram (Positive Logic)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | VALUE | | UNIT |
|------------|--|-------|---------|------|
| | | MIN | MAX | |
| V_{CC} | Supply voltage range ⁽²⁾ | -0.5 | 7 | V |
| I_{IK} | Input clamp current ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) | | ±20 | mA |
| I_{OK} | Output clamp current ($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) | | ±20 | mA |
| I_O | Switch current ($V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) | | ±25 | mA |
| I_O | Output source or sink current per output pin ($V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) | | ±25 | mA |
| | Continuous current through V_{CC} or GND | | ±50 | mA |
| T_J | Maximum junction temperature | | 150 | °C |
| T_{stg} | Storage temperature range | -65 | 150 | °C |
| ESD Rating | Human Body Model (HBM) AEC-Q100 classification level H1A | | 400 | V |
| | Charged Device Model (CDM) AEC-Q100 classification level C2 | | 250 | V |
| | Latch-up per JESD78D | | Class 1 | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are referenced to GND, unless otherwise specified.

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | CD74HCT4067-Q1 | UNIT |
|-------------------------------|--|----------------|------|
| | | DW (24 PINS) | |
| θ_{JA} | Junction-to-ambient thermal resistance | 62.3 | °C/W |
| θ_{JcTop} | Junction-to-case (top) thermal resistance | 30.5 | |
| θ_{JB} | Junction-to-board thermal resistance | 31.8 | |
| ψ_{JT} | Junction-to-top characterization parameter | 7.7 | |
| ψ_{JB} | Junction-to-board characterization parameter | 31.5 | |
| θ_{JcBot} | Junction-to-case (bottom) thermal resistance | N/A | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|----------|---------------------------------------|------------------|----------|------|
| V_{CC} | Supply voltage | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | V |
| V_I | Input voltage | 0 | V_{CC} | V |
| V_O | Output voltage | 0 | V_{CC} | V |
| t_t | Input transition (rise and fall) time | | 500 | ns |
| | | $V_{CC} = 4.5$ V | | |
| T_A | Operating free-air temperature | -40 | 125 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _I | V _{CC} | T _A = 25°C | | | T _A = -40°C to 125°C | | UNIT |
|------------------|---|--|------------------------|-----------------------|-----|------|---------------------------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| I _I | Logic input | V _{CC} or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| I _{Iz} | V _{IS} = V _{CC} or GND, \bar{E} = V _{CC} | | 5.5 V | | | ±0.8 | | ±8 | μA |
| r _{on} | I _O = 1 mA | V _{IS} = V _{CC} or GND | V _{CC} or GND | 4.5 V | 70 | 160 | | 200 | Ω |
| | | V _{IS} = V _{CC} to GND | V _{CC} to GND | 4.5 V | 90 | 180 | | 225 | |
| Δr _{on} | Between any two switches | | 4.5 V | | 10 | | | | Ω |
| I _{CC} | | V _{CC} or GND | 5.5 V | | | 8 | | 80 | μA |
| ΔI _{CC} | Per input pin: 1 unit load ⁽¹⁾ | V _{CC} - 2.1 V | 4.5 V to 5.5 V | | 100 | 360 | | 450 | μA |
| C _I | Control inputs | | | | | 10 | | 10 | pF |

(1) For dual-supply systems, theoretical worst-case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING

| INPUT | UNIT LOADS ⁽¹⁾ |
|---------------------------------|---------------------------|
| S ₀ - S ₃ | 0.5 |
| \bar{E} | 0.3 |

(1) Unit load is ΔI_{CC} limit specified in the electrical characteristics table, for example, 360 μA max at 25°C.

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted) see [Figure 5](#)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | V _{CC} | T _A = 25°C | | | T _A = -40°C TO 125°C | | UNIT |
|------------------|----------------|-------------|------------------------|-----------------|-----------------------|-----|-----|---------------------------------|-----|------|
| | | | | | MIN | TYP | MAX | MIN | MAX | |
| t _{pd} | I _n | Common I/O | C _L = 15 pF | 5 V | | 6 | | | ns | |
| | | | C _L = 50 pF | 4.5 V | | 15 | | 19 | | |
| t _{en} | \bar{E} | Common I/O | C _L = 15 pF | 5 V | | 25 | | | ns | |
| | | | C _L = 50 pF | 4.5 V | | 60 | | 75 | | |
| t _{en} | S _n | Common I/O | C _L = 15 pF | 5 V | | 25 | | | ns | |
| | | | C _L = 50 pF | 4.5 V | | 60 | | 75 | | |
| t _{dis} | \bar{E} | Common I/O | C _L = 15 pF | 5 V | | 23 | | | ns | |
| | | | C _L = 50 pF | 4.5 V | | 55 | | 69 | | |
| t _{dis} | S _n | Common I/O | C _L = 15 pF | 5 V | | 21 | | | ns | |
| | | | C _L = 50 pF | 4.5 V | | 58 | | 73 | | |

OPERATING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--|-----|-----|-----|------|
| C _{pd} | Power dissipation capacitance ⁽¹⁾ | | 96 | | pF |

(1) C_{pd} is used to determine the dynamic power consumption (P_D), per package.

$$P_D = (C_{pd} \times V_{CC}^2 \times f_i) + \sum (C_L + C_S) \times V_{CC}^2 \times f_o$$

f_o = output frequency

f_i = input frequency

C_L = output load capacitance

C_S = switch capacitance

V_{CC} = supply voltage

ANALOG CHANNEL CHARACTERISTICS

T_A = 25°C

| | PARAMETER | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|------------------|--|--|-----------------|-------|------|
| f _{max} | Switch frequency response bandwidth at -3 dB | See Figure 1 and Figure 7 ^{(1) (2)} | 4.5 V | 89 | MHz |
| | Sine-wave distortion | See Figure 2 | 4.5 V | 0.051 | % |
| | Switch OFF signal feedthrough | See Figure 4 and Figure 8 | 4.5 V | -75 | dB |
| C _S | Switch input capacitance | | | 5 | pF |
| C _{COM} | Common capacitance | | | 50 | pF |

- (1) Adjust input voltage to obtain 0 dBm at output, f = 1 MHz.
- (2) V_{IS} is centered at V_{CC} / 2

PARAMETER MEASUREMENT INFORMATION

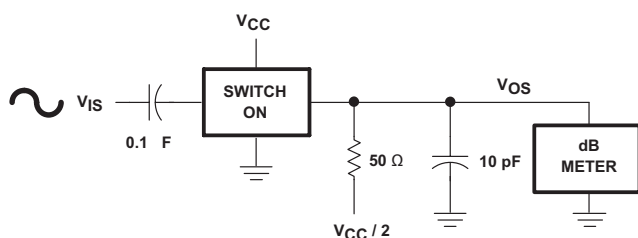


Figure 1. Frequency-Response Test Circuit

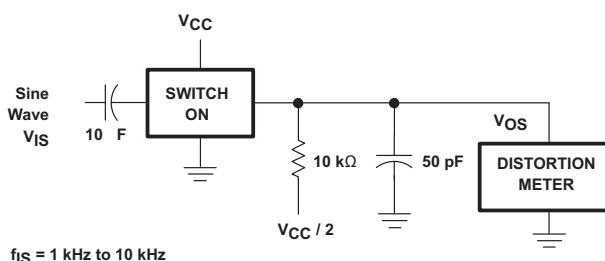


Figure 2. Sine-Wave Distortion Test Circuit

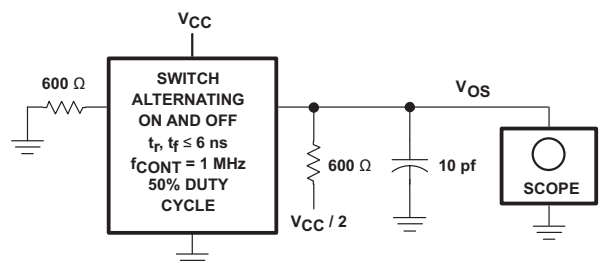


Figure 3. Control-to-Switch Feedthrough Noise Test Circuit

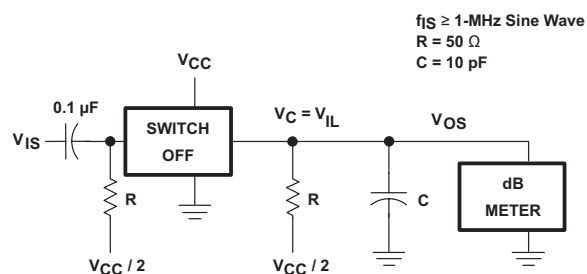
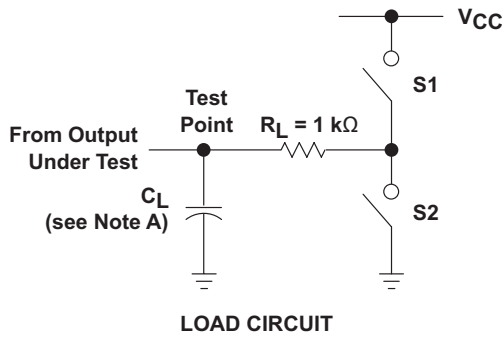
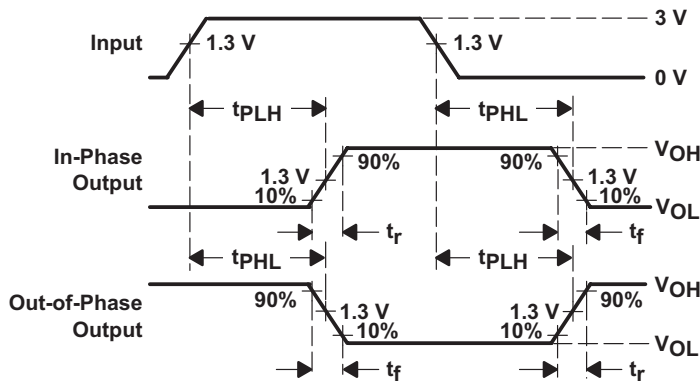


Figure 4. Switch OFF Signal Feedthrough Test Circuit

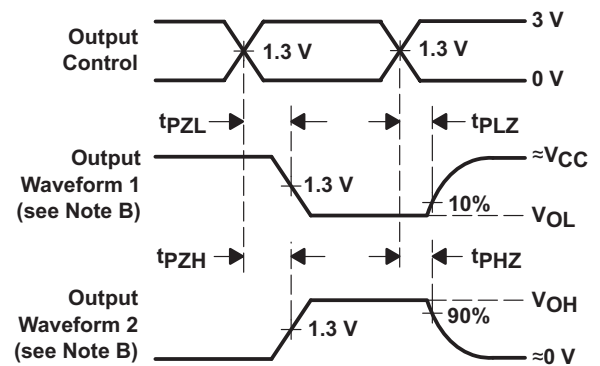
PARAMETER MEASUREMENT INFORMATION (continued)



| PARAMETER | S1 | S2 | |
|-----------|------|--------|--------|
| t_{en} | tpZH | Open | Closed |
| | tpZL | Closed | Open |
| t_{dis} | tpHZ | Open | Closed |
| | tpLZ | Closed | Open |
| t_{pd} | Open | Open | |



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

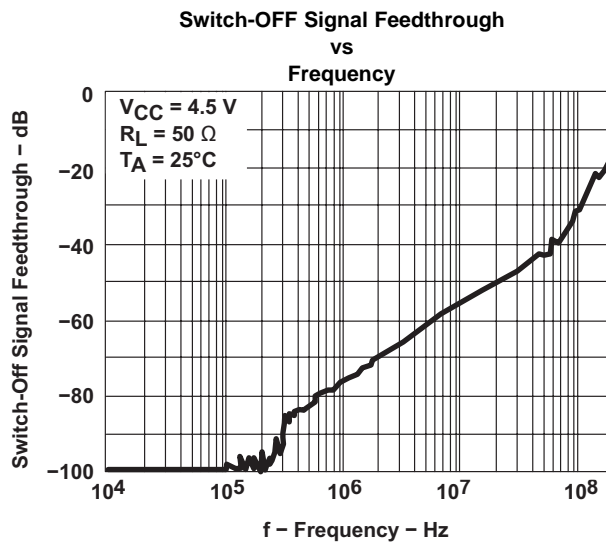
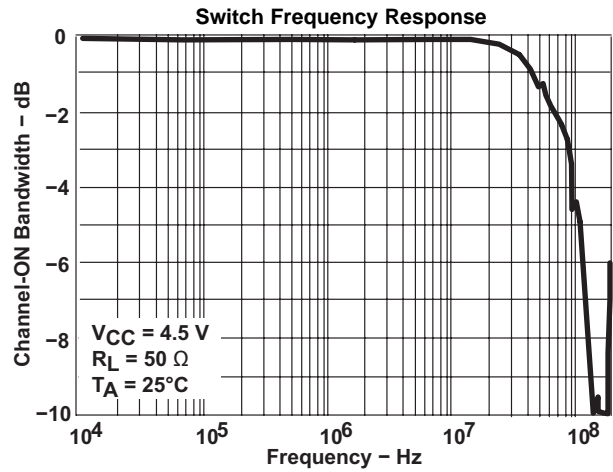
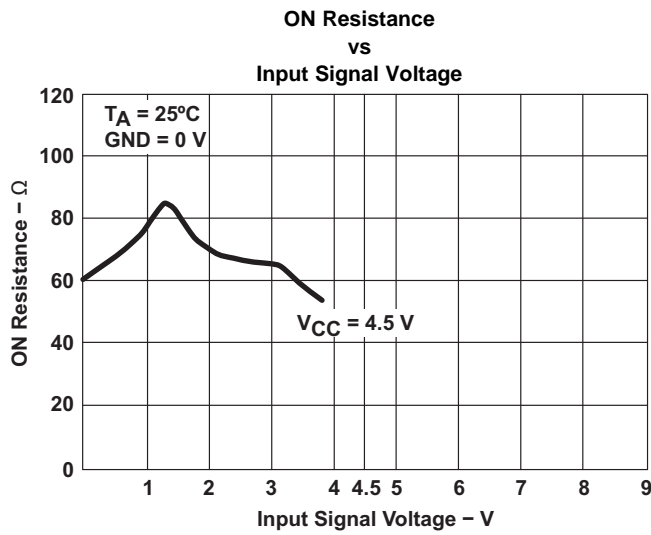


VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time, with one input transition per measurement.
 - F. t_{pLZ} and t_{pHZ} are the same as t_{dis} .
 - G. t_{pZL} and t_{pZH} are the same as t_{en} .
 - H. t_{pLH} and t_{pHL} are the same as t_{pd} .

Figure 5. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



REVISION HISTORY

| Changes from Revision A (April, 2008) to Revision B | Page |
|--|------|
| • Changed H2 to H1A and C3B to C2 throughout document | 1 |
| • Added AEC-Q100 info to Features | 1 |
| • Removed from Features: Wide Operating Temperature Range: –40°C to 85°C | 1 |
| • Added applications | 1 |
| • Replaced SOIC-M package info in ordering info table with new row for DW-SOIC-M package | 1 |
| • Added ESD ratings to Abs Max table | 3 |
| • Added latch-up row in Abs Max table | 3 |
| • Changed max T _A value from 85°C to 125°C | 3 |
| • Changed T _A = –40°C to 85°C column to T _A = –40°C to 125°C | 4 |
| • Changed T _A = –40°C to 85°C column to T _A = –40°C to 125°C | 4 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| CD74HCT4067IM96Q1 | ACTIVE | SOIC | DW | 24 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT4067I | Samples |
| CD74HCT4067QM96Q1 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HCT4067I | Samples |
| D24067IM96G4Q1 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT4067I | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF CD74HCT4067-Q1 :

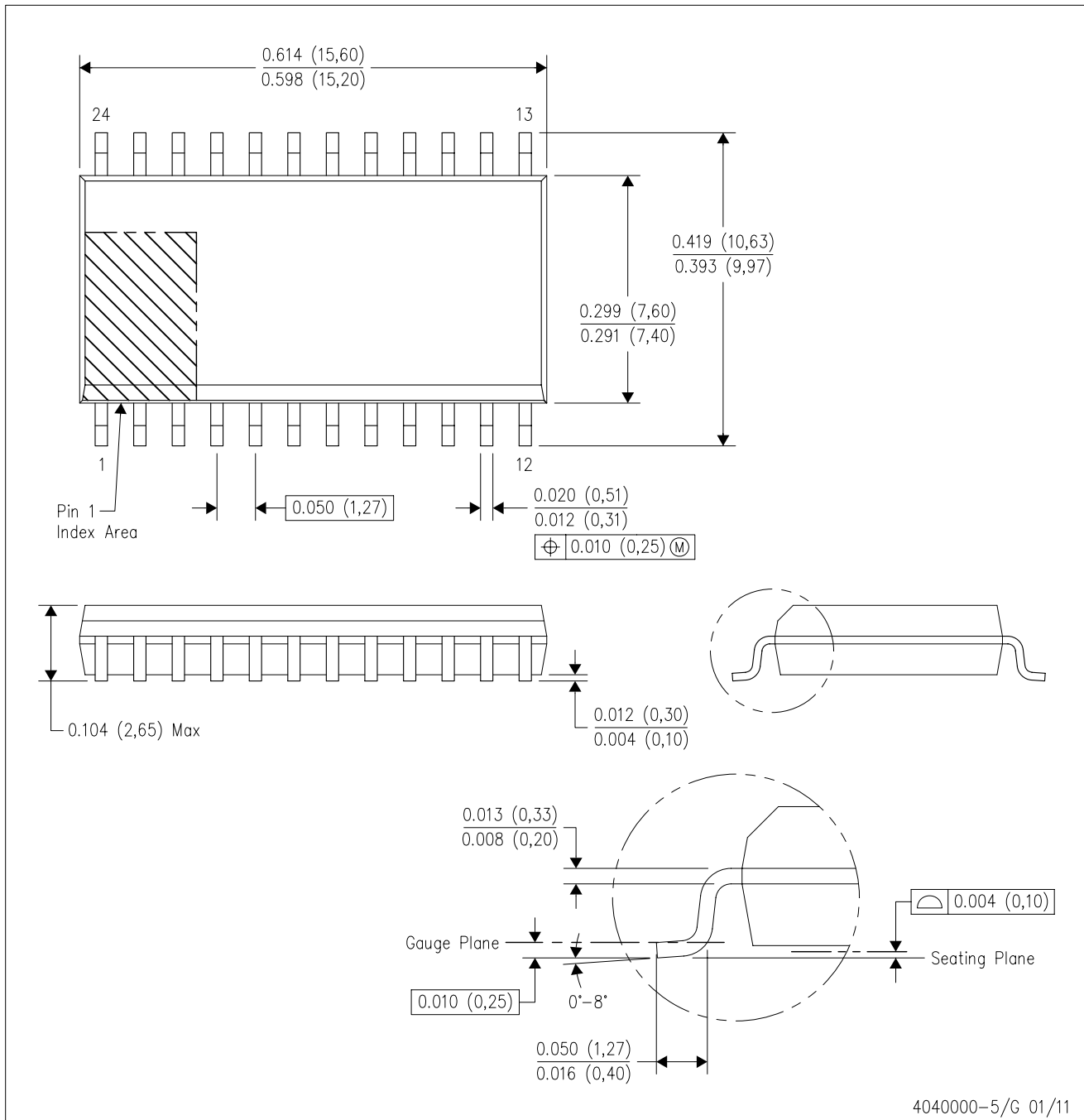
- Catalog: [CD74HCT4067](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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