

FDMF6707V — Extra-Small, High-Performance, High-Frequency DrMOS Module

Benefits

- Ultra-Compact 6x6mm PQFN, 72% Space-Saving Compared to Conventional Discrete Solutions
- Fully Optimized System Efficiency
- Clean Switching Waveforms with Minimal Ringing
- High-Current Handling

Features

- Over 93% Peak-Efficiency
- Internal 12V to 5V Linear Regulator
- High-Current Handling: 50A
- High-Performance PQFN Copper-Clip Package
- 3-State 3.3V PWM Input Driver
- Skip-Mode SMOD# (Low-Side Gate Turn Off) Input
- Thermal Warning Flag for Over-Temperature Condition
- Driver Output Disable Function (DISB# Pin)
- Internal Pull-Up and Pull-Down for SMOD# and DISB# Inputs, Respectively
- Fairchild PowerTrench® Technology MOSFETs for Clean Voltage Waveforms and Reduced Ringing
- Fairchild SyncFET™ (Integrated Schottky Diode) Technology in the Low-Side MOSFET
- Integrated Bootstrap Schottky Diode
- Adaptive Gate Drive Timing for Shoot-through Protection
- Under-Voltage Lockout (UVLO)
- Optimized for Switching Frequencies up to 1MHz
- Low-Profile SMD Package
- Fairchild Green Packaging and RoHS Compliant
- Based on the Intel® 4.0 DrMOS Standard

Description

The XS™ DrMOS family is Fairchild's next-generation, fully optimized, ultra-compact, integrated MOSFET plus driver power stage solution for high-current, high-frequency, synchronous buck DC-DC applications. The FDMF6707V integrates a driver IC, two power MOSFETs, and a bootstrap Schottky diode into a thermally enhanced, ultra-compact 6x6mm PQFN package.

With an integrated approach, the complete switching power stage is optimized for driver and MOSFET dynamic performance, system inductance, and power MOSFET $R_{DS(ON)}$. XS™ DrMOS uses Fairchild's high-performance PowerTrench® MOSFET technology, which dramatically reduces switch ringing, eliminating the snubber circuit in most buck converter applications.

A new driver IC, with reduced dead times and propagation delays, further enhances performance. An internal 12V to 5V linear regulator enables the FDMF6707V to operate from a single 12V supply. A thermal warning function warns of potential over-temperature situations. FDMF6707V also incorporates features such as Skip Mode (SMOD) for improved light-load efficiency, along with a 3-state 3.3V PWM input for compatibility with a wide range of PWM controllers.

Applications

- High-Performance Gaming Motherboards
- Compact Blade Servers, V-Core and Non-V-Core DC-DC Converters
- Desktop Computers, V-Core and Non-V-Core DC-DC Converters
- Workstations
- High-Current DC-DC Point-of-Load (POL) Converters
- Networking and Telecom Microprocessor Voltage Regulators
- Small Form-Factor Voltage Regulator Modules

Ordering Information

| Part Number | Current Rating | Package | Top Mark |
|-------------|----------------|---|-----------|
| FDMF6707V | 50A | 40-Lead, Clipbond PQFN DrMOS, 6.0mm x 6.0mm Package | FDMF6707V |

Typical Application Circuit

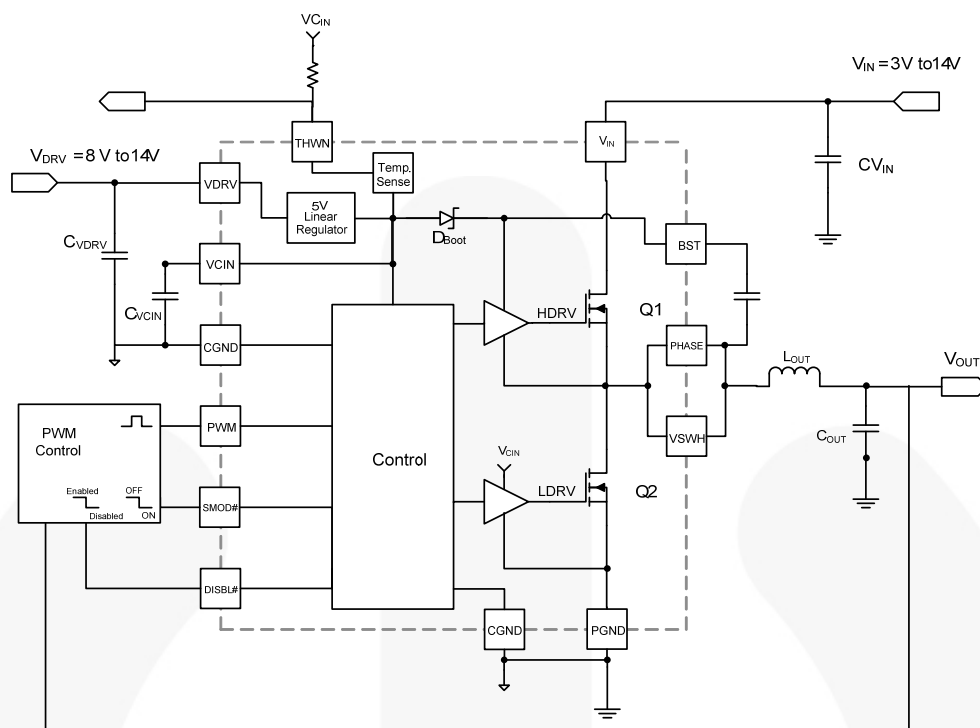


Figure 1. Typical Application Circuit

DrMOS Block Diagram

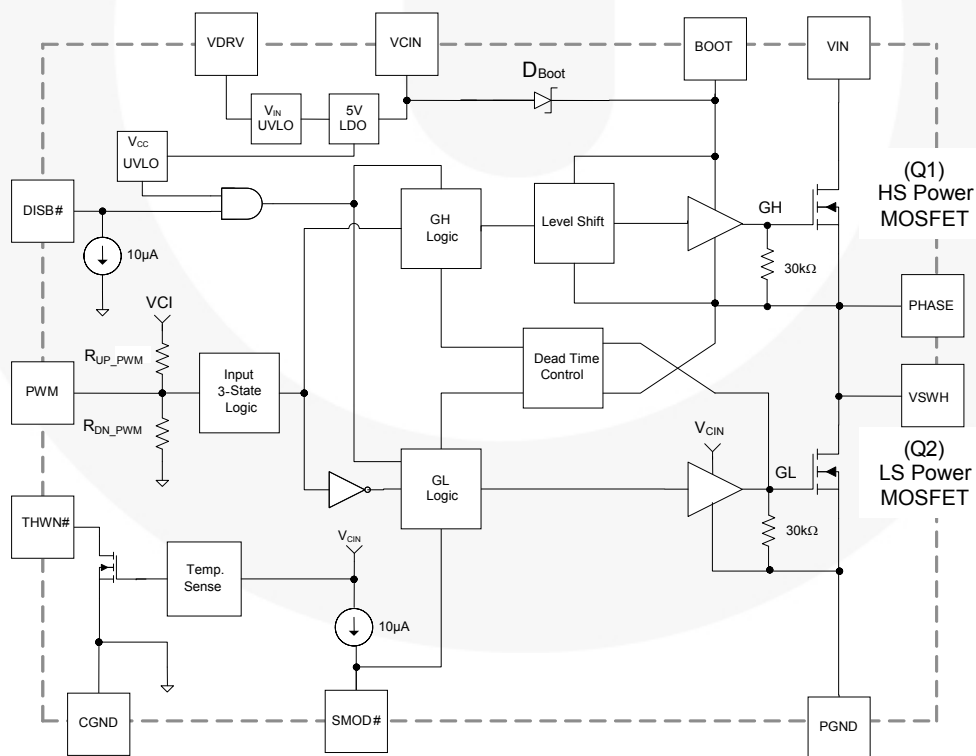


Figure 2. DrMOS Block Diagram

Pin Configuration

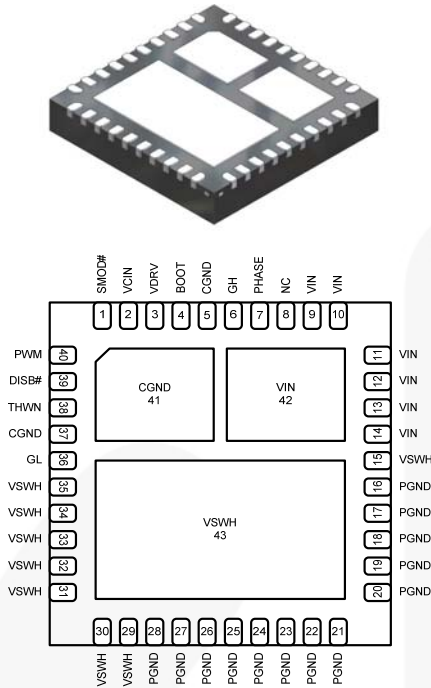


Figure 3. Bottom View

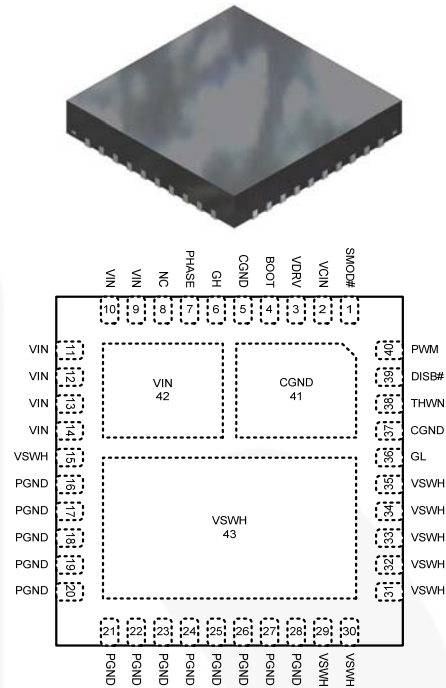


Figure 4. Top View

Pin Definitions

| Pin # | Name | Description |
|-----------------|-------|--|
| 1 | SMOD# | When SMOD#=HIGH, the low-side driver is the inverse of PWM input. When SMOD#=LOW, the low-side driver is disabled. This pin has a 10μA internal pull-up current source. Do not add a noise filter capacitor. |
| 2 | VCIN | Linear regulator 5V output. Minimum 1μF ceramic capacitor recommended from this pin to CGND. |
| 3 | VDRV | Linear regulator input. Minimum 1μF ceramic capacitor is recommended connected as close as possible from this pin to CGND. |
| 4 | BOOT | Bootstrap supply input. Provides voltage supply to the high-side MOSFET driver. Connect a bootstrap capacitor from this pin to PHASE. |
| 5, 37, 41 | CGND | IC ground. Ground return for driver IC. |
| 6 | GH | For manufacturing test only. This pin must float: it must not be connected to any pin. |
| 7 | PHASE | Switch node pin for bootstrap capacitor routing; electrically shorted to VSWH pin. |
| 8 | NC | No connect. The pin is not electrically connected internally, but can be connected to VIN for convenience. |
| 9 - 14, 42 | VIN | Power input. Output stage supply voltage. |
| 15, 29 - 35, 43 | VSWH | Switch node input. Provides return for high-side bootstrapped driver and acts as a sense point for the adaptive shoot-through protection. |
| 16 – 28 | PGND | Power ground. Output stage ground. Source pin of the low-side MOSFET. |
| 36 | GL | For manufacturing test only. This pin must float. It must not be connected to any pin. |
| 38 | THWN# | Thermal warning flag, open collector output. When temperature exceeds the trip limit, the output is pulled LOW. THWN# does not disable the module. |
| 39 | DISB# | Output disable. When LOW, this pin disables the power MOSFET switching (GH and GL are held LOW). This pin has a 10μA internal pull-down current source. Do not add a noise filter capacitor. |
| 40 | PWM | PWM signal input. This pin accepts a 3-state 3.3V PWM signal from the controller. |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Unit |
|-----------------------------------|---|-----------------------------------|------|------|------|
| | VCIN, DISB#, PWM, SMOD#, GL, THWN# to CGND Pins | | -0.3 | 6.0 | V |
| | VIN to PGND, CGND Pins | | -0.3 | 25.0 | |
| | VDRV to PGND, CGND Pins | | | 16.0 | |
| | BOOT, GH to VSWH, PHASE Pins | | -0.3 | 6.0 | |
| | BOOT, PHASE, GH to CGND Pins | | -0.3 | 25.0 | |
| | VSWH to CGND/PGND (DC Only) | | -0.3 | 25.0 | |
| | VSWH to PGND (< 20ns) | | -8.0 | 25.0 | |
| | BOOT to VCIN | | | 22.0 | |
| I _{THWN#} | THWN# Sink Current | | -0.1 | 7.0 | mA |
| I _{O(AV)} ⁽¹⁾ | V _{IN} =12V, V _O =1.0V | f _{SW} =350kHz | | 45 | A |
| | | f _{SW} =1MHz | | 42 | |
| θ _{JPCB} | Junction-to-PCB Thermal Resistance | | | 3.5 | °C/W |
| T _A | Ambient Temperature Range | | -40 | +125 | °C |
| T _J | Maximum Junction Temperature | | | +150 | °C |
| T _{STG} | Storage Temperature Range | | -55 | +150 | °C |
| ESD | Electrostatic Discharge Protection | Human Body Model, JESD22-A114 | 2000 | | V |
| | | Charged Device Model, JESD22-C101 | 1000 | | |

Note:

1. I_{O(AV)} is rated using Fairchild's DrMOS evaluation board, T_A = 25°C, natural convection cooling. This rating is limited by the peak DrMOS temperature, T_J = 150°C, and varies depending on operating conditions and PCB layout. This rating can be changed with different application settings.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|-----------------------------------|------|------|-------------------|------|
| V _{DRV} | Gate Drive Circuit Supply Voltage | 8 | 12 | 15 | V |
| V _{IN} | Output Stage Supply Voltage | 3 | 12 | 15 ⁽²⁾ | V |

Note:

2. Operating at high V_{IN} can create excessive AC overshoots on the VSWH-to-GND and BOOT-to-GND nodes during MOSFET switching transients. For reliable DrMOS operation, VSWH-to-GND and BOOT-to-GND must remain at or below the Absolute Maximum Ratings shown in the table above. Refer to the "Application Information" and "PCB Layout Guidelines" sections of this datasheet for additional information.

Electrical Characteristics

Typical values are $V_{IN} = 12V$, $V_{DRV} = 12V$, and $T_A = +25^\circ C$ unless otherwise noted.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|-------------------------------------|-----------------------------|--|------|------|------|------------|
| Basic Operation | | | | | | |
| I_Q | Quiescent Current | $I_Q = I_{VDRV}$, PWM=LOW or HIGH or Float | | 2 | 5 | mA |
| Internal 5V Linear regulator | | | | | | |
| I_{VDRV} | Input Current | $8V < V_{DRV} < 14V$, $f_{SW} = 1MHz$ | | 36 | | mA |
| V_{CIN} | Output Voltage | $V_{DRV} = 8V$, $I_{LOAD} = 5mA$ | 4.8 | 5.0 | 5.2 | V |
| P_{VDRV} | Power Dissipation | $V_{DRV} = 12V$, $f_{SW} = 1MHz$ | | 250 | | mW |
| C_{VCIN} | VCIN Bypass Capacitor | X7R or X5R Ceramic | 1 | | 10 | μF |
| | Line Regulation | $8V < V_{DRV} < 14V$, $I_{LOAD} = 5mA$ | | 20 | | mV |
| | Load Regulation | $V_{DRV} = 8V$, $5mA < I_{LOAD} < 100mA$ | | 75 | | mV |
| | Short-Circuit Current Limit | $8V < V_{DRV} < 14V$ | | 200 | | mA |
| UVLO | UVLO Threshold | V_{DRV} Rising | 6.8 | 7.3 | 7.8 | V |
| UVLO _{Hyst} | UVLO Hysteresis | | | 435 | | mV |
| PWM Input | | | | | | |
| R_{UP_PWM} | Pull-Up Impedance | | | 26 | | k Ω |
| R_{DN_PWM} | Pull-Down Impedance | | | 12 | | k Ω |
| V_{IH_PWM} | PWM High Level Voltage | | 2.01 | 2.25 | 2.48 | V |
| V_{TRI_HI} | 3-State Upper Threshold | | 1.96 | 2.20 | 2.44 | V |
| V_{TRI_LO} | 3-State Lower Threshold | | 0.76 | 0.95 | 1.14 | V |
| V_{IL_PWM} | PWM Low Level Voltage | | 0.67 | 0.85 | 1.08 | V |
| $t_{D_HOLD-OFF}$ | 3-State Shutoff Time | | | 160 | 200 | ns |
| V_{HIz_PWM} | 3-State Open Voltage | | 1.4 | 1.6 | 1.9 | V |
| DISB# Input | | | | | | |
| V_{IH_DISB} | High-Level Input Voltage | | 2 | | | V |
| V_{IL_DISB} | Low-Level Input Voltage | | | | 0.8 | V |
| I_{PLD} | Pull-Down Current | | | 10 | | μA |
| t_{PD_DISBL} | Propagation Delay | PWM=GND, Delay Between DISB# from HIGH to LOW to GL from HIGH to LOW | | 25 | | ns |
| t_{PD_DISBH} | Propagation Delay | PWM=GND, Delay Between DISB# from LOW to HIGH to GL from LOW to HIGH | | 25 | | ns |
| SMOD# Input | | | | | | |
| V_{IH_SMOD} | High-Level Input Voltage | | 2 | | | V |
| V_{IL_SMOD} | Low-Level Input Voltage | | | | 0.8 | V |
| I_{PLU} | Pull-Up Current | | | 10 | | μA |
| t_{PD_SLGLL} | Propagation Delay | PWM=GND, Delay Between SMOD# from HIGH to LOW to GL from HIGH to LOW | | 10 | | ns |
| t_{PD_SHGLH} | Propagation Delay | PWM=GND, Delay Between SMOD# from LOW to HIGH to GL from LOW to HIGH | | 10 | | ns |

Continued on the following page...

Electrical Characteristics

Typical values are $V_{IN} = 12V$, $V_{DRV} = 12V$, and $T_A = +25^\circ C$ unless otherwise noted.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|------------------------------|---|---|------|------|------|------------|
| Thermal Warning Flag | | | | | | |
| T_{ACT} | Activation Temperature | | | 150 | | $^\circ C$ |
| T_{RST} | Reset Temperature | | | 135 | | $^\circ C$ |
| R_{THWN} | Pull-Down Resistance | $I_{PLD}=5mA$ | | 30 | | Ω |
| 250ns Timeout Circuit | | | | | | |
| $t_{D_TIMEOUT}$ | Timeout Delay | SW=0V, Delay Between GH from HIGH to LOW and GL from LOW to HIGH | | 250 | | ns |
| High-Side Driver | | | | | | |
| R_{SOURCE_GH} | Output Impedance, Sourcing | Source Current=100mA | | 1 | | Ω |
| R_{SINK_GH} | Output Impedance, Sinking | Sink Current=100mA | | 0.8 | | Ω |
| t_{R_GH} | Rise Time | GH=10% to 90%, $C_{LOAD}=1.1nF$ | | 6 | | ns |
| t_{F_GH} | Fall Time | GH=90% to 10%, $C_{LOAD}=1.1nF$ | | 5 | | ns |
| t_{D_DEADON} | LS to HS Deadband Time | GL going LOW to GH going HIGH, 1V GL to 10 % GH | | 10 | | ns |
| t_{PD_PLGHL} | PWM LOW Propagation Delay | PWM going LOW to GH going LOW, V_{IL_PWM} to 90% GH | | 16 | 30 | ns |
| t_{PD_PHGHH} | PWM HIGH Propagation Delay (SMOD# Held LOW) | PWM going HIGH to GH going HIGH, V_{IH_PWM} to 10% GH (SMOD#=LOW) | | 30 | | ns |
| t_{PD_TSGHH} | Exiting 3-State Propagation Delay | PWM (from 3-State) going HIGH to GH going HIGH, V_{IH_PWM} to 10% GH | | 30 | | ns |
| Low-Side Driver | | | | | | |
| R_{SOURCE_GL} | Output Impedance, Sourcing | Source Current=100mA | | 1 | | Ω |
| R_{SINK_GL} | Output Impedance, Sinking | Sink Current=100mA | | 0.5 | | Ω |
| t_{R_GL} | Rise Time | GL=10% to 90%, $C_{LOAD}=5.9nF$ | | 20 | | ns |
| t_{F_GL} | Fall Time | GL=90% to 10%, $C_{LOAD}=5.9nF$ | | 13 | | ns |
| $t_{D_DEADOFF}$ | HS to LS Deadband Time | SW going LOW to GL going HIGH, 2.2V SW to 10% GL | | 12 | | ns |
| t_{PD_PHGLL} | PWM-HIGH Propagation Delay | PWM going HIGH to GL going LOW, V_{IH_PWM} to 90% GL | | 9 | 25 | ns |
| t_{PD_TSGLL} | Exiting 3-State Propagation Delay | PWM (from 3-State) going LOW to GL going HIGH, V_{IL_PWM} to 10% GL | | 20 | | ns |
| Boot Diode | | | | | | |
| V_F | Forward-Voltage Drop | $I_F=10mA$ | | 0.35 | | V |
| V_R | Breakdown Voltage | $I_R=1mA$ | 22 | | | V |

Timing Diagram

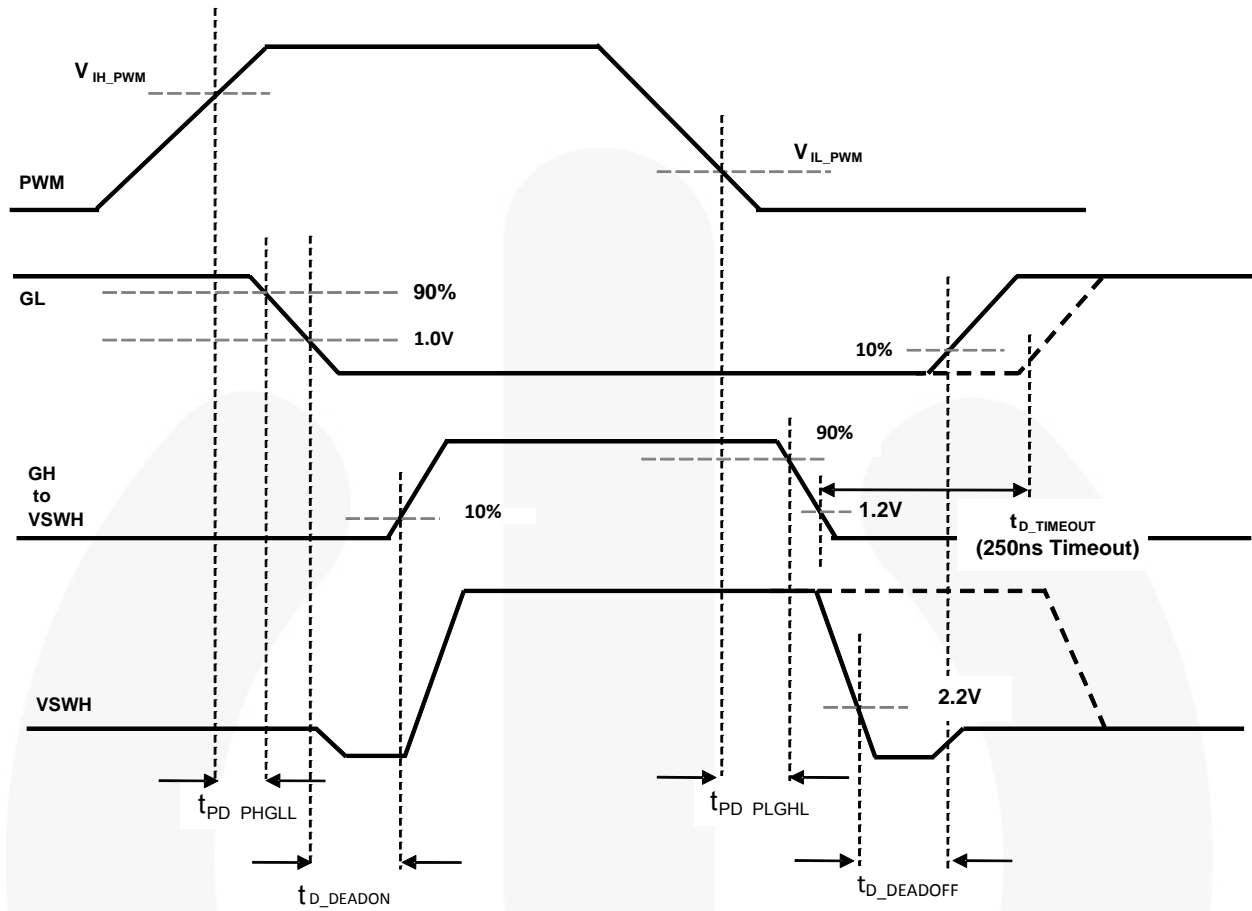


Figure 5. PWM Timing Diagram

Typical Performance Characteristics

Test Conditions: $V_{IN}=12V$, $V_{OUT}=1.0V$, $V_{CIN}=5V$, $V_{DRV}=5V$, $L_{OUT}=320nH$, $T_A=25^{\circ}C$, and natural convection cooling, unless otherwise specified.

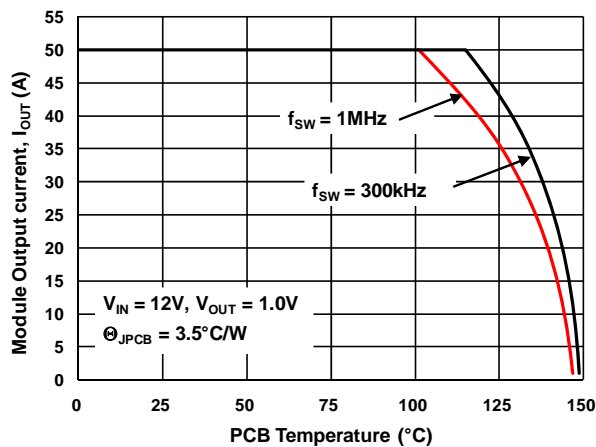


Figure 6. Safe Operating Area

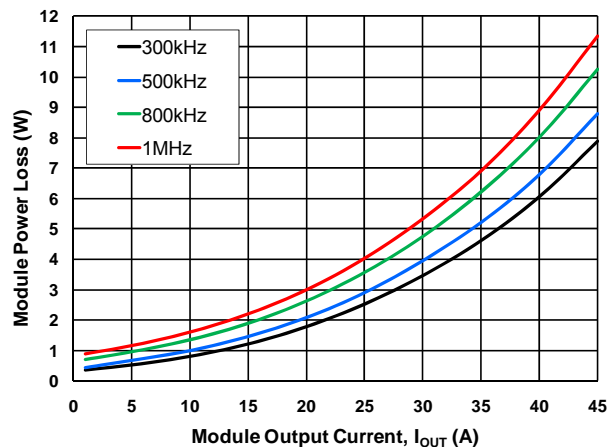


Figure 7. Module Power Loss vs. Output Current

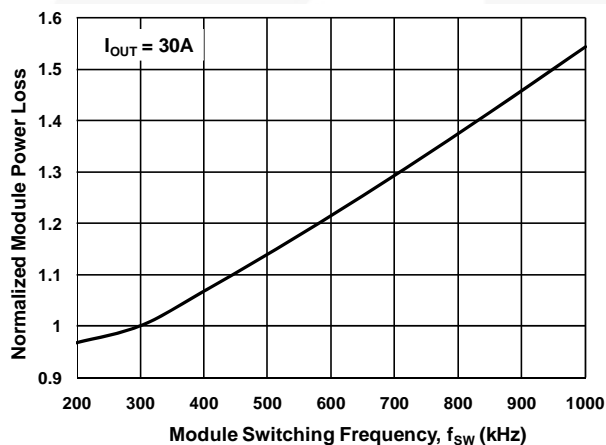


Figure 8. Power Loss vs. Switching Frequency

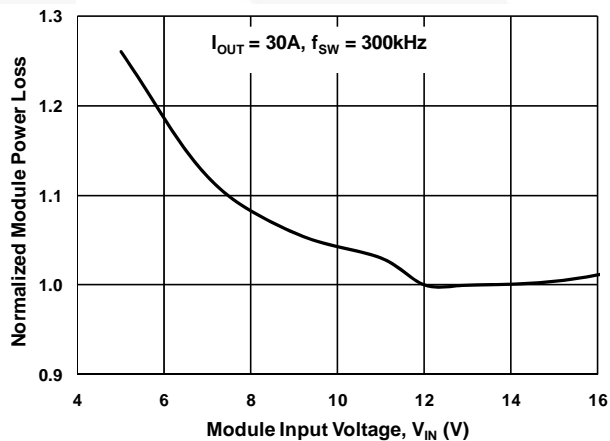


Figure 9. Power Loss vs. Input Voltage

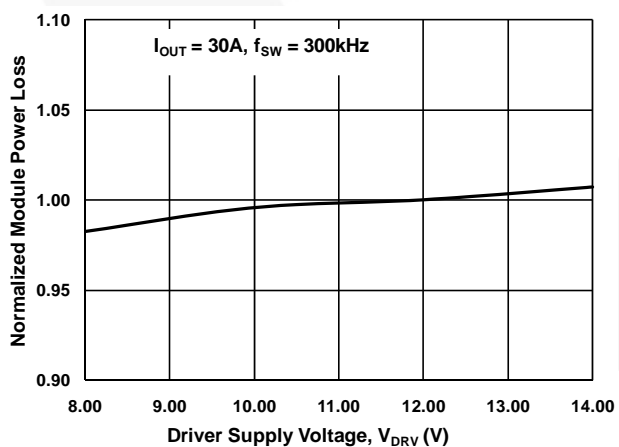


Figure 10. Power Loss vs. Driver Supply Voltage

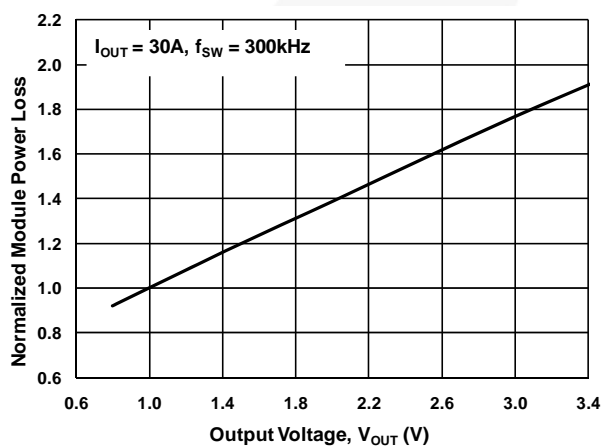


Figure 11. Power Loss vs. Output Voltage

Typical Performance Characteristics (Continued)

Test Conditions: $V_{IN}=12V$, $V_{OUT}=1.0V$, $V_{CIN}=5V$, $V_{DRV}=5V$, $L_{OUT}=320nH$, $T_A=25^{\circ}C$, and natural convection cooling, unless otherwise specified.

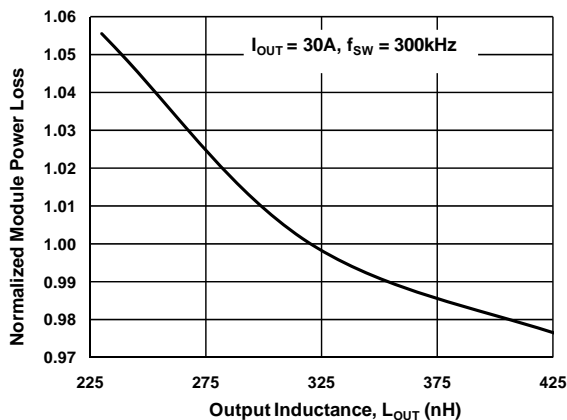


Figure 12. Power Loss vs. Output Inductance

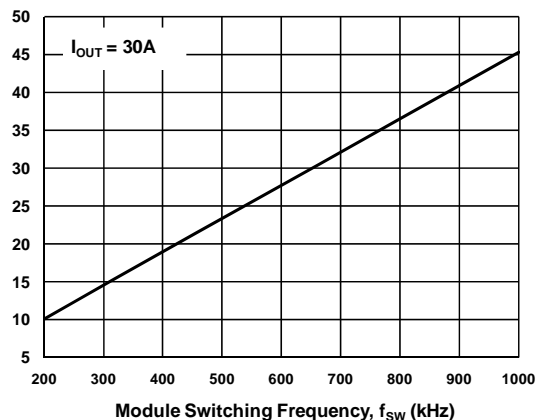


Figure 13. Driver Supply Current vs. Frequency

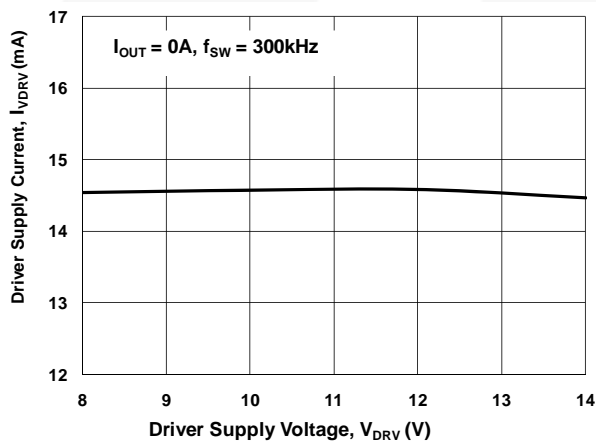


Figure 14. Driver Supply Current vs. Driver Supply Voltage

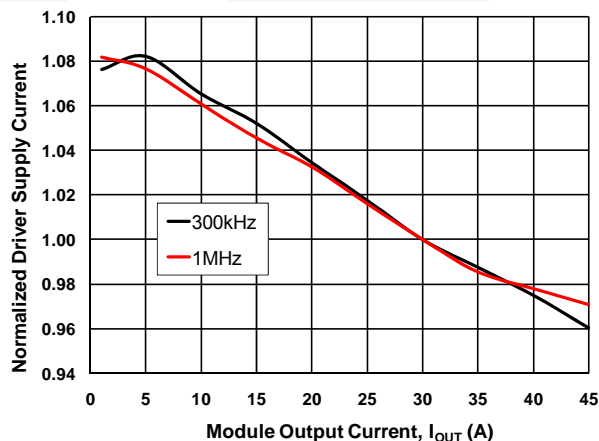


Figure 15. Driver Supply Current vs. Output Current

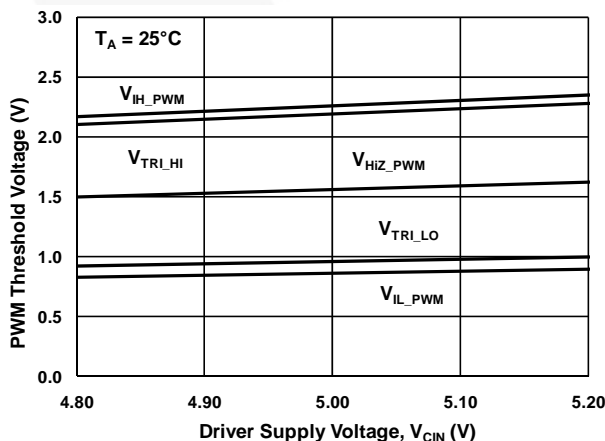


Figure 16. PWM Thresholds vs. Driver Supply Voltage

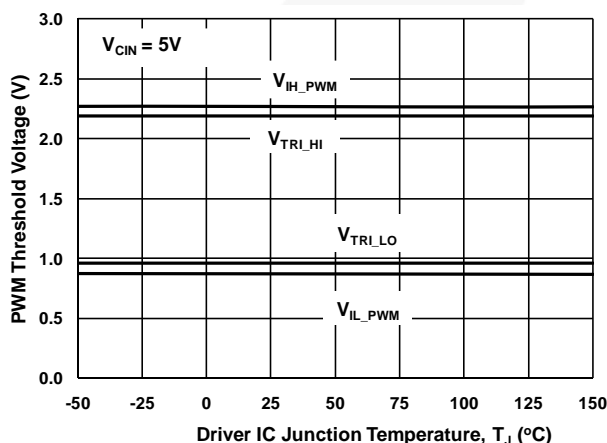


Figure 17. PWM Thresholds vs. Temperature

Typical Performance Characteristics (Continued)

Test Conditions: $V_{IN}=12V$, $V_{OUT}=1.0V$, $V_{CIN}=5V$, $V_{DRV}=5V$, $L_{OUT}=320nH$, $T_A=25^{\circ}C$, and natural convection cooling, unless otherwise specified.

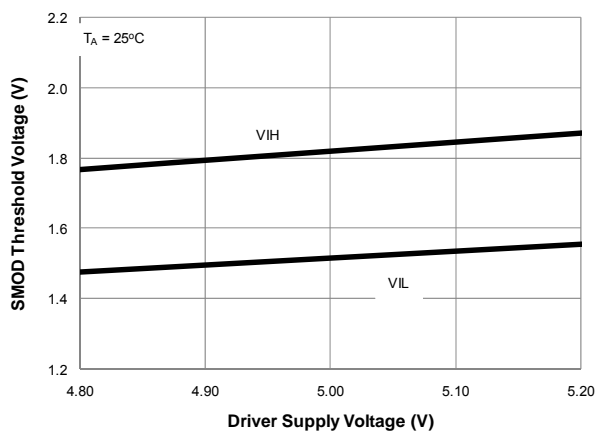


Figure 18. SMOD# Thresholds vs. Driver Supply Voltage

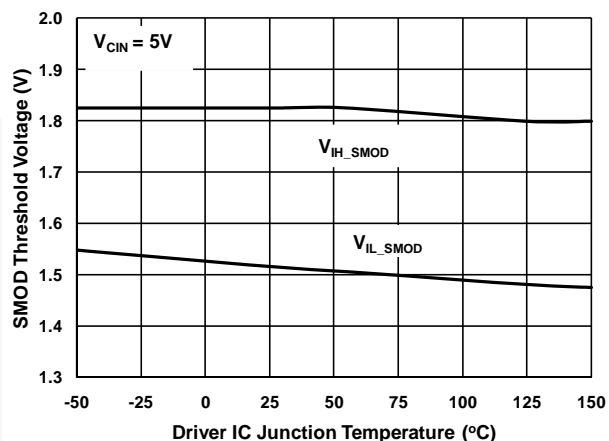


Figure 19. SMOD# Thresholds vs. Temperature

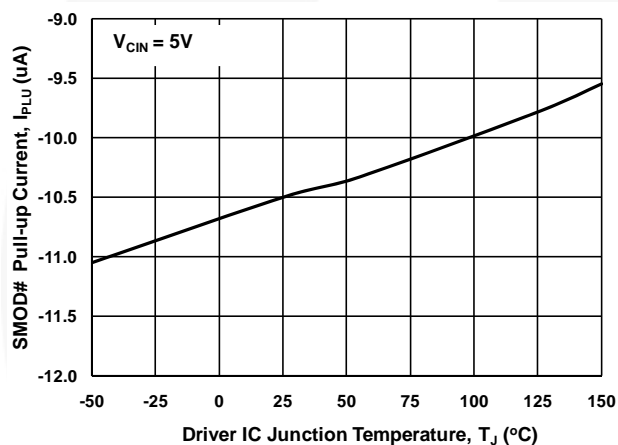


Figure 20. SMOD# Pull-Up Current vs. Temperature

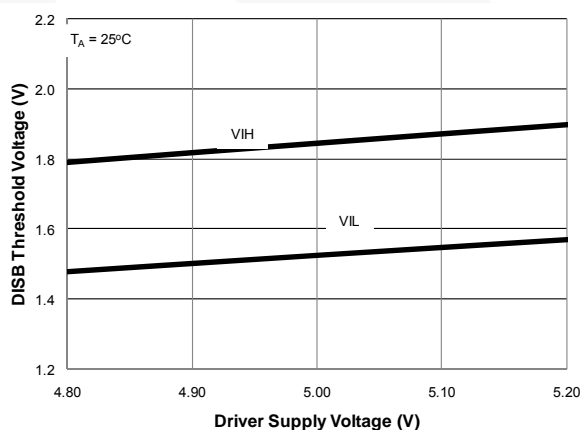


Figure 21. Disable Thresholds vs. Driver Supply Voltage

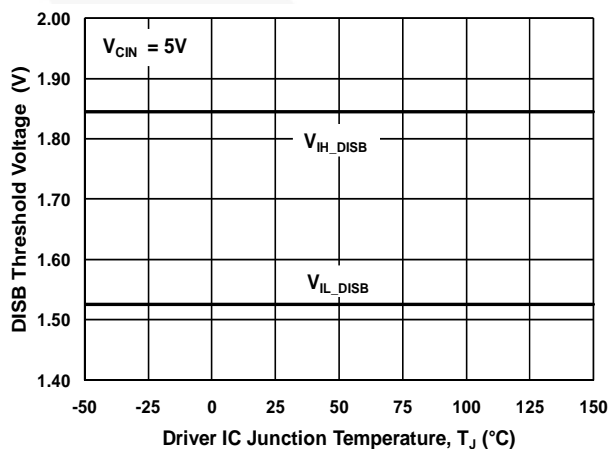


Figure 22. Disable Thresholds vs. Temperature

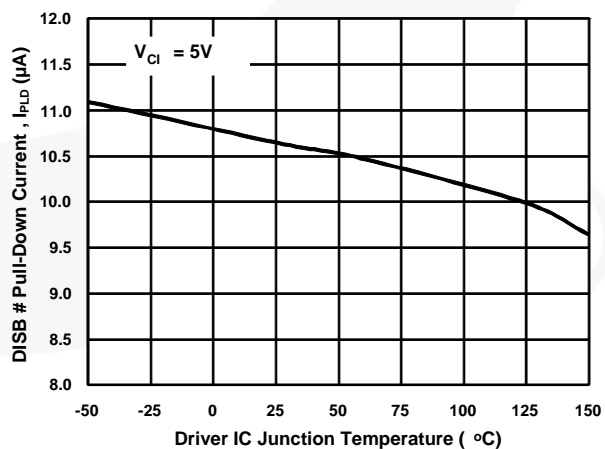


Figure 23. Disable Pull-Down Current vs. Temperature

Functional Description

The FDMF6707V is a driver-plus-FET module optimized for the synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each part is capable of driving speeds up to 1MHz.

VDRV and Disable (DISB#)

The VDRV pin is monitored by an under-voltage lockout (UVLO) circuit. When VDRV rises above $\sim 7.5V$, the driver is enabled. When VDRV falls below $\sim 7.0V$, the driver is disabled (GH, GL = 0). The driver can also be disabled by pulling the DISB# pin LOW (DISB# < V_{IL_DISB}), which holds both GL and GH LOW regardless of the PWM input state. The driver can be enabled by raising the DISB# pin voltage HIGH (DISB# > V_{IH_DISB}).

Table 1. UVLO and Disable Logic

| UVLO | DISB# | Driver State |
|------|-------|-----------------------|
| 0 | X | Disabled (GH, GL=0) |
| 1 | 0 | Disabled (GH, GL=0) |
| 1 | 1 | Enabled (See Table 2) |
| 1 | Open | Disabled (GH, GL=0) |

Note:

3. DISB# internal pull-down current source is 10 μA .

Thermal Warning Flag (THWN#)

The FDMF6707V provides a thermal warning flag (THWN#) to advise of over-temperature conditions. The thermal warning flag uses an open-drain output that pulls to CGND when the activation temperature (150°C) is reached. The THWN# output returns to high-impedance state once the temperature falls to the reset temperature (135°C). For use, the THWN# output requires a pull-up resistor, which can be connected to VCIN. THWN# does NOT disable the DrMOS module.

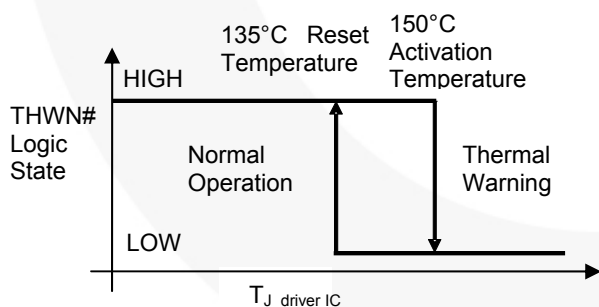


Figure 24. THWN Operation

3-State PWM Input

The FDMF6707V incorporates a 3-state 3.3V PWM input gate drive design. The 3-state gate drive has both logic HIGH level and LOW level, along with a 3-state shutdown window. When the PWM input signal enters and remains within the 3-state window for a defined hold-off time ($t_{D_HOLD-OFF}$), both GL and GH are pulled LOW. This feature enables the gate drive to shut down both high-and low-side MOSFETs to support features such as phase shedding, a common feature on multi-phase voltage regulators.

Exiting 3-State Condition

When exiting a valid 3-state condition, the FDMF6707V design follows the PWM input command. If the PWM input goes from 3-state to LOW, the low-side MOSFET is turned on. If the PWM input goes from 3-state to HIGH, the high-side MOSFET is turned on, as illustrated in Figure 25. The FDMF6707V design allows for short propagation delays when exiting the 3-state window (see *Electrical Characteristics*).

Low-Side Driver

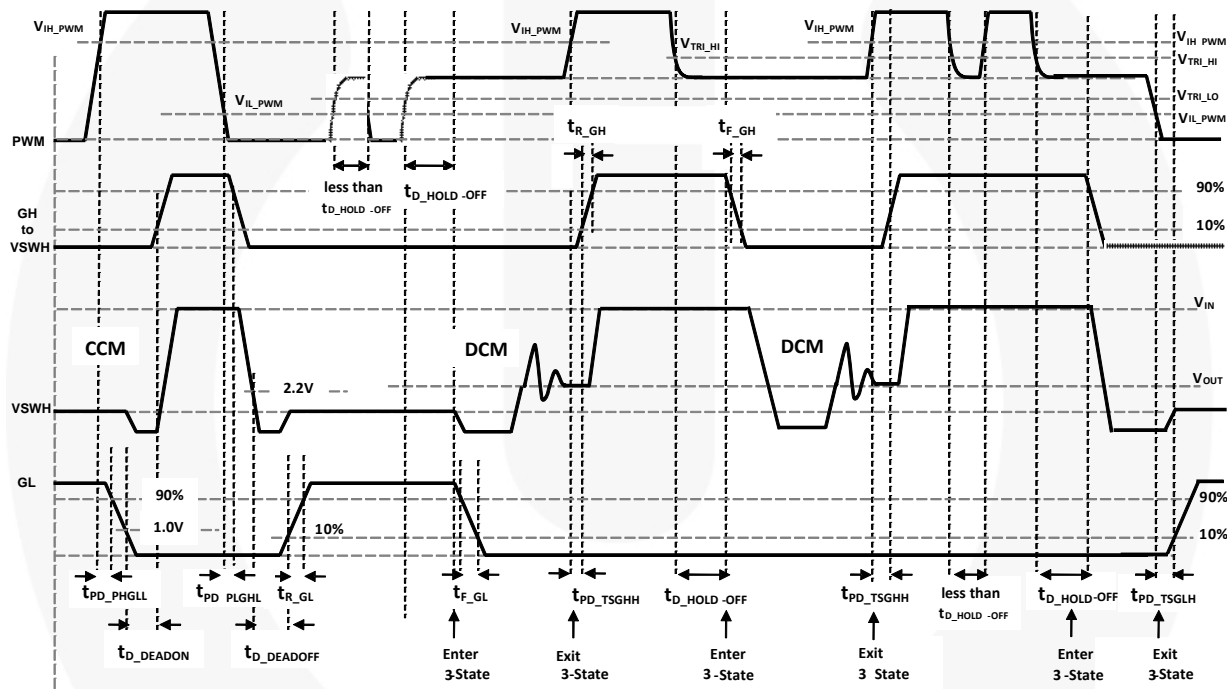
The low-side driver (GL) is designed to drive a ground-referenced low $R_{DS(ON)}$ N-channel MOSFET. The bias for GL is internally connected between VDRV and CGND. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the driver is disabled (DISB#=0V), GL is held LOW.

High-Side Driver

The high-side driver is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit consisting of the internal Schottky diode and external bootstrap capacitor (C_{BOOT}). During startup, V_{SWH} is held at PGND, allowing C_{BOOT} to charge to V_{DRV} through the internal diode. When the PWM input goes HIGH, GH begins to charge the gate of the high-side MOSFET (Q1). During this transition, the charge is removed from C_{BOOT} and delivered to the gate of Q1. As Q1 turns on, V_{SWH} rises to V_{IN} , forcing the BOOT pin to $V_{IN} + V_{BOOT}$, which provides sufficient V_{GS} enhancement for Q1. To complete the switching cycle, Q1 is turned off by pulling GH to V_{SWH} . C_{BOOT} is then recharged to V_{DRV} when V_{SWH} falls to PGND. GH output is in-phase with the PWM input. The high-side gate is held LOW when the driver is disabled or the PWM signal is held within the 3-state window for longer than the 3-state hold-off time, $t_{D_HOLD-OFF}$.

The driver IC design ensures minimum MOSFET dead time while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive adaptively to prevent simultaneous conduction. Figure 25 provides the relevant timing waveforms. To prevent overlap during the LOW-to-HIGH switching transition (Q2 off to Q1 on), the adaptive circuitry monitors the voltage at the GL pin. When the PWM signal goes HIGH, Q2 begins to turn off after a propagation delay (t_{PD_PHGLL}). Once the GL pin is discharged below $\sim 1V$, Q1 begins to turn on after adaptive delay t_{D_DEADON} .

To prevent overlap during the HIGH-to-LOW transition (Q1 off to Q2 on), the adaptive circuitry monitors the voltage at the VSWH pin. When the PWM signal goes LOW, Q1 begins to turn off after a propagation delay (t_{PD_PLGHL}). Once the VSWH pin falls below $\sim 2.2V$, Q2 begins to turn on after adaptive delay $t_{D_DEADOFF}$. Additionally, $V_{GS(Q1)}$ is monitored. When $V_{GS(Q1)}$ is discharged below $\sim 1.2V$, a secondary adaptive delay is initiated that results in Q2 being driven on after $t_{D_TIMEOUT}$, regardless of VSWH state. This function is implemented to ensure C_{BOOT} is recharged each switching cycle in the event that the VSWH voltage does not fall below the 2.2V adaptive threshold. Secondary delay $t_{D_TIMEOUT}$ is longer than $t_{D_DEADOFF}$.



Notes:

t_{PD_xxx} = propagation delay from external signal (PWM, SMOD#, etc.) to IC generated signal. Example (t_{PD_PHGLL} – PWM going HIGH to LS V_{GS} (GL) going LOW)

t_{D_xxx} = delay from IC generated signal to IC generated signal. Example ($t_{D_DEADON} - LS V_{GS} (GL) \text{ LOW to HS } V_{GS} (GH) \text{ HIGH}$)

PWM

$$t_{PD_PHGLL} = \text{PWM rise to LS } V_{GS} \text{ fall, } V_{IH_PWM} \text{ to 90\% LS } V_{GS}$$
$$t_{PD_PLGHL} = \text{PWM fall to HS } V_{GS} \text{ fall, } V_{IL_PWM} \text{ to } 90\% \text{ HS } V_{GS}$$
$$t_{PD_PHGHH} = \text{PWM rise to HS } V_{GS} \text{ rise, } V_{IH_PWM} \text{ to } 10\% \text{ HS } V_{GS} \text{ (SMOD\# held LOW)}$$

SMOD#

$$t_{PD_SLGLL} = \text{SMOD\# fall to LS } V_{GS} \text{ fall, } V_{IL_SMOD} \text{ to } 90\% \text{ LS } V_{GS}$$
$$t_{PD_SHGLH} = \text{SMOD\# rise to LS } V_{GS} \text{ rise, } V_{IH_SMOD} \text{ to } 10\% \text{ LS } V_{GS}$$

Exiting 3-state

$$t_{PD_TSGHH} = \text{PWM 3-state to HIGH to HS } V_{GS} \text{ rise, } V_{IH_PWM} \text{ to } 10\% \text{ HS } V_{GS}$$

t_{PD_TSGLH} = PWM 3-state to LOW to LS V_{GS} rise, V_{IL_PWM} to 10% LS V_{GS}

Dead Times

t_{D_DEADON} = LS V_{GS} fall to HS V_{GS} rise, LS-comp trip value (~1.0V GL) to 10% HS V_{GS}

t_{D DEADOFF} = VSWH fall to LS V_{GS} rise, SW-comp trip value (~2.2V VSWH) to 10% LS V_{GS}

Figure 25. PWM and 3-StateTiming Diagram

Skip Mode (SMOD#)

The SMOD function allows for higher converter efficiency under light-load conditions. During SMOD, the low-side FET gate signal is disabled (held LOW), preventing discharging of the output capacitors as the filter inductor current attempts reverse current flow – also known as “Diode Emulation” Mode.

When the SMOD# pin is pulled HIGH, the synchronous buck converter works in Synchronous Mode. This mode allows for gating on the low-side FET. When the SMOD# pin is pulled LOW, the low-side FET is gated off. If the SMOD# pin is connected to the PWM controller, the controller can actively enable or disable SMOD when the controller detects light-load condition from output current sensing. This pin is active LOW. See Figure 26 for timing delays.

Table 2. SMOD# Logic

| DISB# | PWM | SMOD# | GH | GL |
|-------|---------|-------|----|----|
| 0 | X | X | 0 | 0 |
| 1 | 3-State | X | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

Note:

- The SMOD feature is intended to have low propagation delay between the SMOD signal and the low-side FET VGS response time to control diode emulation on a cycle-by-cycle basis.

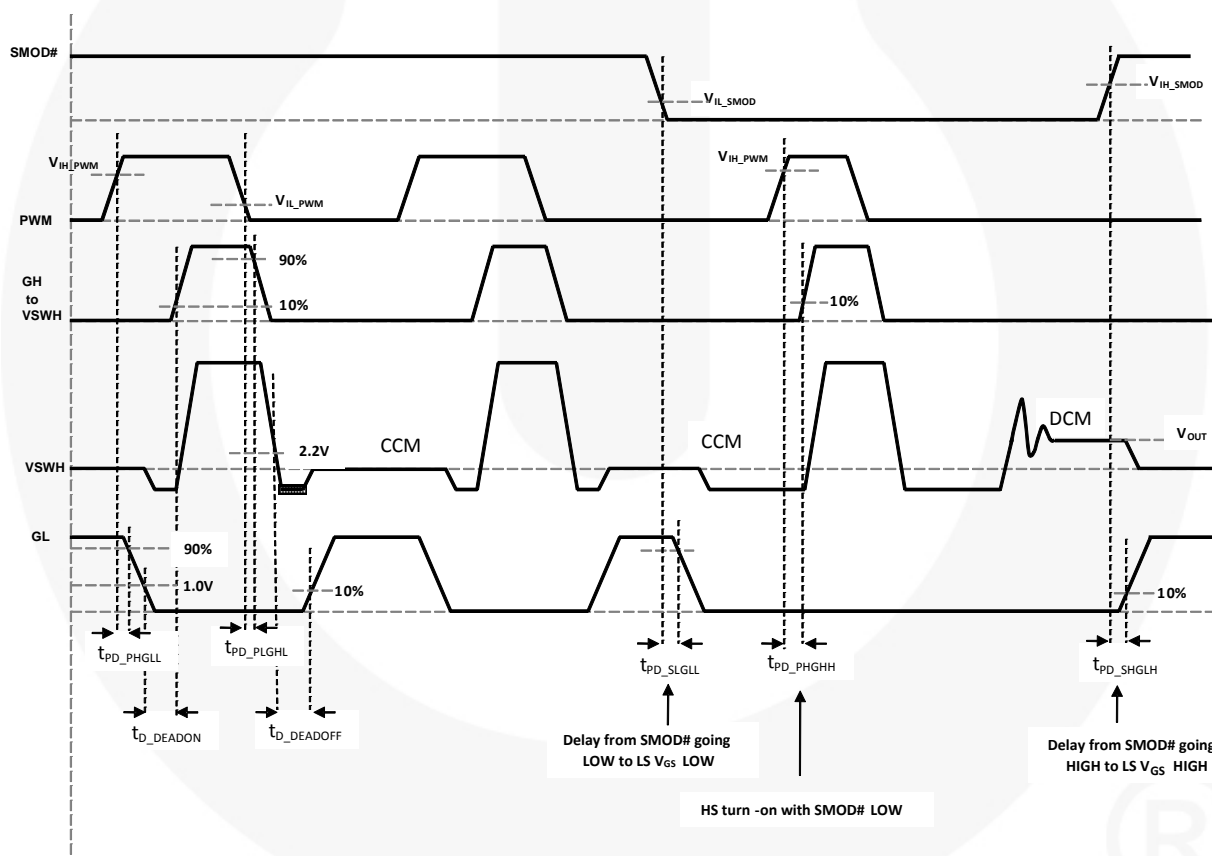


Figure 26. SMOD# Timing Diagram

Application Information

5V Linear Regulator Capacitor Selection

For the linear regulator output (VCIN), a local ceramic bypass capacitor is required for linear regulator stability. This capacitor is also needed to reduce noise and is used to supply the peak Power MOSFET low side gate current and boot capacitor charging current. Use at least a 1 μ F, X7R, or X5R capacitor. Keep this capacitor close to the VCIN pin and connect it to ground plane with vias. A bypass capacitor of 1 μ F, X7R or X5R, is also recommended from VDRV to ground.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}), as shown in Figure 27. A bootstrap capacitance of 100nF X7R or X5R capacitor is typically adequate. A series bootstrap resistor may be needed for specific applications to improve switching noise immunity. The

boot resistor may be required when operating near the maximum rated V_{IN} and is effective at controlling the high-side MOSFET turn-on slew rate and V_{SWH} overshoot. Typical R_{BOOT} values from 0.5 Ω to 2.0 Ω are effective in reducing V_{SWH} overshoot.

Power Loss and Efficiency

Measurement and Calculation

Refer to Figure 27 for power loss testing method. Power loss calculations are:

$$P_{IN} = (V_{IN} \times I_{IN}) + (V_{5V} \times I_{5V}) \text{ (W)}$$

$$P_{SW} = V_{SW} \times I_{OUT} \text{ (W)}$$

$$P_{OUT} = V_{OUT} \times I_{OUT} \text{ (W)}$$

$$P_{LOSS_MODULE} = P_{IN} - P_{SW} \text{ (W)}$$

$$P_{LOSS_BOARD} = P_{IN} - P_{OUT} \text{ (W)}$$

$$EFF_{MODULE} = 100 \times P_{SW} / P_{IN} \text{ (\%)}$$

$$EFF_{BOARD} = 100 \times P_{OUT} / P_{IN} \text{ (\%)}$$

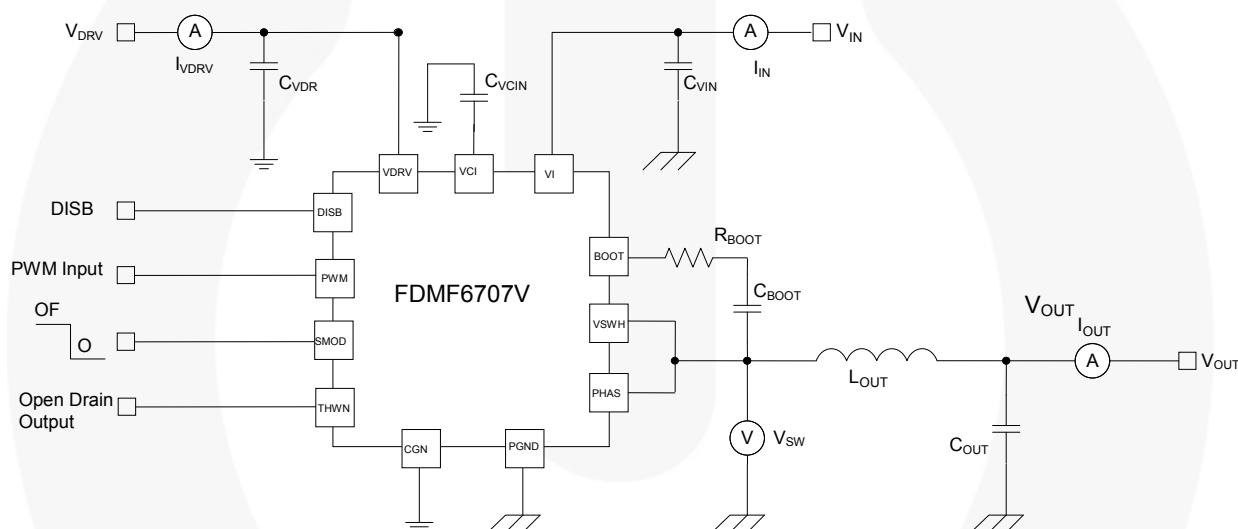


Figure 27. Power Loss Measurement Block Diagram

PCB Layout Guidelines

Figure 28 and Figure 29 provide the top and bottom views of an example of a proper layout for the FDMF6707V and critical components. All of the high-current paths, such as V_{IN} , V_{SWH} , V_{OUT} , and GND copper, should be short and wide for low inductance and resistance. This technique achieves a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

The following guidelines are recommendations for the PCB designer:

1. Input ceramic bypass capacitors must be placed close to the V_{IN} and PGND pins. This helps reduce the high-current power loop inductance and the input current ripple induced by the power MOSFET switching operation.

2. The V_{SWH} copper trace serves two purposes. In addition to being the high-frequency current path from the DrMOS package to the output inductor, it also serves as a heat sink for the low-side MOSFET in the DrMOS package. The trace should be short and wide enough to present a low-impedance path for the high-frequency, high-current flow between the DrMOS and inductor to minimize losses and temperature rise. Note that the V_{SWH} node is a high-voltage and high-frequency switching node with high noise potential. Care should be taken to minimize coupling to adjacent traces. Since this copper trace also acts as a heat sink for the lower FET, balance using the largest area possible to improve DrMOS cooling while maintaining acceptable noise emission.

3. An output inductor should be located close to the FDMF6707V to minimize the power loss due to the VSWH copper trace. Care should also be taken so the inductor dissipation does not heat the DrMOS.
4. PowerTrench® MOSFETs are used in the output stage. The power MOSFETs are effective at minimizing ringing due to fast switching. In most cases, no VSWH snubber is required. If a snubber is used, it should be placed close to the VSWH and PGND pins. The resistor and capacitor need to be of proper size for the power dissipation.
5. VCIN, VDRV, and BOOT capacitors should be placed as close as possible to the VCIN to CGND, VDRV to CGND, and BOOT to PHASE pins to ensure clean and stable power. Routing width and length should be considered as well.
6. Include a trace from PHASE to VSWH to improve noise margin. Keep the trace as short as possible.
7. The layout should include a placeholder to insert a small-value series boot resistor (R_{BOOT}) between the boot capacitor (C_{BOOT}) and DrMOS BOOT pin. The BOOT-to-VSWH loop size, including R_{BOOT} and C_{BOOT} , should be as small as possible. The boot resistor may be required when operating near the maximum rated V_{IN} . The boot resistor is effective at controlling the high-side MOSFET turn-on slew rate and VSWH overshoot. R_{BOOT} can improve noise operating margin in synchronous buck designs that may have noise issues due to ground bounce or high positive and negative VSWH ringing. However, inserting a boot resistance lowers the DrMOS efficiency. Efficiency versus noise trade-offs must be considered. R_{BOOT} values from 0.5Ω to 2.0Ω are typically effective in reducing VSWH overshoot.
8. The VIN and PGND pins handle large current transients with frequency components greater than 100MHz. If possible, these pins should be connected directly to the VIN and board GND planes. The use of thermal relief traces in series with these pins is **discouraged** because this adds inductance to the power path. Added inductance in series with the VIN or PGND pin degrades system noise immunity by increasing positive and negative VSWH ringing.
9. CGND pad and PGND pins should be connected to the GND plane copper with multiple vias for stable grounding. Poor grounding can create a noise transient offset voltage level between CGND and PGND. This could lead to faulty operation of the gate driver and MOSFETs.
10. Ringing at the BOOT pin is most effectively controlled by close placement of the boot capacitor. Do not add an additional BOOT to the PGND capacitor: this may lead to excess current flow through the BOOT diode.
11. The SMOD# and DISB# pins have weak internal pull-up and pull-down current sources, respectively. These pins should not have any noise filter capacitors. Do not float these pins unless absolutely necessary.
12. Use multiple vias on each copper area to help distribute current flow and heat conduction. Vias should be relatively large and of reasonably low inductance. Critical high-frequency components, such as R_{BOOT} , C_{BOOT} , the RC snubber, and bypass capacitors should be located as close to the respective DrMOS module pins as possible on the top layer of the PCB. If this is not feasible, they should be connected from the backside through a network of low-inductance vias.

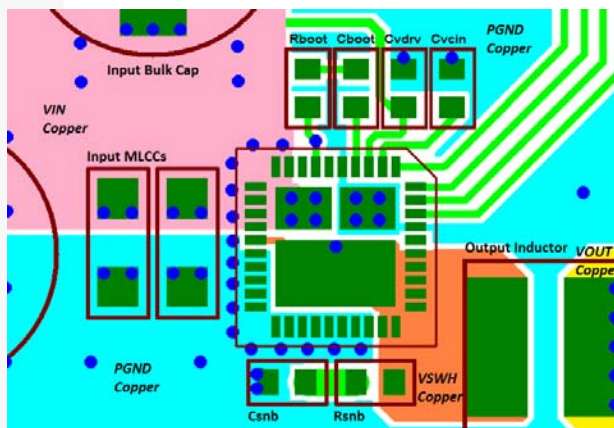


Figure 28. PCB Layout Example (Top View)

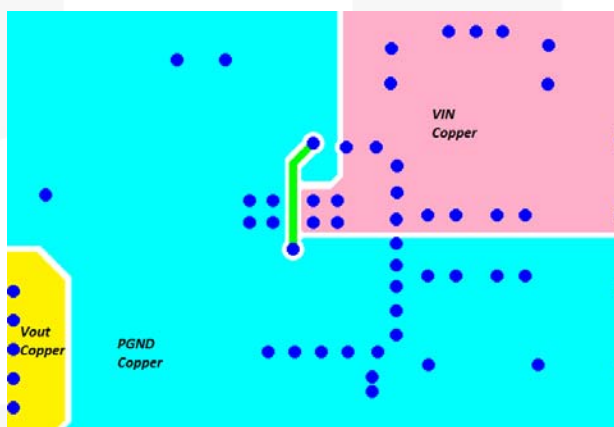


Figure 29. PCB Layout Example (Bottom View)

Physical Dimensions

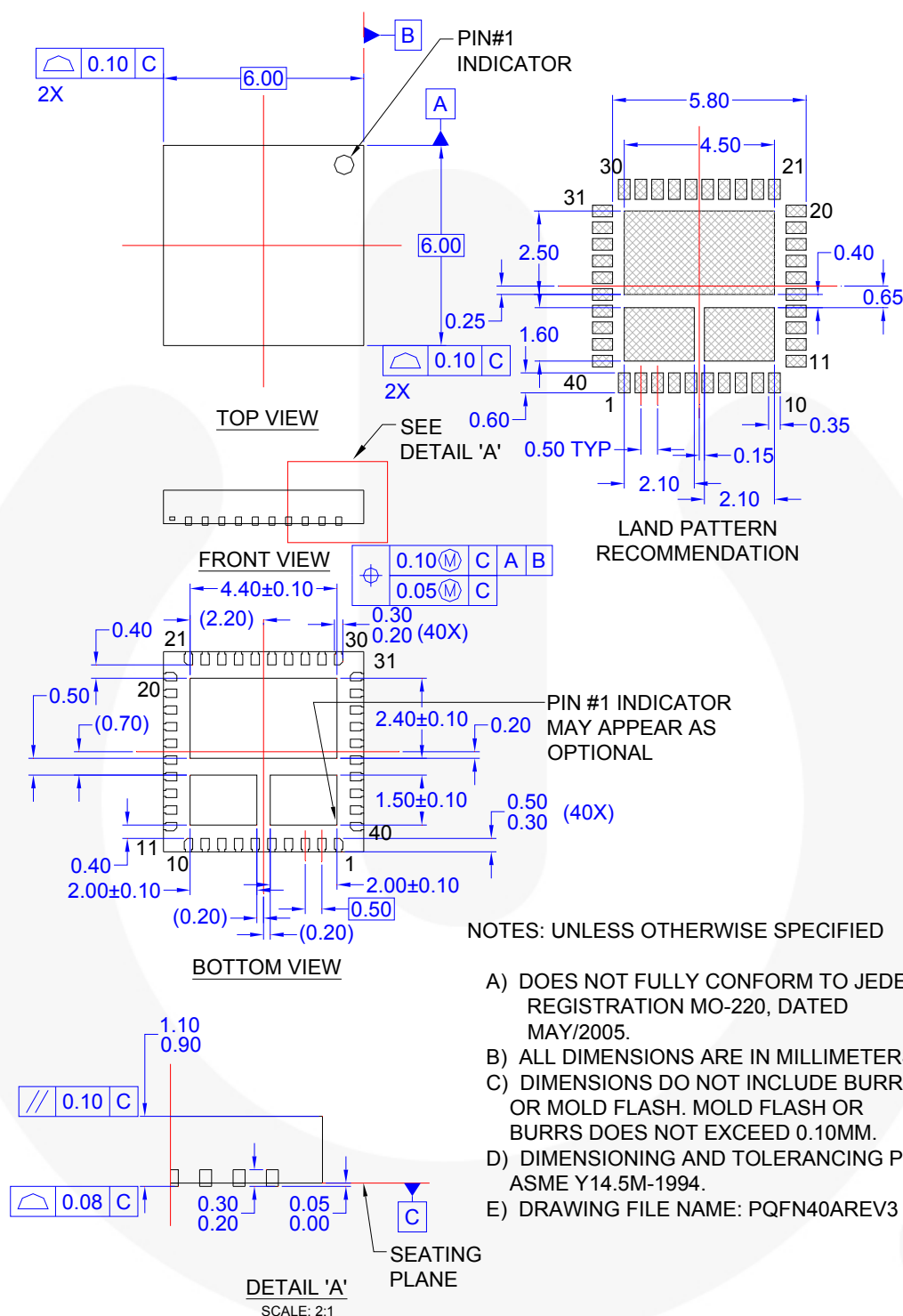


Figure 30. 40-Lead, Clipbond PQFN DrMOS, 6.0x6.0mm Package



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