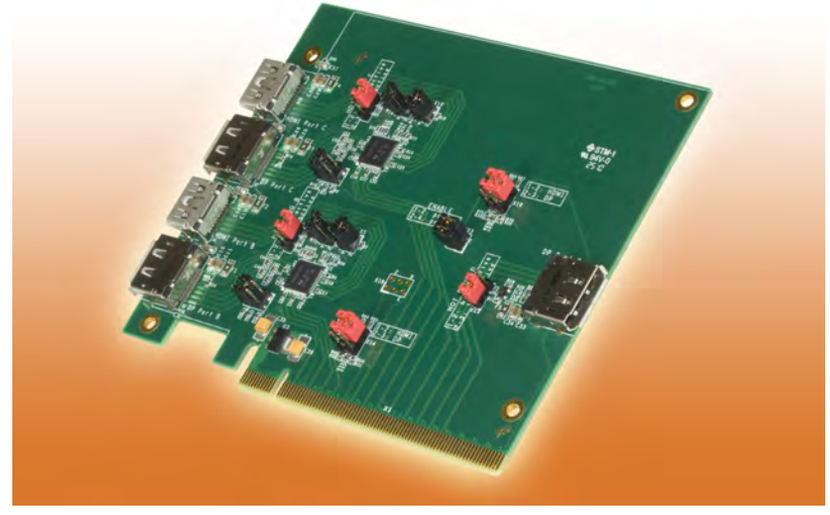

Multiple Graphics Channel Adapter

Short description of congatec's conga-HDMI/DisplayPort adapter.

Short Description

Revision 1.1

Revision History

Revision	Date (dd.mm.yy)	Author	Changes
1.0	07.12.10	GDA	Official release
1.1	20.12.11	GDA	Changed name of product to conga-HDMI/DisplayPort adapter from conga-ADD2DP.

Preface

This short description provides information about the features, connectors and schematics for the conga-HDMI/DisplayPort adapter.

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Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Link to connector layout diagram

This link icon is located in the top right corner of each page. It provides a direct link to the connector layout on page 11 of this document.

Terminology

Term	Description
MGCA	Multi Graphics Channel Adapter
HDMI	High Definition Multimedia Interface
DVI	Digital Visual Interface
DP	DisplayPort
PEG Port	PCI Express Graphics Port
ADD2	Advanced Digital Display 2nd Generation
TMDS	Transition Minimized Differential Signaling
SDVO	Serial Digital Video Output
DDC	Display Data Channel (I2C bus to read display information)

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Contents

1 Introduction

The latest Intel® chipsets used on congatec COM Express™ modules not only provide LVDS and SDVO graphics interfaces but also the new generation of digital display interfaces such as HDMI and DisplayPort.

1.1 High Definition Multimedia Interface (HDMI)

HDMI is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data and audio data into TMDS for digital transmission and is fully backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video. Additionally, HDMI adds the ability to send up to 8 separate channels of uncompressed digital audio and auxiliary control data during the horizontal and vertical blanking intervals of the TDMS video stream.

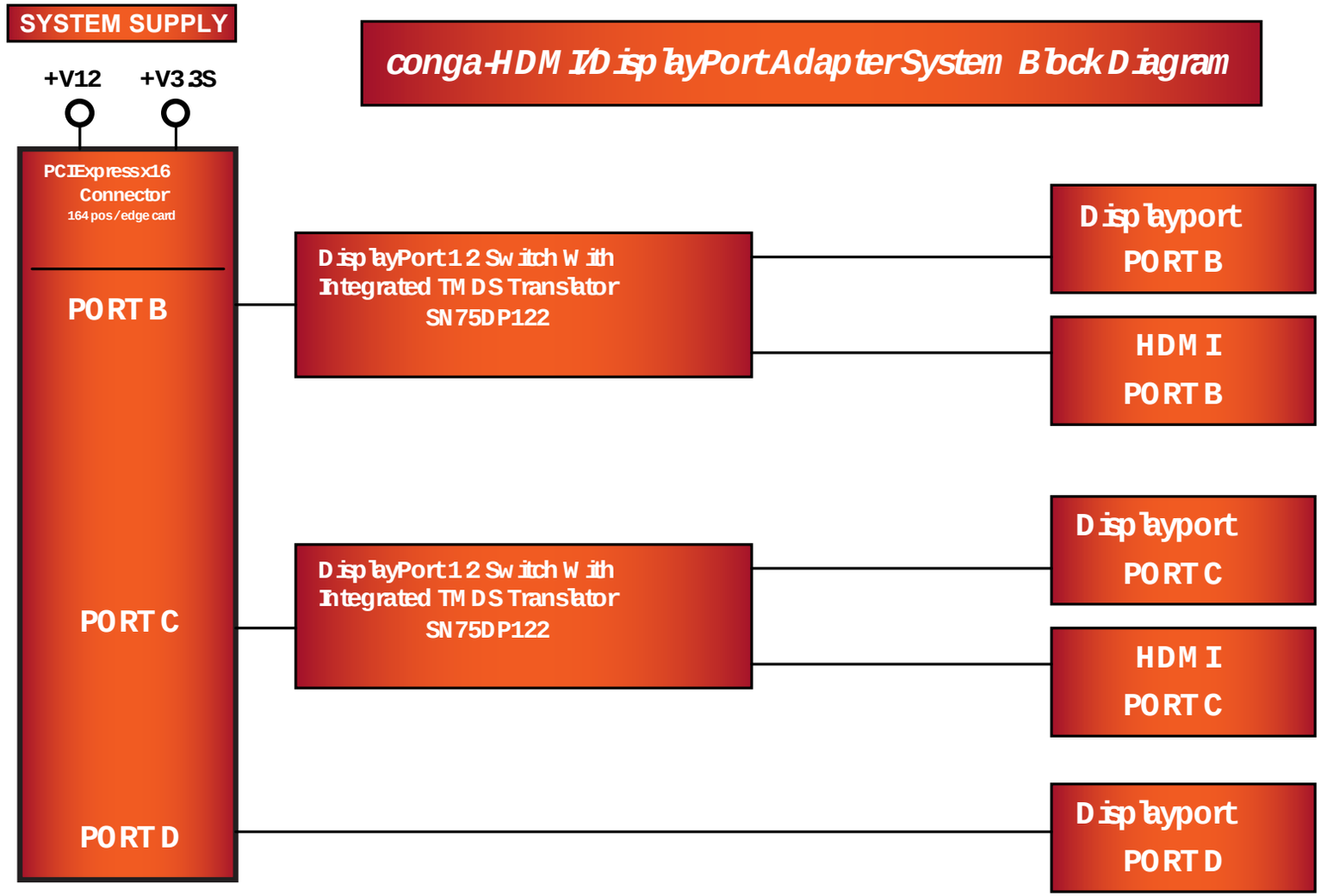
1.2 DisplayPort (DP)

DP is an open industry standard digital display interface that is under development within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect intended to be used primarily between a computer and its display monitor.

conga-HDMI/DisplayPort is an adapter card for testing the new digital display interfaces (DDI) HDMI and DisplayPort on Type 2 COM Express modules. Intel®'s GM45 GMCH was the first chipset supporting these new DDIs. With this chipset, the HDMI and DisplayPort signals are multiplexed with the PEG interface and were made available externally via the COM Express Type 2 definition. Future Intel® chipsets, such as the HM55/QM57 do not have the DDIs multiplexed with the PEG port so it's up to the vendor to either route the PEG or the HDMI/DisplayPort/SDVO signals to the COM Express Type 2 pins dedicated to PEG. The conga-HDMI/DisplayPort adapter allows the connection of HDMI and DisplayPort devices to COM Express Type 2 systems supporting the new DDIs on the PEG port pins. The concept is pretty much the same as with ADD2 cards, which are used to connect 3rd party transmitters to Intel®'s SDVO interface. As with HDMI and DP, the SDVO interface is also multiplexed with the PCI Express graphics port.

Note

For more information, refer to congatec Application Note 17 "HDMI and DisplayPort Implementation" that can be found on the congatec website. This document also describes how to enable HDMI and DisplayPort in the BIOS setup program.



The conga-HDMI/DisplayPort adapter block diagram helps understand the functions the card provides.

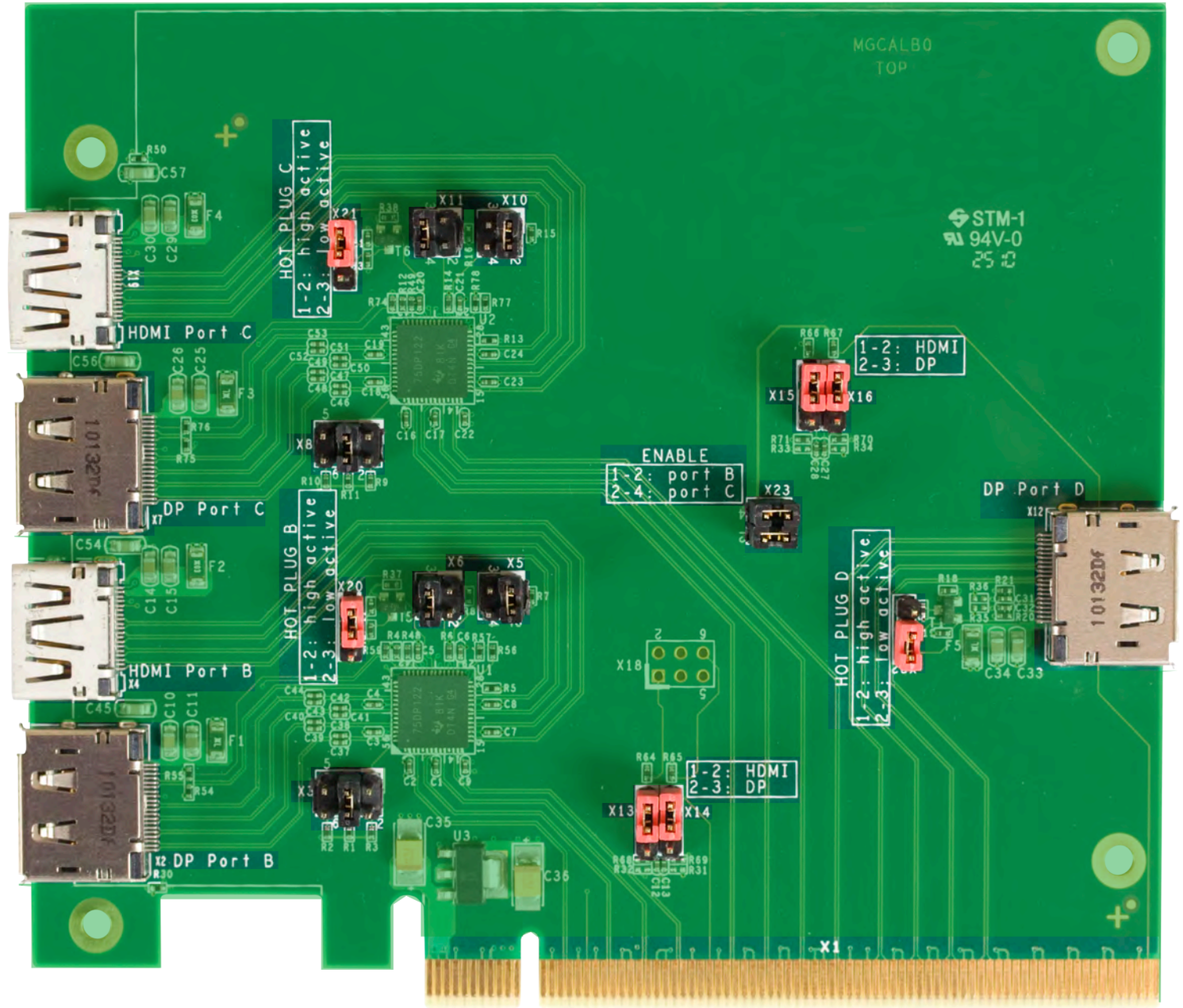
The Texas Instrument's SN75DP122 is a one Dual-Mode DisplayPort input to one Dual-Mode DisplayPort output or one TMDS output. The TMDS output has a built in level translator compliant with Digital Video Interface (DVI) 1.0 and High Definition Multimedia Interface (HDMI) 1.3b.

When inserting the conga-HDMI/DisplayPort adapter into the PEG port connector on the carrier board, the Intel® GM45 chipset is automatically strapped to support DisplayPort or HDMI instead of the PEG port.

2 Connector Layout

The connector layout picture on the right shows the location of the connectors and the jumpers. Select the Adobe 'Zoom-In-Tool' and zoom in on a given component to see the descriptive text. Hover over the component and the 'Zoom-In-Tool' will change indicating there is a link. Click on the link to navigate to the area in the document where the component is described in detail.

Use the mouse icon in the top left hand corner of the destination page to return to the connector layout picture.



3 Connectors

The following section describes the connectors located on the conga-HDMI/DisplayPort adapter. Each connector's pinout is listed as well a description of the mating connector that should be used to connect to the specific connector located on the conga-HDMI/DisplayPort adapter.

3.1 X1 PEG Slot Finger Edge Pinout

Table 1 Shared signals for PCI Express, SDVO, HDMI and DisplayPort on congatec COM Express™ modules

COM Express™		X16 PCI Express		Corresponds with SDVO signal		Corresponds with HDMI signal		Corresponds with DisplayPort signal	
Pin	Name	Pin	Name	Pin Name	Description	Pin Name	Description	Pin Name	Description
D52	PEG_TX[0]+	B14	HSOp(0)	SDVOB_RED+	Digital Video B red output differential pair	TMDS_B_DATA2+	HDMI Port B Data2 output differential pair.	DPB_LANE0+	DisplayPort B Lane0 output differential pair.
D53	PEG_TX[0]-	B15	HSOn(0)	SDVOB_REDSerial		TMDS_B_DATA2-		DPB_LANE0-	
D55	PEG_TX[1]+	B19	HSOp(1)	SDVOB_GRN+	Digital Video B green output differential pair	TMDS_B_DATA1+	HDMI Port B Data1 output differential pair.	DPB_LANE1+	DisplayPort B Lane1 output differential pair.
D56	PEG_TX[1]-	B20	HSOn(1)	SDVOB_GRNSerial		TMDS_B_DATA1-		DPB_LANE1-	
D58	PEG_TX[2]+	B23	HSOp(2)	SDVOB_BLU+	Digital Video B blue output differential pair	TMDS_B_DATA0+	HDMI Port B Data0 output differential pair.	DPB_LANE2+	DisplayPort B Lane2 output differential pair.
D59	PEG_TX[2]-	B24	HSOn(2)	SDVOB_BLUSerial		TMDS_B_DATA0-		DPB_LANE2-	
D61	PEG_TX[3]+	B27	HSOp(3)	SDVOB_CK+	Digital Video B clock output differential pair	TMDS_B_CLK +	HDMI Port B Clock output differential pair.	DPB_LANE3+	DisplayPort B Lane3 output differential pair.
D62	PEG_TX[3]-	B28	HSOn(3)	SDVOB_CKSerial		TMDS_B_CLK -		DPB_LANE3-	
D65	PEG_TX[4]+	B33	HSOp(4)	SDVOC_RED+	Digital Video C red output differential pair	TMDS_C_DATA2+	HDMI Port C Data2 output differential pair.	DPC_LANE0+	DisplayPort C Lane0 output differential pair.
D66	PEG_TX[4]-	B34	HSOn(4)	SDVOC_REDSerial		TMDS_C_DATA2-		DPC_LANE0-	
D68	PEG_TX[5]+	B37	HSOp(5)	SDVOC_GRN+	Digital Video C green output differential pair	TMDS_C_DATA1+	HDMI Port C Data1 output differential pair.	DPC_LANE1+	DisplayPort C Lane1 output differential pair.
D69	PEG_TX[5]-	B38	HSOn(5)	SDVOC_GRNSerial		TMDS_C_DATA1-		DPC_LANE1-	
D71	PEG_TX[6]+	B41	HSOp(6)	SDVOC_BLU+	Digital Video C blue output differential pair	TMDS_C_DATA0+	HDMI Port C Data0 output differential pair.	DPC_LANE2+	DisplayPort C Lane2 output differential pair.
D72	PEG_TX[6]-	B42	HSOn(6)	SDVOC_BLUSerial		TMDS_C_DATA0-		DPC_LANE2-	
D74	PEG_TX[7]+	B45	HSOp(7)	SDVOC_CK+	Digital Video C clock output differential pair	TMDS_C_CLK +	HDMI Port C Clock output differential pair.	DPC_LANE3+	DisplayPort C Lane3 output differential pair.
D75	PEG_TX[7]-	B46	HSOn(7)	SDVOC_CKSerial		TMDS_C_CLK -		DPC_LANE3-	
D78	PEG_TX[8]+	B50	HSOp(8)	-		-		DPD_LANE0+	DisplayPort D Lane0 output differential pair.
D79	PEG_TX[8]-	B51	HSOn(8)	-		-		DPD_LANE0-	
D81	PEG_TX[9]+	B54	HSOp(9)	-		-		DPD_LANE1+	DisplayPort D Lane1 output differential pair.
D82	PEG_TX[9]-	B55	HSOn(9)	-		-		DPD_LANE1-	
D85	PEG_TX[10]+	B58	HSOp(10)	-		-		DPD_LANE2+	DisplayPort D Lane2 output differential pair.
D86	PEG_TX[10]-	B59	HSOn(10)	-		-		DPD_LANE2-	
D88	PEG_TX[11]+	B62	HSOp(11)	-		-		DPD_LANE3+	DisplayPort D Lane3 output differential pair.
D89	PEG_TX[11]-	B63	HSOn(11)	-		-		DPD_LANE3-	
C52	PEG_RX[0]+	A16	HSIp(0)	SDVO_TVCLKIN+	Digital Video TVOUT synchronization clock input differential pair	-		-	
C53	PEG_RX[0]-	A17	HSIn(0)	SDVO_TVCLKINSerial		-		-	
C55	PEG_RX[1]+	A21	HSIp(1)	SDVOB_INT+	Digital Video B interrupt input differential pair	-		-	
C56	PEG_RX[1]-	A22	HSIn(1)	SDVOB_INTSerial		-		-	
C58	PEG_RX[2]+	A25	HSIp(2)	SDVO_FLDSTALL+	Digital Video Field Stall input differential pair	-		DPB_AUX+	DisplayPort B Aux input differential pair.
C59	PEG_RX[2]-	A26	HSIn(2)	SDVO_FLDSTALLSerial		-		DPB_AUX-	

COM Express™		x16 PCI Express		Corresponds with SDVO signal		Corresponds with HDMI signal		Corresponds with DisplayPort signal	
Pin	Name	Pin	Name	Pin Name	Description	Pin Name	Description	Pin Name	Description
C61	PEG_RX[3]+	A29	HSIp(3)	-		TMDS_B_HPD#	HDMI Port B Hot-plug detect.	DPB_HPD#	DisplayPort B Hot-plug detect.
C65	PEG_RX[5]+	A39	HSIp(5)	SDVOC_INT+	Digital Video C interrupt input differential pair	-		-	
C66	PEG_RX[5]-	A40	HSIn(5)	SDVOC_INTSerial		-		-	
C71	PEG_RX[6]+	A43	HSIp(6)	-		-		DPC_AUX+	DisplayPort C Aux input differential pair.
C72	PEG_RX[6]-	A44	HSIn(6)	-		-		DPC_AUX-	
C74	PEG_RX[7]+	A47	HSIp(7)	-		TMDS_C_HPD#	HDMI Port C Hot-plug detect.	DPC_HPD#	DisplayPort C Hot-plug detect.
C85	PEG_RX[10]+	A60	HSIp(10)	-		-		DPD_AUX+	DisplayPort D Aux input differential pair.
C86	PEG_RX[10]-	A61	HSIn(10)	-		-		DPD_AUX-	
C88	PEG_RX[11]+	A64	HSIp(11)	-		-		DPD_HPD#	DisplayPort D Hot-plug detect.
D73	SDVO_CLK	B17	PRSNT#2	SDVO_I2C_CK	SDVO I²C clock line to set up SDVO peripherals	DDPB_CTRLCLK	HDMI port B Control Clock	-	
C73	SDVO_DATA	B31	PRSNT#2	SDVO_I2C_DAT	SDVO I²C data line to set up SDVO peripherals	DDPB_CTRLDATA	HDMI port B Control Data DDPB_CTRLDATA is a boot strap signal (see note below)	DDPB_CTRLDATA	DDPB_CTRLDATA is a boot strap signal (see note below)
D63	RSVD	A1	PRSNT#1	-		DDPC_CTRLCLK	HDMI port C Control Clock	-	
D64	RSVD	B81	PRSNT#2	-		DDPC_CTRLDATA	HDMI port C Control Data DDPC_CTRLDATA is a boot strap signal (see note below)	DDPC_CTRLDATA	DDPC_CTRLDATA is a boot strap signal (see note below)
							Not supported on conga-BM45, conga-CS45 and conga-BS45		

3.2 DisplayPort Connectors X2, X7 and X12

Table 2 DisplayPort Connector Shared Signals Pinout

Pin	Signal	Description	Pin	Signal	Description
1	DP_LANE0+	DisplayPort Lane 0 (positive)	2	GND	Ground
3	DP_LANE0-	DisplayPort Lane 0 (negative)	4	DP_LANE1+	DisplayPort Lane 1 (positive)
5	GND	Ground	6	DP_LANE1-	DisplayPort Lane 1 (negative)
7	DP_LANE2+	DisplayPort Lane 2 (positive)	8	GND	Ground
9	DP_LANE2-	DisplayPort Lane 2 (negative)	10	DP_LANE3+	DisplayPort Lane 3 (positive)
11	GND	Ground	12	DP_LANE3-	DisplayPort Lane 3 (negative)
13	CONFIG1	Configuration Pin 1 (connected to Ground)	14	CONFIG2	Configuration Pin 2 (connected to Ground)
15	DP_AUX+	Auxiliary Channel (positive)	16	GND	Ground
17	DP_AUX-	Auxiliary Channel (negative)	18	DP_HPD#	Hot Plug Detect
19	RETURN	Return For Power	20	DP_PWR	Power For Connector

3.3 HDMI Connectors X4 and X19

Table 3 HDMI Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	TMDS Data 2+	HDMI Lane 2 (positive)	2	TMDS Data 2 Shield	Shield of Data 2 pair
3	TMDS Data 2-	HDMI Lane 2 (negative)	4	TMDS Data 1+	HDMI Lane 1 (positive)
5	TMDS Data 1 Shield	Shield of Data 1 pair	6	TMDS Data 1-	HDMI Lane 1 (negative)
7	TMDS Data 0+	HDMI Lane 0 (positive)	8	TMDS Data0 Shield	Shield of Data 0 pair
9	TMDS Data 0-	HDMI Lane 0 (negative)	10	TMDS Clock-	HDMI Clock (positive)
11	TMDS Clock Shield	Shield of Clock pair	12	TMDS Clock-	HDMI Clock (negative)
13	CEC	Consumer Electronics Control Interface	14	Reserved	N.C.
15	DDC Clock	DDC based control signal (clock)	16	DDC Data	DDC based control signal (data)
17	GND	Ground	18	+5V	+5V Power Supply
19	HPD	Hot plug detect			

4 Configuration

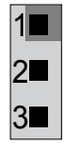
4.1 Hot Plug Detection

The active level of the hot-plug detection signal has changed between the Intel® Montevina and the more recent Calpella platform. For this reason it was necessary to add three jumpers on the conga-HDMI/DisplayPort adapter to set the active level for the hot-plug signal from the HDMI/DP interface.

4.1.1 Jumper Configurations

Table 4 X20 Hot-Plug Detection active level for Port B

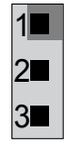
Jumper X20



Jumper X20	Configuration
1 - 2	High active hot-plug detect signal (default)
2 - 3	Low active hot-plug detect signal

Table 5 X21 Hot-Plug Detection active level for Port C

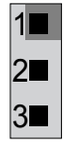
Jumper X21



Jumper X21	Configuration
1 - 2	High active hot-plug detect signal (default)
2 - 3	Low active hot-plug detect signal

Table 6 X22 Hot-Plug Detection active level for Port D

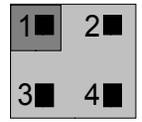
Jumper X22



Jumper X22	Configuration
1 - 2	High active hot-plug detect signal (default)
2 - 3	Low active hot-plug detect signal

Table 7 X23 Enable Port B and C

Jumper X23



Jumper X23	Configuration
1 - 2	Set to enable port B (default)
3 - 4	Set to enable port C (default)

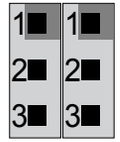
4.2 DDC Bus Selection

In order to provide the correct DDC Bus to the HDMI/DP switch, it was necessary to design-in jumpers to select either the HDMI or DP DDC bus routed to the switch.

4.2.1 Jumper Configurations

Table 8 X13/X14 DDC Bus Selection for Port B

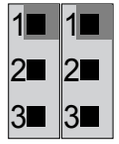
Jumper X13/X14



Jumper X13/X14	Configuration
1 - 2	HDMI
2 - 3	DisplayPort (default)

Table 9 X15/X16 DDC Bus Selection for Port C

Jumper X15/X16



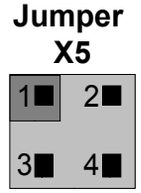
Jumper X15/X16	Configuration
1 - 2	HDMI
2 - 3	DisplayPort (default)

4.3 HDMI/DVI Connector Selection

The DisplayPort switch can support HDMI and DVI on the TMDS output. Although the conga-HDMI/DisplayPort adapter does not have a DVI connector, it is possible to select the connector type for Port B and Port C via two jumpers.

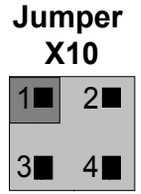
4.3.1 Jumper Configurations

Table 10 X5 DVI/HDMI Connector Selection for Port B TMDS



Jumper X5	Configuration
1 - 2	HDMI (default)
3 - 4	DVI

Table 11 X10 DVI/HDMI Connector Selection for Port C TMDS



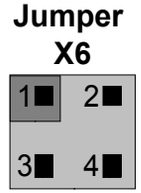
Jumper X10	Configuration
1 - 2	HDMI (default)
3 - 4	DVI

4.4 HDMI/DP Priority Selection

In a situation where a DP and a HDMI display are connected at the same time to a port, priority can be given to either one of them using two jumpers.

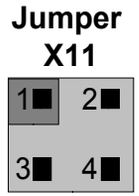
4.4.1 Jumper Configurations

Table 12 X6 DP/HDMI Priority Selection for Port B



Jumper X6	Configuration
1 - 2	TMDS port has priority
3 - 4	DisplayPort has priority (default)

Table 13 X11 DP/HDMI Priority Selection for Port C



Jumper X11	Configuration
1 - 2	TMDS port has priority
3 - 4	DisplayPort has priority (default)

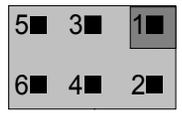
4.5 DisplayPort Link

The SN75DP122 is designed to support DisplayPort's high speed differential main link through the DisplayPort port. The main link I/O of the SN75DP122 are designed to track the magnitude and frequency characteristics of the input waveform and replicate them on the output. A feature has also been incorporated in the SN75DP122 to either increase or decrease the output amplitude via the resistor connected between the DPVADJ pin and ground. The two jumper fields X3 and X8 help to select the resistors for this feature. **Do not change these jumpers**.

4.5.1 Jumper Configurations

Table 14 X3 DisplayPort Link Characteristics for Port B

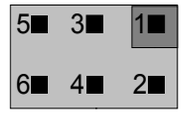
Jumper X3



Jumper X3	Configuration
1 - 2	Main link displayport output has an increased voltage swing
3 - 4	Main link displayport output has a nominal voltage swing (default)
5 - 6	Main link displayport output has a decreased voltage swing

Table 15 X8 DisplayPort Link Characteristics for Port C

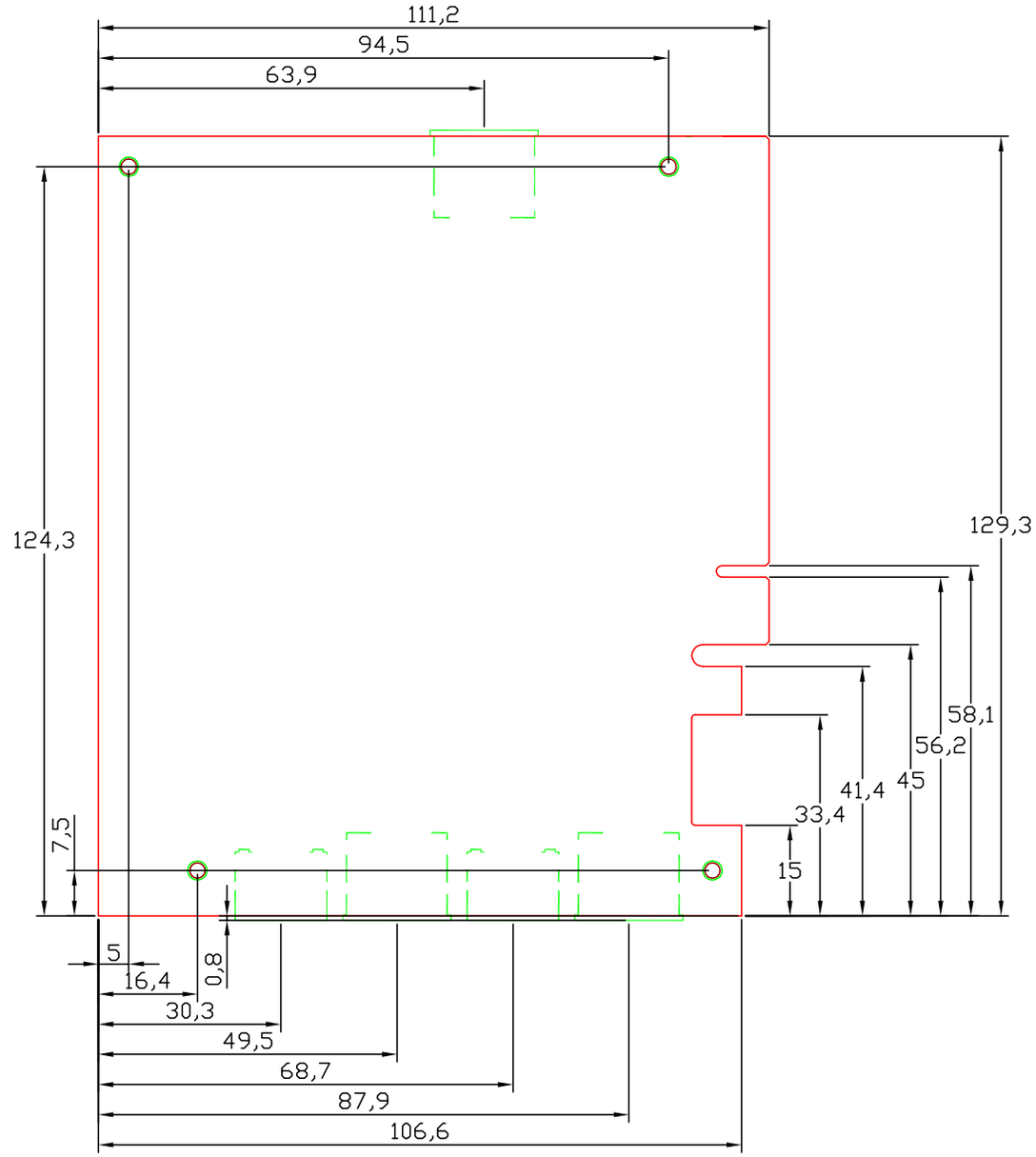
Jumper X8



Jumper X8	Configuration
1 - 2	Main link displayport output has an increased voltage swing
3 - 4	Main link displayport output has a nominal voltage swing (default)
5 - 6	Main link displayport output has a decreased voltage swing

5 Mechanical Dimensions

Mechanical dimensions of the conga-HDMI/DisplayPort adapter. All measurements are in millimeters.



6 Maximum Ratings

6.1 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. The maximum operating temperature refers to any measurable spot on the card's surface.

Humidity specifications are for non-condensing conditions.

AMEYA360

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