74HC123; 74HCT123

Dual retriggerable monostable multivibrator with reset

Rev. 9 — 19 January 2015 Product data sheet

1. General description

The 74HC123; 74HCT123 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC123; 74HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods:

1. The basic pulse is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input (n$\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, n$\overline{Q}$ = LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input n$\overline{RD}$, which also inhibits the triggering.
3. An internal connection from n$\overline{RD}$ to the input gates makes it possible to trigger the circuit by a HIGH-going signal at input n$\overline{RD}$ as shown in Table 3.

Schmitt-trigger action in the n$\overline{A}$ and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

The 74HC123; 74HCT123 are identical to the 74HC423; 74HCT423 but can be triggered via the reset input.

2. Features and benefits

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC123N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT123N				
74HC123D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT123D				
74HC123DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT123DB				
74HC123PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT123PW				
74HC123BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

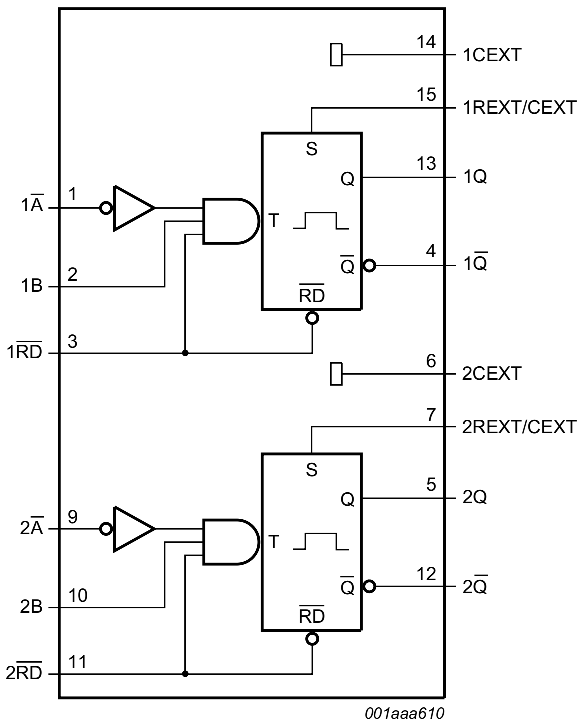


Fig 1. Functional diagram

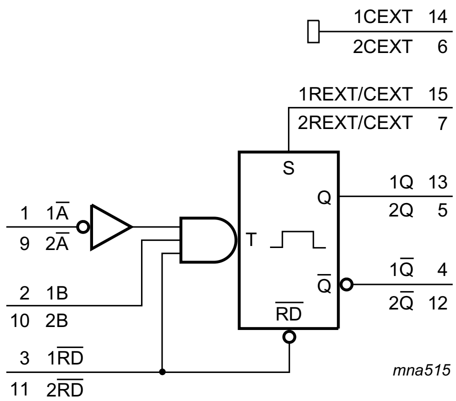


Fig 2. Logic symbol

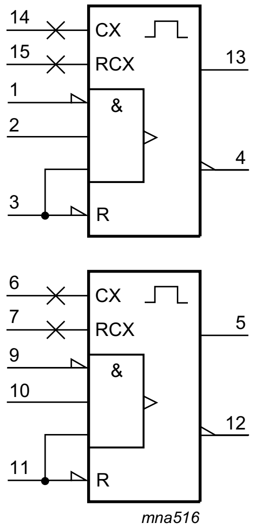


Fig 3. IEC logic symbol

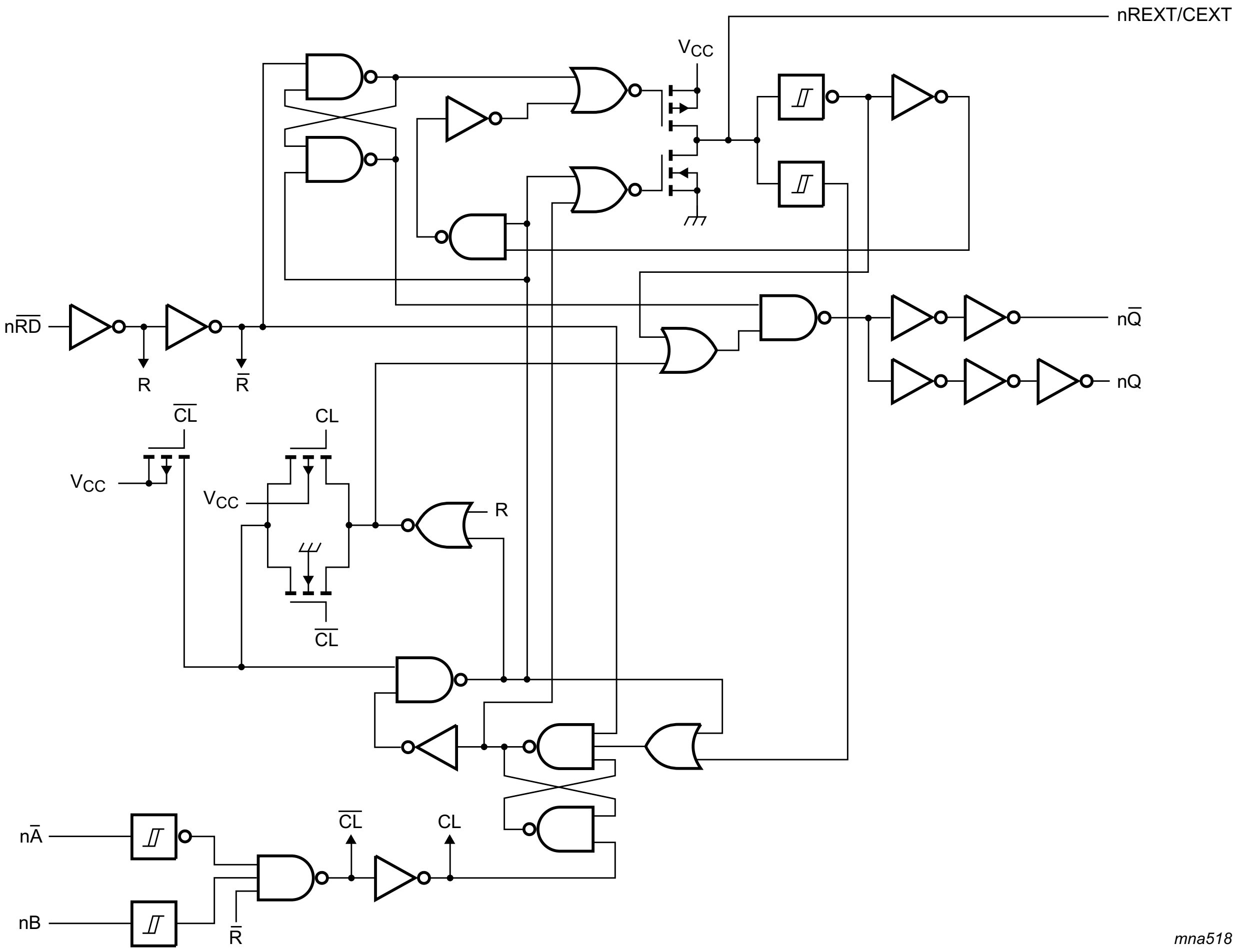


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

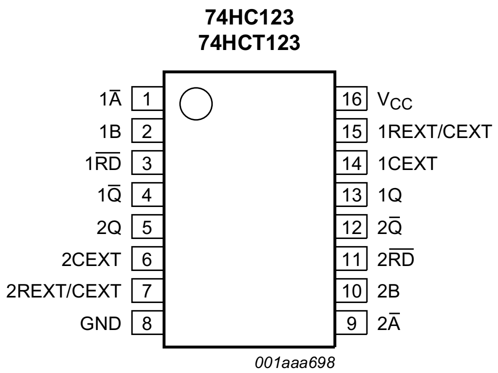
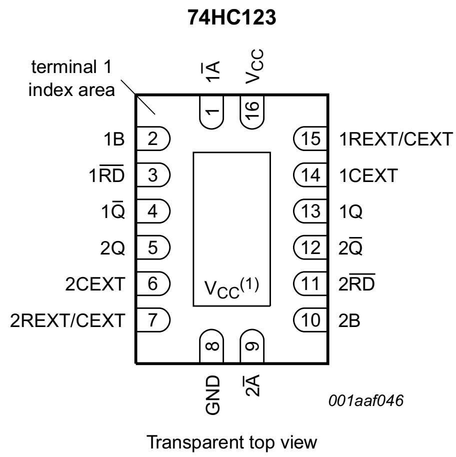


Fig 5. Pin configuration for DIP16, SO16, SSOP16 and TSSOP16



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to V_{CC}.

Fig 6. Pin configuration for DHVQFN16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{A}$	1	negative-edge triggered input 1
1B	2	positive-edge triggered input 1
1$\overline{RD}$	3	direct reset LOW and positive-edge triggered input 1
1$\overline{Q}$	4	active LOW output 1
2Q	5	active HIGH output 2
2CEXT	6	external capacitor connection 2
2REXT/CEXT	7	external resistor and capacitor connection 2
GND	8	ground (0 V)
2$\overline{A}$	9	negative-edge triggered input 2
2B	10	positive-edge triggered input 2
2$\overline{RD}$	11	direct reset LOW and positive-edge triggered input 2
2$\overline{Q}$	12	active LOW output 2
1Q	13	active HIGH output 1
1CEXT	14	external capacitor connection 1
1REXT/CEXT	15	external resistor and capacitor connection 1
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table[1]

Input			Output	
$\overline{nRD}$	$\overline{nA}$	nB	nQ	$\overline{nQ}$
L	X	X	L	H
X	H	X	L[2]	H[2]
X	X	L	L[2]	H[2]
H	L	↑	⎍	⊔
H	↓	H	⎍	⊔
↑	L	H	⎍	⊔

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition;

⎍ = one HIGH level output pulse; ⊔ = one LOW level output pulse.

[2] If the monostable was triggered before this condition was established, the pulse will continue as programmed.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±20	mA
I_O	output current	except for pins nREXT/CEXT; $V_O = -0.5$ V to (V_{CC} + 0.5 V)		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-	−50	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation					
	DIP16 package		[1]	-	750	mW
	SO16 package		[2]	-	500	mW
	SSOP16 package		[3]	-	500	mW
	TSSOP16 package		[3]	-	500	mW
	DHVQFN16 package		[4]	-	500	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN16 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC123			74HCT123			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
Δt/ΔV	input transition rise and fall rate	n$\overline{RD}$ input							
		V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC123										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA

Table 6. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT123										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = –20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	per input pin; I_O = 0 A; $V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V								
		pins $n\overline{A}$, nB	-	35	125	-	160	-	170	μA
		pin $n\overline{RD}$	-	50	180	-	225	-	245	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 12.

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC123										
t_{pd}	propagation delay	$n\overline{RD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$; C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 9 [1]								
		V_{CC} = 2.0 V	-	83	255	-	320	-	385	ns
		V_{CC} = 4.5 V	-	30	51	-	64	-	77	ns
		V_{CC} = 5 V; C_L = 15 pF	-	26	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	24	43	-	54	-	65	ns
		$n\overline{RD}$ (reset) to nQ or $n\overline{Q}$; C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 9								
		V_{CC} = 2.0 V	-	66	215	-	270	-	325	ns
		V_{CC} = 4.5 V	-	24	43	-	54	-	65	ns
		V_{CC} = 5 V; C_L = 15 pF	-	20	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	19	37	-	46	-	55	ns
t_t	transition time	see Figure 9 [1]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	$n\overline{A}$ LOW; see Figure 10								
		V_{CC} = 2.0 V	100	8	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	3	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	2	-	21	-	26	-	ns
		nB HIGH; see Figure 10								
		V_{CC} = 2.0 V	100	17	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	6	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	5	-	21	-	26	-	ns
		$n\overline{RD}$ LOW; see Figure 11								
		V_{CC} = 2.0 V	100	14	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	5	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	4	-	21	-	26	-	ns
		nQ HIGH and $n\overline{Q}$ LOW; V_{CC} = 5.0 V; see Figure 10 and 11 [2]								
		C_{EXT} = 100 nF; R_{EXT} = 10 kΩ	-	450	-	-	-	-	-	µs
		C_{EXT} = 0 pF; R_{EXT} = 5 kΩ	-	75	-	-	-	-	-	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 12.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{rtrig}	retrigger time	n$\overline{A}$, nB; C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 5.0 V; see Figure 10 [3][4]	-	110	-	-	-	-	-	ns
R_{EXT}	external timing resistor	see Figure 7								
		V_{CC} = 2.0 V	10	-	1000	-	-	-	-	kΩ
		V_{CC} = 5.0 V	2	-	1000	-	-	-	-	kΩ
C_{EXT}	external timing capacitor	V_{CC} = 5.0 V; see Figure 7 [4]	-	-	-	-	-	-	-	pF
C_{PD}	power dissipation capacitance	per monostable; V_I = GND to V_{CC} [5]	-	54	-	-	-	-	-	pF
74HCT123										
t_{PHL}	HIGH to LOW propagation delay	n$\overline{RD}$, n$\overline{A}$, nB to nQ or n$\overline{Q}$; C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 9								
		V_{CC} = 4.5 V	-	30	51	-	64	-	77	ns
		V_{CC} = 5 V; C_L = 15 pF	-	26	-	-	-	-	-	ns
		n$\overline{RD}$ (reset) to nQ or n$\overline{Q}$; C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 9								
		V_{CC} = 4.5 V	-	27	46	-	58	-	69	ns
		V_{CC} = 5 V; C_L = 15 pF	-	23	-	-	-	-	-	ns
t_{PLH}	LOW to HIGH propagation delay	n$\overline{RD}$, n$\overline{A}$, nB to nQ or n$\overline{Q}$; C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 9								
		V_{CC} = 4.5 V	-	28	51	-	64	-	77	ns
		V_{CC} = 5 V; C_L = 15 pF	-	26	-	-	-	-	-	ns
		n$\overline{RD}$ (reset) to nQ or n$\overline{Q}$; C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 9								
		V_{CC} = 4.5 V	-	23	46	-	58	-	69	ns
		V_{CC} = 5 V; C_L = 15 pF	-	23	-	-	-	-	-	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 9 [1]	-	7	15	-	19	-	22	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 12.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_W	pulse width	V_{CC} = 4.5 V								
		n$\overline{A}$ LOW; see Figure 10	20	3	-	25	-	30	-	ns
		nB HIGH; see Figure 10	20	5	-	25	-	30	-	ns
		n$\overline{RD}$ LOW; see Figure 11	20	7	-	25	-	30	-	ns
		nQ HIGH and n$\overline{Q}$ LOW; V_{CC} = 5.0 V; see Figure 10 and 11 [2]								
		C_{EXT} = 100 nF; R_{EXT} = 10 kΩ	-	450	-	-	-	-	-	μs
		C_{EXT} = 0 pF; R_{EXT} = 5 kΩ	-	75	-	-	-	-	-	ns
t_{rtrig}	retrigger time	n$\overline{A}$, nB; C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 5.0 V; see Figure 10 [3][4]	-	110	-	-	-	-	-	ns
R_{EXT}	external timing resistor	V_{CC} = 5.0 V; see Figure 7	2	-	1000	-	-	-	-	kΩ
C_{EXT}	external timing capacitor	V_{CC} = 5.0 V; see Figure 7 [4]	-	-	-	-	-	-	-	pF
C_{PD}	power dissipation capacitance	per monostable; V_I = GND to V_{CC} – 1.5 V [5]	-	56	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}; t_t is the same as t_{THL} and t_{TLH}

[2] For other R_{EXT} and C_{EXT} combinations see Figure 7. If C_{EXT} > 10 nF, the next formula is valid.

$t_W = K \times R_{EXT} \times C_{EXT}$, where:

t_W = typical output pulse width in ns;

R_{EXT} = external resistor in kΩ;

C_{EXT} = external capacitor in pF;

K = constant = 0.45 for V_{CC} = 5.0 V and 0.55 for V_{CC} = 2.0 V.

The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is approximately 7 pF.

[3] The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}. The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If C_{EXT} >10 pF, the next formula (at V_{CC} = 5.0 V) for the setup time of a retrigger pulse is valid:

$t_{rtrig} = 30 + 0.19 \times R_{EXT} \times C_{EXT}^{0.9} + 13 \times R_{EXT}^{1.05}$, where:

t_{rtrig} = retrigger time in ns;

C_{EXT} = external capacitor in pF; R_{EXT} = external resistor in kΩ.

The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is 7 pF.

[4] When the device is powered-up, initiate the device via a reset pulse, when C_{EXT} < 50 pF.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

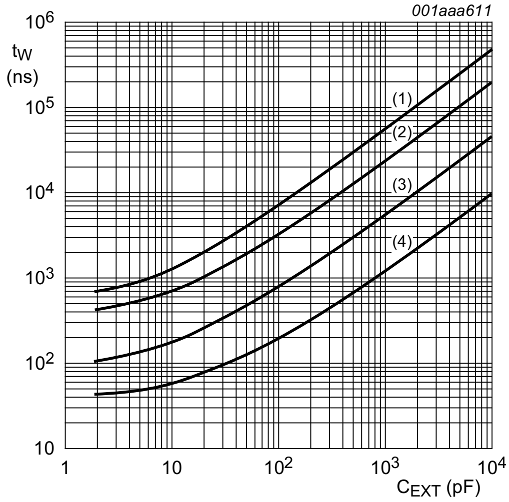
D = duty factor in %;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

C_{EXT} = timing capacitance in pF;

$\sum(C_L \times V_{CC}^2 \times f_o)$ sum of outputs.



V_{CC} = 5.0 V; T_{amb} = 25 °C.

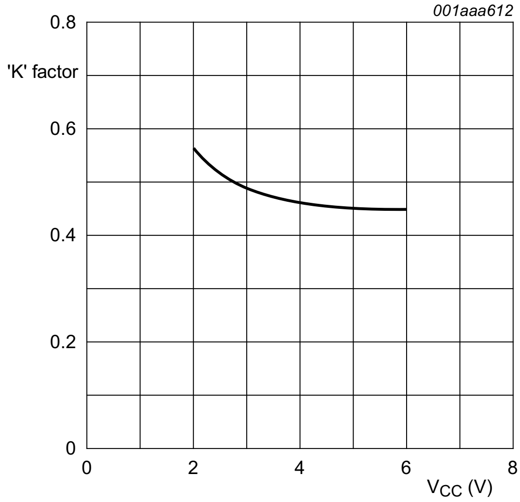
(1) R_{EXT} = 100 kΩ

(2) R_{EXT} = 50 kΩ

(3) R_{EXT} = 10 kΩ

(4) R_{EXT} = 2 kΩ

Fig 7. Typical output pulse width as a function of the external capacitor value

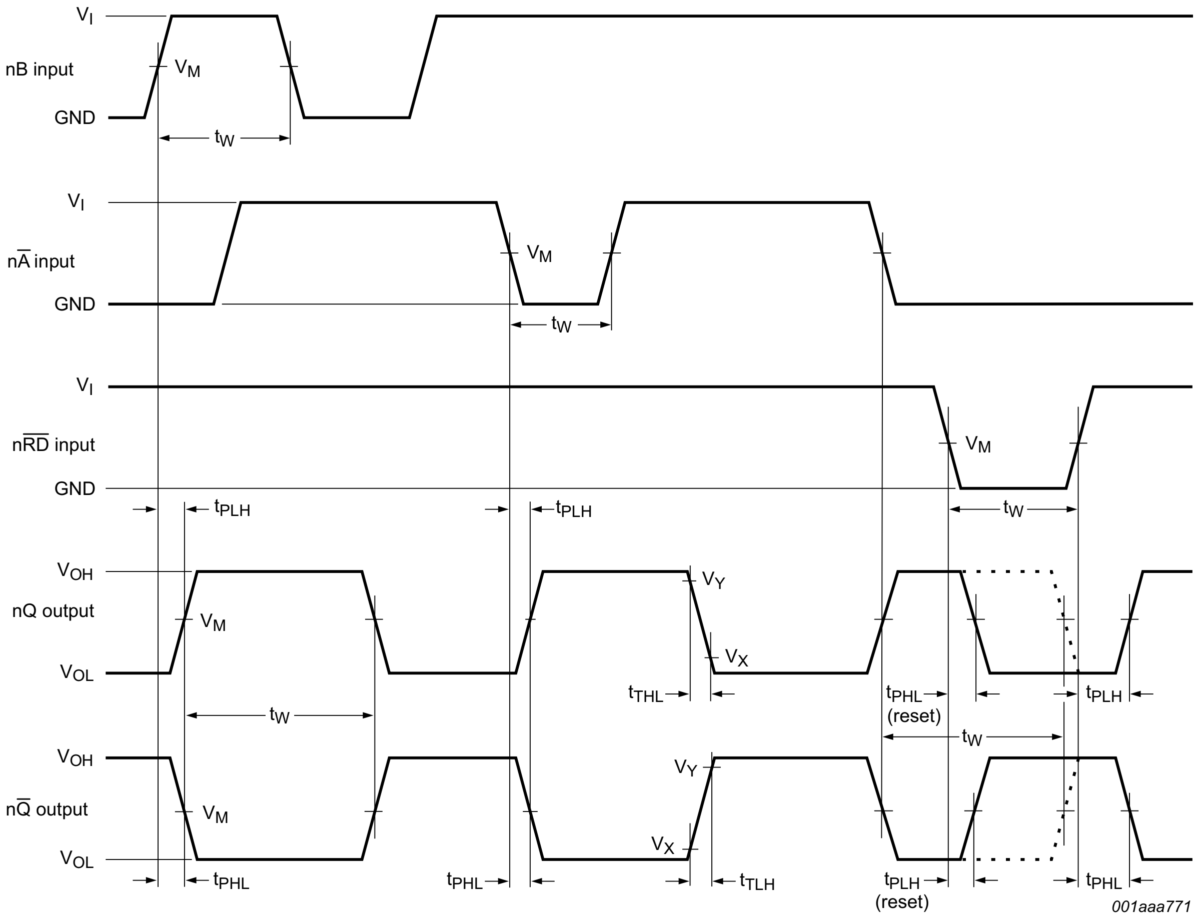


C_{EXT} = 10 nF; R_{EXT} = 10 kΩ to 100 kΩ.

T_{amb} = 25 °C.

Fig 8. 74HC123 typical 'K' factor as function of V_{CC}

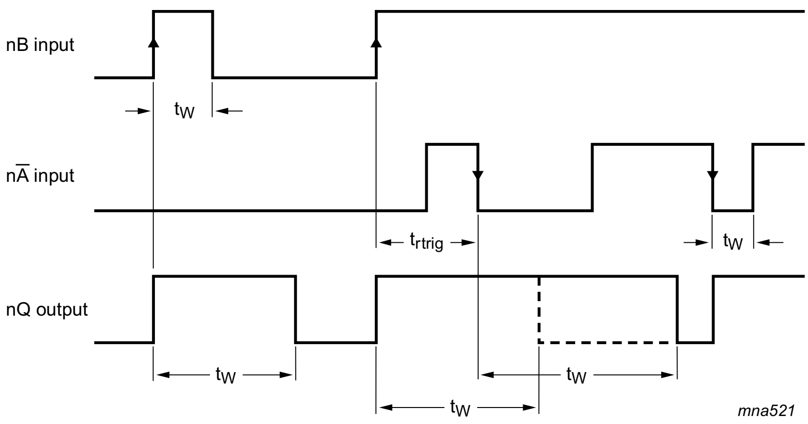
11. Waveforms



Measurement points are given in Table 8.

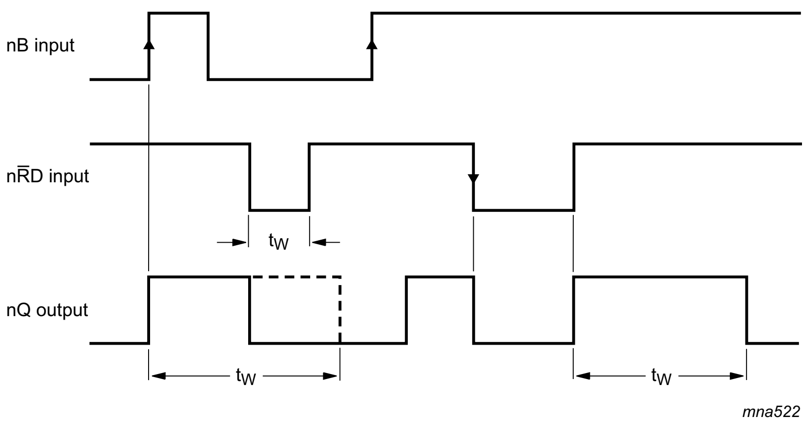
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Propagation delays from inputs (n$\overline{A}$, nB, n$\overline{RD}$) to outputs (nQ, n$\overline{Q}$) and output transition times



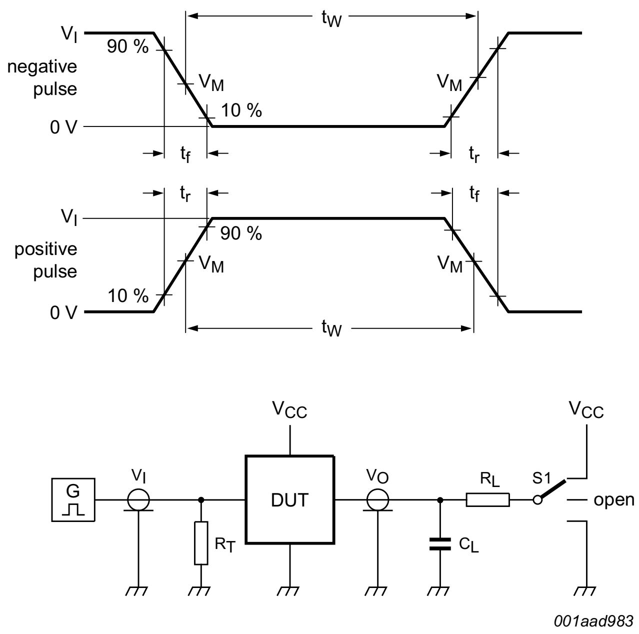
$n\overline{RD}$ = HIGH

Fig 10. Output pulse control using retrigger pulse



$n\overline{A}$ = LOW

Fig 11. Output pulse control using reset input $n\overline{RD}$



Test data is given in Table 8.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 12. Test circuit for measuring switching times

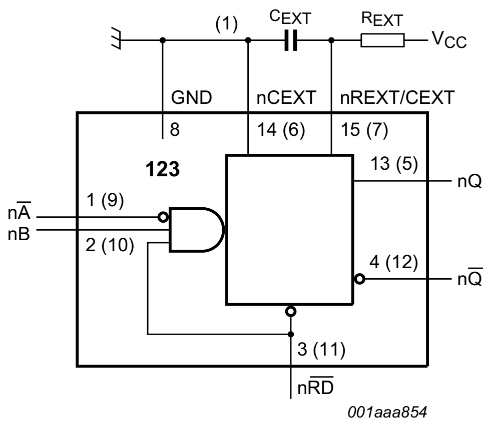
Table 8. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC123	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open
74HCT123	3 V	6 ns	15 pF, 50 pF	1 kΩ	open

12. Application information

12.1 Timing component connections

The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}.



(1) For minimum noise generation it is recommended to ground pins 6 (2CEXT) and 14 (1CEXT) externally to pin 8 (GND).

Fig 13. Timing component connections

12.2 Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_{EXT} and C_{EXT}. This output pulse can be eliminated using the circuit shown in Figure 14.

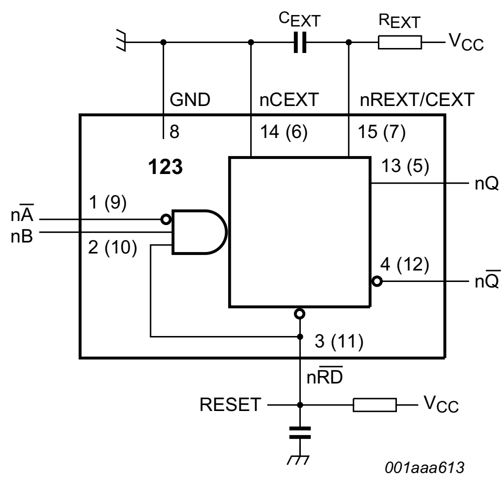


Fig 14. Power-up output pulse elimination circuit

12.3 Power-down considerations

A large capacitor C_{EXT} may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Figure 15.

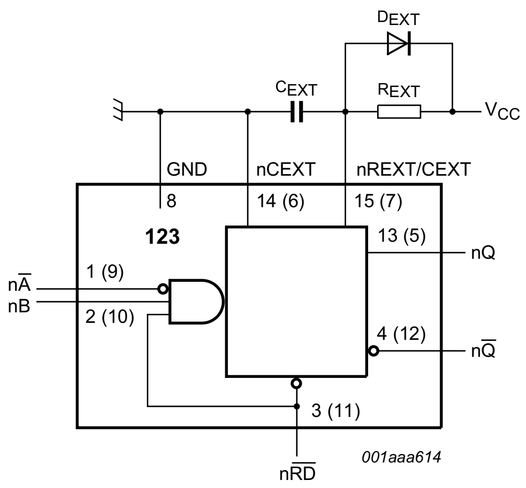
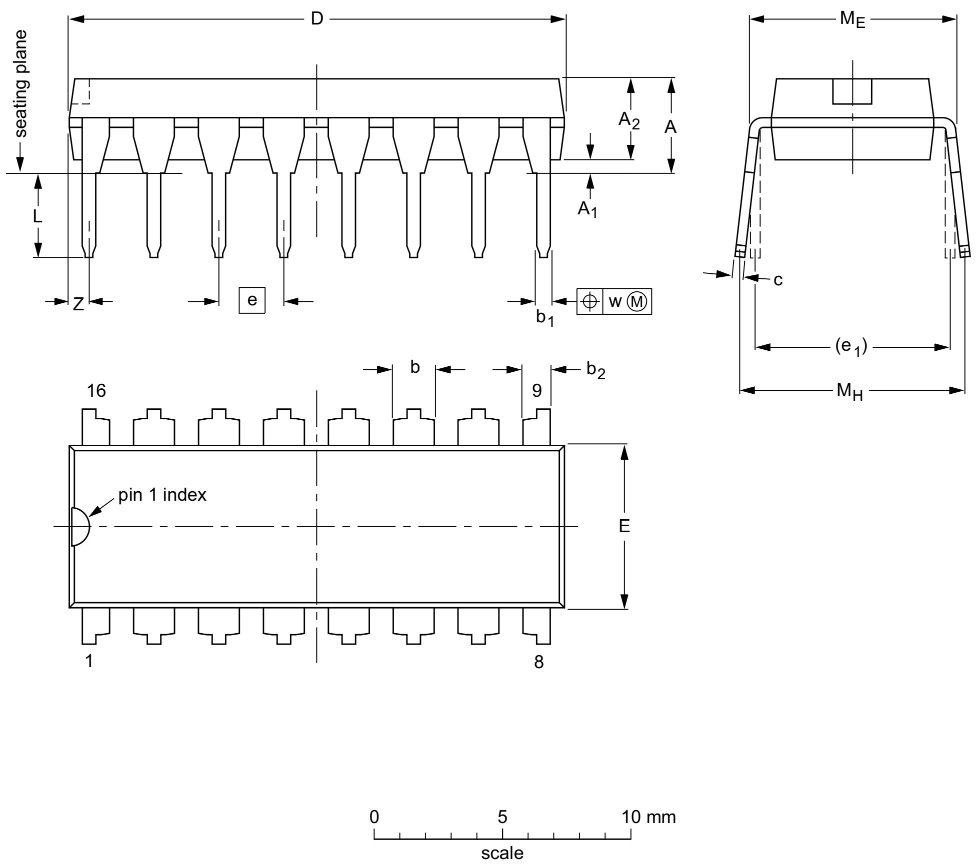


Fig 15. Power-down protection circuit

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

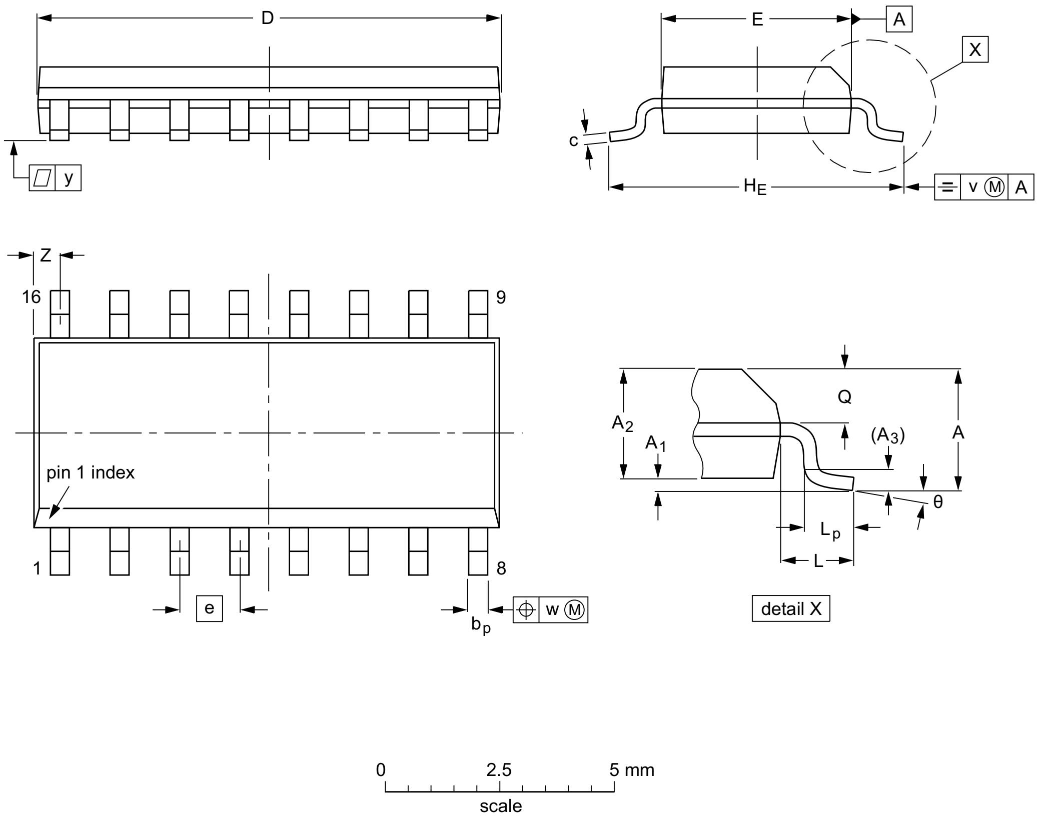
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 16. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

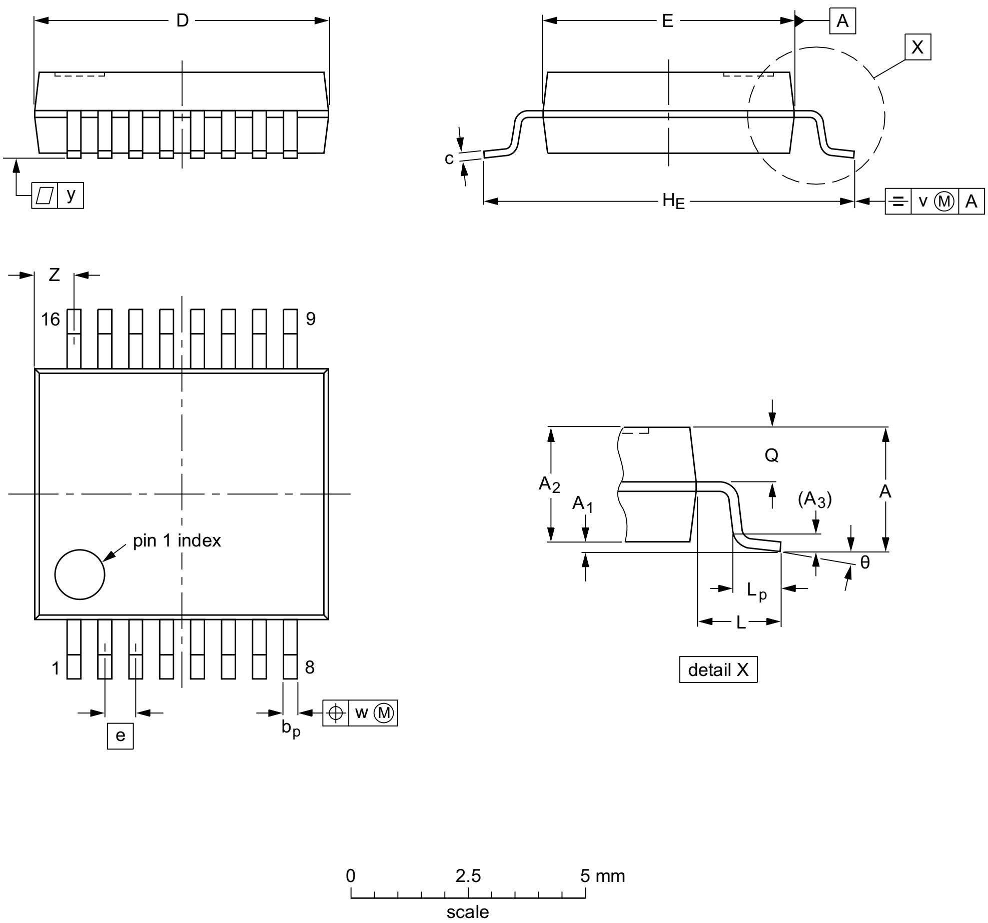
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 17. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

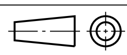
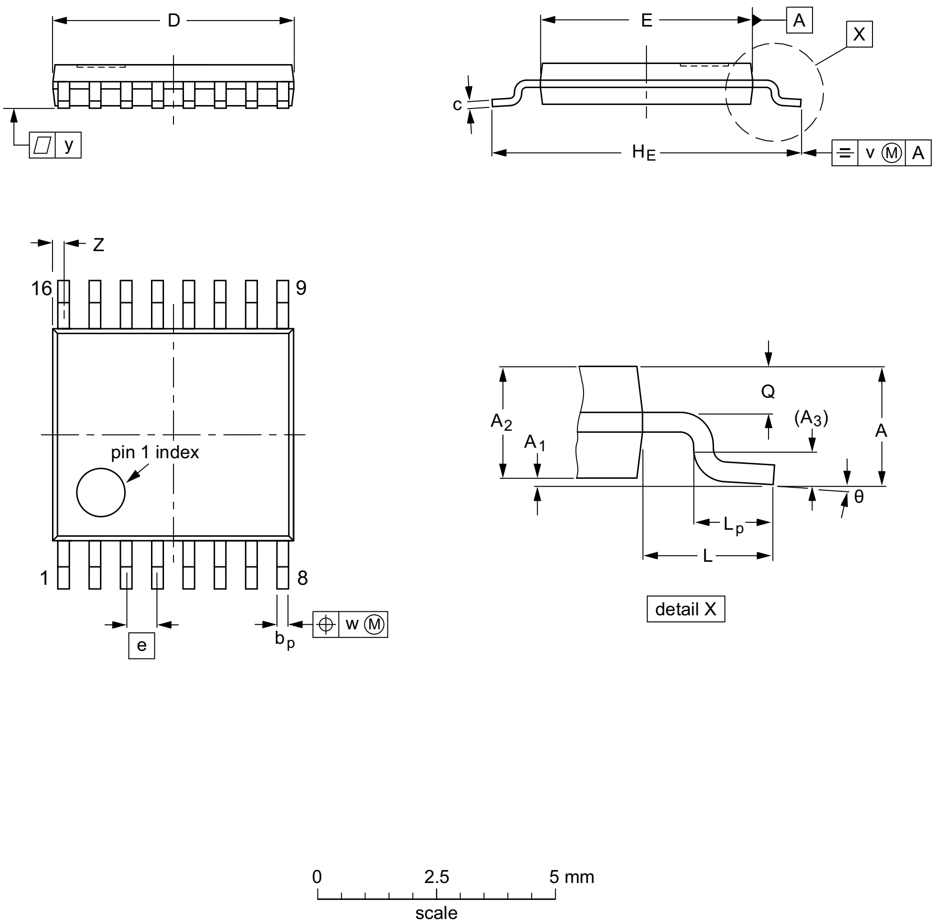
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 18. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

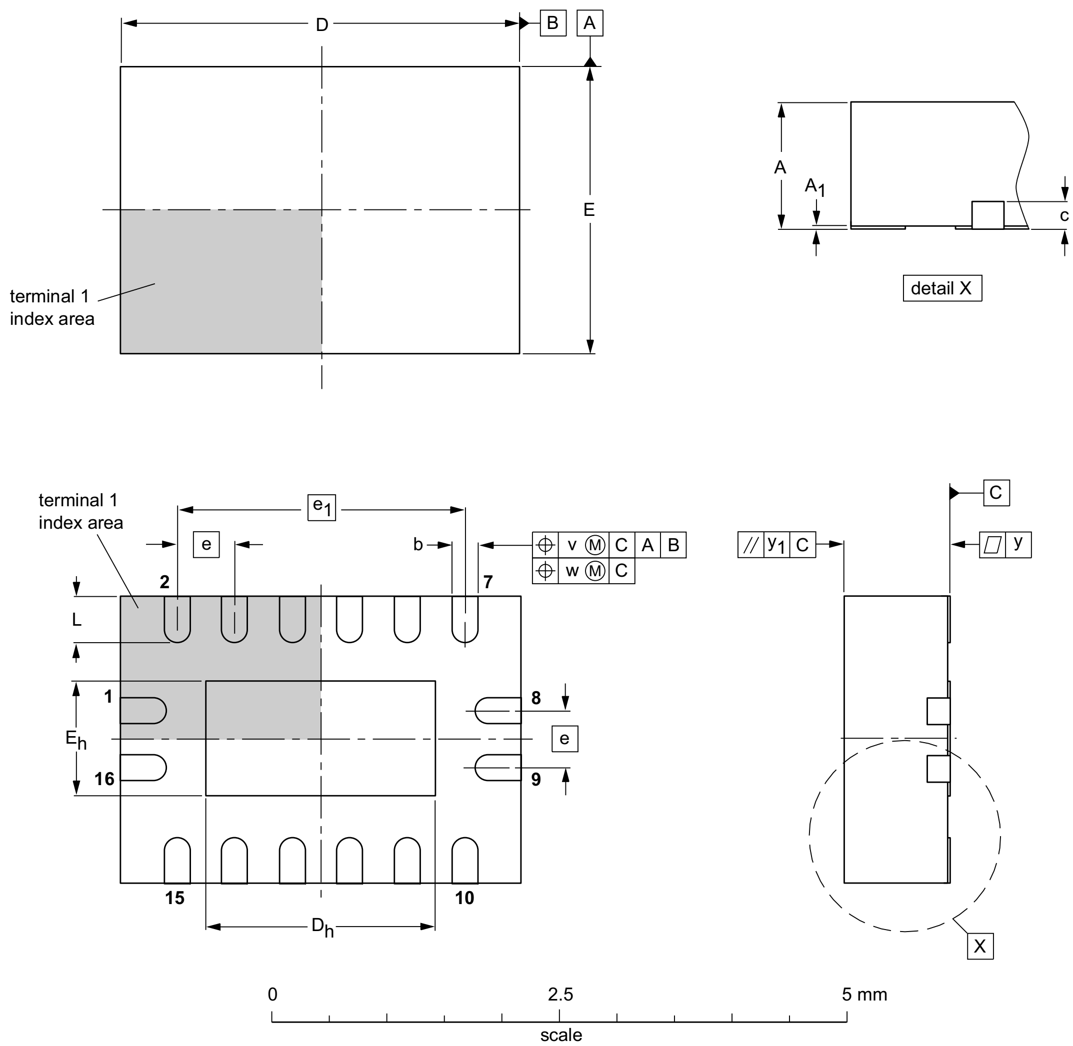
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 19. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 20. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 9. Abbreviations

Acronym	Abbreviation
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT123 v.9	20150119	Product data sheet	-	74HC_HCT123 v.8
Modifications:	• Table 7: Power dissipation capacitance condition for 74HCT123 is corrected.			
74HC_HCT123 v.8	20111216	Product data sheet	-	74HC_HCT123 v.7
Modifications:	• Legal pages updated.			
74HC_HCT123 v.7	20110825	Product data sheet	-	74HC_HCT123 v.6
74HC_HCT123 v.6	20110314	Product data sheet	-	74HC_HCT123 v.5
74HC_HCT123 v.5	20090713	Product data sheet	-	74HC_HCT123 v.4
74HC_HCT123 v.4	20060616	Product data sheet	-	74HC_HCT123 v.3
74HC_HCT123 v.3	20040511	Product specification	-	74HC_HCT123_CNV v.2
74HC_HCT123_CNV v.2	19980708	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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