μA78L00 Series Positive-Voltage Regulators

Check for Samples: μA78L00

FEATURES

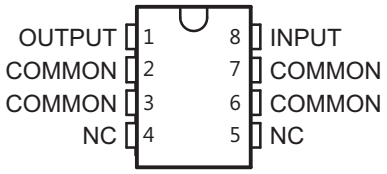
- **3-Terminal Regulators**
- **Output Current up to 100 mA**
- **No External Components**
- **Internal Thermal-Overload Protection**
- **Internal Short-Circuit Current Limiting**

DESCRIPTION

This series of fixed-voltage integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power-pass elements to make high-current voltage regulators. One of these regulators can deliver up to 100 mA of output current. The internal limiting and thermal-shutdown features of these regulators essentially make them immune to overload. When used as a replacement for a Zener diode-resistor combination, an effective improvement in output impedance can be obtained, together with lower bias current.

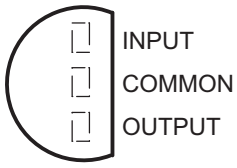
The μA78L00C and μA78L00AC series devices are characterized for operation over the virtual junction temperature range of 0°C to 125°C. The μA78L05AI device is characterized for operation over the virtual junction temperature range of −40°C to 125°C.

D PACKAGE
(TOP VIEW)



NC – No internal connection

LP PACKAGE
(TO-92, TO-226AA)
(TOP VIEW)



PK PACKAGE
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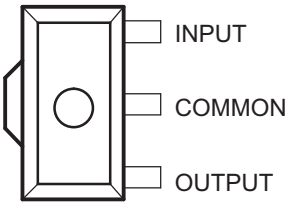
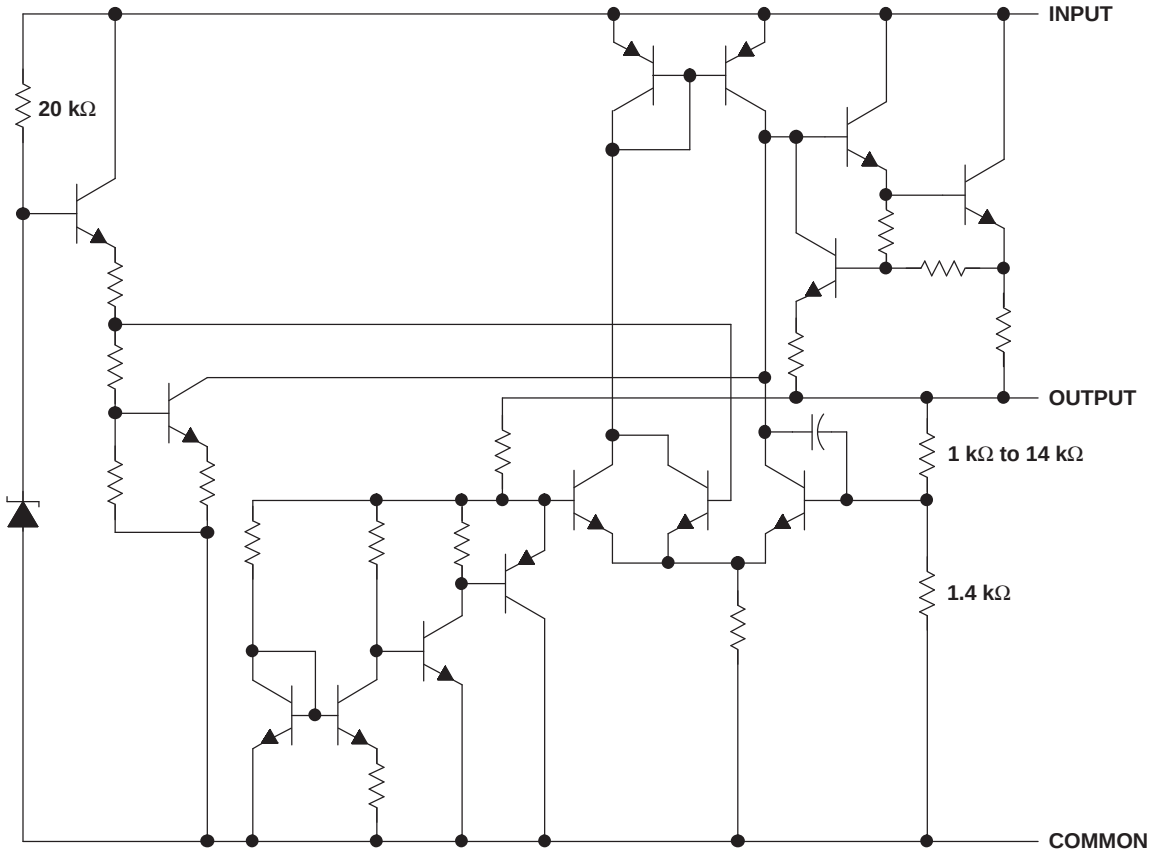


This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Schematic



NOTE: Resistor values shown are nominal.

Absolute Maximum Ratings(1)

over virtual junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage	μA78L02AC, μA78L05C–μA78L09C, μA78L10AC		30	V
		μA78L12C, μA78L12AC, μA78L15C, μA78L15AC		35	
T_J	Virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Package Thermal Data(1)

PACKAGE	BOARD	θ_{JC}	θ_{JA}
SOIC (D)	High K, JESD 51-7	39°C/W	97°C/W
TO-92/TO-226AA (LP)	High K, JESD 51-7	55°C/W	140°C/W
SOT-89 (PK)	High K, JESD 51-7	9°C/W	52°C/W

(1) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal-overload protection may be activated at power levels slightly above or below the rated dissipation.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_I	Input voltage	μA78L02AC	4.75	20	V
		μA78L05C, μA78L05AC	7	20	
		μA78L06C, μA78L06AC	8.5	20	
		μA78L08C, μA78L08AC	10.5	23	
		μA78L09C, μA78L09AC	11.5	24	
		μA78L10AC	12.5	25	
		μA78L12C, μA78L12AC	14.5	27	
		μA78L15C, μA78L15AC	17.5	30	
I_O	Output current			100	mA
T_J	Operating virtual junction temperature	μA78LxxC and μA78LxxAC series	0	125	°C
		μA78L05AI	–40	125	

uA78L02 Electrical Characteristics

at specified virtual junction temperature, V_I = 9 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J[1]	μA78L02AC			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 4.75 V to 20 V, I_O = 1 mA to 40 mA	25°C	2.5	2.6	2.7	V
		0°C to 125°C	2.45		2.75	
	I_O = 1 mA to 70 mA	0°C to 125°C	2.45		2.75	
Input voltage regulation	V_I = 4.75 V to 20 V	25°C		20	100	mV
	V_I = 5 V to 20 V			16	75	
Ripple rejection	V_I = 6 V to 20 V, f = 120 Hz	25°C	43	51		dB
Output voltage regulation	I_O = 1 mA to 100 mA	25°C		12	50	mV
	I_O = 1 mA to 40 mA			6	25	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		30		μV
Dropout voltage		25°C		1.7		V
Bias current		25°C		3.6	6	mA
		125°C			5.5	
Bias current change	V_I = 5 V to 20 V	0°C to 125°C			2.5	mA
	I_O = 1 mA to 40 mA				0.1	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

uA78L05 Electrical Characteristics

at specified virtual junction temperature, V_I = 10 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J[1]	μA78L05C			μA78L05AC μA78L05AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	V_I = 7 V to 20 V, I_O = 1 mA to 40 mA	25°C	4.6	5	5.4	4.8	5	5.2	V
		Full range	4.5		5.5	4.75		5.25	
	I_O = 1 mA to 70 mA	Full range	4.5		5.5	4.75		5.25	
Input voltage regulation	V_I = 7 V to 20 V	25°C		32	200		32	150	mV
	V_I = 8 V to 20 V			26	150		26	100	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	25°C	40	49		41	49		dB
Output voltage regulation	I_O = 1 mA to 100 mA	25°C		15	60		15	60	mV
	I_O = 1 mA to 40 mA			8	30		8	30	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		42			42		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.8	6		3.8	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 8 V to 20 V	Full range			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Full range for the μA78L05AC is T_J = 0°C to 125°C, and full range for the μA78L05AI is T_J = –40°C to 125°C.

uA78L06 Electrical Characteristics

at specified virtual junction temperature, V_I = 12 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J[1]	μA78L06C			μA78L06AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	V_I = 8.5 V to 20 V, I_O = 1 mA to 40 mA	25°C	5.7	6.2	6.7	5.95	6.2	6.45	V
		0°C to 125°C	5.6		6.8	5.9		6.5	
	I_O = 1 mA to 70 mA	0°C to 125°C	5.6		6.8	5.9		6.5	
Input voltage regulation	V_I = 8.5 V to 20 V	25°C		35	200		35	175	mV
	V_I = 9 V to 20 V			29	150		29	125	
Ripple rejection	V_I = 10 V to 20 V, f = 120 Hz	25°C	39	48		40	48		dB
Output voltage regulation	I_O = 1 mA to 100 mA	25°C		16	80		16	80	mV
	I_O = 1 mA to 40 mA			9	40		9	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		46			46		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.9	6		3.9	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 9 V to 20 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

uA78L08 Electrical Characteristics

at specified virtual junction temperature, V_I = 14 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J[1]	μA78L08C			μA78L08AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	V_I = 10.5 V to 23 V, I_O = 1 mA to 40 mA	25°C	7.36	8	8.64	7.7	8	8.3	V
		0°C to 125°C	7.2		8.8	7.6		8.4	
	I_O = 1 mA to 70 mA	0°C to 125°C	7.2		8.8	7.6		8.4	
Input voltage regulation	V_I = 10.5 V to 23 V	25°C		42	200		42	175	mV
	V_I = 11 V to 23 V			36	150		36	125	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	25°C	36	46		37	46		dB
Output voltage regulation	I_O = 1 mA to 100 mA	25°C		18	80		18	80	mV
	I_O = 1 mA to 40 mA			10	40		10	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		54			54		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4	6		4	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 11 V to 23 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

uA78L09 Electrical Characteristics

at specified virtual junction temperature, V_I = 16 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J(1)	μA78L09C			μA78L09AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	V_I = 12 V to 24 V, I_O = 1 mA to 40 mA	25°C	8.3	9	9.7	8.6	9	9.4	V
		0°C to 125°C	8.1		9.9	8.55		9.45	
	I_O = 1 mA to 70 mA	0°C to 125°C	8.1		9.9	8.55		9.45	
Input voltage regulation	V_I = 12 V to 24 V	25°C		45	225		45	175	mV
	V_I = 13 V to 24 V			40	175		40	125	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	25°C	36	45		38	45		dB
Output voltage regulation	I_O = 1 mA to 100 mA	25°C		19	90		19	90	mV
	I_O = 1 mA to 40 mA			11	40		11	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		58			58		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.1	6		4.1	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 13 V to 24 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

uA78L10 Electrical Characteristics

at specified virtual junction temperature, V_I = 14 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J(1)	μA78L10AC			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 13 V to 25 V, I_O = 1 mA to 40 mA	25°C	9.6	10	10.4	V
		0°C to 125°C	9.5		10.5	
	I_O = 1 mA to 70 mA	0°C to 125°C	9.5		10.5	
Input voltage regulation	V_I = 13 V to 25 V	25°C		51	175	mV
	V_I = 14 V to 25 V			42	125	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	25°C	37	44		dB
Output voltage regulation	I_O = 1 mA to 100 mA	25°C		20	90	mV
	I_O = 1 mA to 40 mA			11	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		62		μV
Dropout voltage		25°C		1.7		V
Bias current		25°C		4.2	6	mA
		125°C			5.5	
Bias current change	V_I = 14 V to 25 V	0°C to 125°C			1.5	mA
	I_O = 1 mA to 40 mA				0.1	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

uA78L12 Electrical Characteristics

at specified virtual junction temperature, V_I = 19 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J[1]	μA78L12C			μA78L12AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	V_I = 14 V to 27 V, I_O = 1 mA to 40 mA	25°C	11.1	12	12.9	11.5	12	12.5	V
		0°C to 125°C	10.8		13.2	11.4		12.6	
	I_O = 1 mA to 70 mA	0°C to 125°C	10.8		13.2	11.4		12.6	
Input voltage regulation	V_I = 14.5 V to 27 V	25°C		55	250		55	250	mV
	V_I = 16 V to 27 V			49	200		49	200	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	25°C	36	42		37	42		dB
Output voltage regulation	I_O = 1 mA to 100 mA	25°C		22	100		22	100	mV
	I_O = 1 mA to 40 mA			13	50		13	50	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		70			70		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.3	6.5		4.3	6.5	mA
		125°C			6			6	
Bias current change	V_I = 16 V to 27 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

uA78L15 Electrical Characteristics

at specified virtual junction temperature, V_I = 23 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J[1]	μA78L15C			μA78L15AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	V_I = 17.5 V to 30 V, I_O = 1 mA to 40 mA	25°C	13.8	15	16.2	14.4	15	15.6	V
		0°C to 125°C	13.5		16.5	14.25		15.75	
	I_O = 1 mA to 70 mA	0°C to 125°C	13.5		16.5	14.25		15.75	
Input voltage regulation	V_I = 17.5 V to 30 V	25°C		65	300		65	300	mV
	V_I = 20 V to 30 V			58	250		58	250	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	25°C	33	39		34	39		dB
Output voltage regulation	I_O = 1 mA to 100 mA	25°C		25	150		25	150	mV
	I_O = 1 mA to 40 mA			15	75		15	75	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		82			82		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.6	6.5		4.6	6.5	mA
		125°C			6			6	
Bias current change	V_I = 10 V to 30 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

APPLICATION INFORMATION

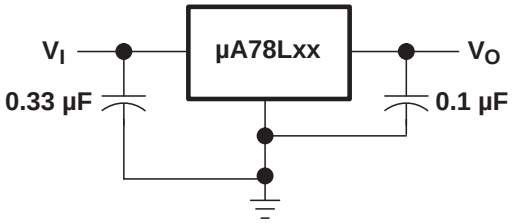


Figure 1. Fixed-Output Regulator

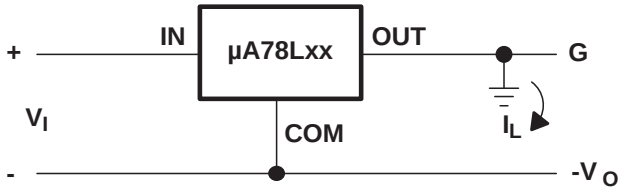


Figure 2. Positive Regulator in Negative Configuration (V_I Must Float)

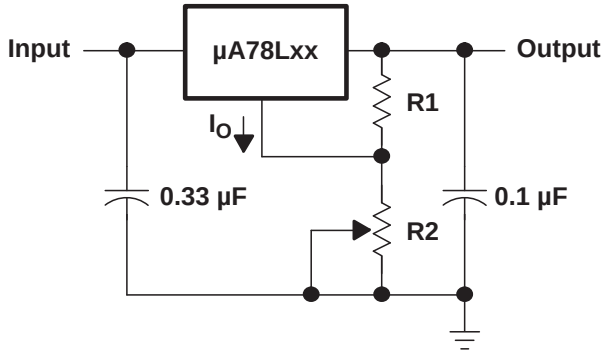
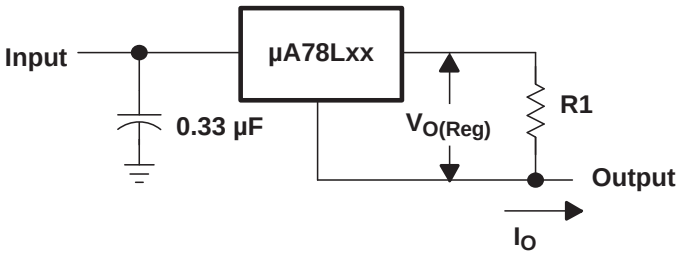


Figure 3. Adjustable-Output Regulator



$I_O = (V_O/R1) + I_O$ Bias Current

Figure 4. Current Regulator

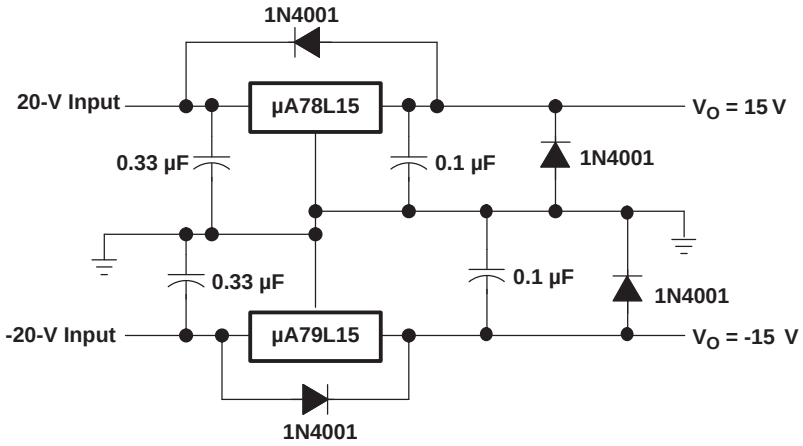


Figure 5. Regulated Dual Supply

Operation With a Load Common to a Voltage of Opposite Polarity

In many cases, a regulator powers a load that is not connected to ground, but instead, is connected to a voltage source of opposite polarity (for example, operational amplifiers, level-shifting circuits, and so on). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 6. This protects the regulator from output polarity reversals during startup and short-circuit operation.

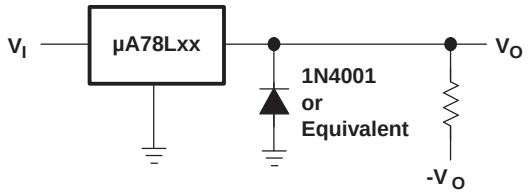


Figure 6. Output Polarity-Reversal-Protection Circuit

Reverse-Bias Protection

Occasionally, the input voltage to the regulator can collapse faster than the output voltage. This can occur, for example, when the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series-pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed as shown in Figure 7.

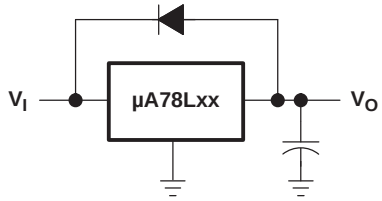


Figure 7. Reverse-Bias-Protection Circuit

REVISION HISTORY

Changes from Revision T (May 2011) to Revision U **Page**

- Updated document to new TI data sheet format - no specification changes. 1
- Added ESD warning. 2
- Deleted Ordering Information table. 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78L02ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L02A	Samples
UA78L02ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L02A	Samples
UA78L02ACLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L02AC	Samples
UA78L02ACLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L02AC	Samples
UA78L05ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L05AC	Samples
UA78L05ACLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L05AC	Samples
UA78L05ACLPM	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L05AC	Samples
UA78L05ACLPME3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L05AC	Samples
UA78L05ACLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L05AC	Samples
UA78L05ACLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L05AC	Samples
UA78L05ACPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	F5	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78L05ACPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	F5	Samples
UA78L05AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI	Samples
UA78L05AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI	Samples
UA78L05AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI	Samples
UA78L05AIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI	Samples
UA78L05AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI	Samples
UA78L05AILP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	78L05AI	Samples
UA78L05AILPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	78L05AI	Samples
UA78L05AILPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	78L05AI	Samples
UA78L05AILPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	78L05AI	Samples
UA78L05AIPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	J5	Samples
UA78L05AIPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	J5	Samples
UA78L05AQD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI			
UA78L05AQDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI			
UA78L05CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C	Samples
UA78L05CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C	Samples
UA78L05CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C	Samples
UA78L05CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C	Samples
UA78L05CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78L05CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L05C	Samples
UA78L05CLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L05C	Samples
UA78L05CLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L05C	Samples
UA78L05CPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	B5	Samples
UA78L05CPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	B5	Samples
UA78L05QLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI			
UA78L05QLPR	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI			
UA78L06ACLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L06AC	Samples
UA78L06ACLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L06AC	Samples
UA78L06ACLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L06AC	Samples
UA78L06ACLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L06AC	Samples
UA78L06ACPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	F6	Samples
UA78L06ACPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	F6	Samples
UA78L08ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L08A	Samples
UA78L08ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L08A	Samples
UA78L08ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 125	78L08A	Samples
UA78L08ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L08A	Samples
UA78L08ACLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L08AC	Samples
UA78L08ACLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L08AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78L08ACLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L08AC	Samples
UA78L08ACLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L08AC	Samples
UA78L08ACPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	F8	Samples
UA78L08ACPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	F8	Samples
UA78L08AILP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI			
UA78L08AQDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI			
UA78L08CLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI	0 to 125		
UA78L08CPK	OBSOLETE	SOT-89	PK	3		TBD	Call TI	Call TI	0 to 125		
UA78L09ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A	Samples
UA78L09ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A	Samples
UA78L09ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A	Samples
UA78L09ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A	Samples
UA78L09ACLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L09AC	Samples
UA78L09ACLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L09AC	Samples
UA78L09ACLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L09AC	Samples
UA78L09ACLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L09AC	Samples
UA78L09ACPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	F9	Samples
UA78L09ACPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	F9	Samples
UA78L10ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A	Samples
UA78L10ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78L10ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A	Samples
UA78L10ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A	Samples
UA78L10ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A	Samples
UA78L10ACLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L10AC	Samples
UA78L10ACLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L10AC	Samples
UA78L10ACLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L10AC	Samples
UA78L10ACLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L10AC	Samples
UA78L10ACPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	FA	Samples
UA78L10ACPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	FA	Samples
UA78L12ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A	Samples
UA78L12ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A	Samples
UA78L12ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 125	78L12A	Samples
UA78L12ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A	Samples
UA78L12ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A	Samples
UA78L12ACLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L12AC	Samples
UA78L12ACLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L12AC	Samples
UA78L12ACLPM	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L12AC	Samples
UA78L12ACLPME3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L12AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78L12ACLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L12AC	Samples
UA78L12ACLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L12AC	Samples
UA78L12ACPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	FC	Samples
UA78L12ACPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	FC	Samples
UA78L12AQDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI			
UA78L12AQLPR	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI			
UA78L15ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A	Samples
UA78L15ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A	Samples
UA78L15ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A	Samples
UA78L15ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A	Samples
UA78L15ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A	Samples
UA78L15ACLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L15AC	Samples
UA78L15ACLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L15AC	Samples
UA78L15ACLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L15AC	Samples
UA78L15ACLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	78L15AC	Samples
UA78L15ACPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	FF	Samples
UA78L15ACPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	FF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

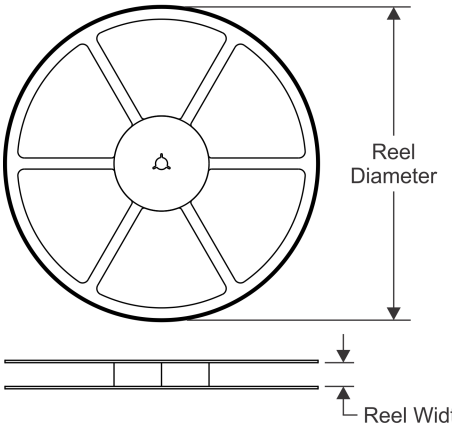
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

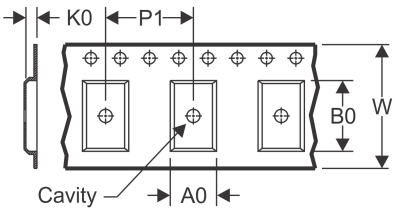
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

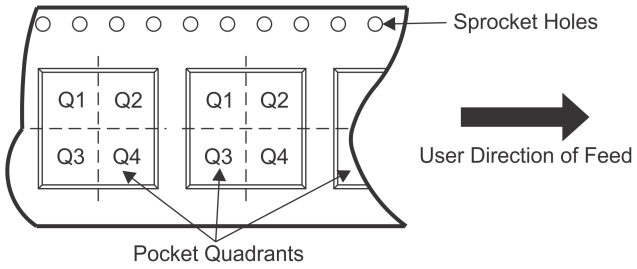


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

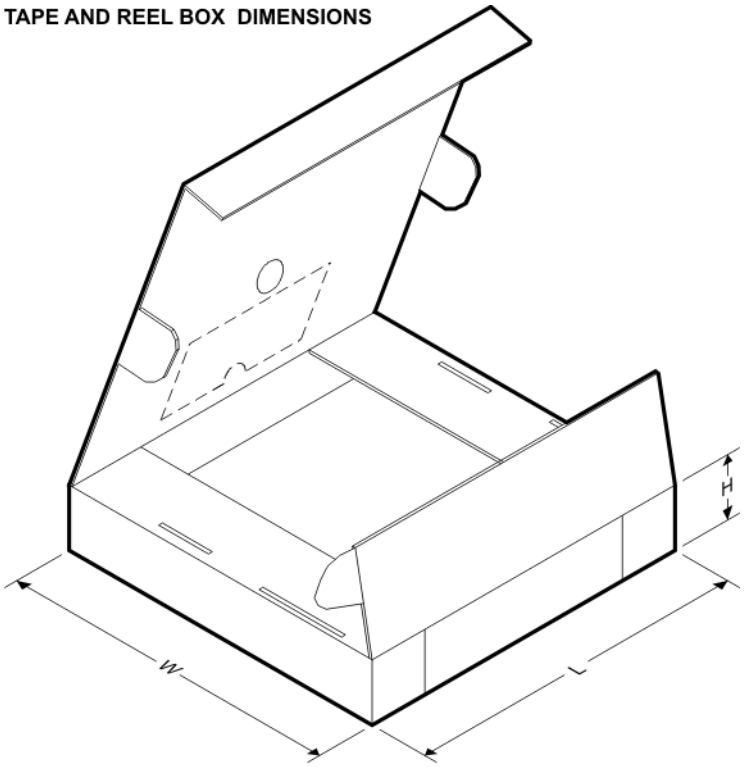


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA78L05ACDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05AIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05CPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L06ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L08ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L08ACDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
UA78L08ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L08ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L09ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L09ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L10ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L10ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L12ACDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA78L12ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L12ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L12ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L15ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L15ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS

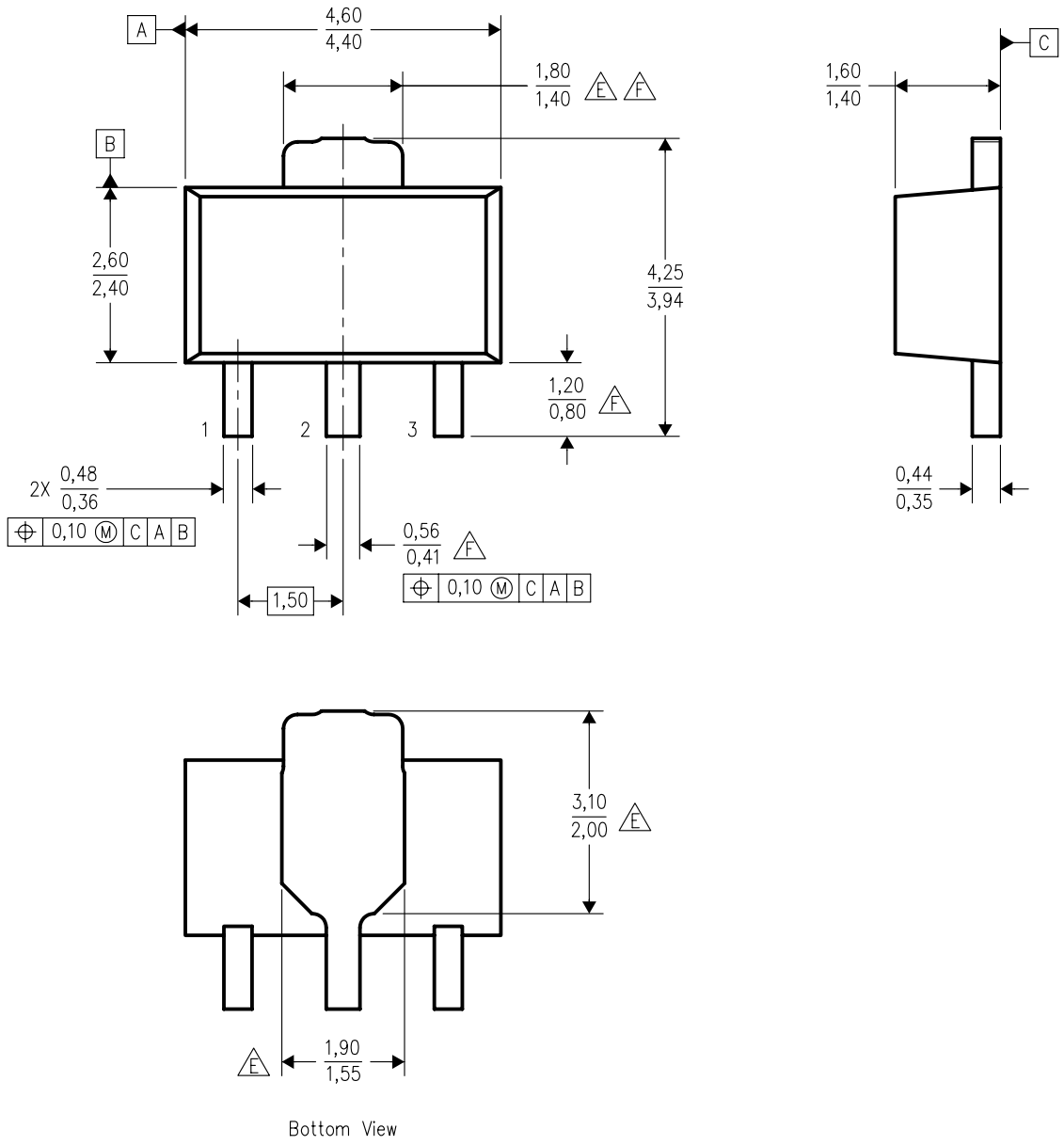


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA78L05ACDR	SOIC	D	8	2500	364.0	364.0	27.0
UA78L05ACDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L05ACDRG4	SOIC	D	8	2500	340.5	338.1	20.6
UA78L05ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L05AIDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L05AIPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L05CDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L05CPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L06ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L08ACDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L08ACDR	SOIC	D	8	2500	364.0	364.0	27.0
UA78L08ACDRG4	SOIC	D	8	2500	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA78L08ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L09ACDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L09ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L10ACDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L10ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L12ACDR	SOIC	D	8	2500	364.0	364.0	27.0
UA78L12ACDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L12ACDRG4	SOIC	D	8	2500	340.5	338.1	20.6
UA78L12ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L15ACDR	SOIC	D	8	2500	340.5	338.1	20.6
UA78L15ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0

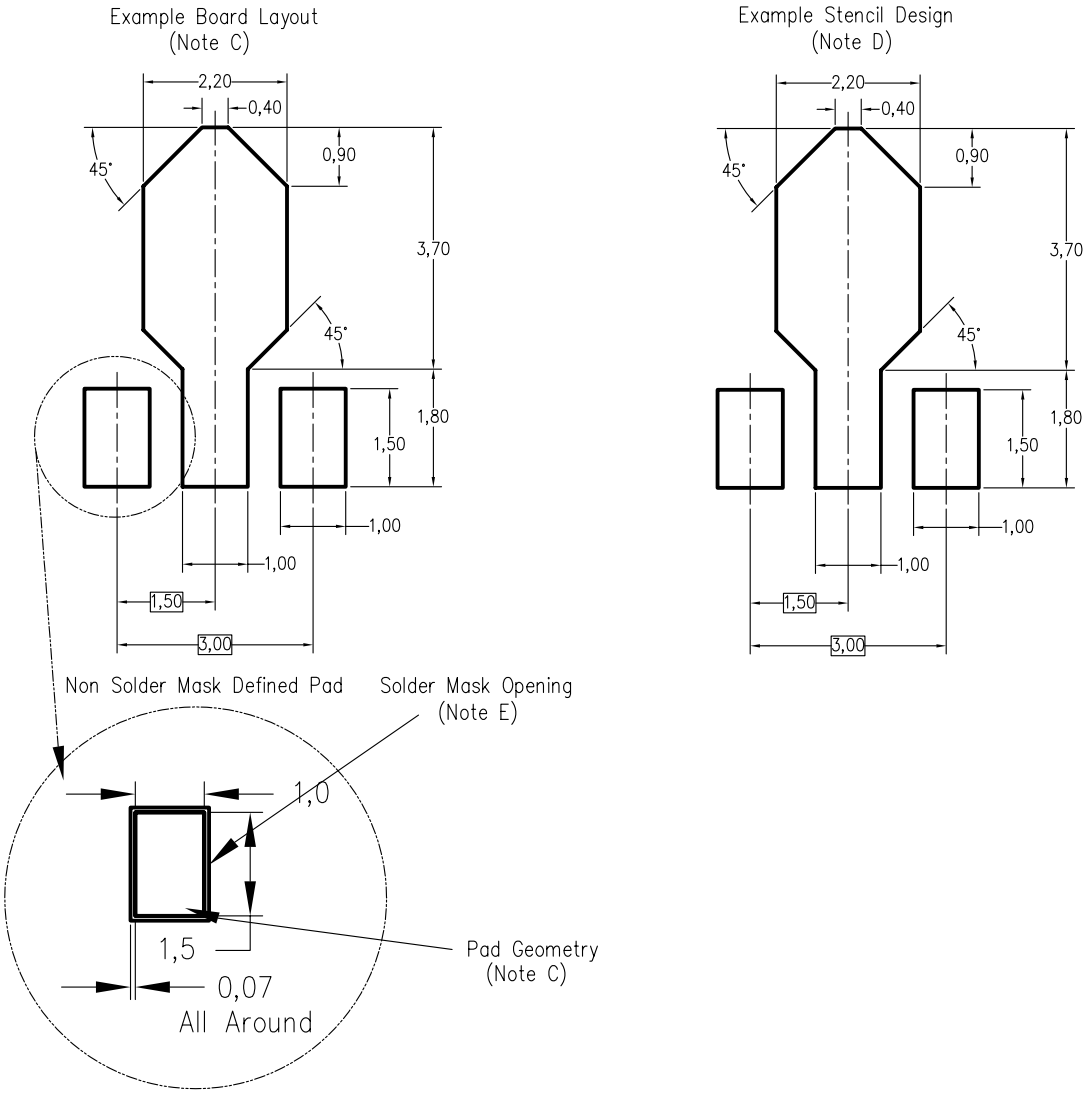
PK (R–PSSO–F3) PLASTIC SINGLE–IN–LINE PACKAGE



4040234/D 02/2006

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.
D. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
E. Thermal pad contour optional within these dimensions.
F. Falls within JEDEC TO–243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

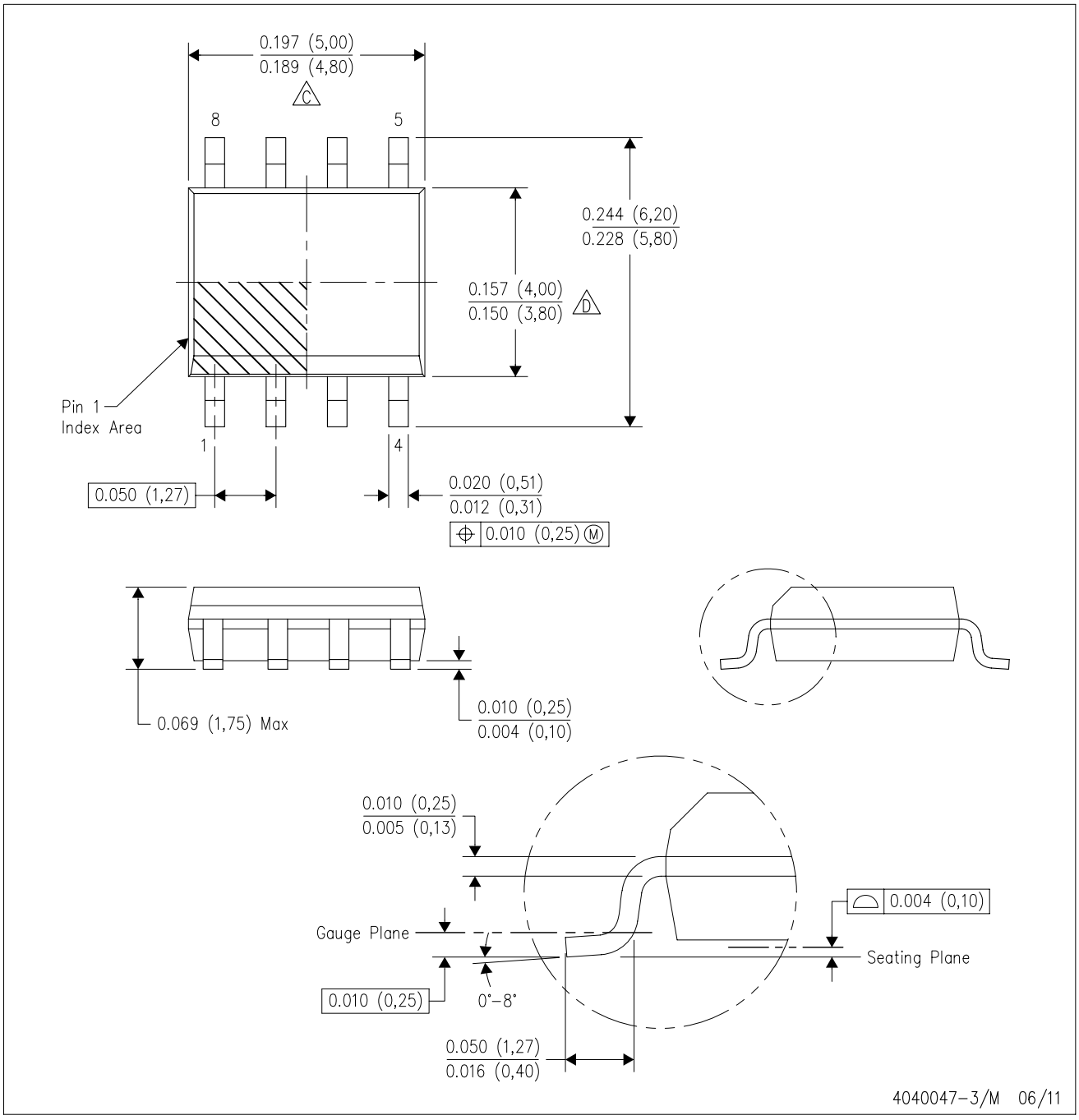
PK (R–PDSO–G3)



4208221/A 09/06

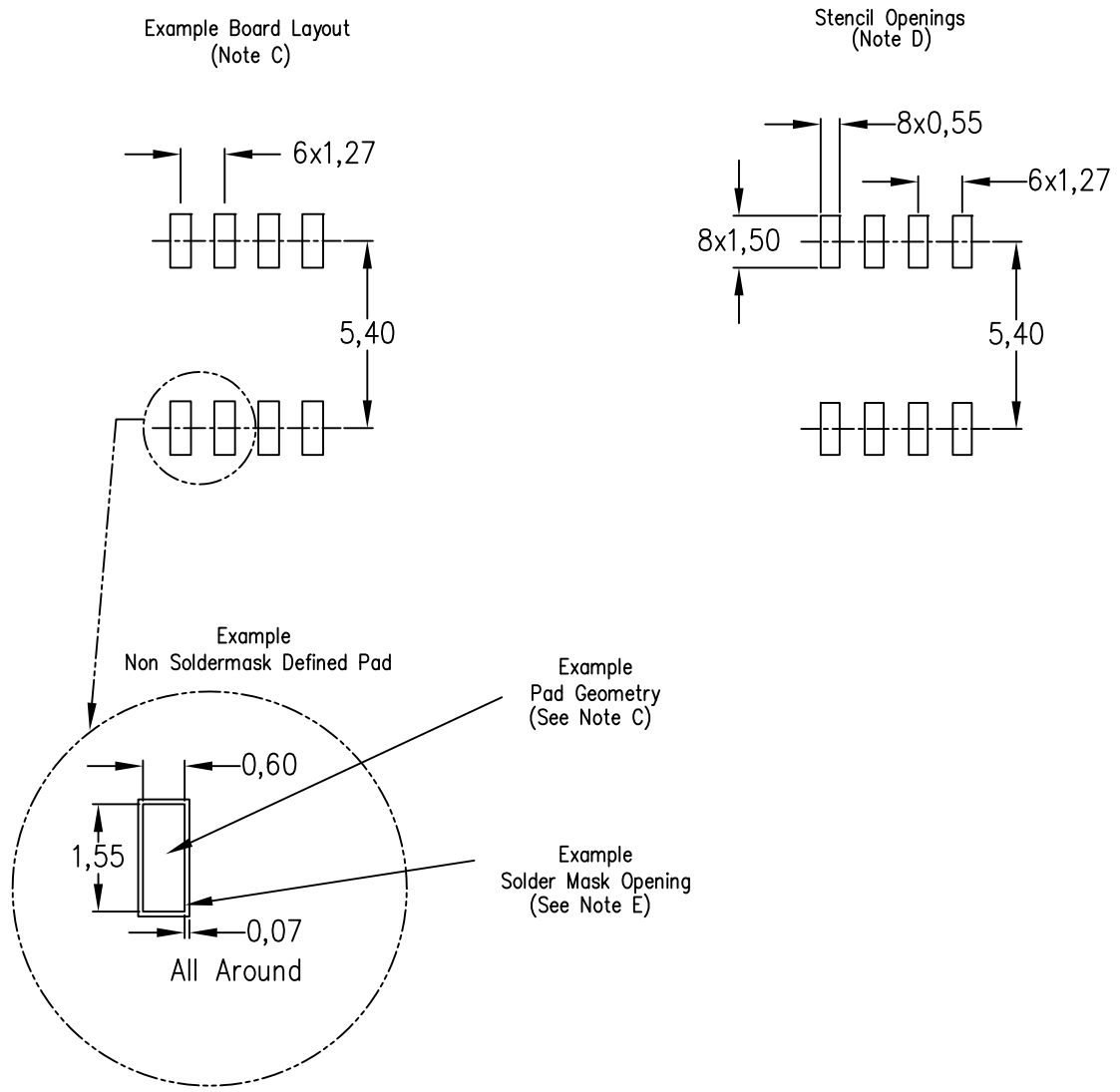
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



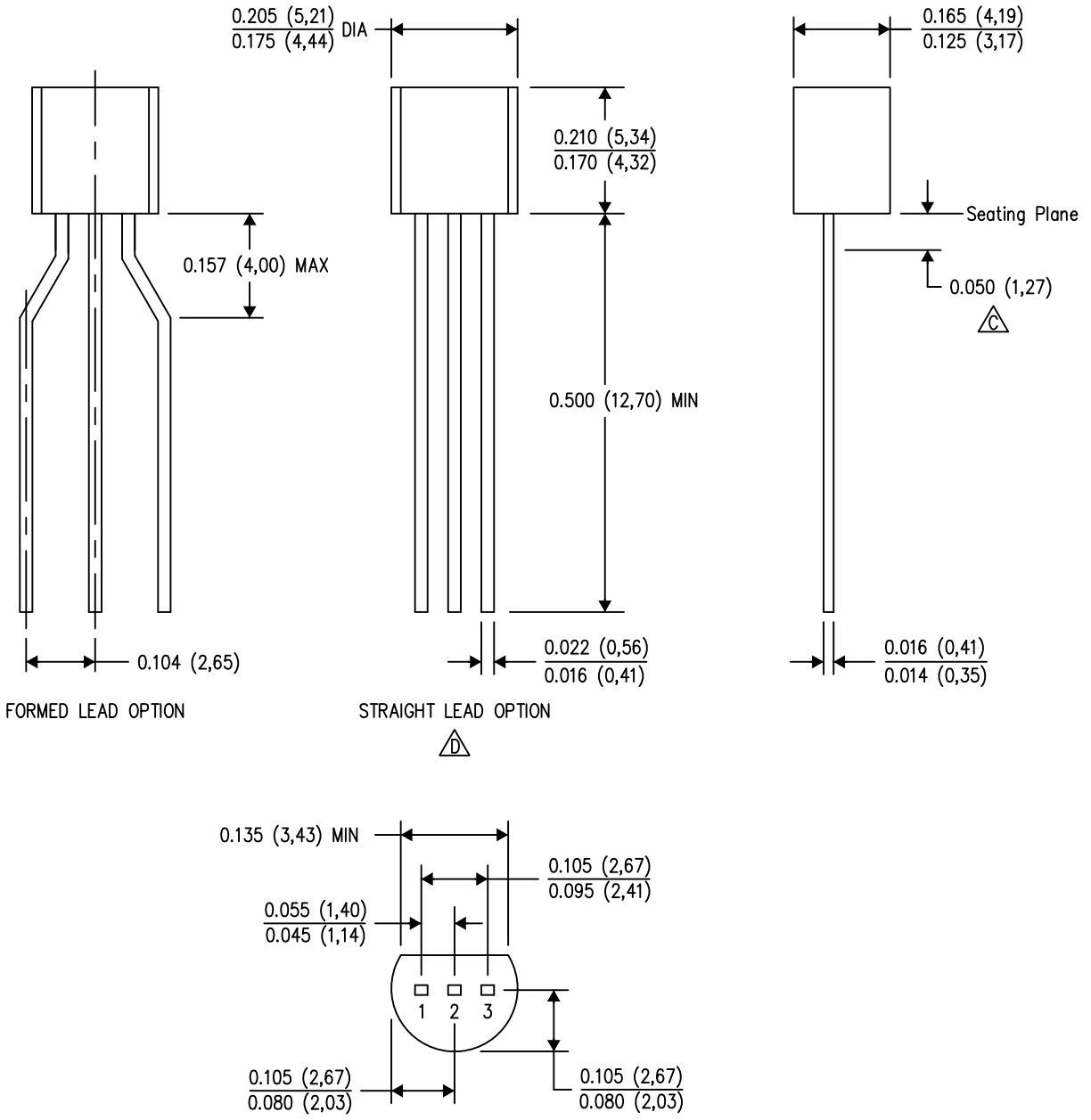
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



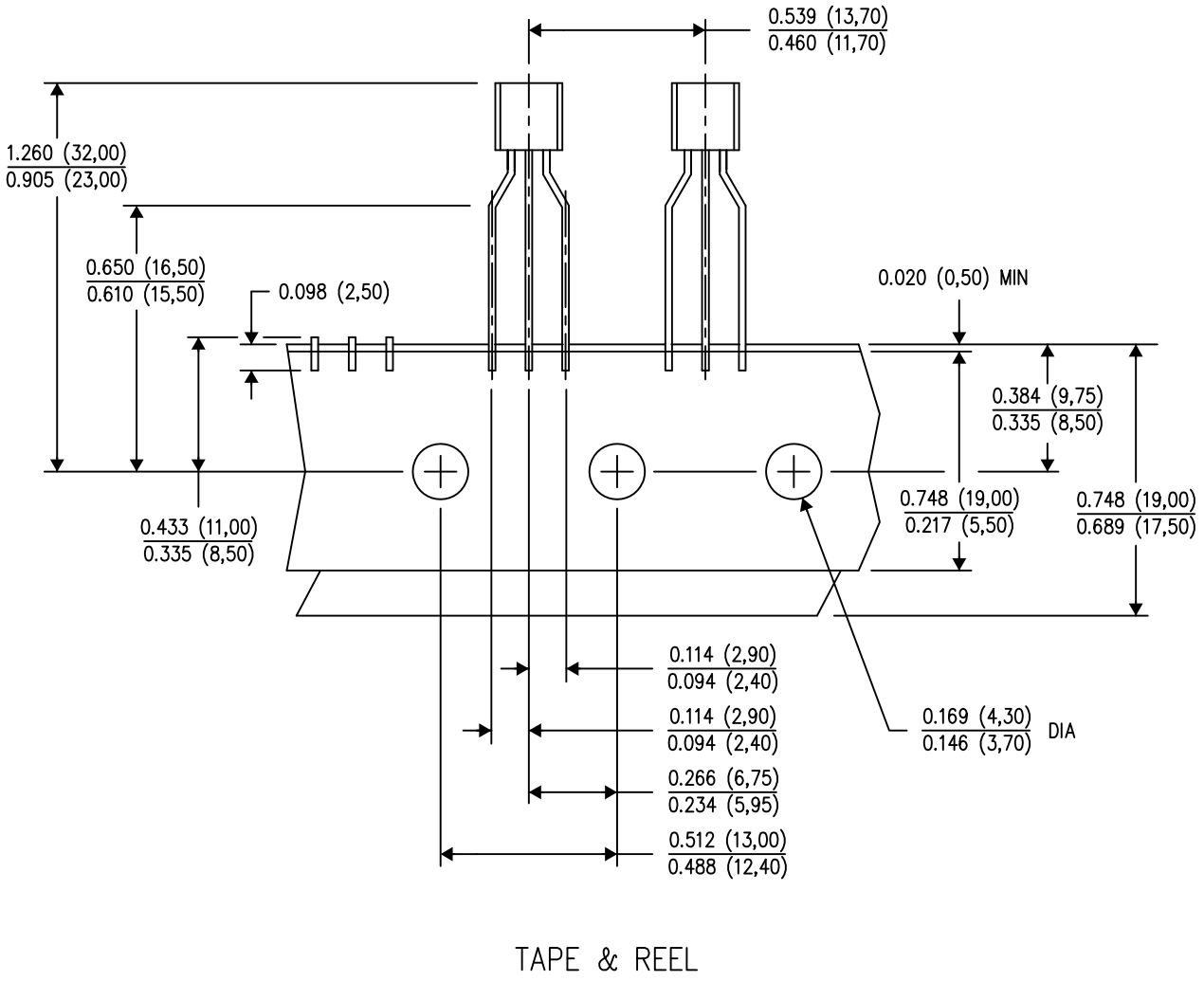
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

LP (O–PBCY–W3) PLASTIC CYLINDRICAL PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. Falls within JEDEC TO–226 Variation AA (TO–226 replaces TO–92).
E. Shipping Method:
Straight lead option available in bulk pack only.
Formed lead option available in tape & reel or ammo pack.
Specific products can be offered in limited combinations of shipping mediums and lead options.
Consult product folder for more information on available options.

LP (O–PBCY–W3) PLASTIC CYLINDRICAL PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Tape and Reel information for the Formed Lead Option package.

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