LOW PIN COUNT SYNCHRONOUS BUCK CONTROLLER

Check for Samples: TPS40190

FEATURES

- **Input Operating Voltage Range: 4.5 V to 15 V**
- **Reference 0.591 V ±1%**
- **Voltage Mode Control**
- **Internal 5-V Regulator For Internal Housekeeping, Driver Power and Light External Loads**
- **Selectable Short-Circuit Protection Thresholds**
- **Pre-Bias Ouput Safe**
- **Fixed Switching Frequency of 300 kHz**
- **Internal Soft-Start**
- **Small 3 mm × 3 mm, 10-Pin SON Package**
- **Bootstrapped Drivers for N-Channel MOSFET**
- **Adaptive Anti-Cross Conduction**
- **Internal Bootstrap Diode**
- **1.2-A Drivers for Decreased Switching Loss**

APPLICATIONS

- **Cable modem CPE**
- **Digital Set Top Box**
- **Graphics/Audio Cards**
- **Entry-level and Mid-Range Servers**

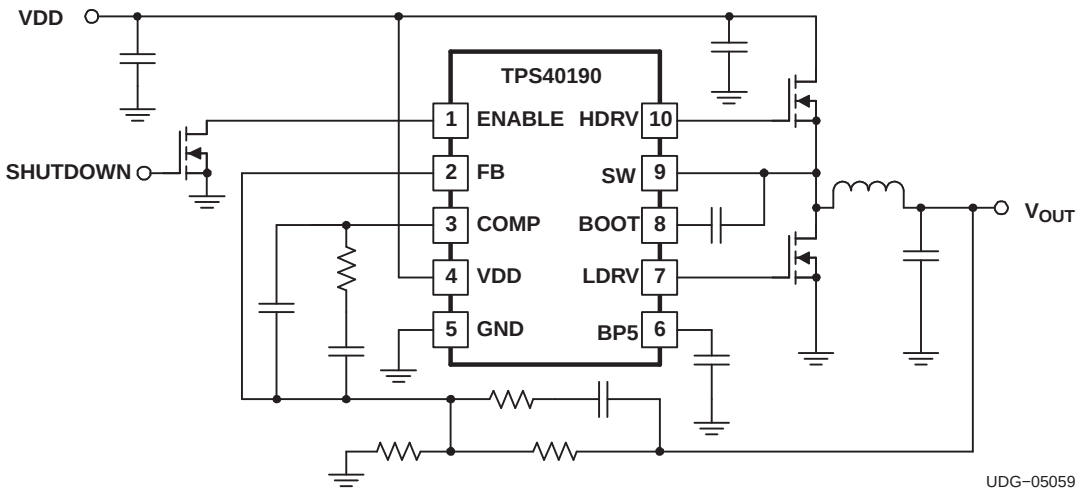
DESCRIPTION

The TPS40190 is a cost-optimized synchronous buck controller that operates from 4.5 V to 15 V nominally, and implements a fixed frequency voltage mode power supply. The controller uses an adaptive anti-cross conduction scheme to prevent both the high-side and the rectifier MOSFET to be turned on at the same time, preventing shoot through current in the two MOSFETs.

The controller also provides a short circuit protection threshold that is user selectable between one of three values. The protection level is set with a single external resistor connected from COMP to GND. During start-up, the impedance connected to COMP is sensed, and the information is decoded to select one of the three thresholds. When the controller senses an output short circuit, both MOSFETs are turned off and a timeout period is observed before attempting to restart. This provides limited power dissipation in the event of a sustained fault.

The TPS40190 provides strong drivers to minimize switching losses in the power stage, reducing heat build up in the MOSFETs and allowing larger MOSFETs to be used without undue switching time penalty.

SIMPLIFIED APPLICATION DIAGRAM



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE	PART NUMBER(1)
-40°C to 85°C	Plastic DRC (SON)	TPS40190DRCR
		TPS40190DRCT

(1) The TPS40190 is available taped and reeled only. Use large reel device type R to order quantities of 3000 units per reel. Use small reel device type T to order quantities of 250 per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TPS40190	UNIT
Input voltage range	VDD	–0.3 to 16.5	V
	SW	–5 to 22	
	BOOT-SW, HDRV-SW (differential from BOOT or HDRV to SW)	–0.3 to 6	
	COMP	–0.3 to 3	
	FB, BP5, LDRV, ENABLE	–0.3 to 6	
T_J	Operating junction temperature range	–40 to 125	°C
T_{stg}	Storage temperature	–55 to 150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$ High-K Board(1) (°C/W)	$R_{\theta JC}$ (2) (°C/W)
DRC	47.9	14.1

(1) The JEDEC High-K (2s2p) board design used to derive this data was a 3-inch x 3-inch (7.5-cm x 7.5-cm), multilayer board with one-ounce internal power and ground planes and two-ounce copper traces on top and bottom of the board.
(2) The junction-to-case impedance is measured from the die to the thermal pad on the device package.

RECOMMENDED OPERATING CONDITIIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Input voltage	4.5		15	V
T_A	Operating free-air temperature	-40		85	°C

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ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, V_{VDD}= 12 V_{dc}, T_A =T_J, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
V_{FB}	Feedback voltage range	0°C ≤ T_J ≤ 85°C	585	591	597	mV
		-40°C ≤ T_J ≤ 85°C	582	591	597	
INPUT SUPPLY						
V_{VDD}	Input voltage range		4.5		15.0	V
I_{VDD}	Operating current	V_{ENABLE} = 2.5 V, Outputs switching			2.5	mA
		V_{ENABLE} = 0.6 V			20	µA
ON BOARD REGULATOR						
V_{5VBP}	Output voltage	V_{VDD} > 6 V, I_{5VBP} ≤ 10 mA	5.1	5.3	5.5	V
V_{DO}	Regulator dropout voltage	V_{VDD} - V_{BP5} , V_{VDD} = 5 V, I_{BP5} ≤ 25 mA		270	400	mV
I_{SC}	Regulator current limit threshold		40			mA
I_{BP5}	Average current(1)				40	
OSCILLATOR						
f_{SW}	Switching frequency		240	300	360	kHz
V_{RMP}	Ramp amplitude(2)			0.75		V
V_{VALLEY}	Valley voltage(2)			0.5		
PWM						
D_{MAX}	Maximum duty cycle(2)		85%			
$t_{ON(min)}$	Minimum controlled pulse(2)				130	ns
t_{DEAD}	Output driver dead time	HDRV off to LDRV on		50		
		LDRV off to HDRV on		25		
SOFT-START						
t_{SS}	Soft-start time		3.0	4.7	7.0	ms
t_{SSDLY}	Soft-start delay time(3)			6		
t_{REG}	Time to regulation			10.5		
ERROR AMPLIFIER						
GBWP	Gain bandwidth product(2)		5			MHz
A_{OL}	DC gain(2)		60			dB
I_{IB}	Input bias current (current out of FB pin)		100		0	nA
I_{EAOP}	Output source current	V_{FB} = 0 V	1			mA
I_{EAOM}	Output sink current	V_{FB} = 2 V	1			
SHORT CIRCUIT PROTECTION						
$t_{PSS(min)}$	Minimum pulse during short circuit(2)				250	ns
t_{BLNK}	Blanking time(2)		100	140	180	
t_{OFF}	Off-time between restart attempts		25	95		ms
V_{ILIM}	Short circuit comparator threshold voltage	$R_{COMP(GND)}$ = OPEN, T_J = 25°C	256	320	384	mV
		$R_{COMP(GND)}$ = 4 kΩ, T_J = 25°C	128	160	192	
		$R_{COMP(GND)}$ = 12 kΩ, T_J = 25°C	368	460	552	

(1) 40 mA is the current available for MOSFET gate drive, the device itself and any external loads. The sum of these must not exceed 40 mA.
(2) Specified by design. Not production tested.
(3) The delay time is the time delay from application of power to the device or from assertion of ENABLE until the output begins to rise.

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ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, V_{VDD}= 12 V_{dc}, T_A =T_J, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVERS						
R_{HDHI}	High-side driver pull-up resistance	V_{BOOT} - V_{SW} = 4.5 V, I_{HDRV} = -100 mA		3	6	Ω
R_{HDLO}	High-side driver pull-down resistance	V_{BOOT} - V_{SW} = 4.5 V, I_{HDRV} = 100 mA		1.5	3.0	
R_{LDHI}	Low-side driver pull-up resistance	I_{LDRV} = -100 mA		2.5	5.0	
R_{LDLO}	Low-side driver pull-down resistance	I_{LDRV} = 100 mA		0.80	1.50	
t_{HRISE}	High-side driver rise time (4)	C_{LOAD} = 1 nF		15	35	ns
t_{HFALL}	High-side driver fall time (4)			10	25	
t_{LRISE}	Low-side driver rise time (4)			15	35	
t_{LFALL}	Low-side driver fall time (4)			10	25	
UVLO						
V_{UVLO}	Turn-on voltage		4.10	4.25	4.40	V
$UVLO_{HYST}$	Hysteresis		270	320	370	mV
SHUTDOWN						
V_{IH}	High-level input voltage, ENABLE				2.8	V
V_{IL}	Low-level input votlage, ENABLE		0.6			
BOOT DIODE						
V_{DFWD}	Bootstrap diode forward voltage	I_{BOOT} = 5 mA	0.6	0.8	1.2	V

(4) Specified by design. Not production tested.

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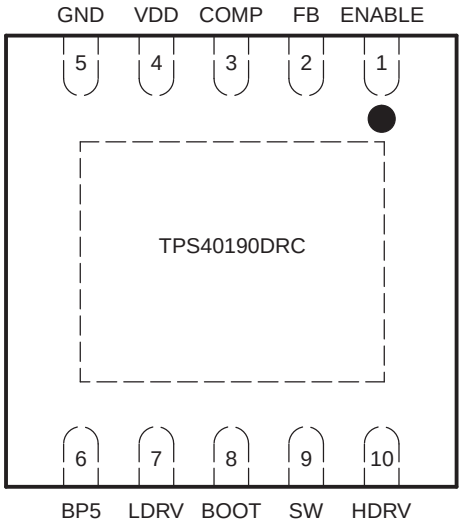
DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BOOT	8	I	Power supply for the flying high-side driver
BP5	6	O	Output bypass for the internal regulator. Connect 4.7-µF capacitor from this pin to GND. Low power, low noise loads may be connected here if desired. The sum of the external load and the gate drive requirements must not exceed 40 mA. The regulator is turned off when the ENABLE pin is pulled low.
COMP	3	O	Output of the error amplifier. Connecting a resistance from COMP to GND sets the output short circuit detection threshold. See applications information for details.
ENABLE	1	I	Logic level input that starts or stops the controller from an external user command. A high level turns the controller on. This pin has a high-impedance internal pull-up integrated into the device. Because this pin is high impedance, a 10-nF capacitor to ground or an external pull-up resistor (100 kΩ) to VDD is recommended to avoid noise coupling to this pin.
FB	2	I	Inverting input to the error amplifier
GND	5	-	Common connection for the controller
HDRV	10	O	Bootstrapped output for driving the gate of the high side N channel FET.
LDRV	7	O	Output to the rectifier FET gate
SW	9	I	Sense line for the adaptive anti cross conduction circuitry. Serves as common connection for the flying high side FET driver
VDD	4	I	Power input to the controller

DRC PACKAGE
(TOP VIEW)



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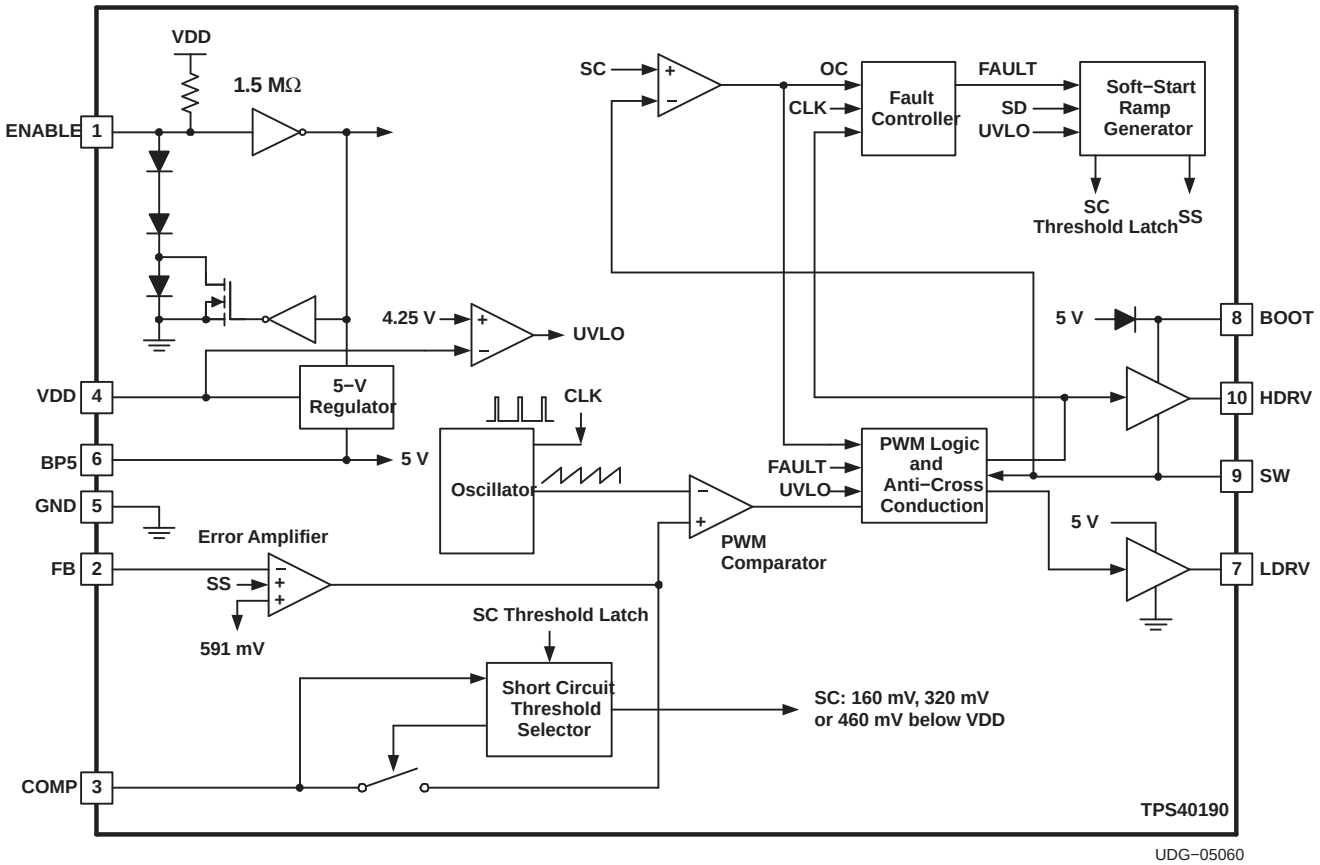
APPLICATION INFORMATION

Introduction

The TPS40190 is a cost optimized controller providing all the necessary features to construct a high-performance DC-DC converter while keeping costs to a minimum. Support for pre-biased outputs eliminates concerns about damaging sensitive loads during startup. Strong gate drivers for the high side and rectifier N-channel MOSFETs decrease switching losses for increased efficiency. Adaptive gate drive timing minimizes body diode conduction in the rectifier MOSFET, also increasing efficiency. Selectable short circuit protection thresholds and hiccup recovery from a short-circuit increase design flexibility and minimize power dissipation in the event of a prolonged output fault. A dedicated enable pin (ENABLE) allows the converter to be placed in a very low quiescent current shutdown mode.



Internally fixed switching frequency and soft-start time reduce external component count, simplifying design and layout, as well as reducing footprint and cost. The 3 mm × 3 mm package size also contributes to a reduced overall converter footprint.

Internally Fixed Parameters

The TPS40190 has a fixed internal switching frequency of 300 kHz. Soft-start time is fixed at 4.7 ms typical and the UVLO level is set between 4.1 V and 4.4 V.

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Output Short Circuit Protection

The short circuit detection in the TPS40190 is done by sensing the voltage drop across the high side FET when it is on. If the voltage drop across this FET exceeds the selected threshold in any given switching cycle, a counter counts up one count and the FET is turned off early. If the voltage drop across that FET does not exceed this threshold, the counter is decremented for that cycle and the FET is allowed to remain on for the normal pulse width commanded by the internal pulse width modulator. If the counter fills up (a count of 7) a fault condition is declared and the drivers turn both FETs off. After a timeout of approximately 95 ms, the controller attempts to restart. If a short circuit is still present at the output, the current ramps quickly up to the short-circuit threshold and another fault condition is declared. The device then waits 95 ms to attempt to restart again.

Typical waveforms during a short circuit event are shown in Figure 1 and Figure 2.

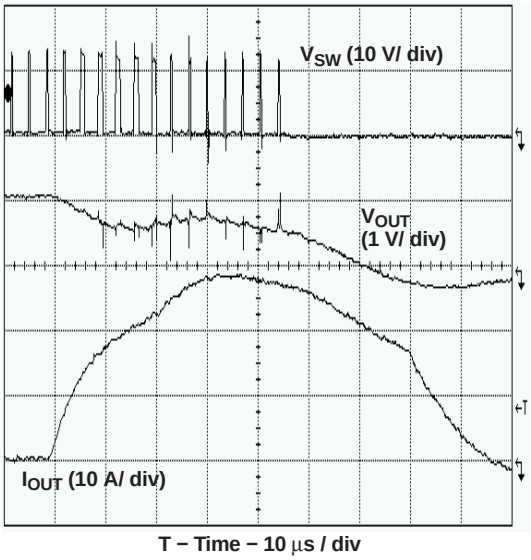

Figure 1. Output Short Circuit Detected (Nominal Threshold 25 A)

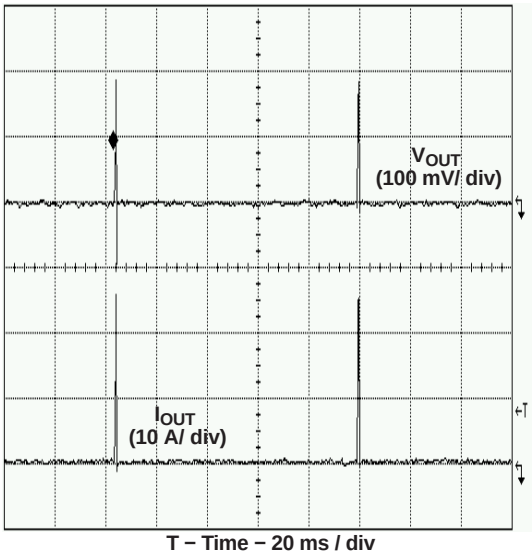

Figure 2. Output Fault Hiccup Restart Timing

The TPS40190 provides three selectable short circuit protection thresholds: 160 mV, 320 mV and 460 mV. The particular threshold is selected by connecting a resistor from COMP to GND. Table 1 gives the short circuit thresholds for corresponding resistors from COMP to GND. Note that since the TPS40190 measures the resistance from COMP to GND during a 2-ms window, the compensation network from COMP to FB should have a time constant significantly less than 1 ms or there can be issues detecting the resistance and setting the correct short circuit threshold. This network should have no DC path from COMP to FB.

The short circuit detection threshold in the TPS40190 has some temperature compensation built in to help offset the high-side FET rise in resistance as its temperature rises. A typical FET has a resistance temperature coefficient of about 4500 ppm/°C. The temperature coefficient of the short circuit threshold is approximately 4200 ppm/°C. Figure 3 shows how the short circuit threshold increases with temperature to help compensate for the FET resistance increase. The relative FET resistance change is based on an estimate of a linear 4500 ppm/°C temperature coefficient. The effectiveness of this compensation depends on how tight the thermal coupling between the TPS40190 and the high-side FET is. Better thermal coupling between the TPS40190 and the high-side FET gives better compensation effectiveness.

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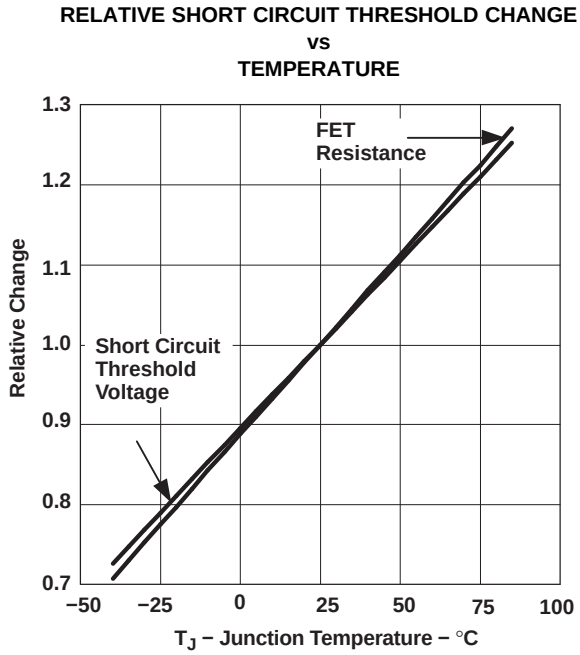

Figure 3.

Table 1. Short Circuit Threshold Voltage Selection

Short Circuit Protection Resistance R_{COMP} (kΩ)	Nominal Current Limit Voltage V_{ILIM} (mV)
10.8 to 13.2	460
OPEN	320
3.6 to 4.4	160

The range of short circuit current thresholds that can be expected is given by Equation 1 and Equation 2.

$$I_{SCP(max)} = \frac{V_{ILIM(max)}}{R_{DS(onMIN)}}$$

$$I_{SCP(min)} = \frac{V_{ILIM(min)}}{R_{DS(onMAX)}} \quad (1)$$

where

- I_{SCP} is the short circuit current
- V_{ILIM} is the short circuit threshold
- $R_{DS(on)}$ is the channel resistance of the high-side MOSFET (2)

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Enable Functionality

The TPS40190 has a dedicated ENABLE pin. This simplifies user level interface design since no multiplexed functions exist. Another benefit is a true low power shutdown mode of operation. In this state, the BP5 regulator is turned off. When the ENABLE pin is pulled to GND, the TPS40190 consumes a typical 20-µA of current. A functionally equivalent circuit to the enable circuitry on the TPS40190 is shown in Figure 4.

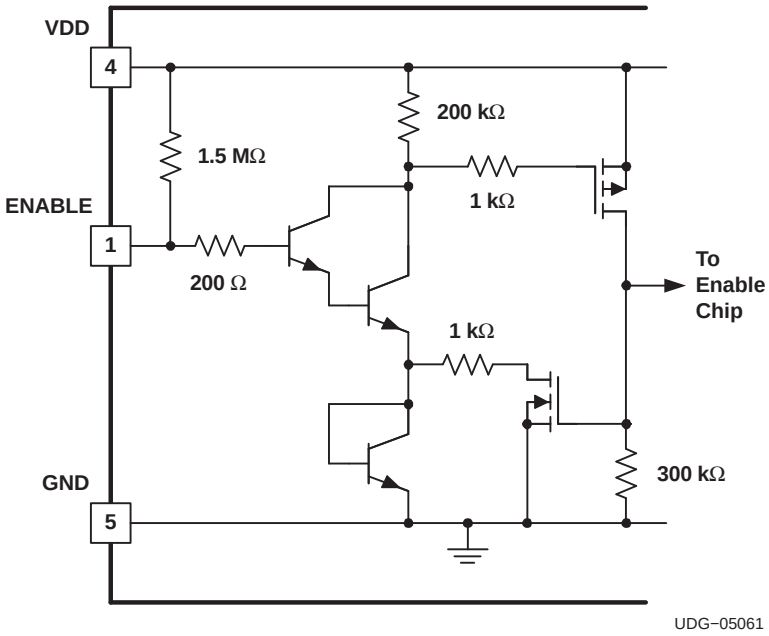

Figure 4. TPS40190 ENABLE Pin Internal Circuitry

If the ENABLE pin is left floating, the chip starts automatically. The pin must be pulled to less than 600 mV to ensure that the TPS40190 is in shutdown mode. Note that the ENABLE pin is relatively high impedance. In some situations, there could be enough noise nearby to cause the ENABLE pin to swing below the 600 mV threshold and give erroneous shutdown commands to the rest of the device. There are two solutions to this problem should it arise.

1. Place a capacitor from ENABLE to GND. A side effect of this is to delay the start of the converter while the capacitor charges past the enable threshold
2. Place a resistor from VDD to ENABLE. This causes more current to flow in the shutdown mode, but does not delay converter startup. If a resistor is used, the total current into the ENABLE pin should be limited to no more than 500 µA.

The ENABLE pin is self-clamping. The clamp voltage can be as low as 1 V with a 1-kΩ ground impedance. Due to this self-clamping feature, the pull-up impedance on the ENABLE pin should be selected to limit the sink current to less than 500 µA. Driving the ENABLE pin with a low-impedance source voltage can result in damage to the device. Because of the self-clamping feature, it requires care when connecting multiple ENABLE pins together. For enabling multiple TPS4019x devices (TPS40190, TPS40192, TPS40193, TPS40195, TPS40197), see the Application Report SLVA509.

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Typical waveforms for startup and shutdown using the ENABLE pin are shown in Figure 5 and Figure 6.

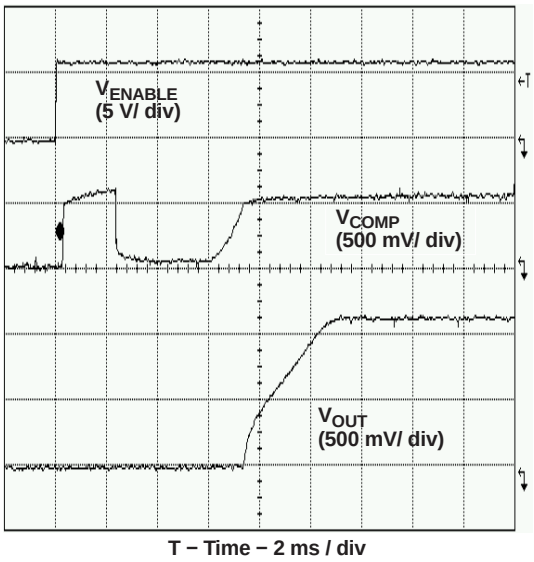

Figure 5. Startup Using ENABLE Pin

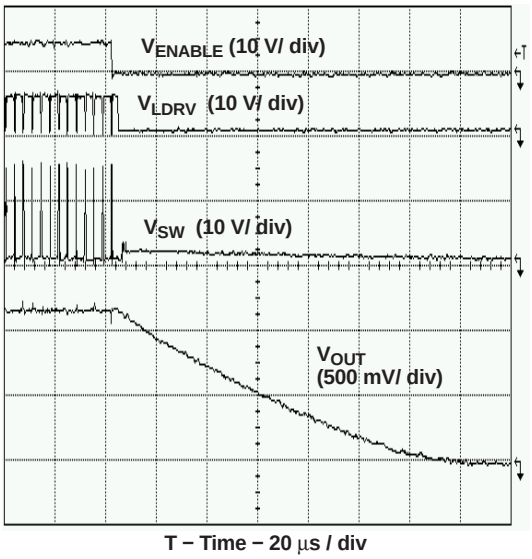

Figure 6. Shutdown Using ENABLE Pin

5-V Regulator

The TPS40190 has an on board 5-V regulator that allows the part to operate from a single voltage feed. No separate 5-V feed to the part is required. This regulator needs to have 4.7-µF of capacitance on the BP5 pin for stability. A ceramic capacitor is suggested for this purpose.

This regulator can also be used to supply power to nearby circuitry, eliminating the need for a separate LDO in some cases. If this pin is used for external loads, keep in mind that this is the power supply for the internals of the TPS40190. While efforts have been made to reduce sensitivity, any noise induced on this line has an adverse effect on the overall performance of the internal circuitry and shows up as increased pulse jitter, or skewed reference voltage. This regulator is turned off when the ENABLE pin is pulled low.

The amount of power available from this pin varies with the size of the power MOSFETs that the drivers must operate. Larger MOSFETs require more gate drive current and reduces the amount of power available on this pin for other tasks.

The total amount of current required by the gate drive and the external circuitry should not exceed 40 mA. The current required to drive the FET gates can be found from Equation 3.

$$I_G = f_{SW} \times \left(Q_{G\,(high)} + Q_{G\,(low)}\right)$$

Where

- I_G is the required gate drive current
- f_{SW} is the switching frequency (300 kHz)
- $Q_{G(high)}$ is the gate charge requirement for the high-side FET at 5 V V_{GS}
- $Q_{G(low)}$ is the gate charge requirement for the low-side FET at 5 V V_{GS} (3)

Startup Sequence and Timing

The TPS40190 startup sequence is as follows. After input power is applied, the 5-V onboard regulator comes up. Once this regulator comes up, the TPS40190 goes through a period where it samples the impedance at the COMP pin and decides the short circuit protection threshold voltage. This is accomplished by placing 400 mV on the COMP pin for approximately 2 ms. During this time, the current is measured and compared against internal thresholds to select the short circuit protection threshold. After this, the COMP pin is brought low for 4 ms. This ensures that the feedback loop is preconditioned at startup and no sudden output rise occurs at the output of the converter when the converter is allowed to start switching. After these initial 6 milliseconds, the internal soft-start circuitry is engaged and the converter is allowed to start. See Figure 7.

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Pre-Bias Outputs

Some applications require that the converter not sink current during startup if a pre-existing voltage is higher than the output. Since synchronous buck converters inherently sink current some method of overcoming this characteristic must be employed. Applications that require this operation are typically power rails for a multi supply processor or ASIC. The method used in this controller, is to not allow the low side or rectifier FET to turn on until there the output voltage commanded by the start up ramp is higher than the pre-existing output voltage. This is detected by monitoring the internal pulse width modulator (PWM) for its first output pulse. Since this controller uses a closed loop startup, the first output pulse from the PWM does not occur until the output voltage is commanded to be higher than the pre-existing voltage. This effectively limits the controller to sourcing current only during the startup sequence.

If the pre-existing voltage is higher than the intended regulation point for the output of the converter, the converter starts and sinks current when the soft-start time has completed. A typical pre-biased startup is shown in Figure 8.

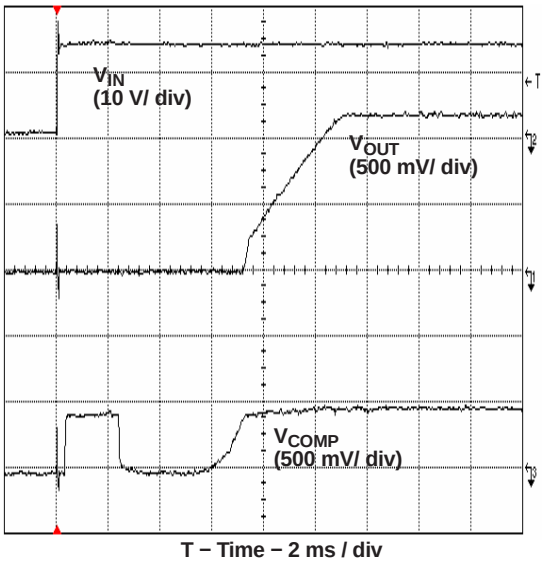

Figure 7. TPS40190 Startup Timing

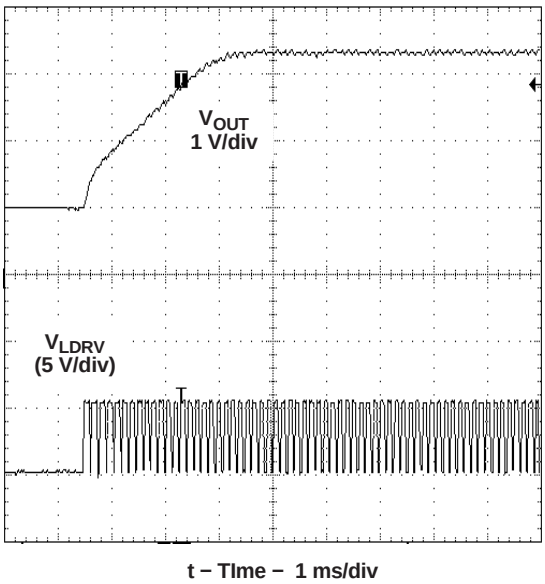

Figure 8. Prebiased Startup Timing

Typical Applications

Some typical applications.

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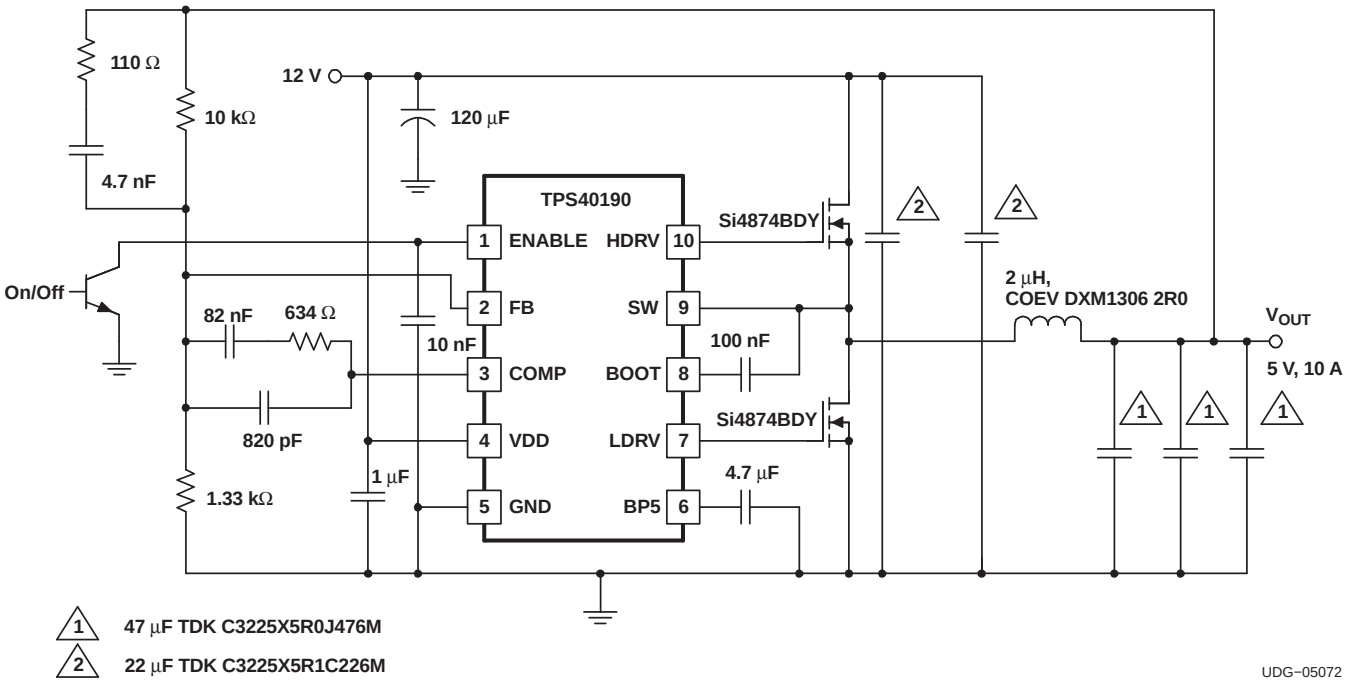

Figure 9. 12-V to 5-V at 10 A

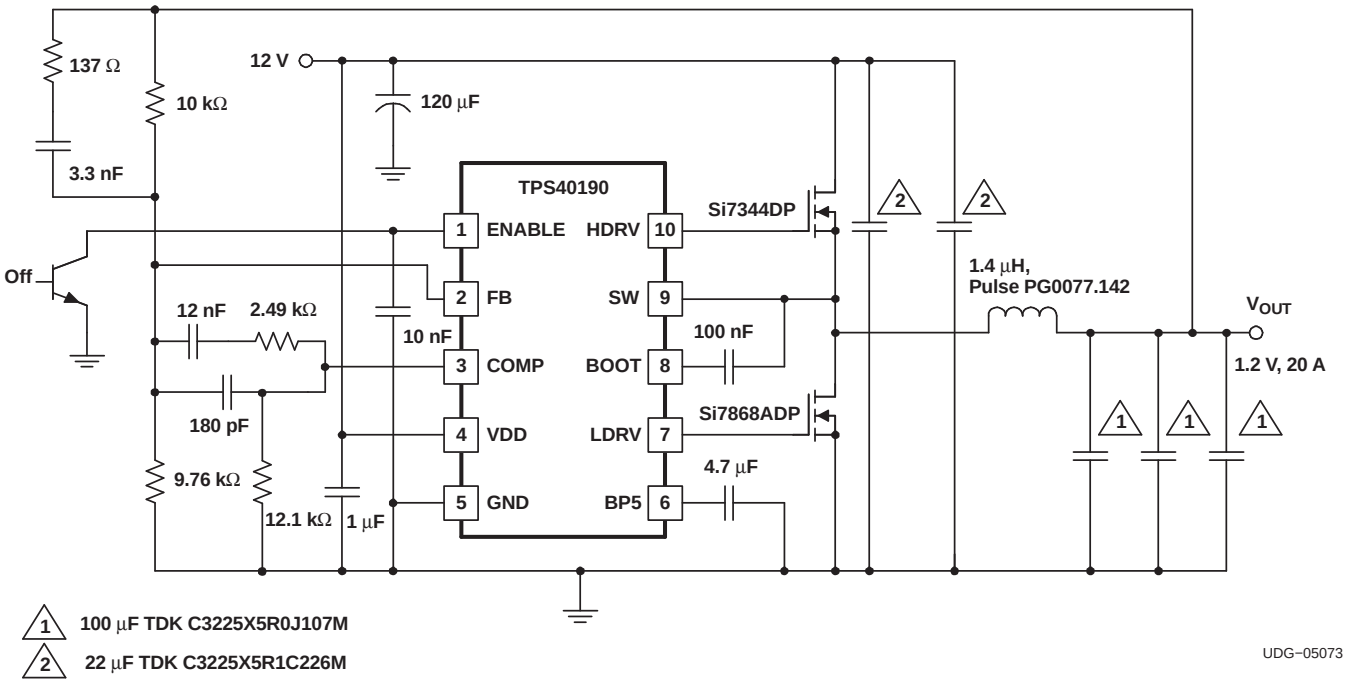

Figure 10. 12-V to 1.2-V at 20 A

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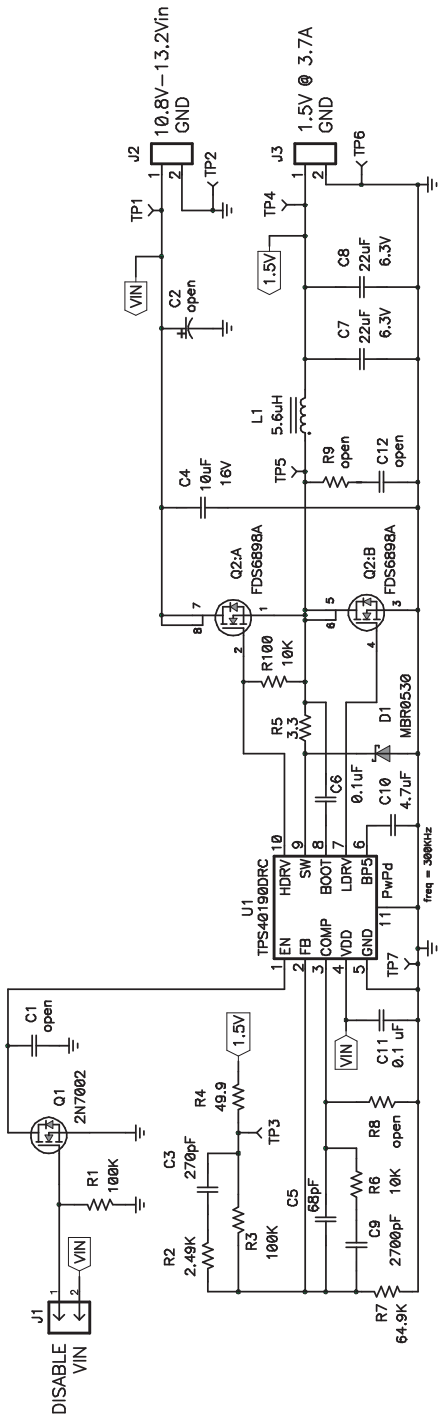

Figure 11. PMP1285, 12-V to 1.5-V, at 3.7 A

Typical Characteristics

REFERENCE VOLTAGE vs TEMPERATURE

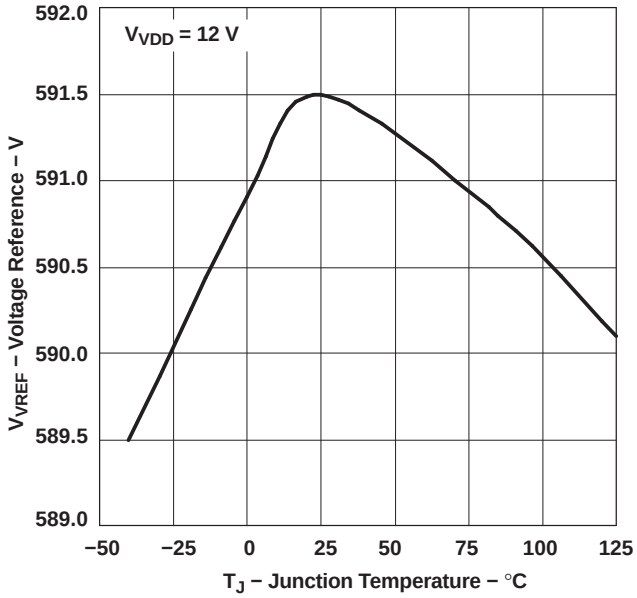

Figure 12.

REFERENCE VOLTAGE vs INPUT VOLTAGE

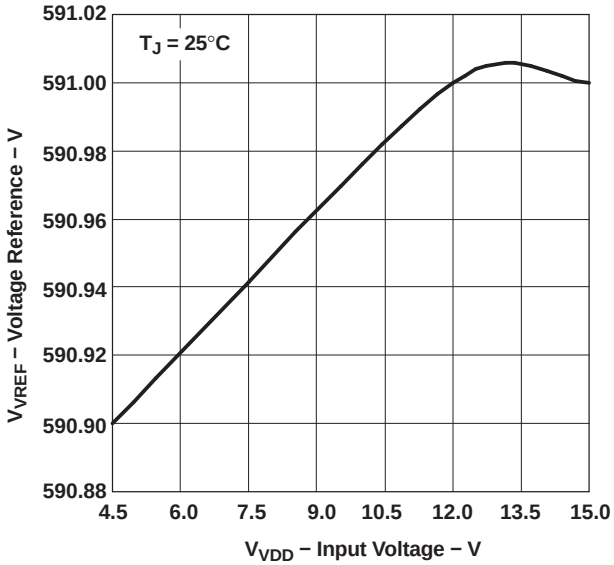

Figure 13.

OSCILATOR FREQUENCY vs TEMPERATURE

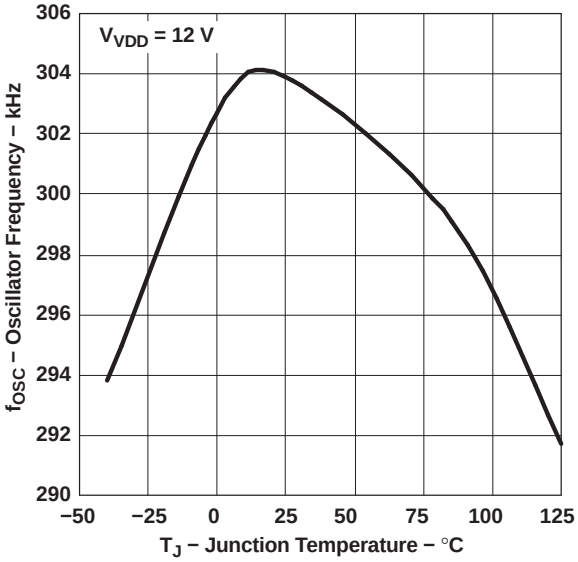

Figure 14.

OSCILATOR FREQUENCY vs INPUT VOLTAGE

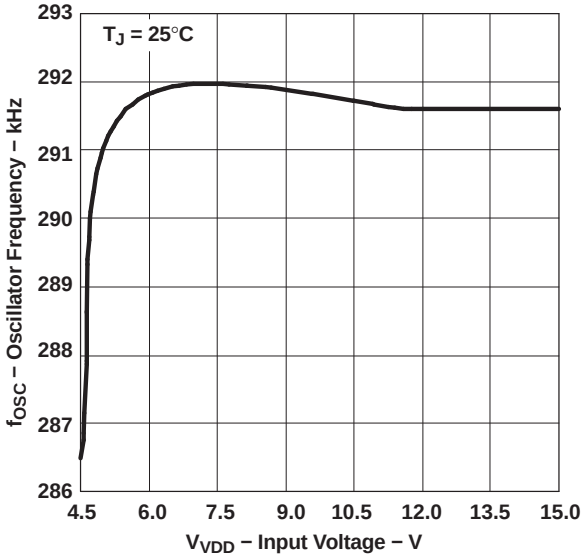

Figure 15.

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Typical Characteristics (continued)

OPERATING CURRENT vs TEMPERATURE

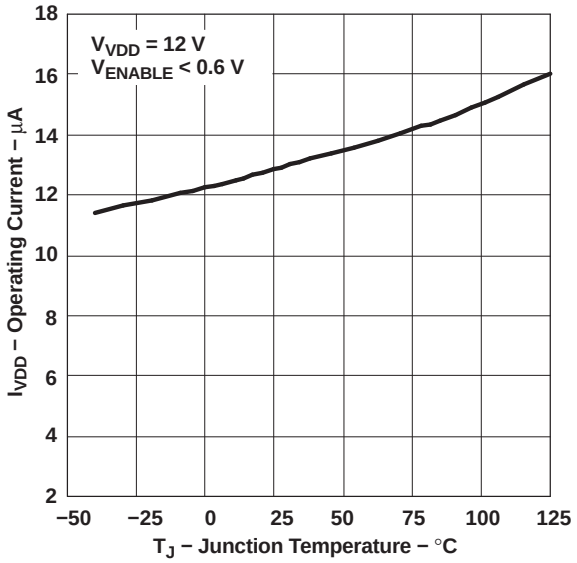

Figure 16.

OPERATING CURRENT vs INPUT VOLTAGE

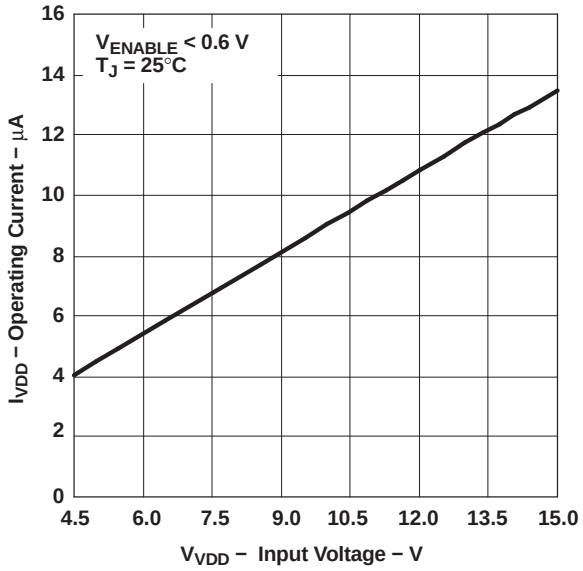

Figure 17.

ENABLE THRESHOLD ON vs TEMPERATURE

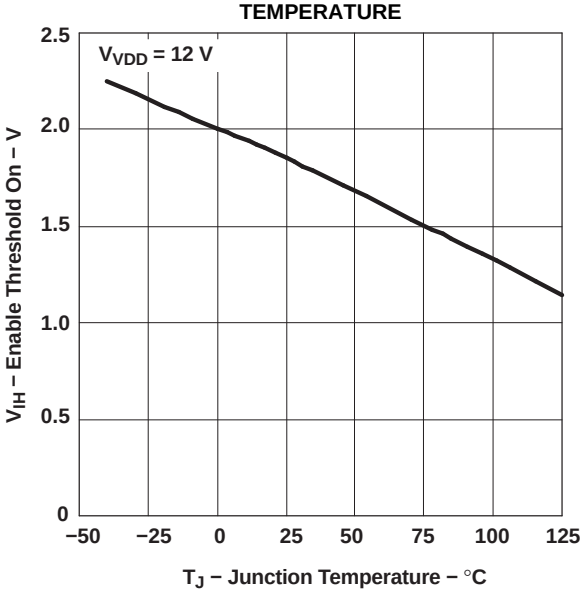

Figure 18.

ENABLE THRESHOLD ON vs INPUT VOLTAGE

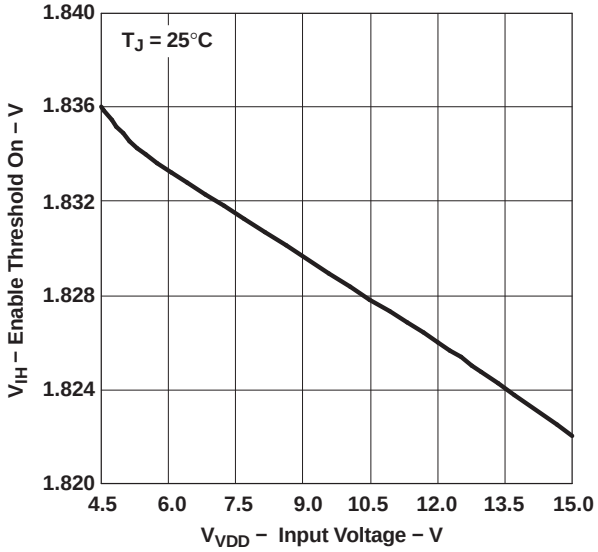

Figure 19.

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Typical Characteristics (continued)

ENABLE THRESHOLD OFF vs TEMPERATURE

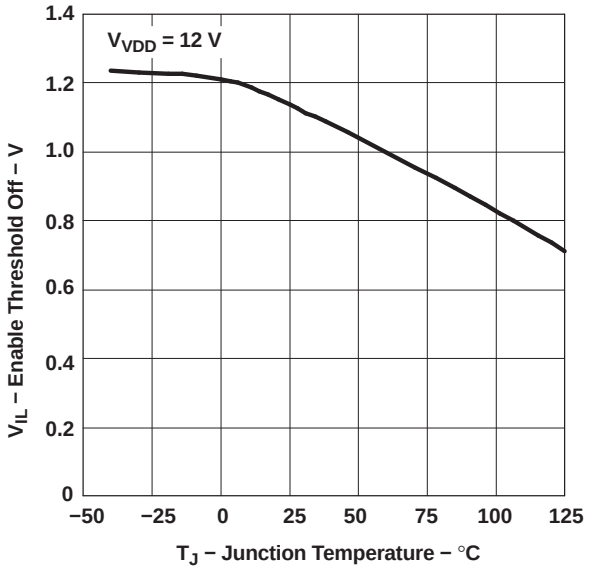

Figure 20.

ENABLE THRESHOLD OFF vs INPUT VOLTAGE

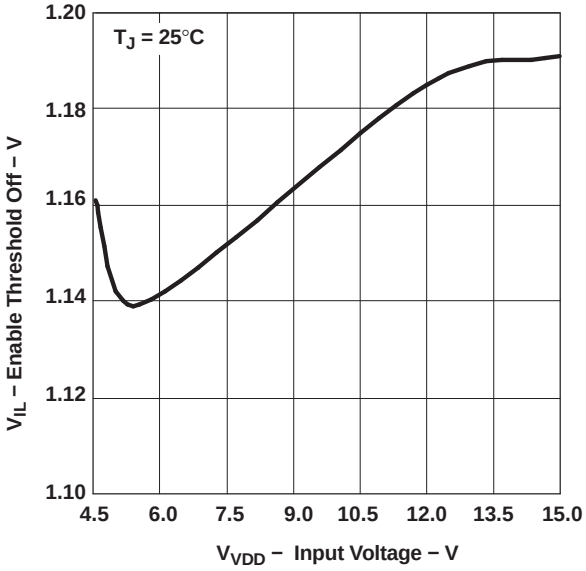

Figure 21.

SOFT START TIMING vs TEMPERATURE

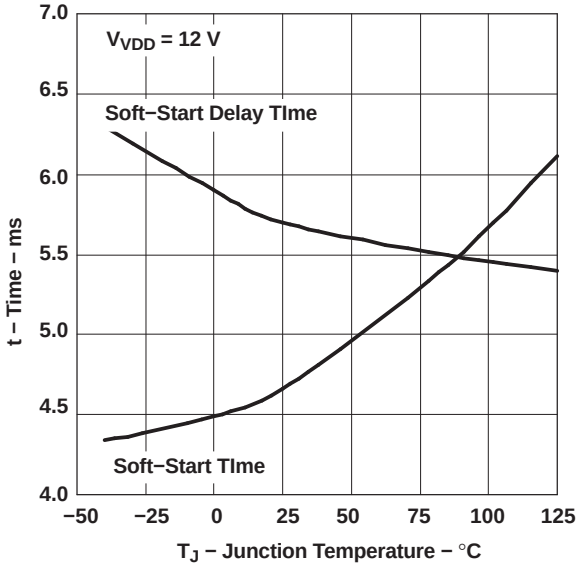

Figure 22.

TOTAL STARTUP TIME vs TEMPERATURE

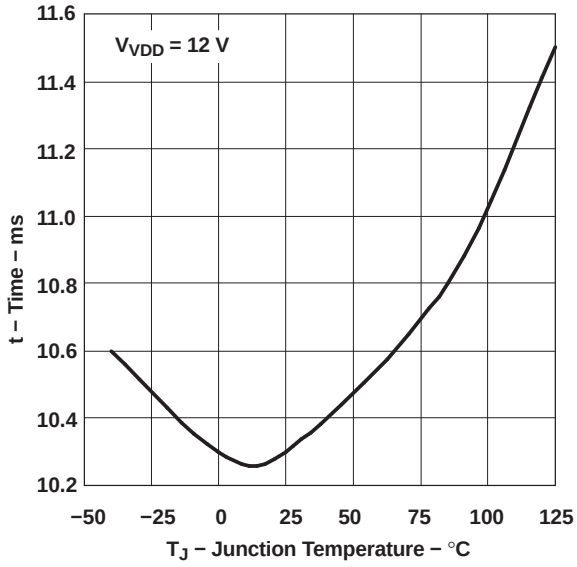

Figure 23.

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Typical Characteristics (continued)

SOFT START TIMING vs INPUT VOLTAGE

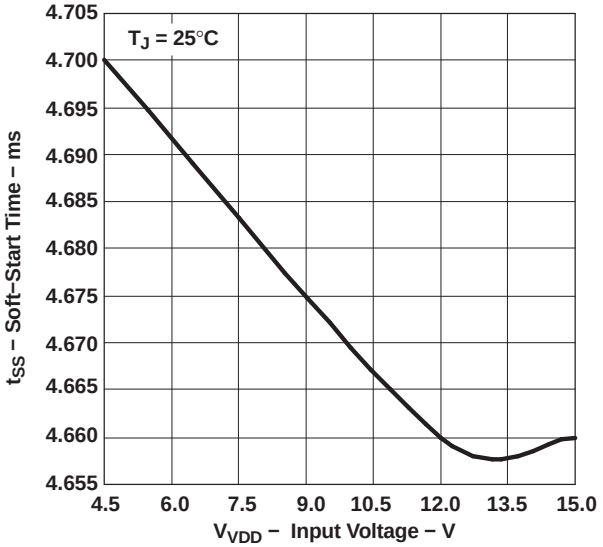

Figure 24.

CURRENT LIMIT THRESHOLD vs TEMPERATURE

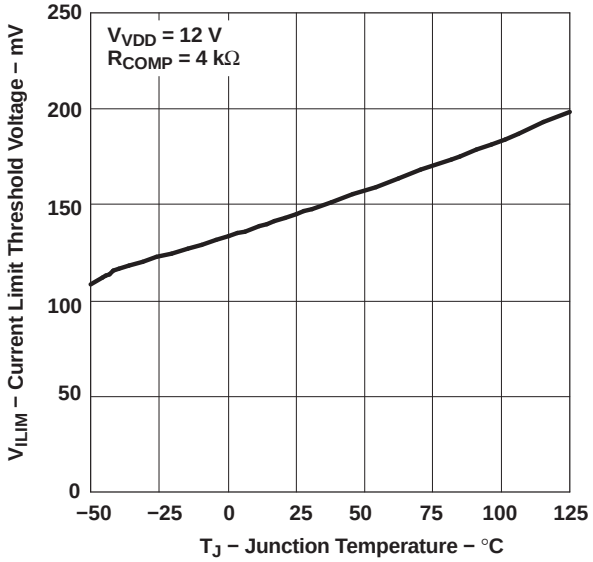

Figure 25.

CURRENT LIMIT THRESHOLD vs INPUT VOLTAGE

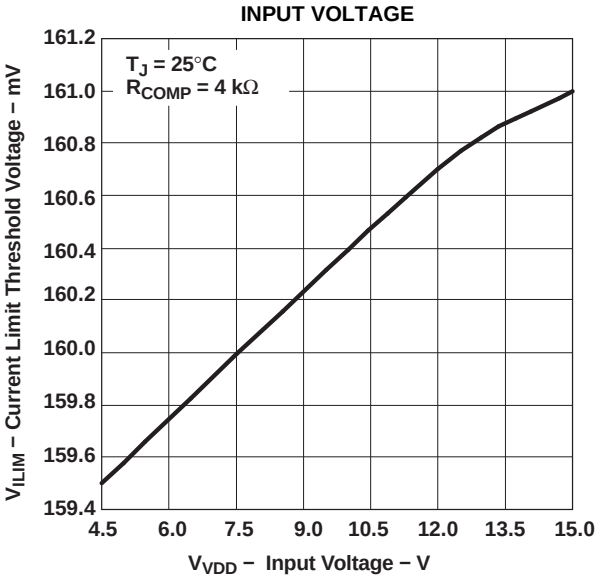

Figure 26.

CURRENT LIMIT THRESHOLD vs TEMPERATURE

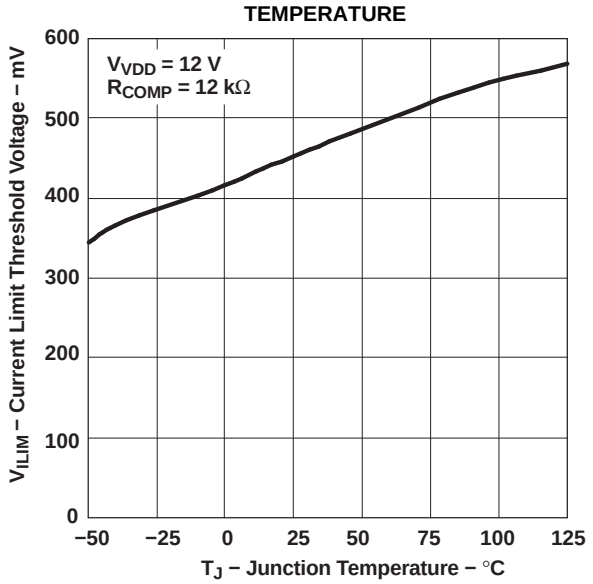

Figure 27.

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Typical Characteristics (continued)

CURRENT LIMIT THRESHOLD vs INPUT VOLTAGE

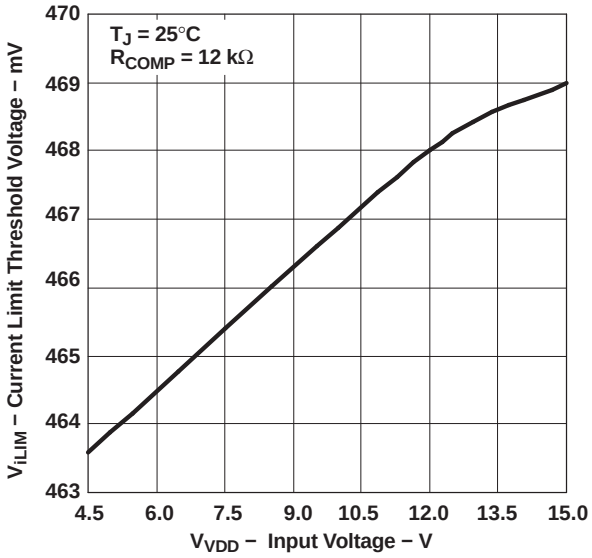

Figure 28.

CURRENT LIMIT THRESHOLD vs TEMPERATURE

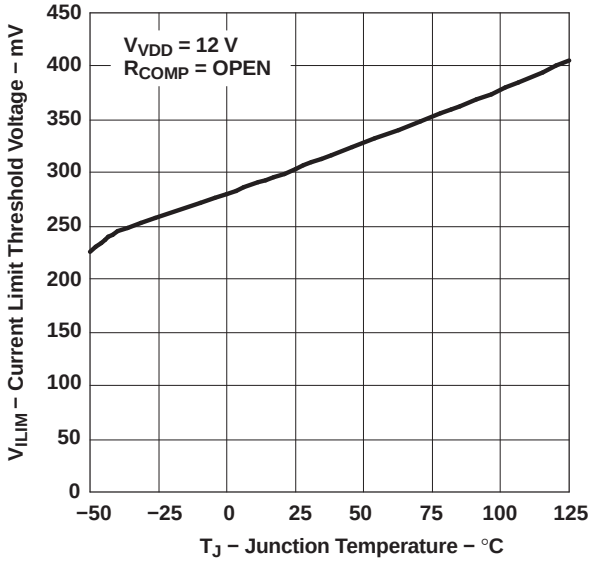

Figure 29.

CURRENT LIMIT THRESHOLD vs INPUT VOLTAGE

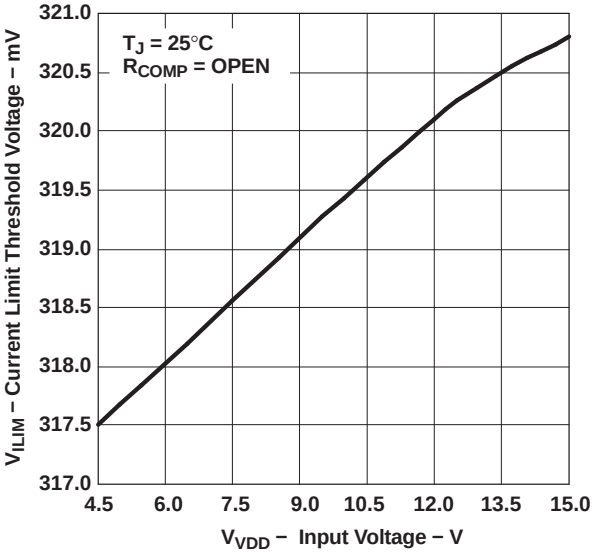

Figure 30.

UNDERVOLTAGE LOCKOUT TURN ON VOLTAGE vs TEMPERATURE

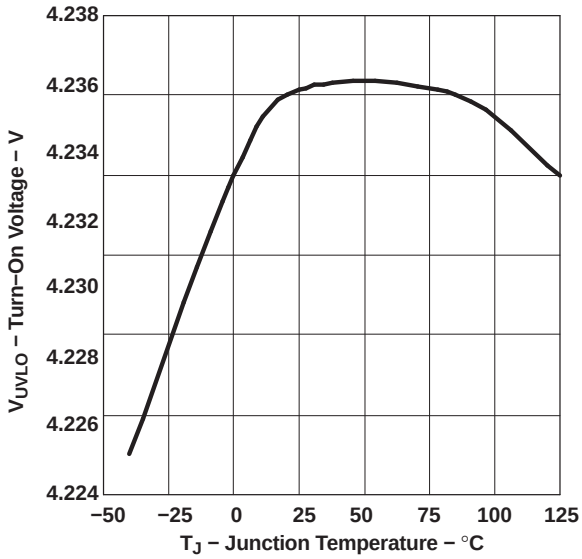

Figure 31.

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REVISION HISTORY

Changes from Revision B (August 2007) to Revision C	Page
• Added a new paragraph to the end of the Enable Functionality section	9

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40190DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0190	Samples
TPS40190DRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0190	Samples
TPS40190DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0190	Samples
TPS40190DRCTG4	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0190	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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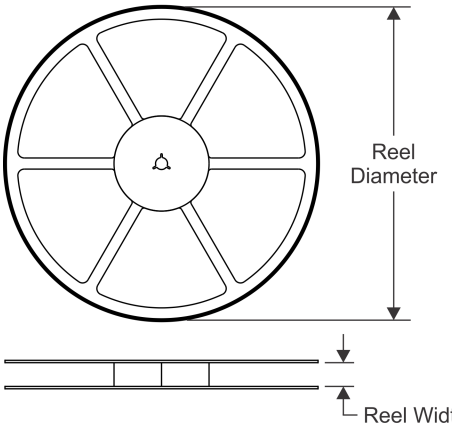
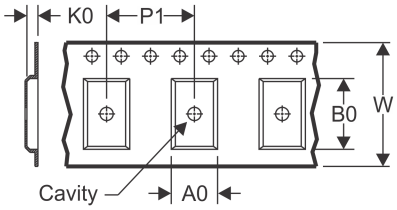
TAPE AND REEL INFORMATION

REEL DIMENSIONS

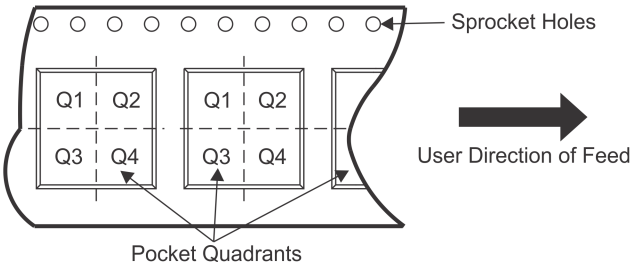


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

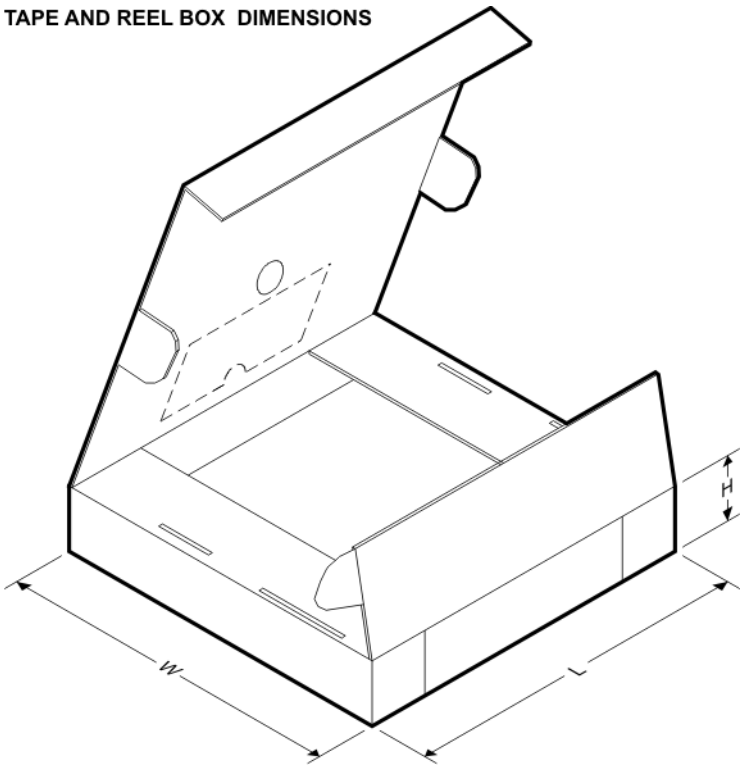
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40190DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS40190DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

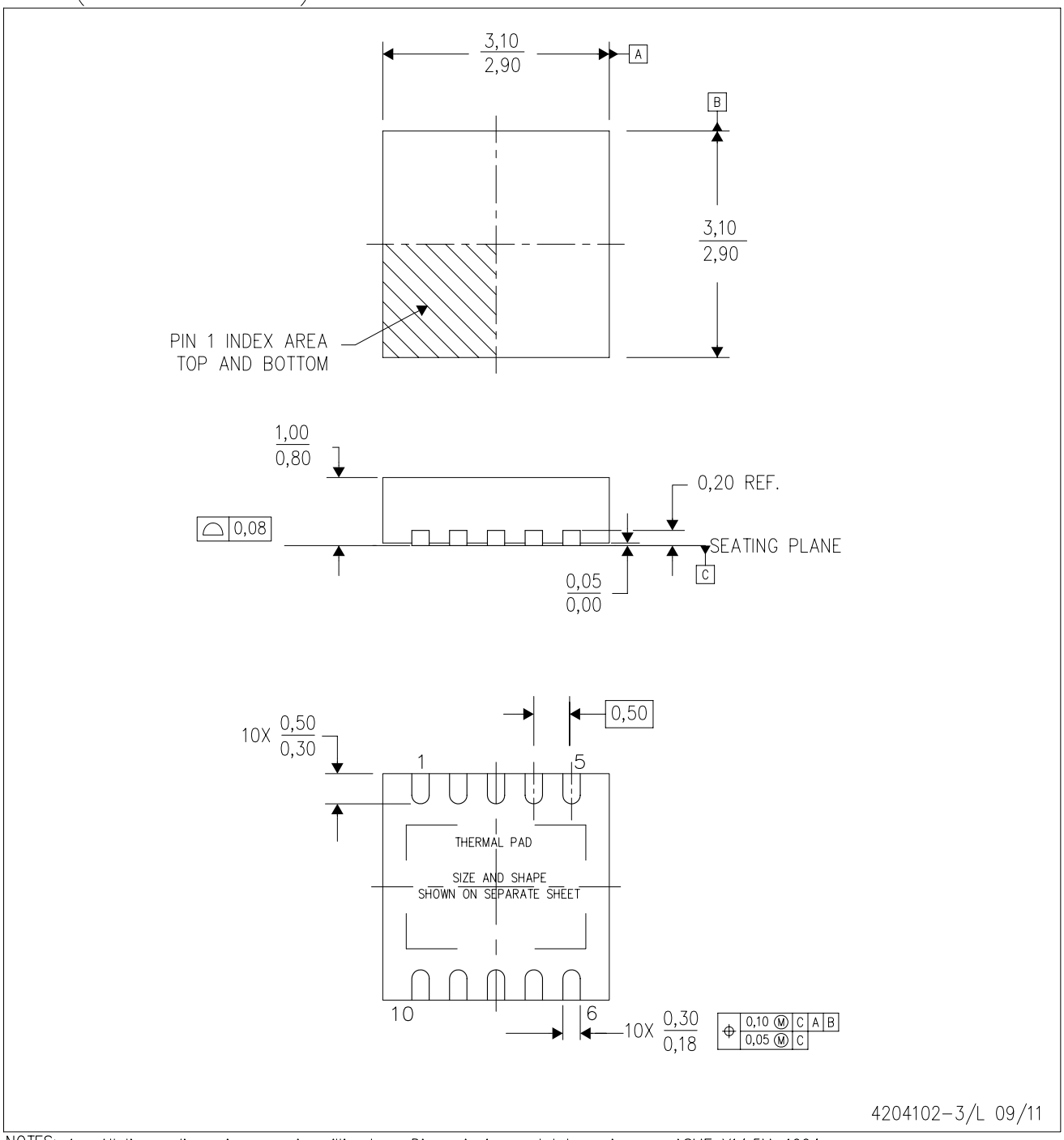
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40190DRCR	VSON	DRC	10	3000	370.0	355.0	55.0
TPS40190DRCT	VSON	DRC	10	250	210.0	185.0	35.0

DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

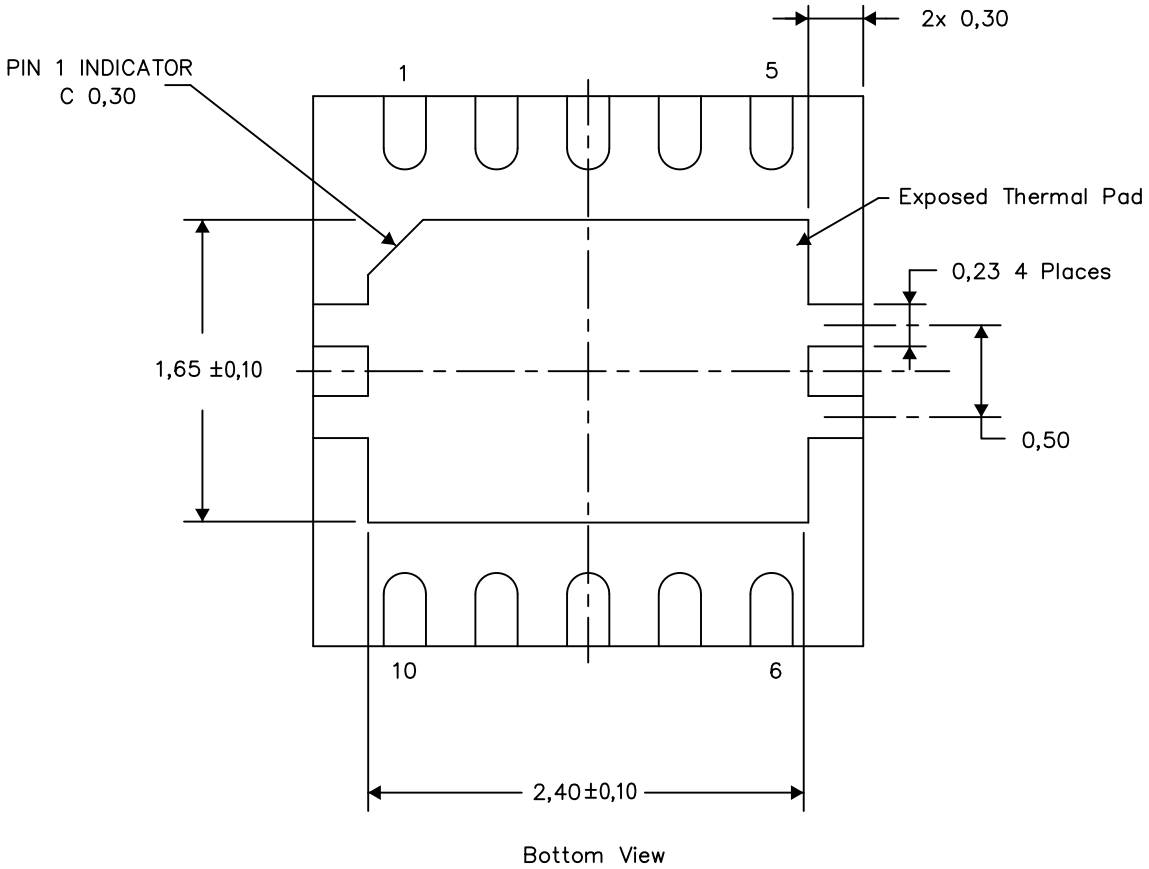
DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

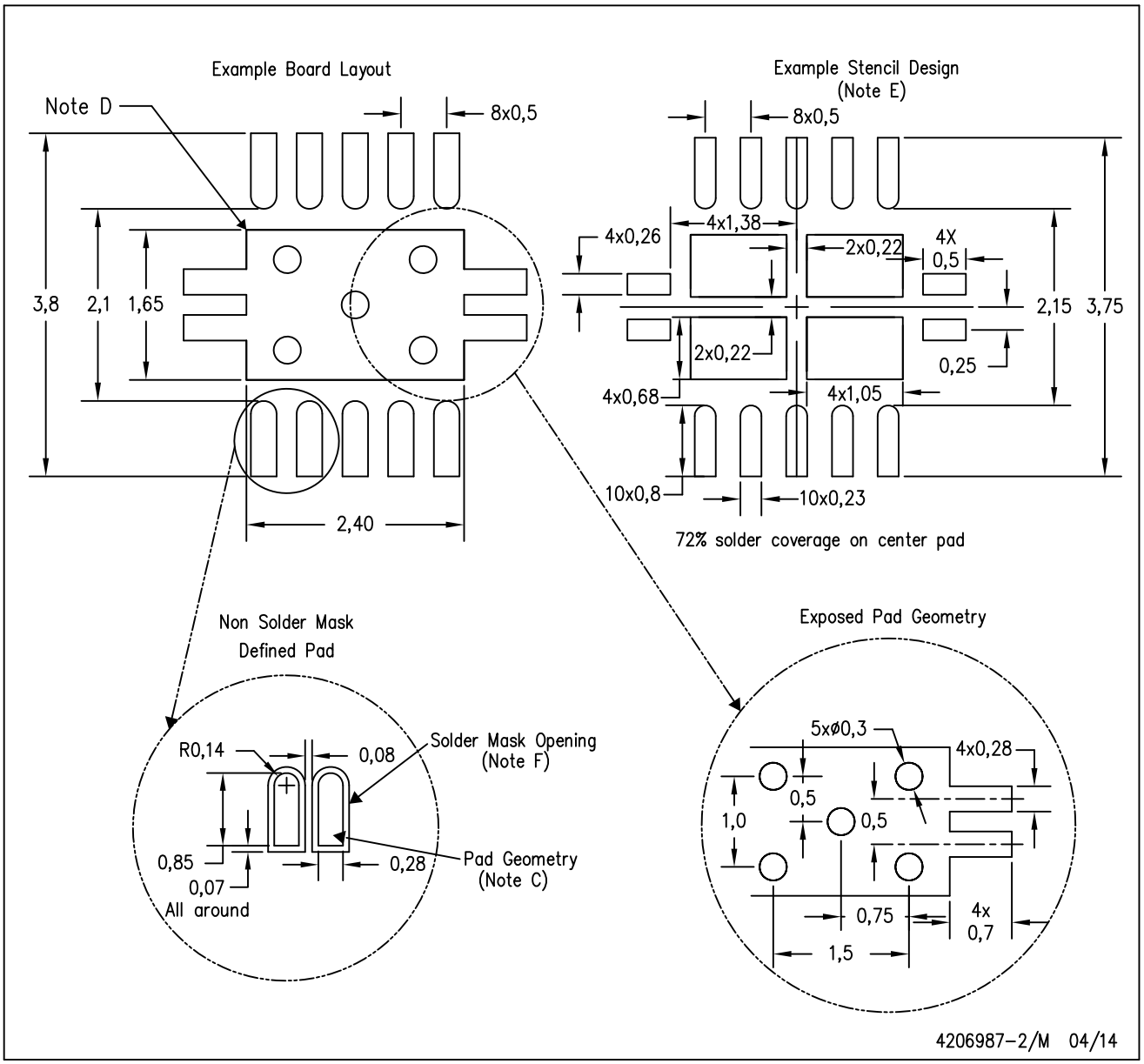


Exposed Thermal Pad Dimensions

4206565-3/U 04/14

NOTE: A. All linear dimensions are in millimeters

DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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