

PBSS4112PANP

120 V, 1 A NPN/PNP low V_{CEsat} (BISS) transistor

29 November 2012

Product data sheet

1. Product profile

1.1 General description

NPN/PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package. NPN/NPN complement: PBSS4112PAN. PNP/PNP complement: PBSS5112PAP.

1.2 Features and benefits

- Very low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain h_{FE} at high I_C
- Reduced Printed-Circuit Board (PCB) requirements
- High efficiency due to less heat generation
- AEC-Q101 qualified

1.3 Applications

- Load switch
- Battery-driven devices
- Power management
- Charging circuits
- Power switches (e.g. motors, fans)

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CEO}	collector-emitter voltage	open base	-	-	120	V
I_C	collector current		-	-	1	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	1.5	A
TR1 (NPN)						
R_{CEsat}	collector-emitter saturation resistance	$I_C = 500$ mA; $I_B = 50$ mA; pulsed; $t_p \leq 300$ μ s; $\delta \leq 0.02$; $T_{amb} = 25$ °C	-	-	240	m Ω



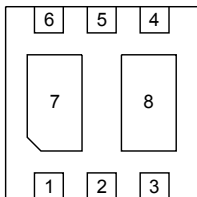
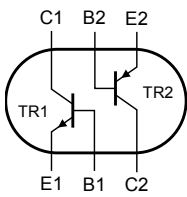
Scan or click this QR code to view the latest information for this product



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR2 (PNP)						
R_{CEsat}	collector-emitter saturation resistance	$I_C = -500\text{ mA}$; $I_B = -50\text{ mA}$; pulsed; $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-	440	m Ω

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 <p>Transparent top view DFN2020-6 (SOT1118)</p>	 <p>sym139</p>
2	B1	base TR1		
3	C2	collector TR2		
4	E2	emitter TR2		
5	B2	base TR2		
6	C1	collector TR1		
7	C1	collector TR1		
8	C2	collector TR2		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4112PANP	DFN2020-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118

4. Marking

Table 4. Marking codes

Type number	Marking code
PBSS4112PANP	2T

5. Limiting values

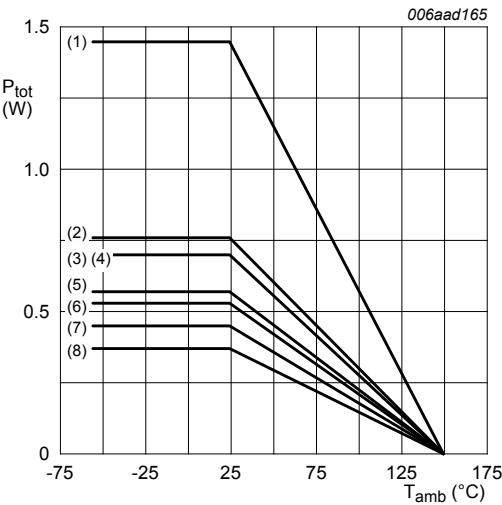
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity					
V_{CBO}	collector-base voltage	open emitter	-	120	V
V_{CEO}	collector-emitter voltage	open base	-	120	V

Symbol	Parameter	Conditions		Min	Max	Unit
V _{EBO}	emitter-base voltage	open collector		-	7	V
I _C	collector current			-	1	A
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms		-	1.5	A
I _B	base current			-	0.3	A
I _{BM}	peak base current	single pulse; t _p ≤ 1 ms		-	1	A
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	370	mW
			[2]	-	570	mW
			[3]	-	530	mW
			[4]	-	700	mW
			[5]	-	450	mW
			[6]	-	760	mW
			[7]	-	700	mW
			[8]	-	1450	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	510	mW
			[2]	-	780	mW
			[3]	-	730	mW
			[4]	-	960	mW
			[5]	-	620	mW
			[6]	-	1040	mW
			[7]	-	960	mW
			[8]	-	2000	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
[3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.
[4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
[5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.
[6] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
[7] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated and standard footprint.
[8] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm².



- (1) 4-layer PCB 70 μm, mounting pad for collector 1 cm²
- (2) FR4 PCB 70 μm, mounting pad for collector 1 cm²
- (3) 4-layer PCB 70 μm, standard footprint
- (4) 4-layer PCB 35 μm, mounting pad for collector 1 cm²
- (5) FR4 PCB 35 μm, mounting pad for collector 1 cm²
- (6) 4-layer PCB 35 μm, standard footprint
- (7) FR4 PCB 70 μm, standard footprint
- (8) FR4 PCB 35 μm, standard footprint

Fig. 1. Per transistor: power derating curves

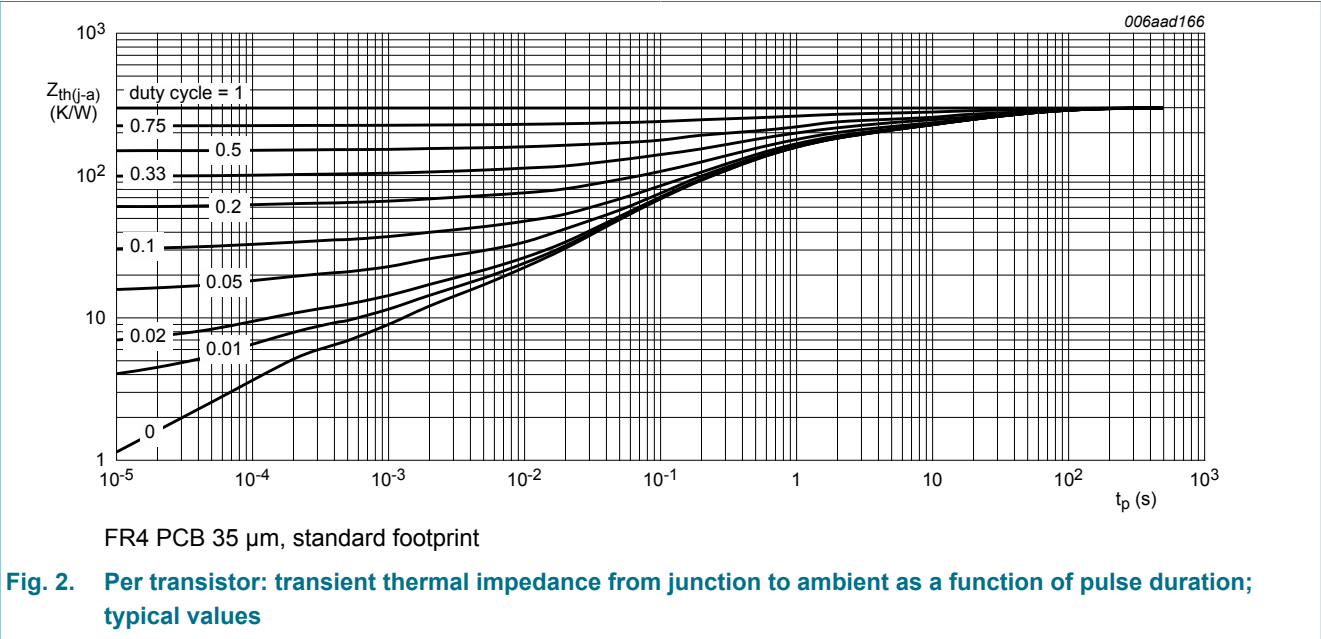
6. Thermal characteristics

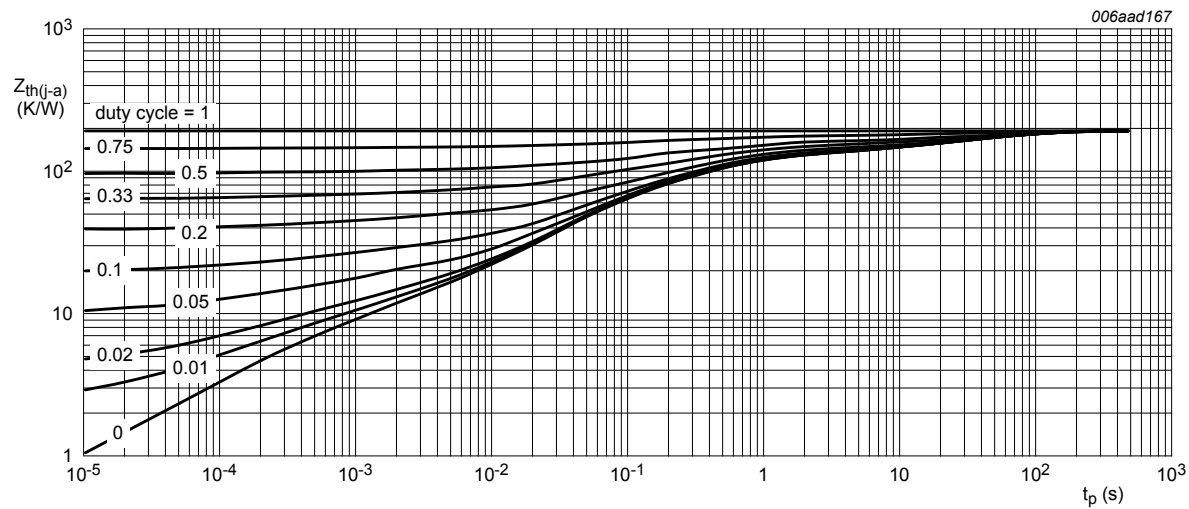
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	338	K/W
			[2]	-	-	219	K/W
			[3]	-	-	236	K/W
			[4]	-	-	179	K/W
			[5]	-	-	278	K/W
			[6]	-	-	164	K/W
			[7]	-	-	179	K/W
			[8]	-	-	86	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	-	30	K/W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per device							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	245	K/W
			[2]	-	-	160	K/W
			[3]	-	-	171	K/W
			[4]	-	-	130	K/W
			[5]	-	-	202	K/W
			[6]	-	-	120	K/W
			[7]	-	-	130	K/W
			[8]	-	-	63	K/W

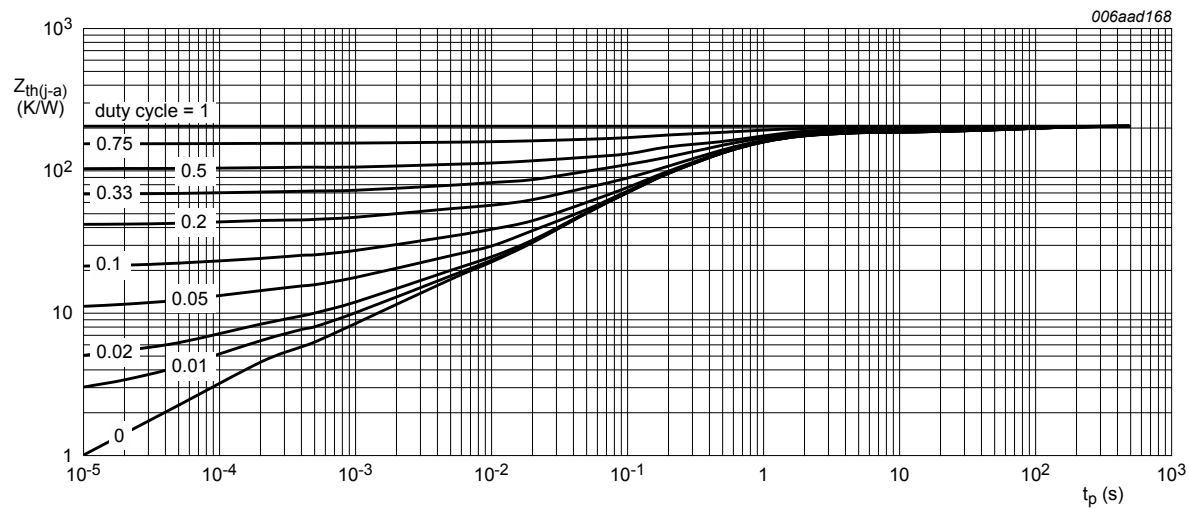
- [1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.
- [4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
- [5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.
- [6] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
- [7] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated and standard footprint.
- [8] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm².





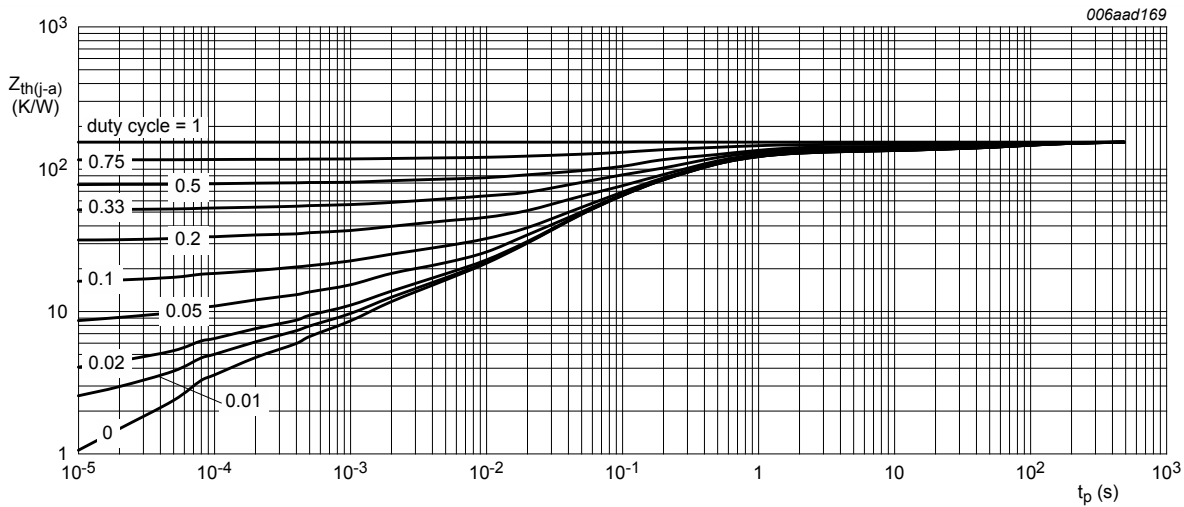
FR4 PCB 35 μ m, mounting pad for collector 1 cm²

Fig. 3. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



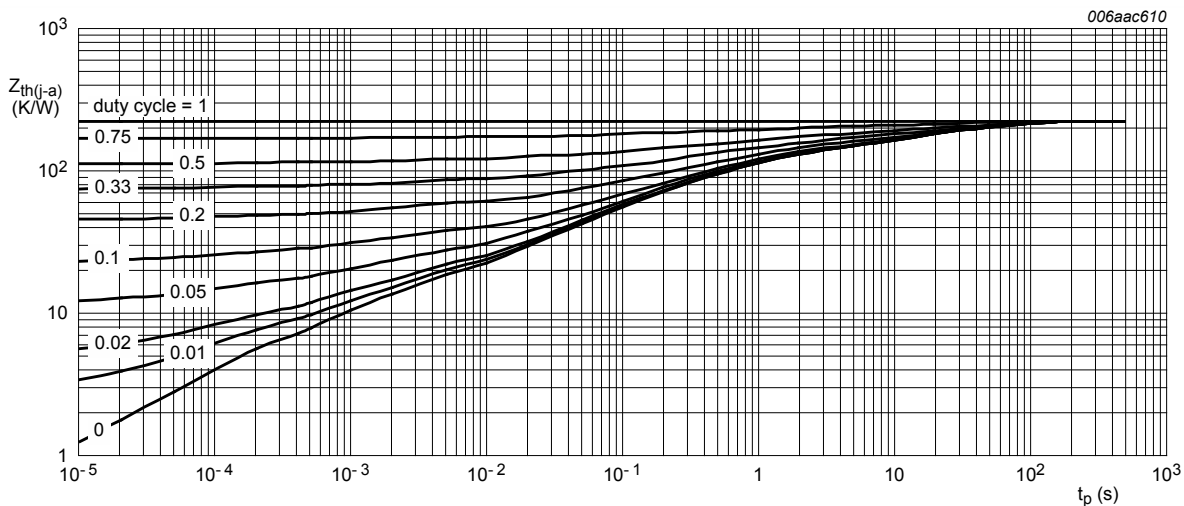
4-layer PCB 35 μ m, standard footprint

Fig. 4. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



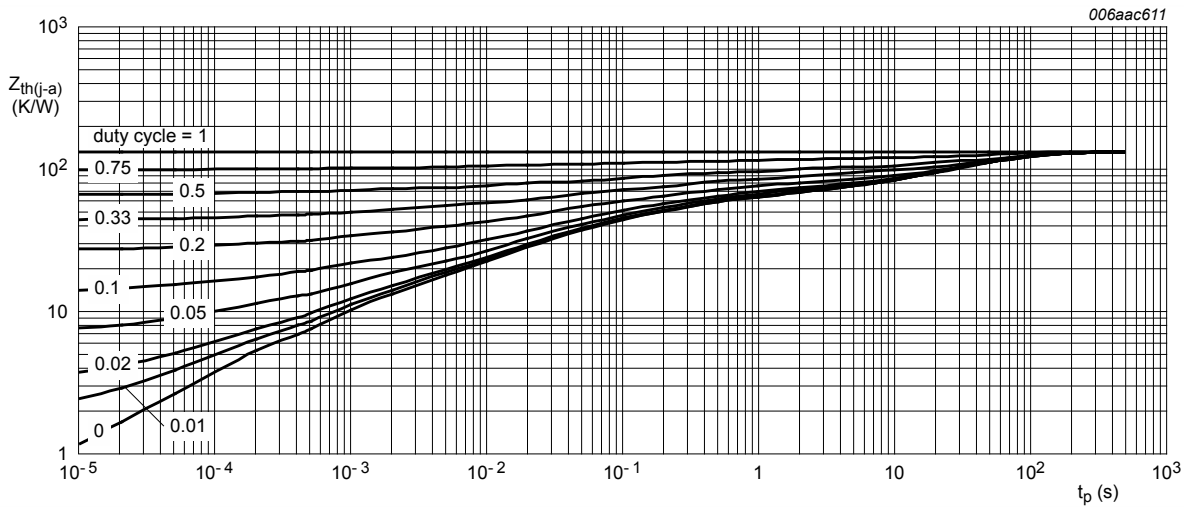
4-layer PCB 35 μm , mounting pad for collector 1 cm^2

Fig. 5. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



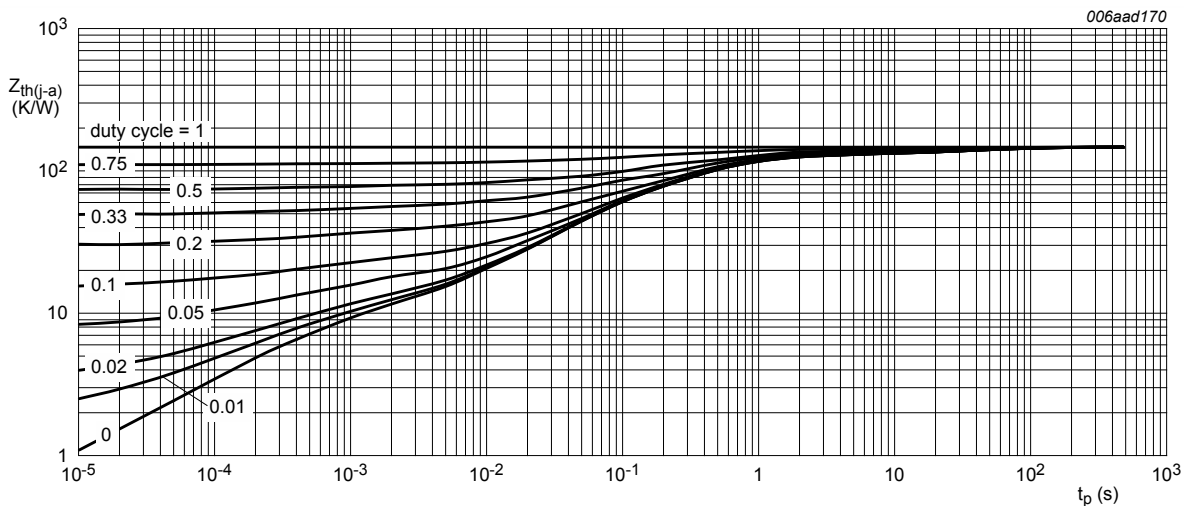
FR4 PCB 70 μm , standard footprint

Fig. 6. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB 70 μ m, mounting pad for collector 1 cm²

Fig. 7. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



4-layer PCB 70 μ m, standard footprint

Fig. 8. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values

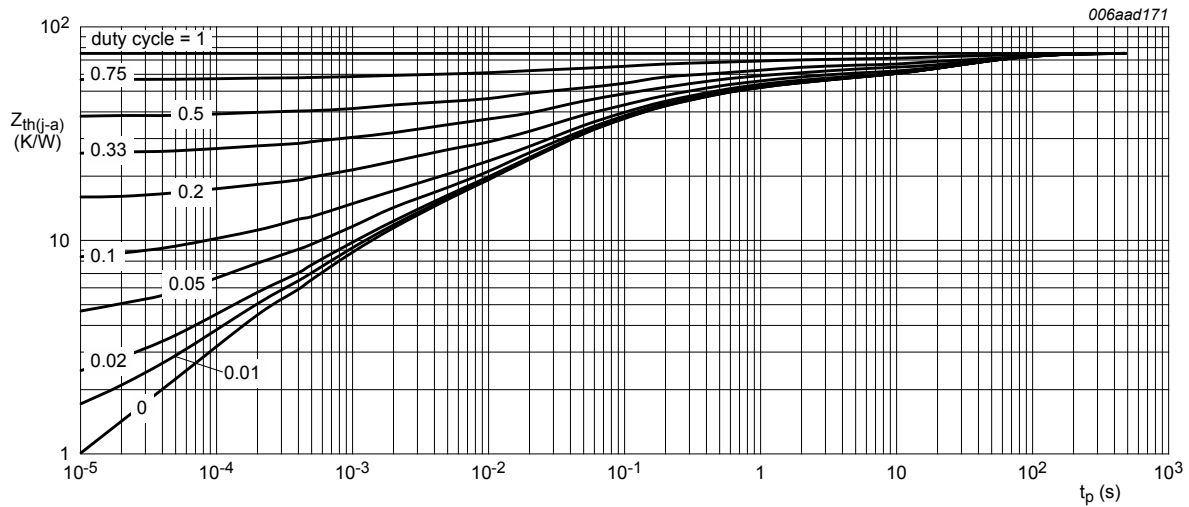


Fig. 9. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values

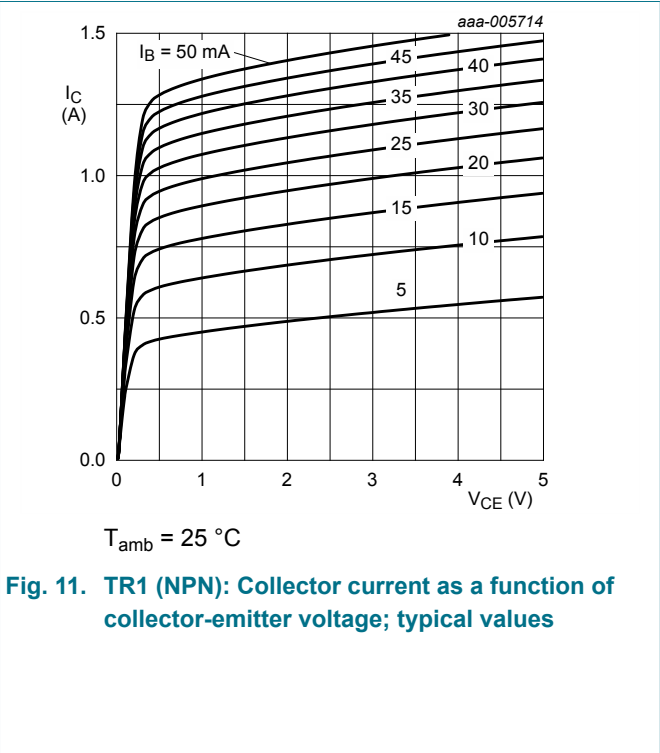
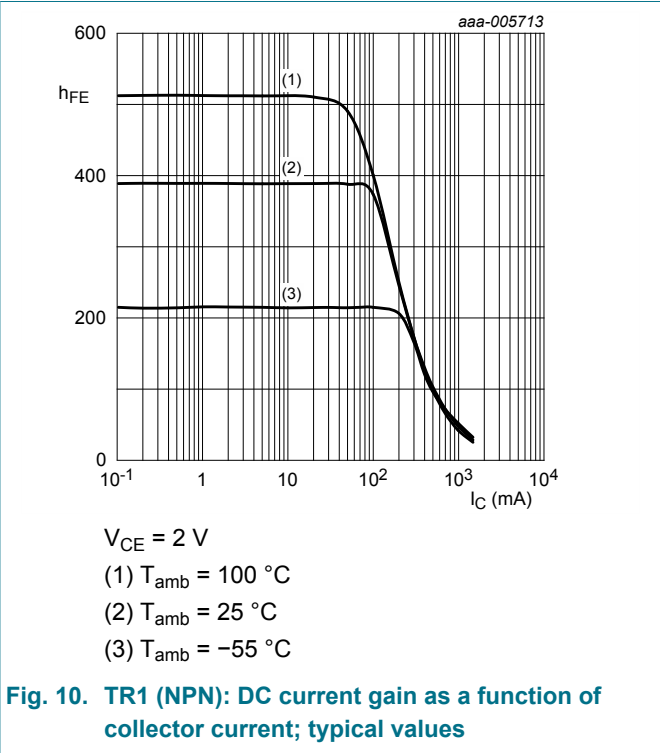
7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1 (NPN)						
I_{CBO}	collector-base cut-off current	$V_{\text{CB}} = 96 \text{ V}; I_{\text{E}} = 0 \text{ A}; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$	-	-	100	nA
		$V_{\text{CB}} = 96 \text{ V}; I_{\text{E}} = 0 \text{ A}; T_{\text{j}} = 150 \text{ }^{\circ}\text{C}$	-	-	50	μA
I_{EBO}	emitter-base cut-off current	$V_{\text{EB}} = 5 \text{ V}; I_{\text{C}} = 0 \text{ A}; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$	-	-	100	nA
h_{FE}	DC current gain	$V_{\text{CE}} = 2 \text{ V}; I_{\text{C}} = 100 \text{ mA}; \text{pulsed}; t_{\text{p}} \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$	240	375	-	
		$V_{\text{CE}} = 2 \text{ V}; I_{\text{C}} = 500 \text{ mA}; \text{pulsed}; t_{\text{p}} \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$	60	100	-	
		$V_{\text{CE}} = 2 \text{ V}; I_{\text{C}} = 1 \text{ A}; \text{pulsed}; t_{\text{p}} \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$	30	45	-	
V_{CEsat}	collector-emitter saturation voltage	$I_{\text{C}} = 500 \text{ mA}; I_{\text{B}} = 50 \text{ mA}; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$	-	90	120	mV
		$I_{\text{C}} = 1 \text{ A}; I_{\text{B}} = 50 \text{ mA}; \text{pulsed}; t_{\text{p}} \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$	-	205	260	mV
		$I_{\text{C}} = 1 \text{ A}; I_{\text{B}} = 100 \text{ mA}; \text{pulsed}; t_{\text{p}} \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$	-	170	220	mV
R_{CEsat}	collector-emitter saturation resistance	$I_{\text{C}} = 500 \text{ mA}; I_{\text{B}} = 50 \text{ mA}; \text{pulsed}; t_{\text{p}} \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$	-	-	240	m Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{BEsat}	base-emitter saturation voltage	I _C = 500 mA; I _B = 50 mA; T _{amb} = 25 °C		-	-	1	V
		I _C = 1 A; I _B = 50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C		-	-	1.1	V
		I _C = 1 A; I _B = 100 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C		-	-	1.1	V
V _{BEon}	base-emitter turn-on voltage	V _{CE} = 2 V; I _C = 0.5 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C		-	-	0.9	V
t _d	delay time	V _{CC} = 10 V; I _C = 500 mA; I _{Bon} = 25 mA; I _{Boff} = -25 mA; T _{amb} = 25 °C		-	20	-	ns
t _r	rise time			-	440	-	ns
t _{on}	turn-on time			-	460	-	ns
t _s	storage time			-	615	-	ns
t _f	fall time			-	390	-	ns
t _{off}	turn-off time			-	1005	-	ns
f _T	transition frequency	V _{CE} = 10 V; I _C = 50 mA; f = 100 MHz; T _{amb} = 25 °C		60	120	-	MHz
C _c	collector capacitance	V _{CB} = 10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C		-	4.5	7	pF
TR2 (PNP)							
I _{CBO}	collector-base cut-off current	V _{CB} = -96 V; I _E = 0 A		-	-	-100	nA
		V _{CB} = -96 V; I _E = 0 A; T _j = 150 °C		-	-	-50	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A		-	-	-100	nA
h _{FE}	DC current gain	V _{CE} = -2 V; I _C = -100 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C		190	305	-	
		V _{CE} = -2 V; I _C = -500 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C		50	85	-	
		V _{CE} = -2 V; I _C = -1 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C		15	25	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = -500 mA; I _B = -50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C		-	-150	-220	mV
		I _C = -1 A; I _B = -100 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C		-	-335	-480	mV
R _{CEsat}	collector-emitter saturation resistance	I _C = -500 mA; I _B = -50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C		-	-	440	mΩ
V _{BEsat}	base-emitter saturation voltage	I _C = -500 mA; I _B = -50 mA; T _{amb} = 25 °C		-	-	-1	V
		I _C = -1 A; I _B = -100 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C		-	-	-1.1	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}$; $I_C = -0.5\text{ A}$; pulsed; $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-	-0.9	V
t_d	delay time	$V_{CC} = -10\text{ V}$; $I_C = -500\text{ mA}$; $I_{Bon} = -25\text{ mA}$; $I_{Boff} = 25\text{ mA}$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	15	-	ns
t_r	rise time		-	245	-	ns
t_{on}	turn-on time		-	260	-	ns
t_s	storage time		-	290	-	ns
t_f	fall time		-	270	-	ns
t_{off}	turn-off time		-	560	-	ns
f_T	transition frequency	$V_{CE} = -10\text{ V}$; $I_C = -50\text{ mA}$; $f = 100\text{ MHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$	50	100	-	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}$; $I_E = 0\text{ A}$; $i_e = 0\text{ A}$; $f = 1\text{ MHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	9.5	13	pF



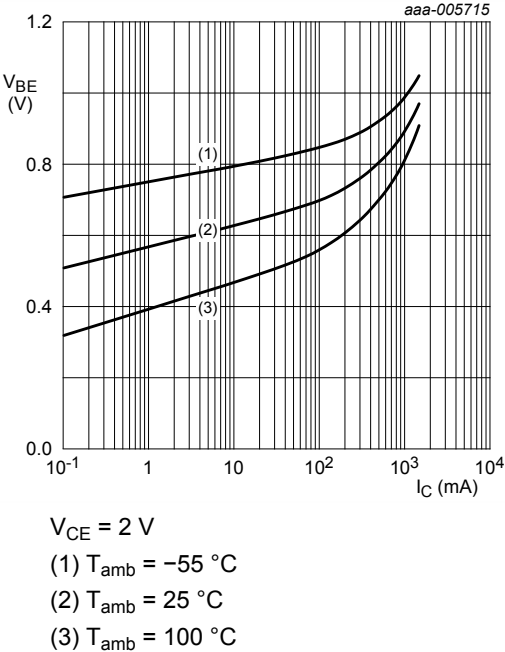


Fig. 12. TR1 (NPN): Base-emitter voltage as a function of collector current; typical values

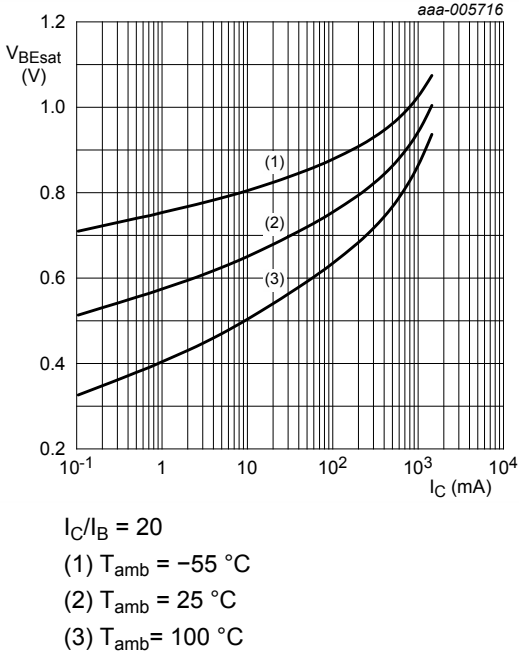


Fig. 13. TR1 (NPN): Base-emitter saturation voltage as a function of collector current; typical values

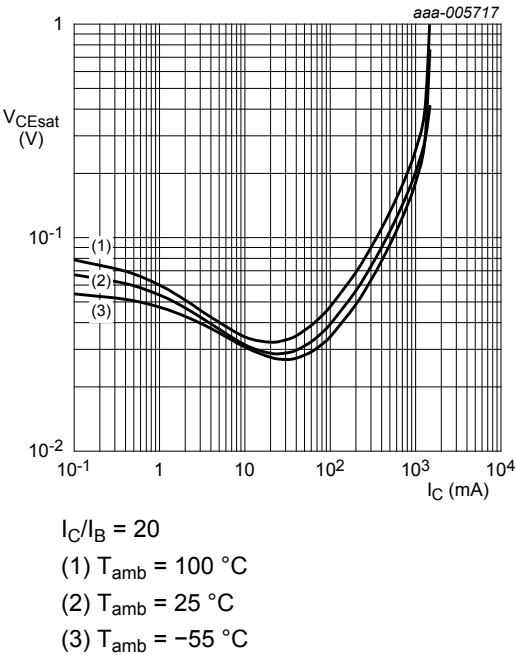


Fig. 14. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

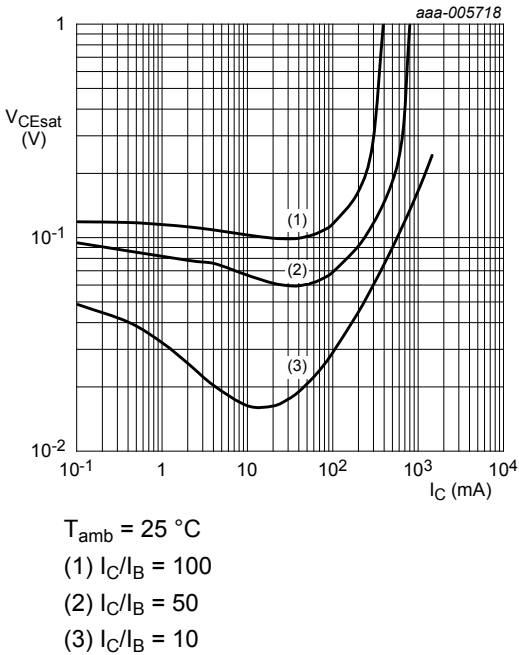


Fig. 15. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

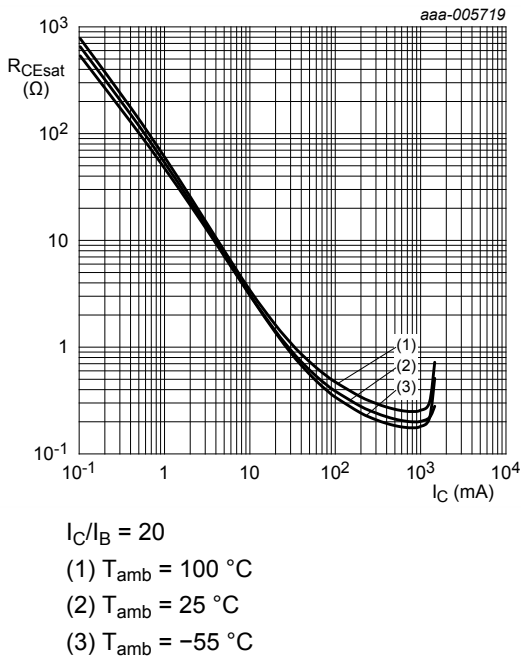


Fig. 16. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values

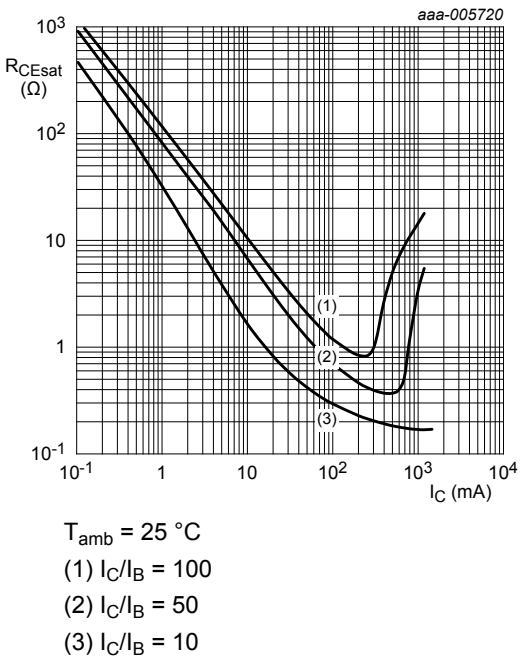


Fig. 17. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values

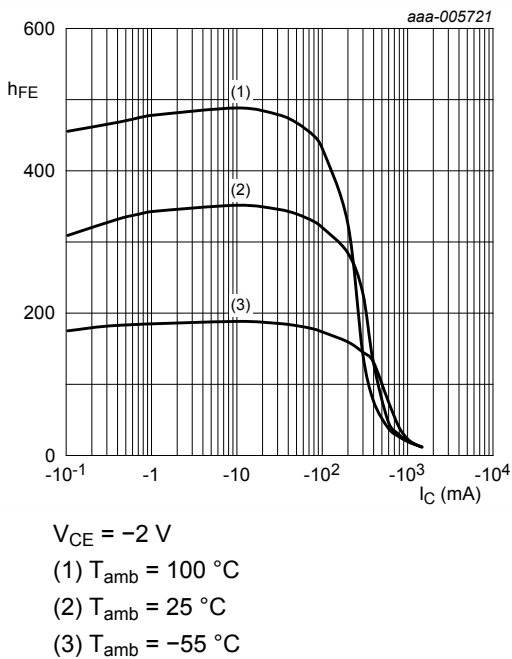


Fig. 18. TR2 (PNP): DC current gain as a function of collector current; typical values

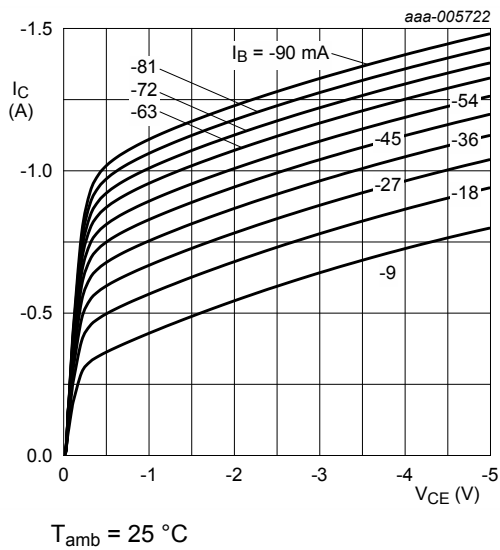


Fig. 19. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values

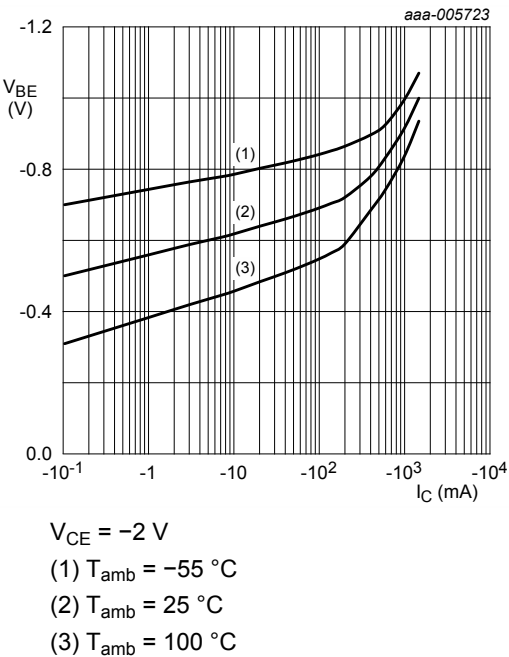


Fig. 20. TR2 (PNP): Base-emitter voltage as a function of collector current; typical values

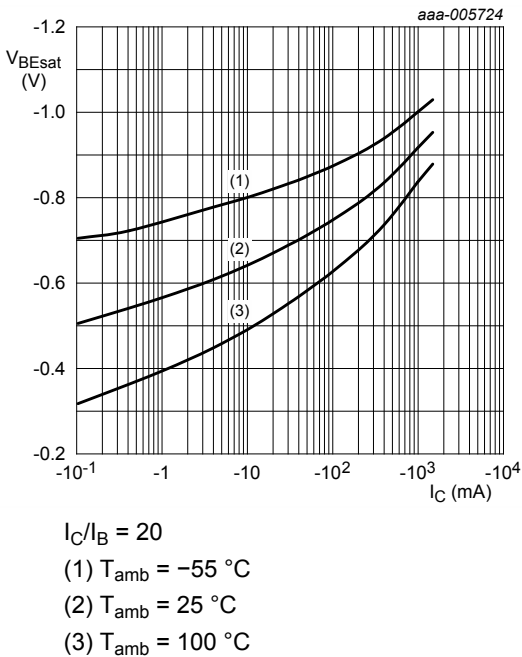


Fig. 21. TR2 (PNP): Base-emitter saturation voltage as a function of collector current; typical values

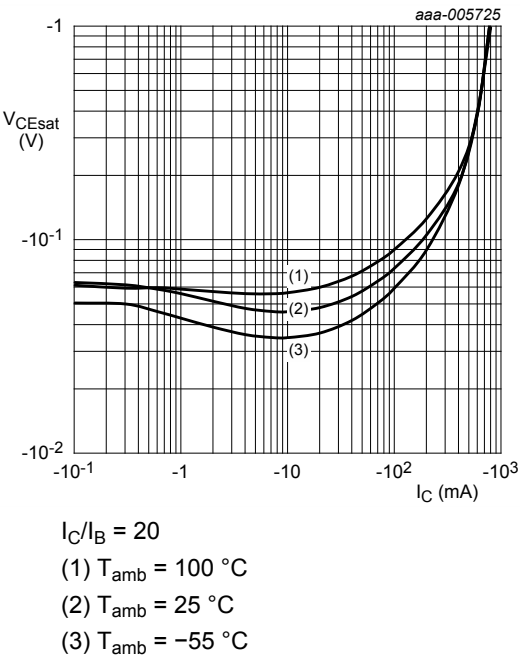


Fig. 22. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

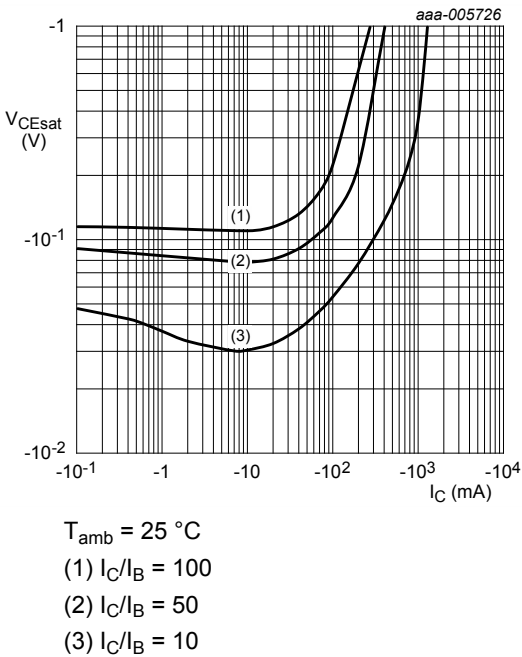
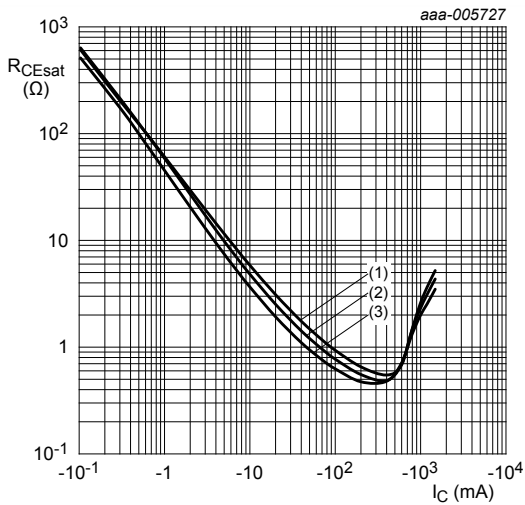
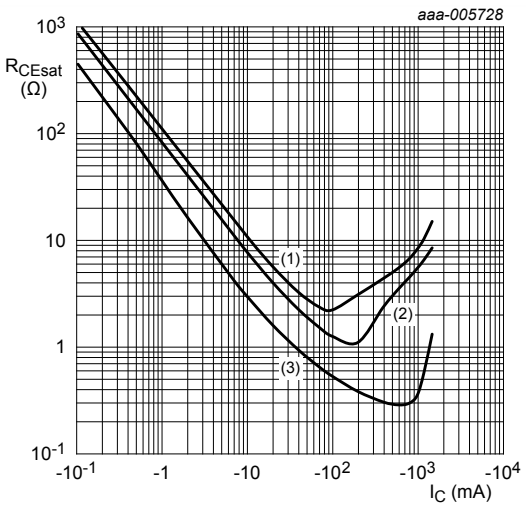


Fig. 23. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



$I_C/I_B = 20$
(1) $T_{amb} = 100^\circ\text{C}$
(2) $T_{amb} = 25^\circ\text{C}$
(3) $T_{amb} = -55^\circ\text{C}$

Fig. 24. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



$T_{amb} = 25^\circ\text{C}$
(1) $I_C/I_B = 100$
(2) $I_C/I_B = 50$
(3) $I_C/I_B = 10$

Fig. 25. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

8. Test information

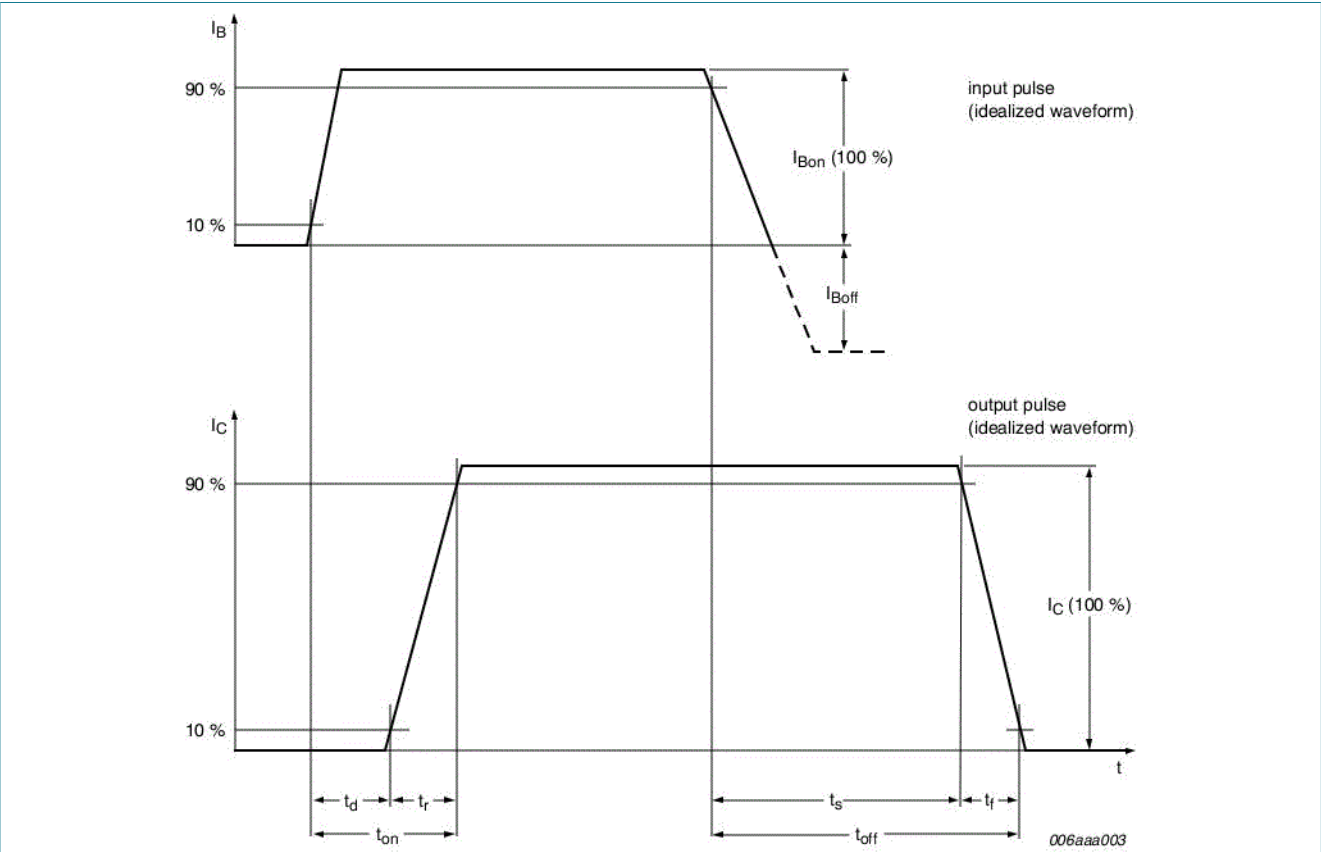


Fig. 26. TR1 (NPN): BISS transistor switching time definition

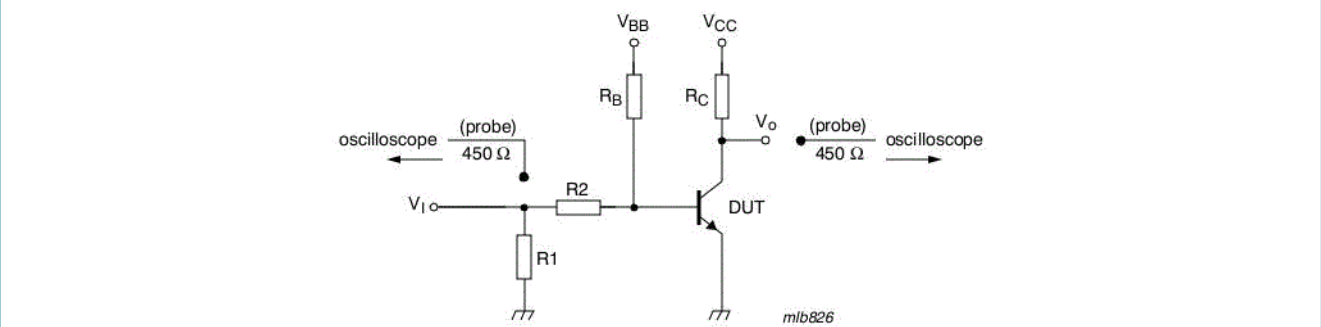


Fig. 27. TR1 (NPN): Test circuit for switching times

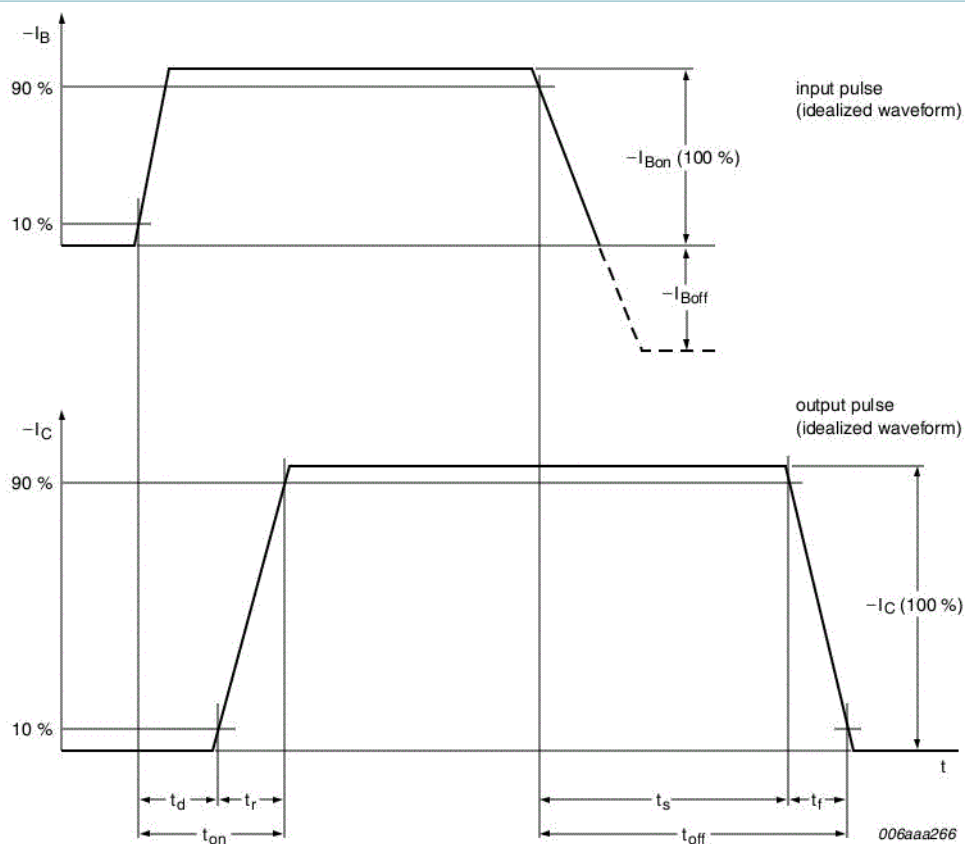


Fig. 28. TR2 (PNP): BISS transistor switching time definition

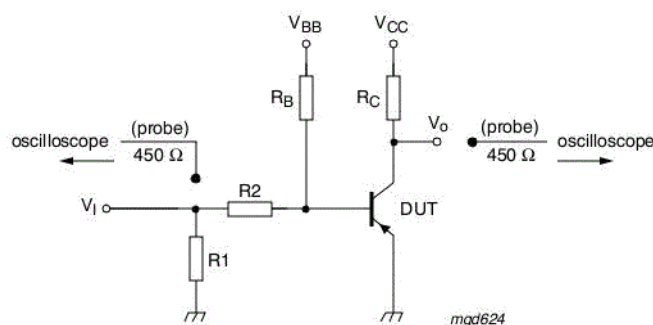
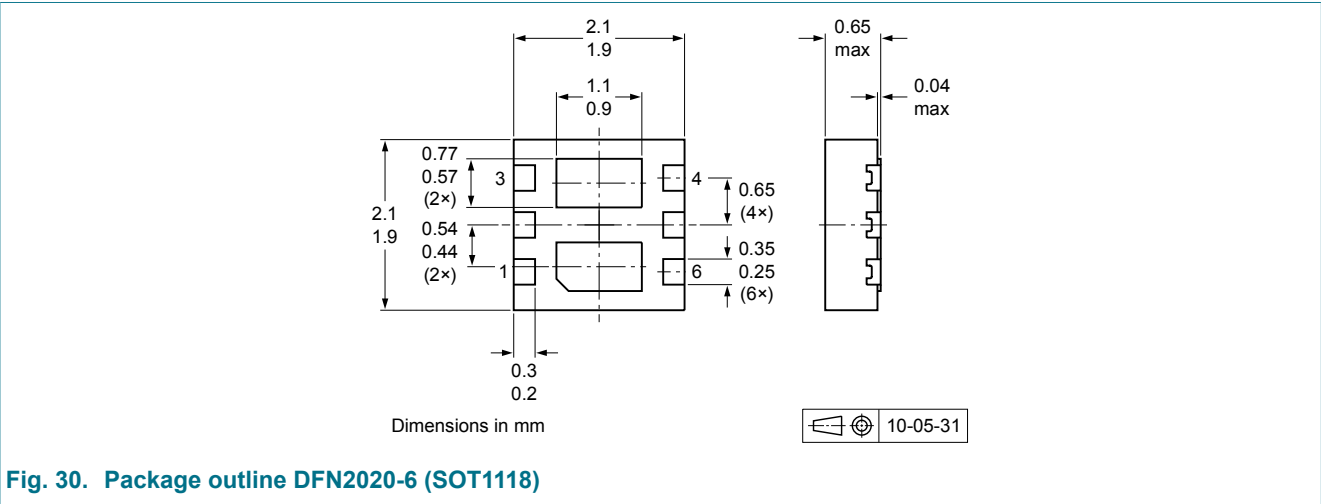


Fig. 29. TR2 (PNP): Test circuit for switching times

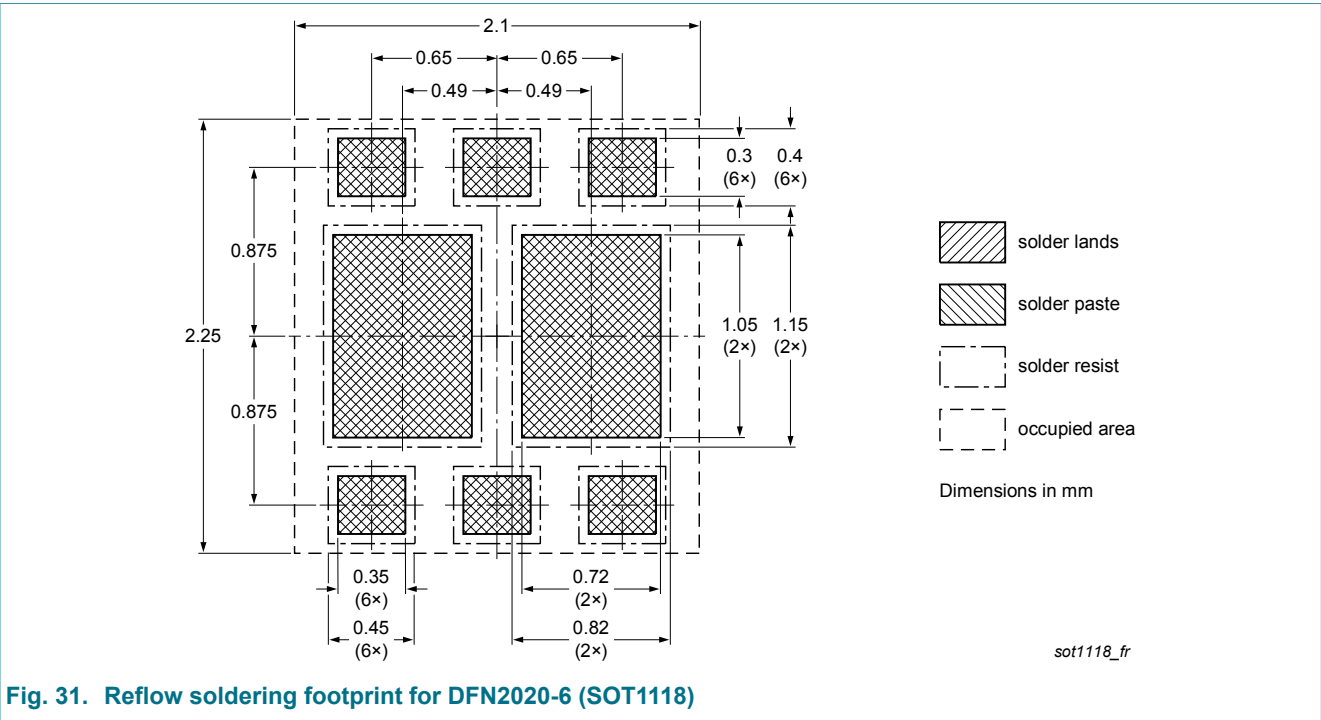
8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline



10. Soldering



11. Revision history

Table 8. Revision history				
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4112PANP v.1	20121129	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

12.2 Definitions

Preview — The document is a preview version only. The document is still subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

12.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Adelante, Bitport, Bitsound, CoolFlux, CoReUse, DESFire, EZ-HV, FabKey, GreenChip, HiPerSmart, HITAG, I²C-bus logo, ICODE, I-CODE, ITEC, Labelution, MIFARE, MIFARE Plus, MIFARE Ultralight, MoReUse, QLPAK, Silicon Tuner, SiliconMAX, SmartXA, STARplug, TOPFET, TOPTriac, TrenchMOS, TriMedia and UCODE — are trademarks of NXP B.V.

HD Radio and **HD Radio** logo — are trademarks of iBiquity Digital Corporation.

13. Contents

1 Product profile 1

1.1 General description 1

1.2 Features and benefits 1

1.3 Applications 1

1.4 Quick reference data 1

2 Pinning information 2

3 Ordering information 2

4 Marking 2

5 Limiting values 2

6 Thermal characteristics 4

7 Characteristics 9

8 Test information 16

8.1 Quality information

9 Package outline 18

10 Soldering 18

11 Revision history 18

12 Legal information 19

12.1 Data sheet status 19

12.2 Definitions 19

12.3 Disclaimers 19

12.4 Trademarks 20

© NXP B.V. 2012. All rights reserved

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 29 November 2012

AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit www.ameya360.com

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692
Email amall@ameya360.com
QQ 800077892
Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333
Email mkt@ameya360.com