EMC-OPTIMIZED HIGH SPEED CAN TRANSCEIVER

Check for Samples: SN65HVDA1050A-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Meets or Exceeds the Requirements of ISO 11898-2**
- **GIFT/ICT Compliant**
- **ESD Protection up to ±12 kV (Human-Body Model) on Bus Pins**
- **High Electromagnetic Compliance (EMC)**
- **SPLIT (V_{REF}) Voltage Source for Common-Mode Stabilization of Bus Via Split Termination**
- **Digital Inputs Compatible With 3.3-V and 5-V Microprocessors**
- **Protection Features**
  - **Bus-Fault Protection of –27 V to 40 V**
  - **TXD Dominant Time-Out**
  - **Thermal Shutdown Protection**
  - **Power-Up/Down Glitch-Free Bus Inputs and Outputs**

APPLICATIONS

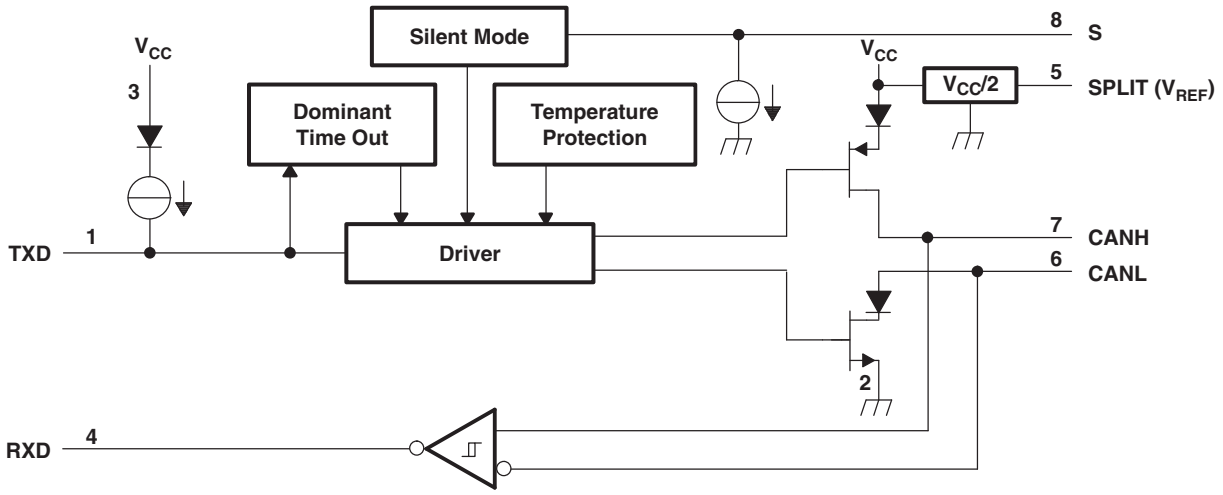
- **GMW3122 Dual-Wire CAN Physical Layer**
- **SAE J2284 High-Speed CAN for Automotive Applications**
- **SAE J1939 Standard Data Bus Interface**
- **ISO 11783 Standard Data Bus Interface**
- **NMEA 2000 Standard Data Bus Interface**

DESCRIPTION

The SN65HVDA1050A meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a Controller Area Network (CAN). The device is qualified for use in automotive applications. As a CAN transceiver, this device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to1 megabit per second (Mbps)(1).

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

FUNCTIONAL BLOCK DIAGRAM



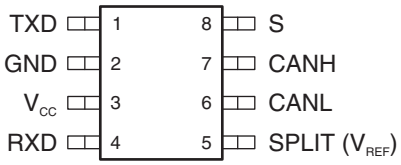
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The device is designed for operation in especially harsh environments and includes many device protection features such as undervoltage lockout, over-temperature thermal shutdown, wide common-mode range, and loss of ground protection. The bus pins are also protected against external cross-wiring, shorts to -27 V to 40 V, and voltage transients according to ISO 7637.

D PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
1	TXD	I	CAN transmit data input (low for dominant bus state, high for recessive bus state)
2	GND	GND	Ground connection
3	VCC	Supply	Transceiver 5V supply voltage input
4	RXD	O	CAN receive data output (low in dominant bus state, high in recessive bus state)
5	SPLIT (V_{REF})	O	Common mode stabilization output for split termination, SPLIT (Vref)
6	CANL	I/O	LOW-level CAN bus line
7	CANH	I/O	HIGH-level CAN bus line
8	S	I	Silent mode select pin (active high)

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	SN65HVDA1050AQDRQ1	A1050A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL DESCRIPTION

Operating Modes

The device has two main operating modes: normal mode and silent mode. Operating mode selection is made via the S input pin.

Table 1. Operating Modes

S PIN	MODE	DRIVER	RECEIVER	RXD PIN
LOW	NORMAL	Enabled (On)	Enabled (On)	Mirrors CAN bus
HIGH	SILENT	Disabled (Off)	Enabled (On)	Mirrors CAN bus

Normal Mode

This is the normal operating mode of the device. It is selected by setting S low. The CAN driver and receiver are fully operational and CAN communication is bidirectional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD. In recessive state the bus pins are biased to 0.5 × V_{CC}. In dominant state the bus pins (CANH and CANL) are driven differentially apart. Logic high is equivalent to recessive on the bus and logic low is equivalent to a dominant (differential) signal on the bus.

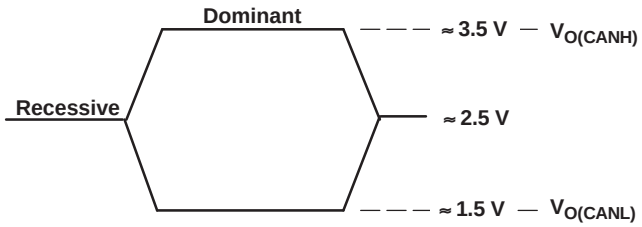


Figure 1. Bus Logic-State Voltage Definitions

The SPLIT (V_{REF}) pin is biased to 0.5 × V_{CC} for bus common mode bus voltage bias stabilization in split termination network applications (see application information).

Silent Mode

This mode disables the driver (transmitter) of the device; however, the receiver still operates and translates the differential signal from CANH and CANL to the digital output on RXD. It is selected by setting S high. The bus pins (CANH and CANL) are biased to 0.5 × V_{CC}. SPLIT (V_{REF}) pin is biased to 0.5 × V_{CC}.

Table 2. Driver Function Table(1)

INPUTS		OUTPUTS		BUS STATE
TXD	S	CANH	CANL	
L	L or Open	H	L	Dominant
H	X	Z	Z	Recessive
Open	X	Z	Z	Recessive
X	H	Z	Z	Recessive

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance

Table 3. Receiver Function Table(1)

DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	OUTPUT RXD	BUS STATE
$V_{ID} \geq 0.9$ V	L	Dominant
0.5 V < V_{ID} < 0.9 V	?	?
$V_{ID} \leq 0.5$ V	H	Recessive
Open	H	Recessive

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance

Protection Features

TXD Dominant State Timeout

During normal mode (only mode where CAN driver is active) the TXD dominant time-out circuit prevents the transceiver from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time out period t_{DST}. The dominant time out circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time-out constant of the circuit expires (t_{DST}) the CAN bus driver is disabled freeing the bus for communication between other network nodes. The CAN driver is re-activated when a recessive signal is seen on TXD pin, thus clearing the dominant state time out. The CAN bus pins will be biased to recessive level during a TXD dominant state time-out and SPLIT (V_{REF}) will remain on.

APPLICATION HINT: The maximum dominant TXD time allowed by the TXD Dominant state time out limits the minimum possible data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t(dom) minimum, limits the minimum bit rate. The minimum bit rate may be calculated by:

Minimum Bit Rate = $11/t_{(dom)}$

Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold the device will turn off the CAN driver circuits. SPLIT (V_{REF}) pin will remain biased. This condition is cleared once the temperature drops below the thermal shut down temperature of the device.

Undervoltage Lockout / Unpowered Device

The device has undervoltage detection and lockout on the V_{CC} supply. If an undervoltage condition is detected on V_{CC}, the device protects the bus.

The TXD pin is pulled up to V_{CC} to force a recessive input level if the pin floats. The S pin is pulled up to GND to force the device in normal mode if the pin floats.

The bus pins (CANH, CANL, and SPLIT (V_{REF})) all have low leakage currents when the device is un-powered.

Application Hints

Using With 3.3-V Microcontrollers

The input level threshold for the digital input pins of this device are 3.3V compatible, however a few application considerations must be taken if using this device with 3.3-V microcontrollers. The TXD input pin has an internal pullup source to V_{CC}. Some microcontroller vendors recommend using an open-drain configuration on their I/O pins in this case even though the pullup limits the current. As such care must be taken at the application level that TXD has sufficient pull up to meet system timing requirements for CAN. The internal pull up on TXD especially may not be sufficient to overcome the parasitic capacitances and allow for adequate CAN timing; thus, an additional external pullup may be required. Care should also be taken with the RXD pin of the microcontroller as this device's RXD output drives the full V_{CC} range (5 V). If the microcontroller RXD input pin is not 5-V tolerant, this must be addressed at the application level. Other options include using a CAN transceiver from Texas Instruments with I/O level adapting or a 3.3-V CAN transceiver.

Using SPLIT (V_{REF}) With Split Termination

The SPLIT (V_{REF}) pin voltage output provides 0.5 × V_{CC} in normal mode. This pin is specified for both the SPLIT sink/source current condition and the V_{REF} sink/source current condition. The circuit may be used by the application to stabilized the common-mode voltage of the bus by connecting it to the center tap of split termination for the CAN network (see Figure 13 and Figure 2). This pin provides a stabilizing recessive voltage drive to offset leakage currents of un-powered transceivers or other bias imbalances that might bring the network common mode voltage away from 0.5 × V_{CC}. Utilizing this feature in a CAN network improves electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltage levels at the start of message transmissions.

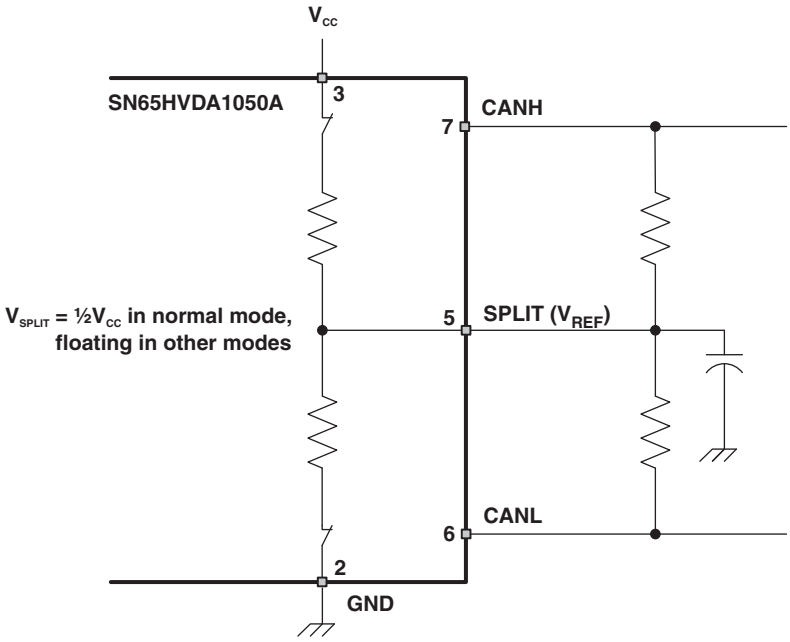


Figure 2. Split Pin Stabilization Circuitry and Application

ABSOLUTE MAXIMUM RATINGS(1)

1.1	V_{CC}	Supply voltage range(2)	–0.3 V to 6 V
1.2		Voltage range at any bus terminal [CANH, CANL, SPLIT (V_{REF})]	–27 V to 40 V
1.3	I_O	Receiver output current	20 mA
1.4	V_I	Voltage input range, ISO 7637 transient pulse(3) (CANH, CANL)	–150 V to 100 V
1.5	V_I	Voltage input range (TXD, S)	–0.3 V to 6 V
1.6	T_J	Junction temperature range	–40°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637 test pulses 1, 2, 3a, 3b per IBEE system level test (Pulse 1 = –100 V, Pulse 2 = 100 V, Pulse 3a = –150 V, Pulse 3b = 100 V). If dc may be coupled with ac transients, externally protect the bus pins within the absolute maximum voltage range at any bus terminal. This device has been tested with dc bus shorts to +40V with leading common-mode chokes. If common-mode chokes are used in the system and the bus lines may be shorted to dc, ensure that the choke type and value in combination with the node termination and shorting voltage either will not create inductive flyback outside of voltage maximum specification or use an external transient-suppression circuit to protect the transceiver from the inductive transients.

ELECTROSTATIC DISCHARGE PROTECTION

	PARAMETER	TEST CONDITIONS		UNIT
2.1	Electrostatic discharge (1)	Human-Body Model(2)	CANH and CANL bus pins(3)	±12 kV
2.2			SPLIT (V_{REF}) pin(4)	±10 kV
2.3			All pins	±4 kV
2.4		Charged-Device Model(5)	All pins	±1.5 kV
2.5		Machine Model(6)		±200 V
2.6		IEC 61400-4-2 according to IBEE CAN EMC test specification	CANH and CANL bus pins to GND	±7 kV

(1) All typical values at 25°C.
(2) Tested in accordance JEDEC Standard 22 Test Method A114F and AEC-Q100-002.
(3) Test method based upon JEDEC Standard 22 Test Method A114F and AEC-Q100-002, CANH and CANL bus pins stressed with respect to each other and GND.
(4) Test method based upon JEDEC Standard 22 Test Method A114F and AEC-Q100-002, SPLIT pin stressed with respect to GND.
(5) Tested in accordance JEDEC Standard 22 Test Method C101D and AEC-Q100-011.
(6) Tested in accordance JEDEC Standard 22, Test Method A115A.

RECOMMENDED OPERATING CONDITIONS

				MIN	MAX	UNIT
3.1	V_{CC}	Supply voltage		4.75	5.25	V
3.2	V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12	12	V
3.3	V_{IH}	High-level input voltage	TXD, S	2	5.25	V
3.4	V_{IL}	Low-level input voltage	TXD, S	0	0.8	V
3.5	V_{ID}	Differential input voltage		–6	6	V
3.6	I_{OH}	High-level output current	Driver	–70		mA
3.7			Receiver (RXD)	–2		
3.8	I_{OL}	Low-level output current	Driver		70	mA
3.9			Receiver (RXD)		2	
3.10	T_A	Operating free-air temperature range	See Thermal Characteristics table	–40	125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions, T_A = –40 to 125°C (unless otherwise noted)

NO.	PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Supply								
4.1	I_{CC}	5-V supply current	Silent mode	S at V_{CC}, V_I = V_{CC}		6	10	mA
4.2			Dominant	V_I = 0 V, 60-Ω load, S = 0 V		50	70	
4.3			Recessive	V_I = V_{CC}, No load, S = 0 V		6	10	
4.4	UV_{CC}	Undervoltage reset threshold			2.8		4	V
Device Switching Characteristics								
5.1	$t_{d(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant		S = 0 V, See Figure 10	90		230	ns
5.2	$t_{d(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive		S = 0 V, See Figure 10	90		230	ns
Driver								
6.1	$V_{O(D)}$	Bus output voltage (dominant)	CANH	V_I = 0 V, S = 0 V, R_L = 60 Ω, See Figure 3 and Figure 1	2.9	3.4	4.5	V
6.2			CANL	0.8		1.5		
6.3	$V_{O(R)}$	Bus output voltage (recessive)		V_I = 3 V, S = 0 V, R_L = 60 Ω, See Figure 3 and Figure 1	2	2.3	3	V
6.4	$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 60 Ω, S = 0 V, See Figure 3, Figure 1, and Figure 4	1.5		3	V
6.5				V_I = 0 V, R_L = 45 Ω, S = 0 V, See Figure 3, Figure 1, and Figure 4	1.4		3	V
6.6	$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, S = 0 V, See Figure 3 and Figure 1	–0.012		0.012	V
6.7				V_I = 3 V, S = 0 V, No Load	–0.5		0.05	
6.8	$V_{OC(ss)}$	Steady state common-mode output voltage		S = 0 V, Figure 9	2	2.3	3	V
6.9	$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage		S = 0 V, Figure 9		30		mV
6.10	V_{IH}	High-level input voltage, TXD input			2			V
6.11	V_{IL}	Low-level input voltage, TXD input					0.8	V
6.12	I_{IH}	High-level input current, TXD input		V_I at V_{CC}	–2		2	µA
6.13	I_{IL}	Low-level input current, TXD input		V_I at 0 V	–50		–10	µA
6.14	$I_{O(off)}$	Power-off TXD output current		V_{CC} at 0 V, TXD at 5 V			1	µA
6.15	$I_{OS(ss)}$	Short-circuit steady-state output current, Dominant		V_{CANH} = –12 V, CANL open, See Figure 12	–105	–72		mA
6.16				V_{CANH} = 12 V, CANL open, See Figure 12		0.36	1	
6.17				V_{CANL} = –12 V, CANH open, See Figure 12	–1	–0.5		
6.18				V_{CANL} = 12 V, CANH open, See Figure 12		71	105	
6.19				V_{CANH} = 0 V, CANL open, TXD = low, See Figure 12	–100	–70		
6.20				V_{CANL} = 32 V, CANH open, TXD = low, See Figure 12		75	140	

(1) All typical values are at 25°C with a 5-V supply.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions, T_A = –40 to 125°C (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
6.21	$I_{OS(ss)}$	Short-circuit steady-state output current, Recessive	-20 V ≤ V_{CANH} ≤ 32 V, CANL open, TXD = high, See Figure 12	–15		15	mA
6.22			-20 V ≤ V_{CANL} ≤ 32 V, CANH open, TXD = high, See Figure 12	–15		15	
6.23	C_O	Output capacitance	See receiver input capacitance				
Driver Switching Characteristics							
7.1	t_{PLH}	Propagation delay time, low-to-high level output	S = 0 V, See Figure 5	25	65	120	ns
7.2	t_{PHL}	Propagation delay time, high-to-low level output	S = 0 V, See Figure 5	25	45	120	ns
7.3	t_r	Differential output signal rise time	S = 0 V, See Figure 5		25		ns
7.4	t_f	Differential output signal fall time	S = 0 V, See Figure 5		50		ns
7.5	t_{en}	Enable time from silent mode to normal mode and transmission of dominant	See Figure 8			1	µs
7.6	$t_{(dom)}$	Dominant time out(2)	↓V_I, See Figure 11	300	450	700	µs
Receiver							
8.1	V_{IT+}	Positive-going input threshold voltage	S = 0 V, See Table 4		800	900	mV
8.2	$V_{IT–}$	Negative-going input threshold voltage	S = 0 V, See Table 4	500	650		mV
8.3	V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)		100	125		mV
8.4	V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 7	4	4.6		V
8.5	V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 7		0.2	0.4	V
8.6	$I_{I(off)}$	Power-off bus input current (unpowered bus leakage current)	CANH or CANL = 5 V, Other pin at 0 V, V_{CC} at 0 V, TXD at 0 V		165	250	µA
8.7	$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0 V, RXD at 5 V			20	µA
8.8	C_I	Input capacitance to ground (CANH or CANL)	TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V		13		pF
8.9	C_{ID}	Differential input capacitance	TXD at 3 V, V_I = 0.4 sin (4E6πt)		6		pF
8.10	R_{ID}	Differential input resistance	TXD at 3 V, S = 0 V	30		80	kΩ
8.11	R_{IN}	Input resistance (CANH or CANL)	TXD at 3 V, S = 0 V	15	30	40	kΩ
8.12	$R_{I(m)}$	Input resistance matching [1 – ($R_{IN\ (CANH)}$ / $R_{IN\ (CANL)}$)] × 100%	$V_{(CANH)}$ = $V_{(CANL)}$	–3	0	3	%
Receiver Switching Characteristics							
9.1	t_{PLH}	Propagation delay time, low-to-high-level output	S = 0 V or V_{CC}, See Figure 7	60	100	130	ns
9.2	t_{PHL}	Propagation delay time, high-to-low-level output	S = 0 V or V_{CC}, See Figure 7	45	70	130	ns
9.3	t_r	Output signal rise time	S = 0 V or V_{CC}, See Figure 7		8		ns
9.4	t_f	Output signal fall time	S = 0 V or V_{CC}, See Figure 7		8		ns

(2) The TXD dominant time out (t(dom)) will disable the driver of the transceiver once the TXD has been dominant longer than $t_{(dom)}$ which will release the bus lines to recessive preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults locking the bus dominant it will limit the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case where five successive dominant bits are followed immediately by an error frame. This along with the $t_{(dom)}$ minimum will limit the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11/ $t_{(dom)}$ = 11 bits / 300µs = 37 kbps.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions, T_A = –40 to 125°C (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
S Pin							
10.1	V_{IH}	High-level input voltage, S input		2			V
10.2	V_{IL}	Low-level input voltage, S input				0.8	V
10.3	I_{IH}	High level input current	S at 2 V	20	40	70	µA
10.4	I_{IL}	Low level input current	S at 0.8 V	5	20	30	µA
SPLIT (V_{REF}) Pin							
11.1	V_O	Output voltage	–50 µA < I_O < 50 µA (V_{REF})	0.4 V_{CC}	0.5 V_{CC}	0.6 V_{CC}	V
11.2			–500 µA < I_O < 500 µA (SPLIT)	0.3 V_{CC}	0.5 V_{CC}	0.7 V_{CC}	
11.3	I_{LKG}	Leakage current, unpowered	V_{CC} = 0 V, –12 V ≤ V_{SPLIT} ≤ 12 V	–5		5	µA

THERMAL CHARACTERISTICS

over recommended operating conditions, T_A = –40 to 125°C (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
12.1	θ_{JA}	Junction-to-air thermal resistance(1)	Low-K thermal resistance(2)		211		°C/W
12.2			High-K thermal resistance(2)		131		
12.3	θ_{JB}	Junction-to-board thermal resistance			53		°C/W
12.4	θ_{JC}	Junction-to-case thermal resistance			79		°C/W
12.5	P_D	Average power dissipation	V_{CC} = 5 V, T_J = 27°C, R_L = 60 Ω, S = 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, CL at RXD = 15 pF		112		mW
12.6			V_{CC} = 5.5 V, T_J = 130°C, R_L = 45 Ω, S = 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, CL at RXD = 15 pF			170	
12.7		Thermal shutdown temperature			190		°C

(1) The junction temperature (T_J) is calculated using the following $T_J = T_A + (P_D \times \theta_{JA})$.
(2) Tested in accordance with the Low-K (EIA/JESD51-3) or High-K (EIA/JESD51-7) thermal metric definitions for leaded surface-mount packages.

PARAMETER MEASUREMENT INFORMATION

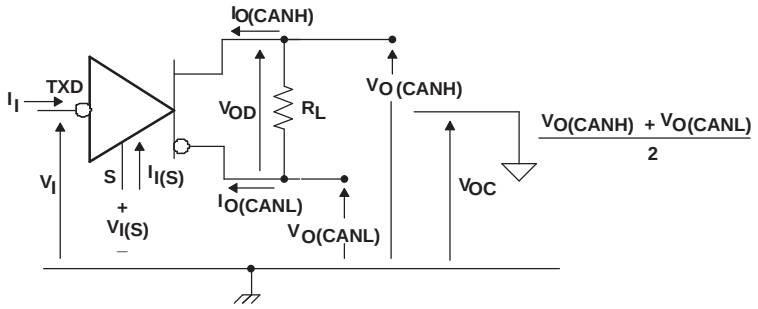


Figure 3. Driver Voltage, Current, and Test Definition

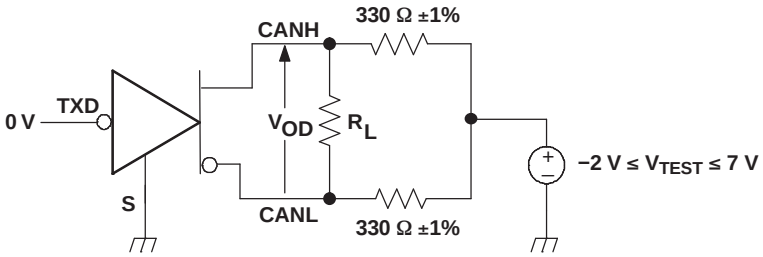


Figure 4. Driver V_{OD} Test Circuit

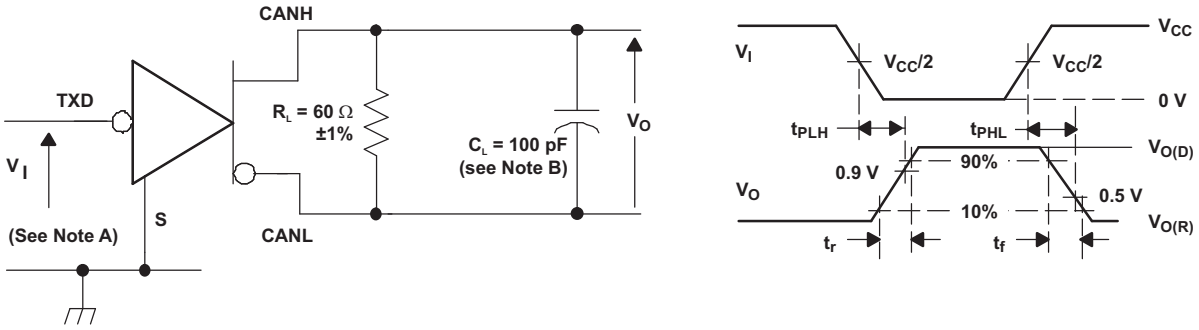


Figure 5. Driver Test Circuit and Voltage Waveforms

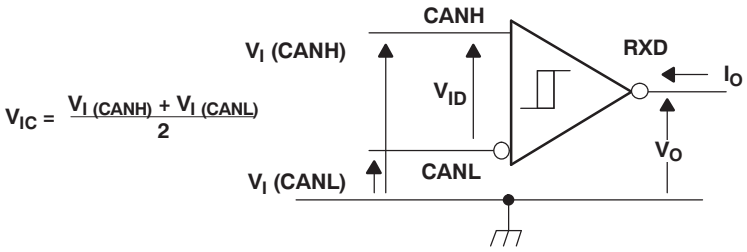
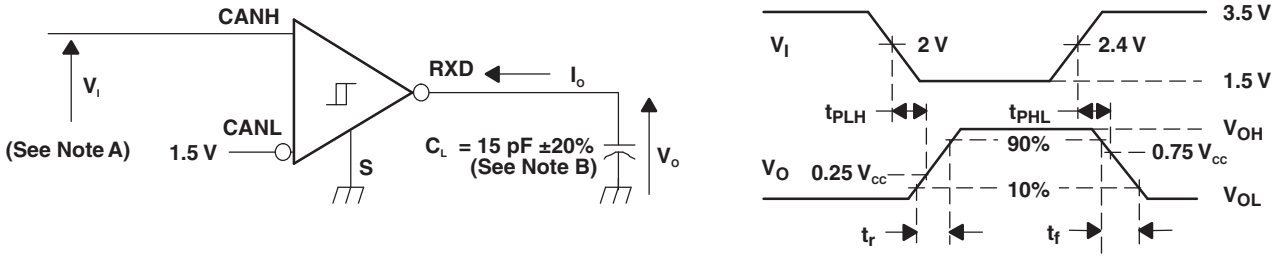


Figure 6. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



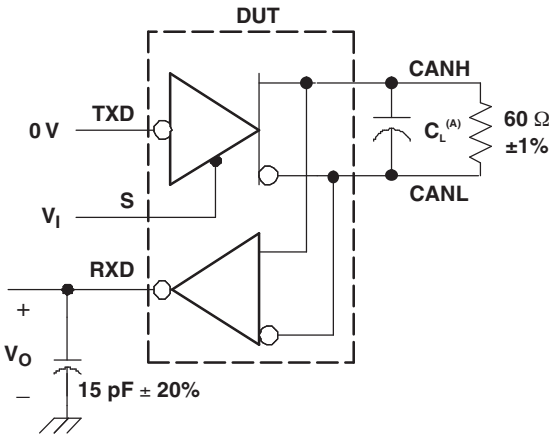
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

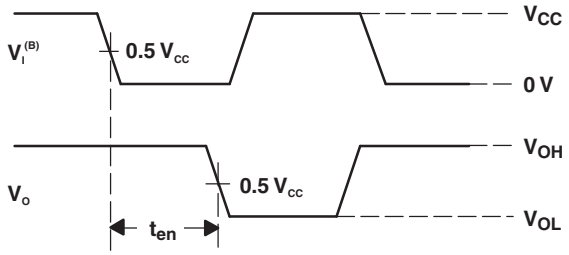
B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 7. Receiver Test Circuit and Voltage Waveforms

Table 4. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	

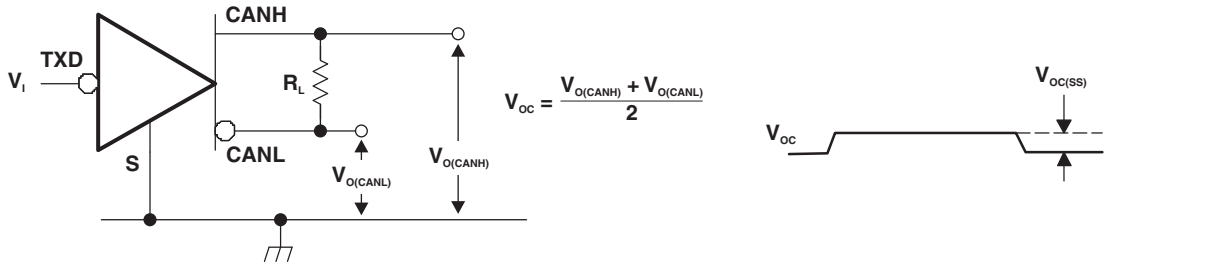




A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.

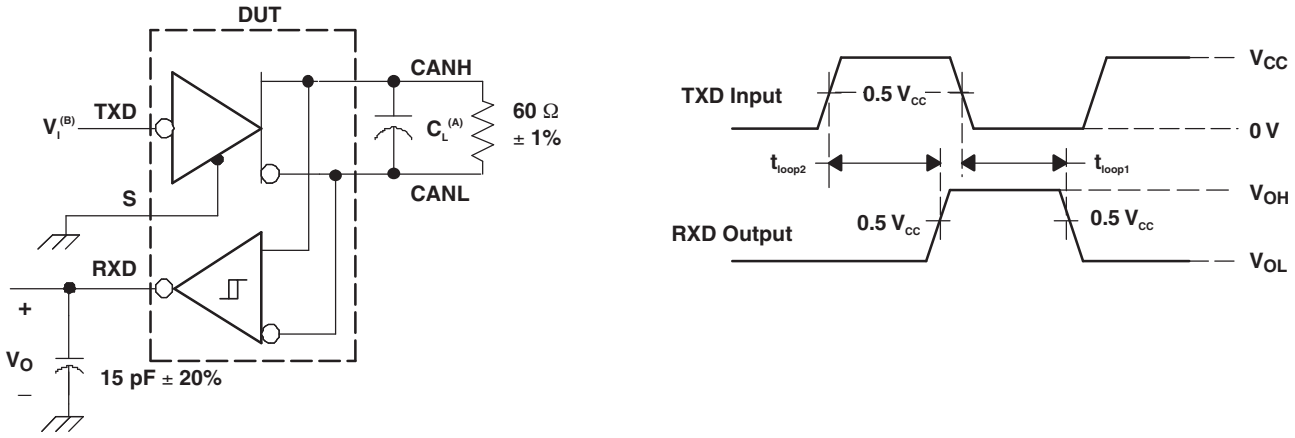
B. All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. t_{en} Test Circuit and Waveforms



NOTE: All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

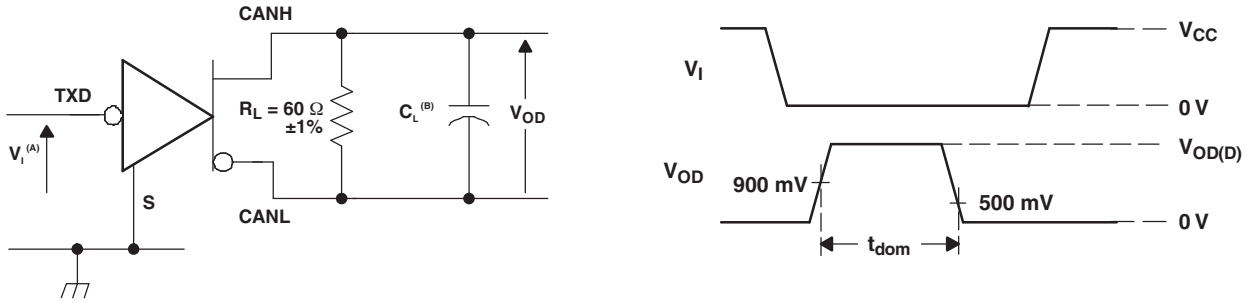
Figure 9. Common-Mode Output Voltage Test and Waveforms



A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 10. $t_{(LOOP)}$ Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 11. Dominant Time-Out Test Circuit and Waveforms

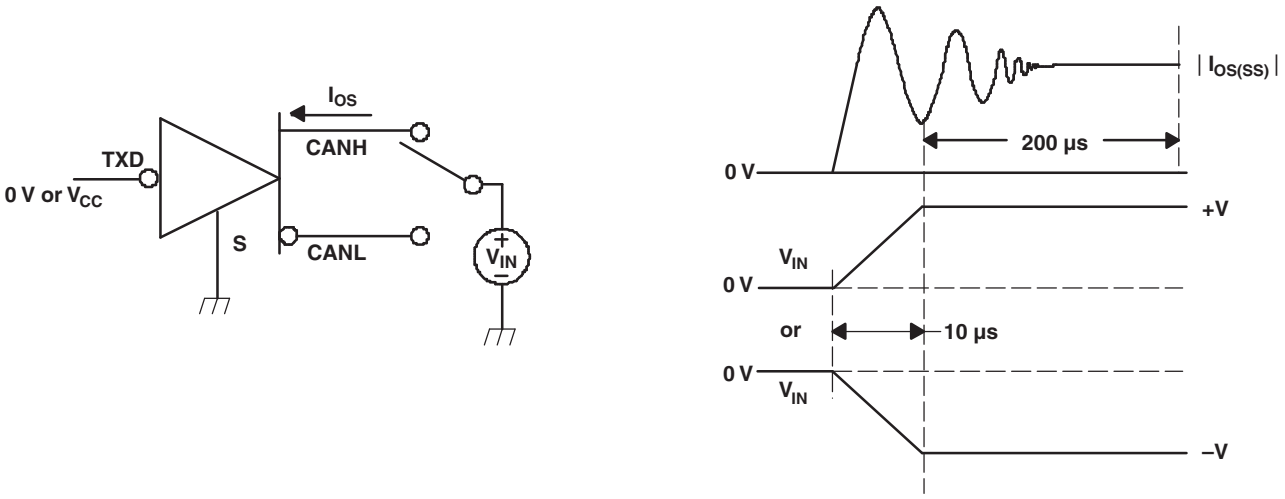


Figure 12. Driver Short-Circuit Current Test and Waveforms

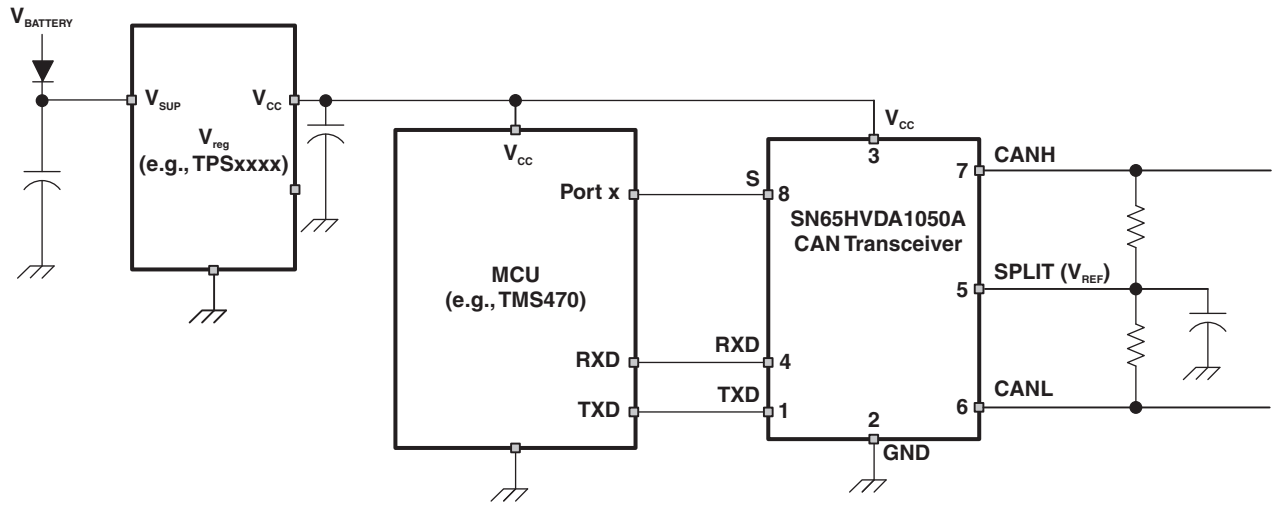
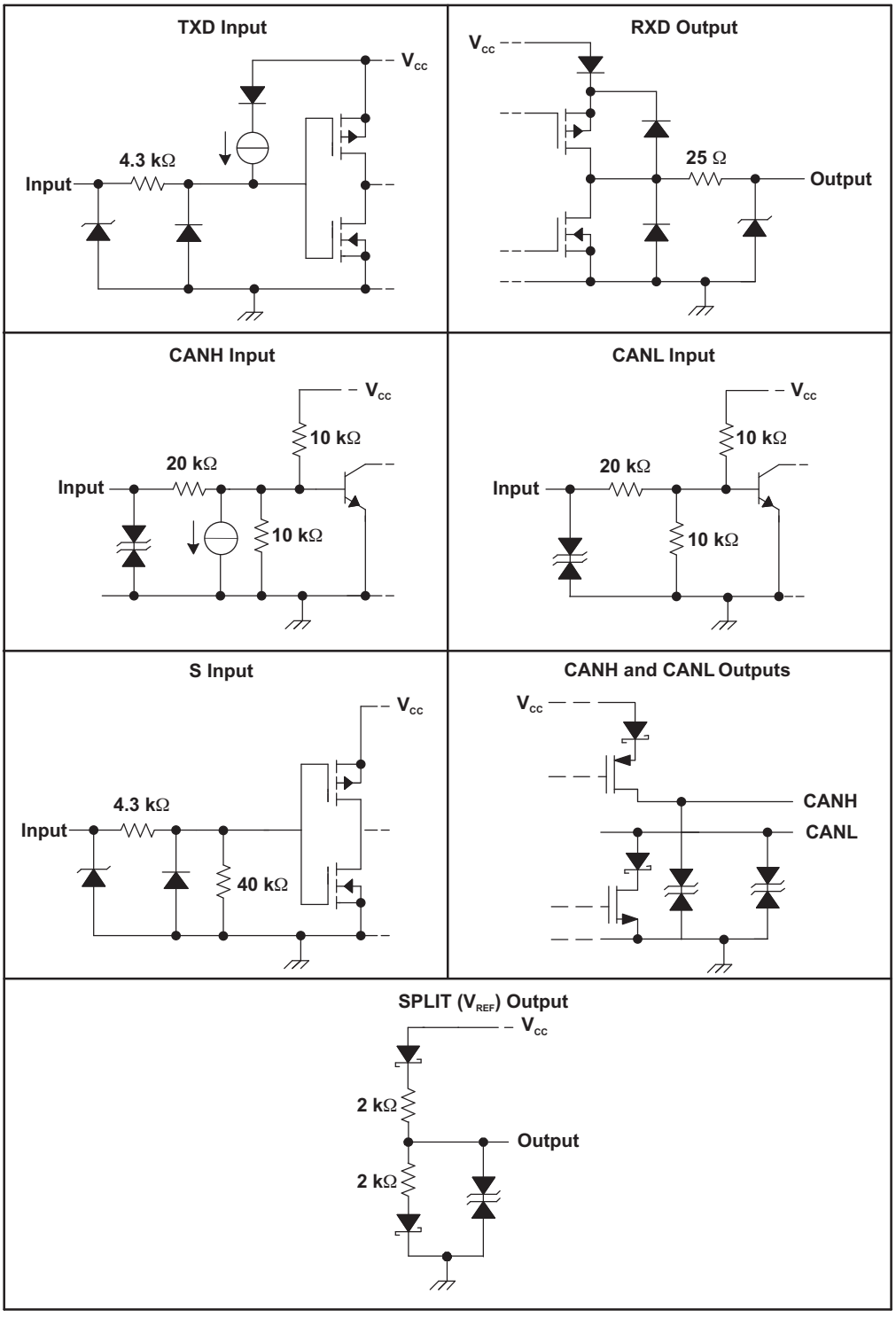


Figure 13. Typical Application Using Split Termination for Stabilization

Equivalent Input and Output Schematic Diagrams



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65HVDA1050AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1050A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

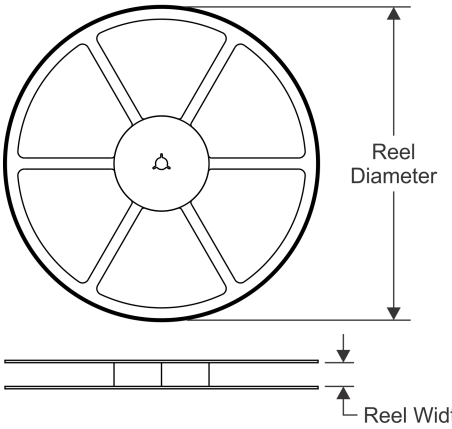
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

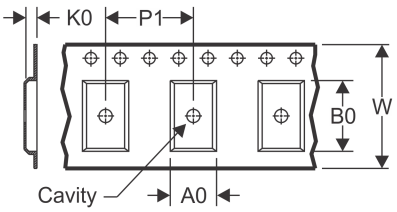
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

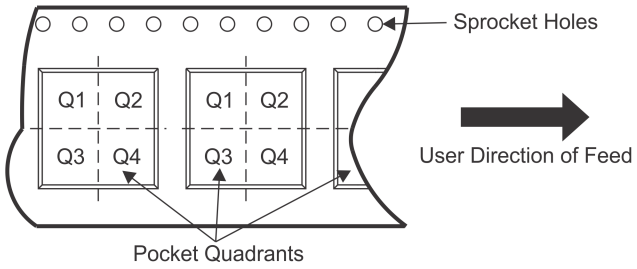


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

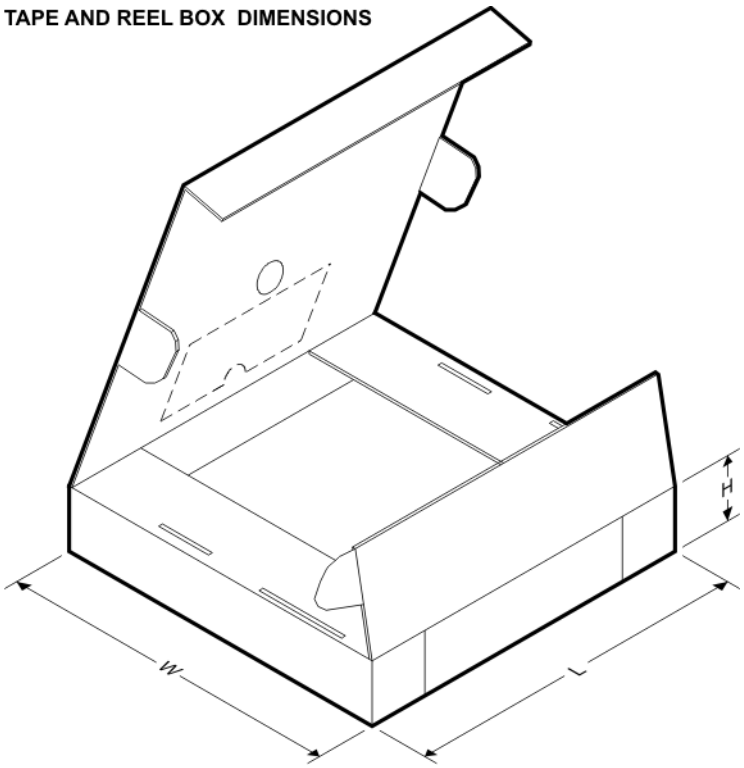
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVDA1050AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVDA1050AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

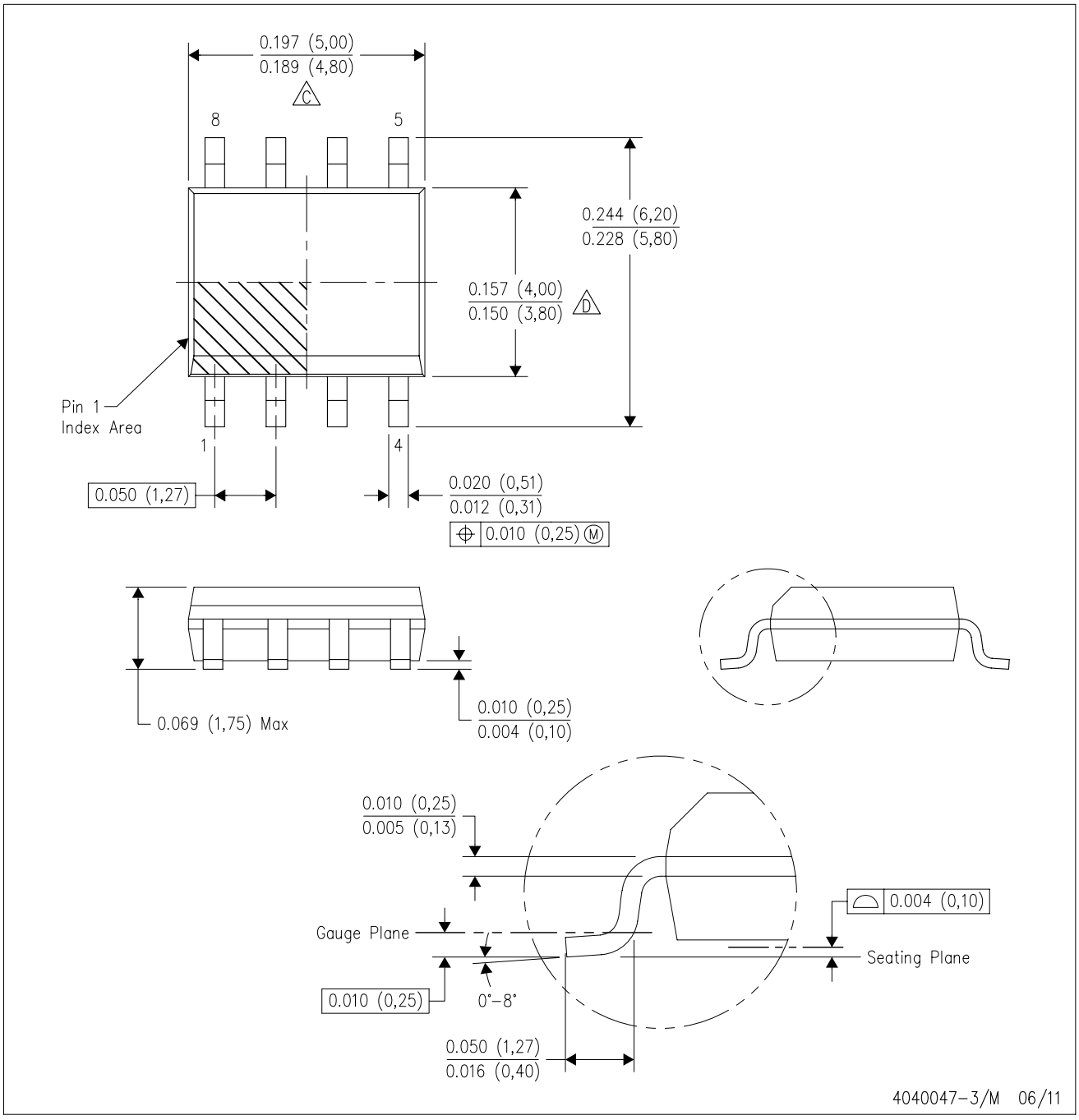
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

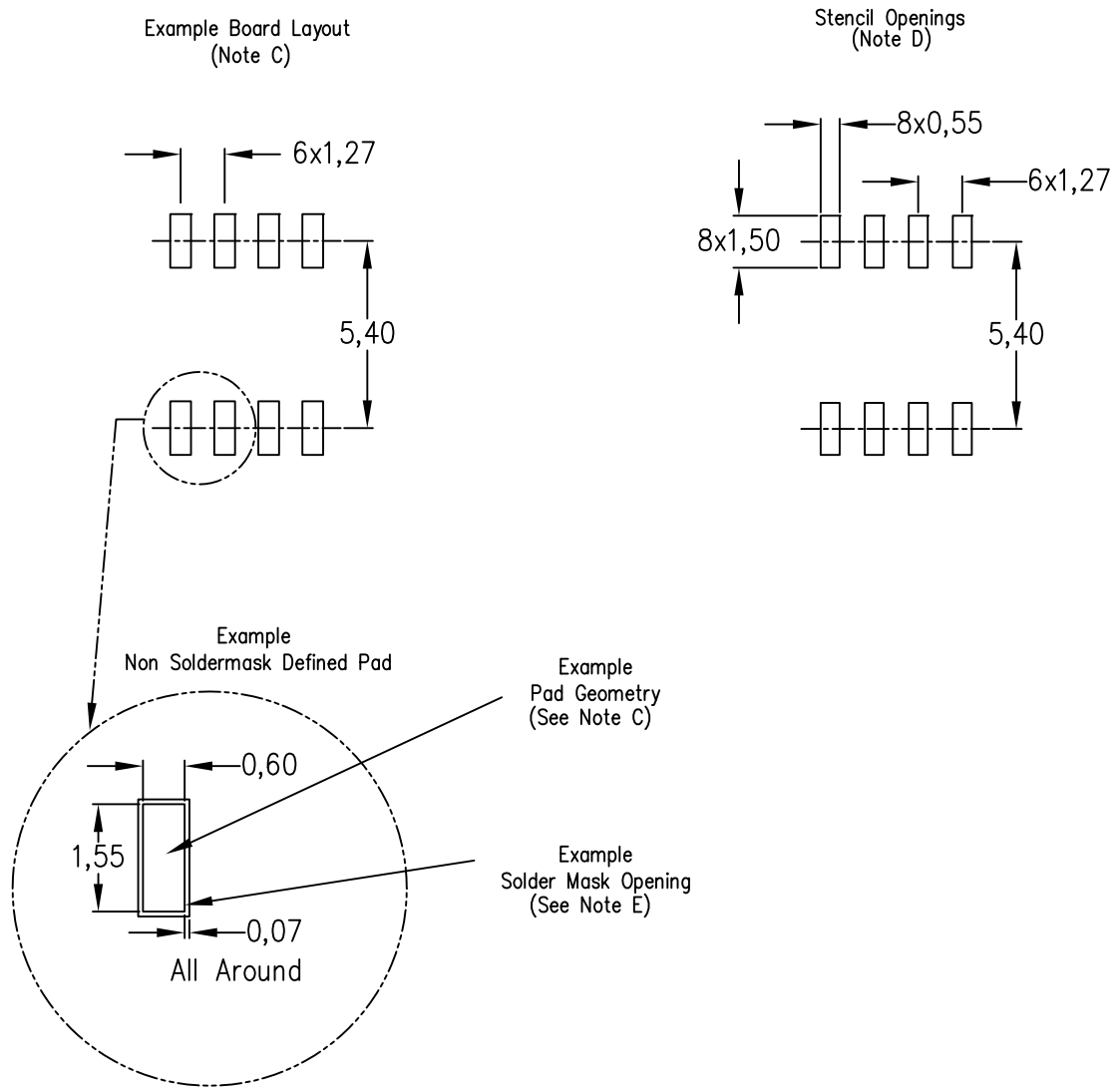
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVDA1050AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVDA1050AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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