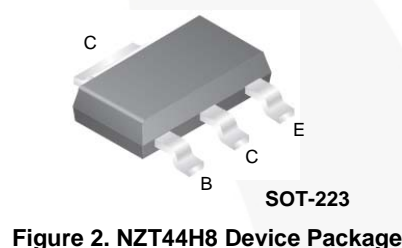
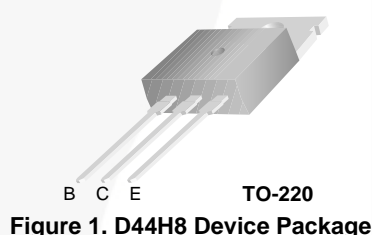


D44H8 / NZT44H8 NPN Power Amplifier

Features

- This device is designed for power amplifier, regulator and switching circuits where speed is important.
- Sourced from process 4Q.



Ordering Information

Part Number	Marking	Package	Packing Method
D44H8	D44H8	TO-220 3L	Rail
NZT44H8	44H8	SOT-223 4L	Tape and Reel

Absolute Maximum Ratings^{(1),(2)}

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{CEO}	Collector-Emitter Voltage	60	V
I_C	Collector Current - Continuous	8.0	A
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Notes:

1. These ratings are based on a maximum junction temperature of 150°C .
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

Thermal Characteristics⁽³⁾

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Max.		Unit
		D44H8	NZT44H8	
P_D	Total Device Dissipation	60	1.5	W
	Derate Above 25°C	480	12	mW/ $^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.1		$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	83.3	$^\circ\text{C}/\text{W}$

Note:

3. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 100\text{ mA}, I_B = 0$	60		V
I_{CBO}	Collector-Base Cut-Off Current	$V_{CB} = 60\text{ V}, I_E = 0$		10	μA
I_{EBO}	Emitter-Base Cut-Off Current	$V_{EB} = 5\text{ V}, I_C = 0$		100	μA
h_{FE}	DC Current Gain	$V_{CE} = 1\text{ V}, I_C = 2\text{ A}$	60		
		$V_{CE} = 1\text{ V}, I_C = 4\text{ A}$	40		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 8\text{ A}, I_B = 0.4\text{ A}$		1.0	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = 8\text{ A}, I_B = 0.8\text{ A}$		1.5	V
$V_{BE(on)}$	Base-Emitter On Voltage	$V_{CE} = 2\text{ V}, I_C = 10\text{ mA}$	0.52	0.65	V
f_T	Current Gain-Bandwidth Product	$I_C = 500\text{ mA}, V_{CE} = 10\text{ V}$	50		MHz

Typical Performance Characteristics

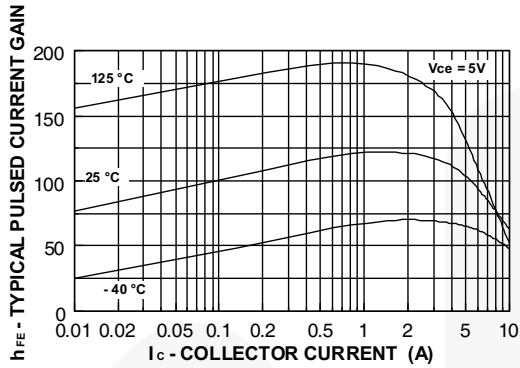


Figure 3. Typical Pulsed Current Gain vs. Collector Current

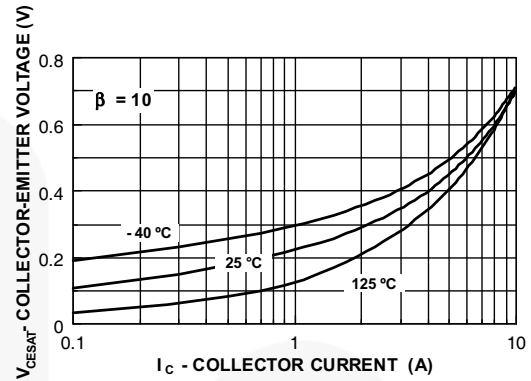


Figure 4. Collector-Emitter Saturation Voltage vs. Collector Current

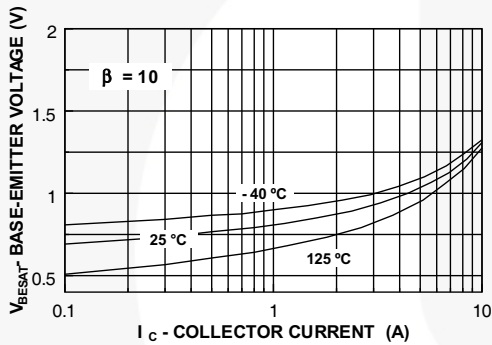


Figure 5. Base-Emitter Saturation Voltage vs. Collector Current

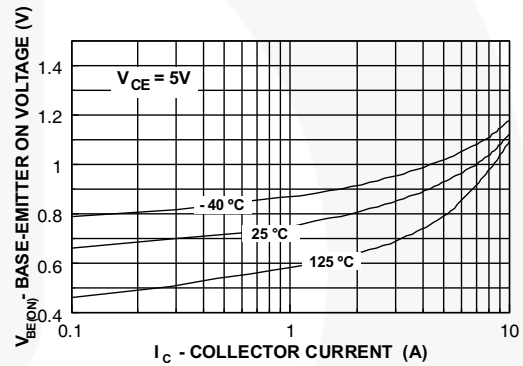


Figure 6. Base-Emitter On Voltage vs. Collector Current

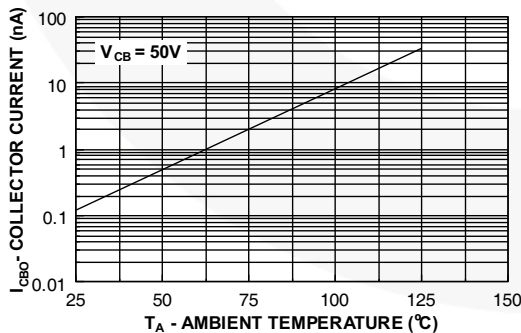


Figure 7. Current Cut-Off Current vs. Ambient Temperature

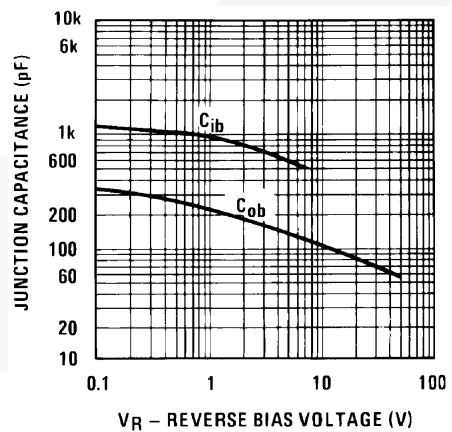


Figure 8. Junction Capacitance vs. Reverse Bias Voltage

Typical Performance Characteristics (Continued)

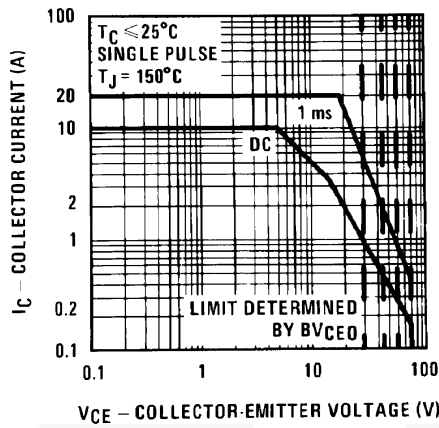


Figure 9. Safe Operating Area TO-220

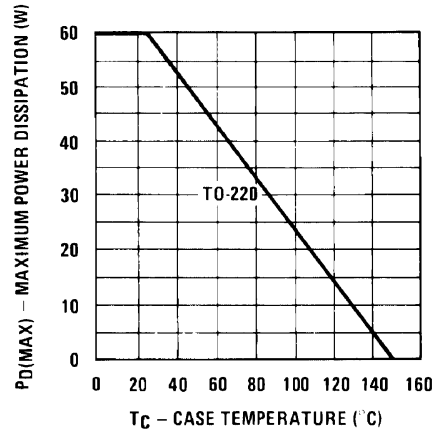


Figure 10. Maximum Power Dissipation vs. Case Temperature

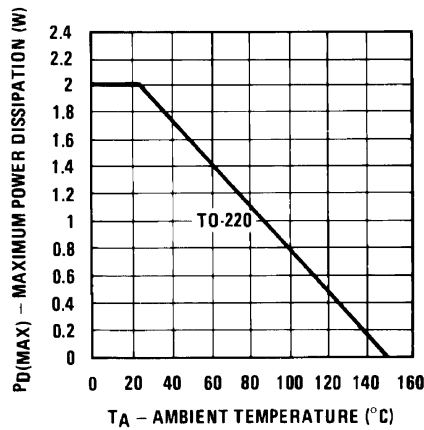


Figure 11. Maximum Power Dissipation vs. Ambient Temperature

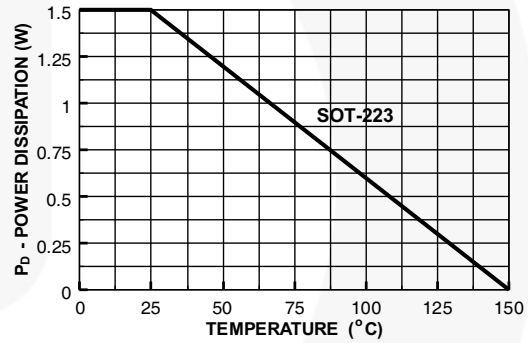


Figure 12. Power Dissipation vs. Ambient Temperature

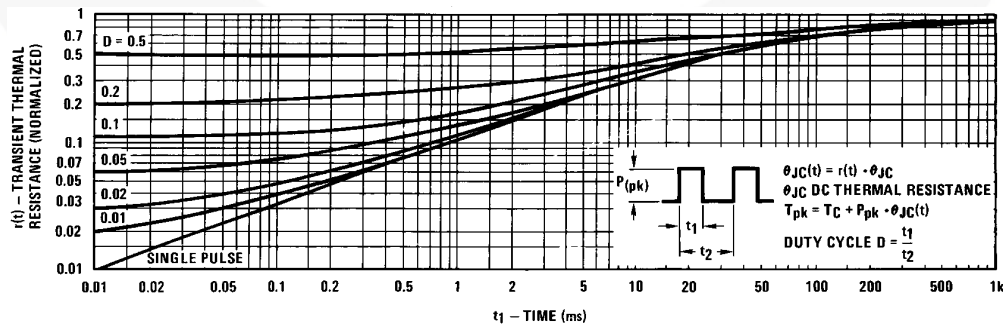
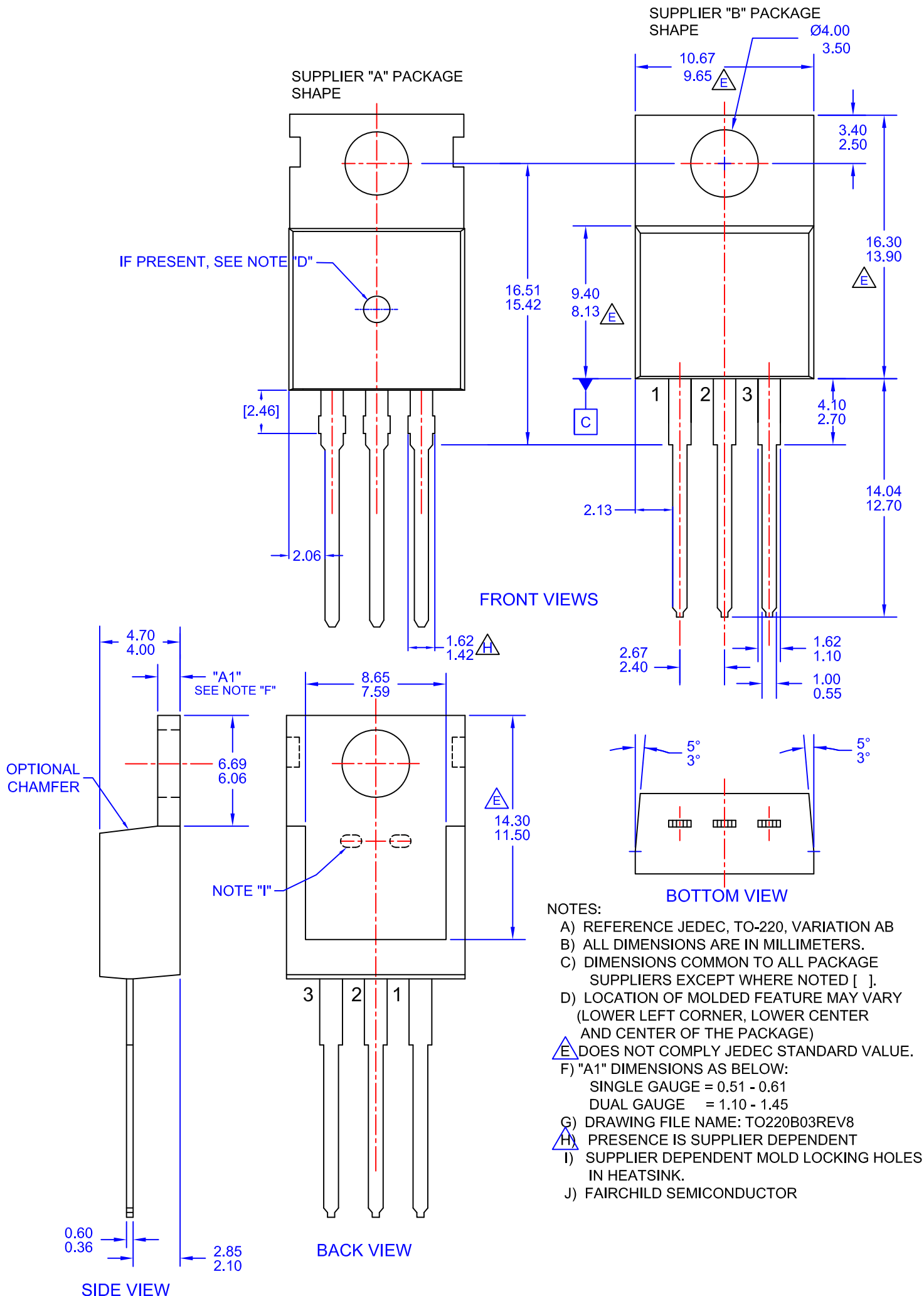
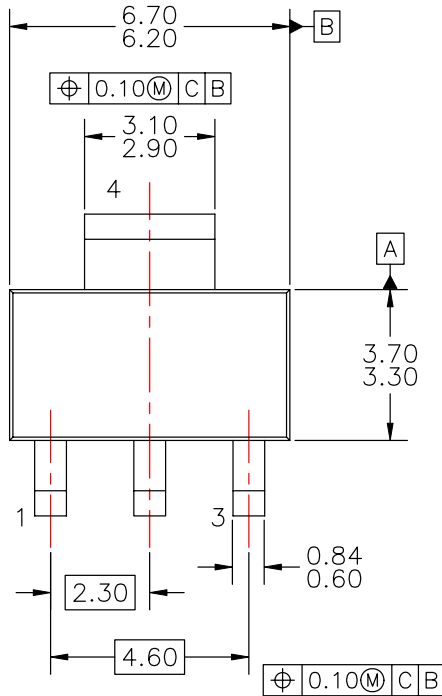


Figure 13. Thermal Response in TO-220 Package

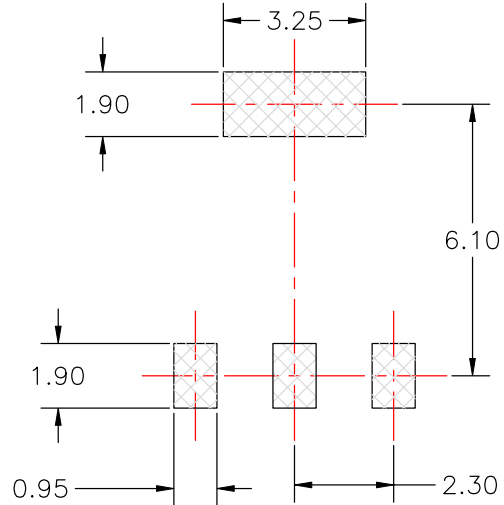


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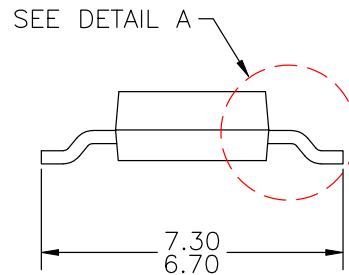
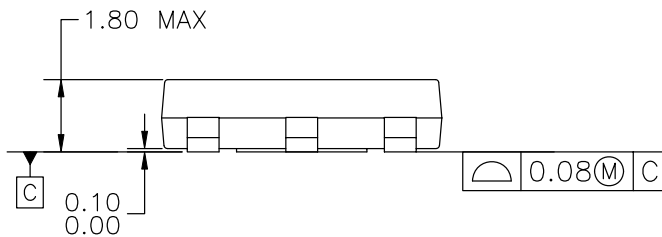
APPROVED
July-14-2008



REVISIONS			
LTR	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	JAN.25.1996	TL/FSCP
2	CHG DWG TEMPLATE FR NATIONAL TO FAIRCHILD; CHG DIM STYLE FR DUAL INCH[MM] TO SINGLE, MM; CHG LD WID FR 0.74 \pm 0.05 TO 0.60-0.84; REMOVE PKG THICK DIM (1.6); CHG TOTAL PKG HT FR 1.5 TO 1.80 MAX; CHG FOOT LANDING DIM FR 0.91 MIN TO 0.60 MIN; CHG LD THICKNESS FR 0.35 \pm 0.08 TO 0.20-0.35; ADD DRAFT ANGLE OF MOLDED BODY TOP & BOT; CHG LD LGTH TO PKG EDGE DIM TO BASIC; CHG LD PITCH FR 2.29 BS TO 2.30 BS; CHG BODY WID FR 3.56 \pm 0.38 TO 3.30; CHG BODY LN FR 6.55 \pm 0.38 TO 6.30; CHG TOTAL PKG WID FR 6.94 \pm 0.38 TO 7.30; CHG PAD SIZE FR 0.99 MAX TO 0.95; CHG PAD PITCH FR 2.286 TO 2.30; CHG THERMAL TAB SIZE FR 3.28 MAX TO 3.25; CHG PAD SIZE FR 1.5 TO 1.90; CHG PAD SPACE FR 6.3 TO 6.10; CHG NOTE '2' TO 'A' W/O DATE; DEL NOTE ON LD FINISH; ADD NOTES B, C, D, E & F.	12FEB08	LZSC/FSCP

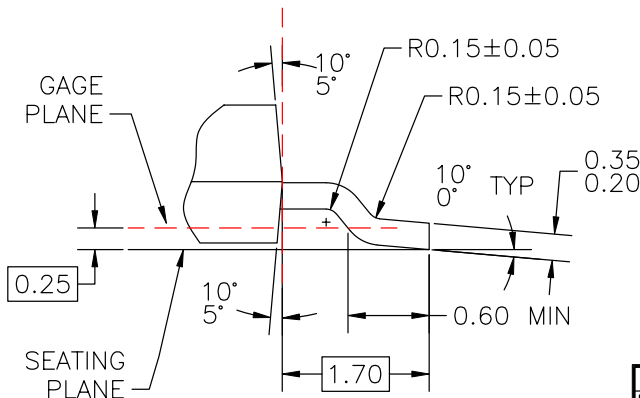


LAND PATTERN RECOMMENDATION





NOTES: UNLESS OTHERWISE SPECIFIED

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- B) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- C) ALL DIMENSIONS ARE IN MILLIMETERS.
- D) DRAWING CONFORMS TO ASME Y14.5M-1994.
- E) LANDPATTERN NAME: SOT230P700X180-4BN
- F) DRAWING FILENAME: MKT-MA04AREV2



DETAIL A
SCALE: 2:1

APPROVALS		DATE			
DRAWN:	J.U. COMPARATIVO JR.	26FEB2008			
CHECKED:	L.Z. STA CRUZ	<div><div>FAIRCHILD</div><div>SEMICONDUCTOR™</div></div> <div>MOLDED PACKAGE</div> <div>SOT-223, 4 LEAD</div>			
APPROVED:	M.R. GESTOLE				
G.S. BAJE					
PROJECTION					
		SCALE	SIZE	DRAWING NUMBER	REV
INCH		1:1	A3	MKT-MA04A	2
		FORMERLY: N/A		SHEET : 1 OF 1	



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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