GC5322 Wideband Digital Predistortion Transmit Processor

Check for Samples: GC5322

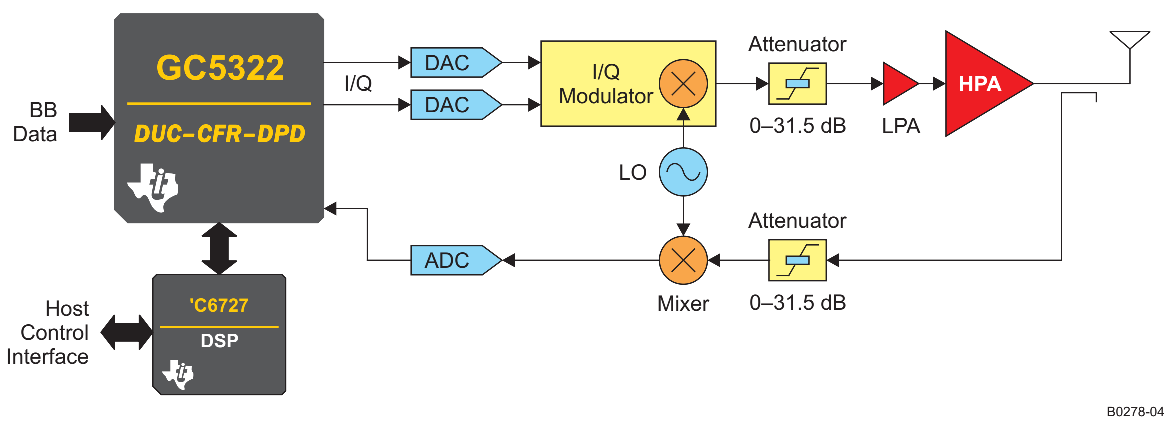
FEATURES

- Integrated DUC, CFR, and DPD Solutions
- 40-MHz (28-Mhz) Signal Bandwidth, Third (Fifth)-Order Expansion BW in DPD Section, Maximum Complex Rate 140 Mhz
- DUC: up to 12 CDMA2000 or TD-SCDMA, 4 W-CDMA, 3–10 MHz or 1–20 MHz OFDMA Carriers
- CFR: Typically Meets 3GPP TS 25.141 <6.5-dB PAR, <8-dB PAR for OFDMA Signals
- DPD: Short-Term and Long-Term Memory Compensation to 1 μs, Typical ACLR Improvement > 20 dB
- Single-Antenna TX Mode, Single or Shared Feedback
- 352-Ball S-PBGA Package, 27-mm × 27-mm
- 1.2-V Core, 1.8-V HSTL, 3.3-V I/O
- Typical Power Consumption < 2.5 W, Configuration Dependent
- Flexible DSP Algorithm Supports Existing and Emerging Wireless Standards
- Supports Direct Interface to TI High-Speed Data Converters

APPLICATIONS

- 3GPP (W-CDMA) Base Stations
- 3GPP2 (CDMA2000) Base Stations
- WiMAX, WiBro, and LTE (OFDMA) Base Stations
- Multicarrier Power Amplifiers (MCPAs)

SYSTEM BLOCK DIAGRAM



DESCRIPTION

The GC5322 is a wideband digital predistortion transmit processor that includes a digital upconverter (DUC) block, crest factor reduction (CFR) block, feedback (FB) block, digital predistortion (DPD) block, and capture buffer (CB) blocks. The GC5322 is operated in single-antenna mode with shared or individual feedback paths.

The GC5322 GPP block receives the interleaved IQ data from the baseband input. The individual IQ channels are then routed to the DUC. The GPP and DUC can be bypassed to input a combined IQ signal. The DUC provides three stages of interpolation and a complex mixer. There are two DUC blocks. The output from the DUC blocks is combined in the sum chain. Each of the 1 to 12 DUC channels can be summed, and the composite signal can be scaled.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

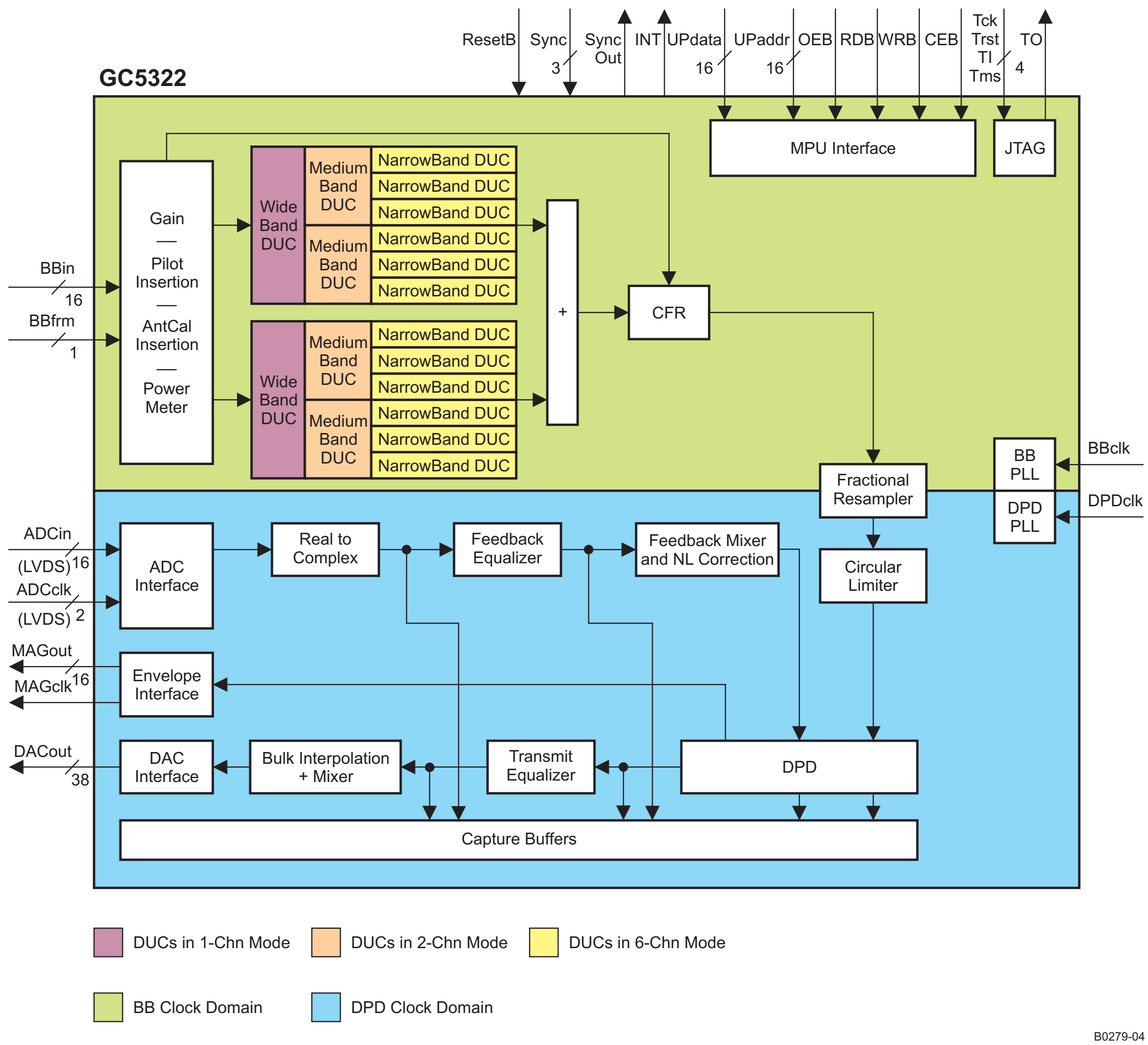
The CFR block has four serial stages of peak detection and cancellation. The CFR block cancellation filter can be programmed as real or complex. The peak-reduced signal is output to the Farrow resampler. The Farrow resampler resamples the CFR output to the DPD clock rate. The Farrow resampler block also has a complex mixer for composite carrier-frequency offset.

The DPD subsystem circularly clips the data, and then applies nonlinear and linear correction. The GC5322 DPD block reduces adjacent-channel leakage ratio (ACLR), or out-of-band energy, by 20 dB or more. The efficiency of follow-on power amplifiers (PAs) is substantially improved by reducing the PAR and ACLR of digital signals. After DPD correction, a bulk upconversion block and DAC interface can increase the IQ output rate, provide a final IF frequency offset, and interface to the DAC5682Z or DAC5688.

The CB signal capture can be based on a timed event (external sync) and delay, or signal statistic values (smart-capture buffer – SCB). There are two signal buffers; typically one captures the transmit path, and the other captures the feedback path.

The FB block receives the LVDS ADC information and performs signal processing to downconvert the received signal to 0IF. The FB block also has a feedback-path receive equalizer.

GC5322 FUNCTIONAL BLOCK DIAGRAM



AVAILABLE OPTIONS

T_C	PACKAGED DEVICE(1)
	352-ball S-PBGA package, 27 mm × 27 mm
–40°C to 85°C	GC5322IZND

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

REFERENCES

1. GC5322_GC5325_architecture_datasheet_ext.pdf (obtain through local TI Field Application Engineer)
2. *GC5325 System Evaluation Kit* user's guide, schematic diagram (obtain through local TI Field Application Engineer)
3. GC5322 configuration (TGTCFG) - (obtain through local TI Field Application Engineer)
4. DSP – TMS320C672x DSP Universal Host Port Interface Reference Guide (SPRU719)
5. DSP – TMS320C672x DSP External Memory Interface (EMIF) User's Guide (SPRU711)

DETAILED DESCRIPTION

GC5322 Introduction

The GC5322 is a flexible transmit sector processor that includes a digital upconverter (DUC) block, a crest factor reduction (CFR) block, and a digital predistortion (DPD) block and its associated feedback chain. The GC5322 processes composite input bandwidths of up to 40 MHz and processes DPD expansion bandwidths of up to 140 MHz. By reducing the peak-to-average ratio (PAR) of the input signals using the CFR block and linearizing the power amplifier (PA) using the DPD block, the GC5322 reduces the costs of multicarrier PAs (MCPA) for wireless infrastructure applications. The GC5322 applies CFR and DPD, and a separate microprocessor (a Texas Instruments TMS320C6727 DSP) is used to optimize performance levels and maintain target PA performance levels.

By including the GC5322 in their system architecture, manufacturers of BTS equipment can realize significant savings on power-amplifier bill of materials (BOM) and overall operational costs due to the PA efficiency improvement. The GC5322 meets multicarrier 3G performance standards (PCDE, composite EVM, and ACLR) at PAR levels down to 6.5 dB and improves the ACLR, at the PA output, by 20 dB or more. The GC5322 integrates easily into the transmit signal chain between baseband processors (such as the Texas Instruments TMS320C64x™ DSP family) and TI high-performance data converters.

A typical GC5322 system application includes the following transmit-chain components:

- TMS320C6727 digital signal processor (DSP)
- DAC5682 16-bit, 1-GSPS DAC; DAC5688 16-bit, 800-Msps DAC (transmit path)
- CDCM7005, CDCE72010 clock generator
- TRF3761 integrated VCO/PLL synthesizer
- TRF3703 quadrature modulator
- ADS5517 11-bit 200-MSPS ADC or ADS6149 14-bit, 250-MSPS ADC (feedback path)
- AMC7823 analog monitoring and control circuit with GPIO and SPI

GC5322 SYSTEM ARCHITECTURE

The GC5322 system architecture can be modified to suit a number of different antenna streams. There is a tradeoff between the number of antenna streams per GC5322, and shared ADC feedback. Figure 1 shows a single-antenna configuration, where one GC5322 is used. There are several other architectures possible:

Architecture	Figure	Benefit	Tradeoff/Complexity
One antenna stream, up to 140-MHz DPD bandwidth, added envelope output (fifth-order correction, 28-Mhz BW)	Figure 1	Magnitude output for power amplifier drain modulator can increase efficiency	
Two antenna streams, up to 140-MHz DPD bandwidth, shared feedback ADC (fifth-order correction, 28-Mhz BW)	Figure 2	Reduced cost of feedback path DSP shared between two GC5322s; GC5325 EVM as example	DSP must output antenna-select value using HD22.20. Antenna-select value is also used to select CS2-CEB(2). Slower adaptation time

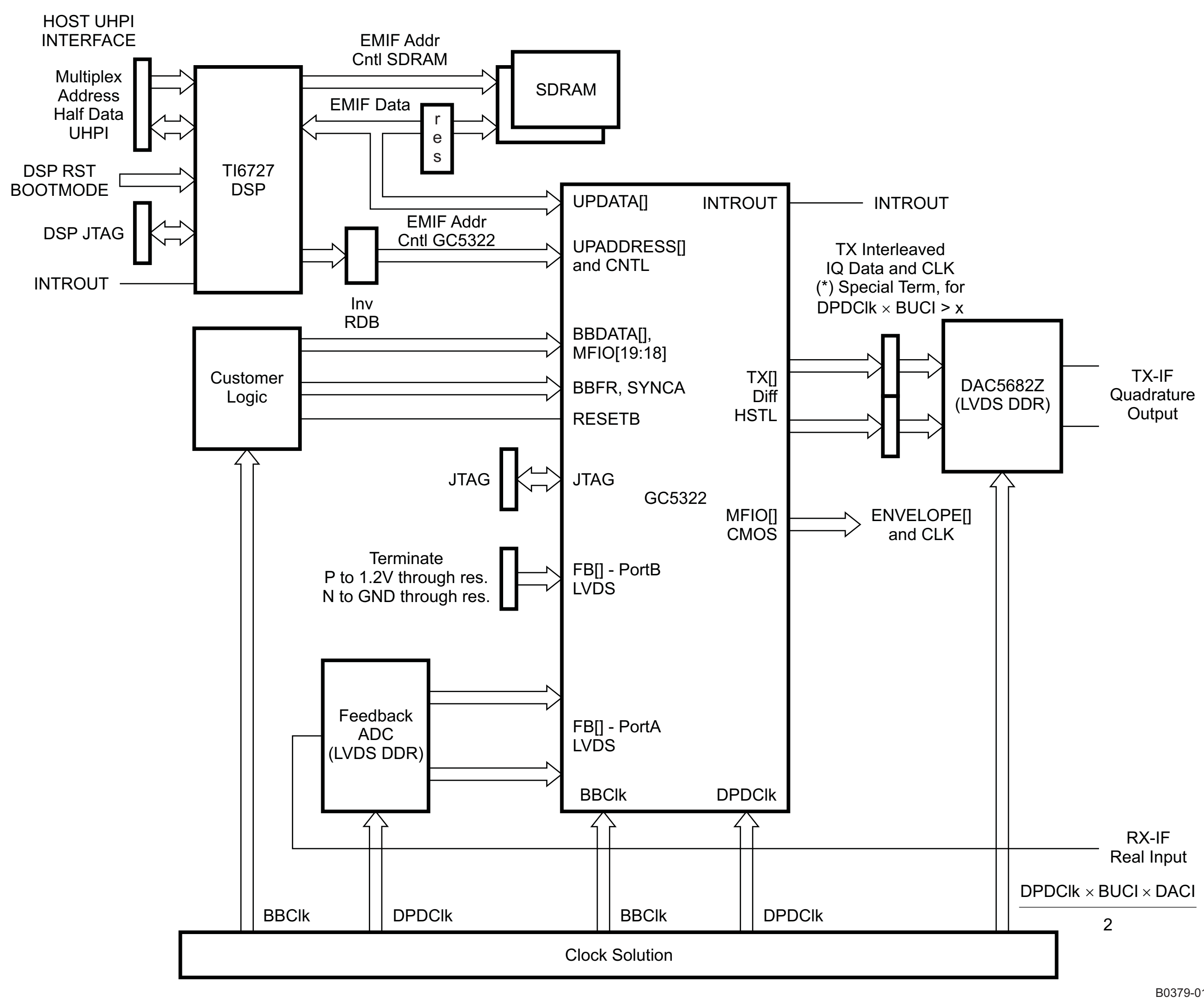


Figure 1. Single-Antenna GC5322 System Diagram (Envelope Output Added)

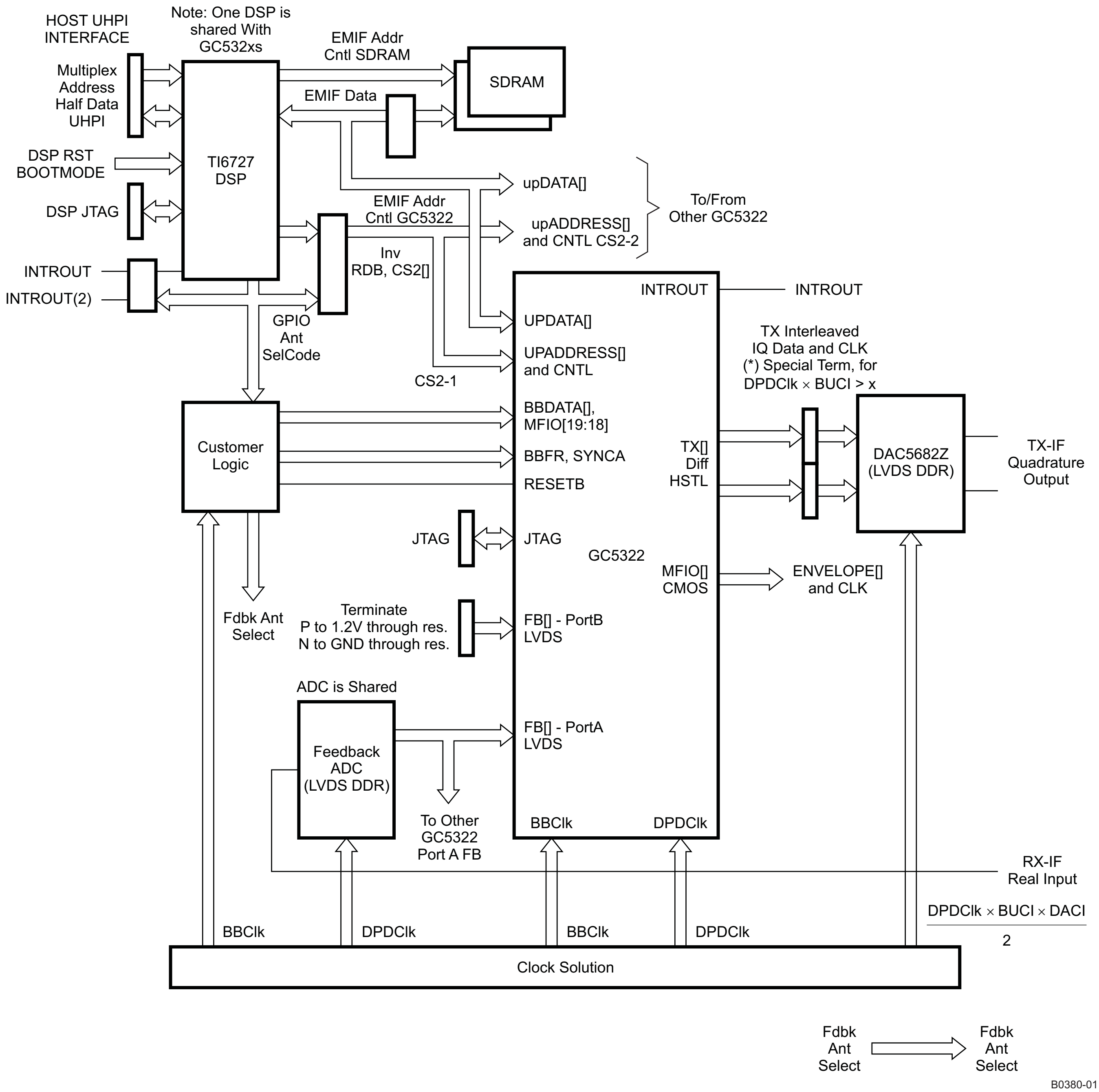


Figure 2. Dual Antenna, Two GC5322s (One Shown), Shared Feedback

Baseband Interface

The GC5322 BB interface block accepts baseband signals over an interleaved IQ parallel interface at a clock rate of up to 93 Mhz. The input interface supports up to 12 separate baseband carriers. The DUC interpolation, baseband clock, and number of channels must be programmed to allow all I and Q DUC channels to be received within the interpolation number of clocks. The GPP and DUC can be bypassed, and the interleaved IQ data can be directly input to CFR; the BB clock can be up to 140 MHz, 70 MHz complex rate in this mode. The baseband interface has 18 bits of data (top 16) BBData[15:0], BBFrame, and two additional data bits (bottom two data) MFIO[18:19].

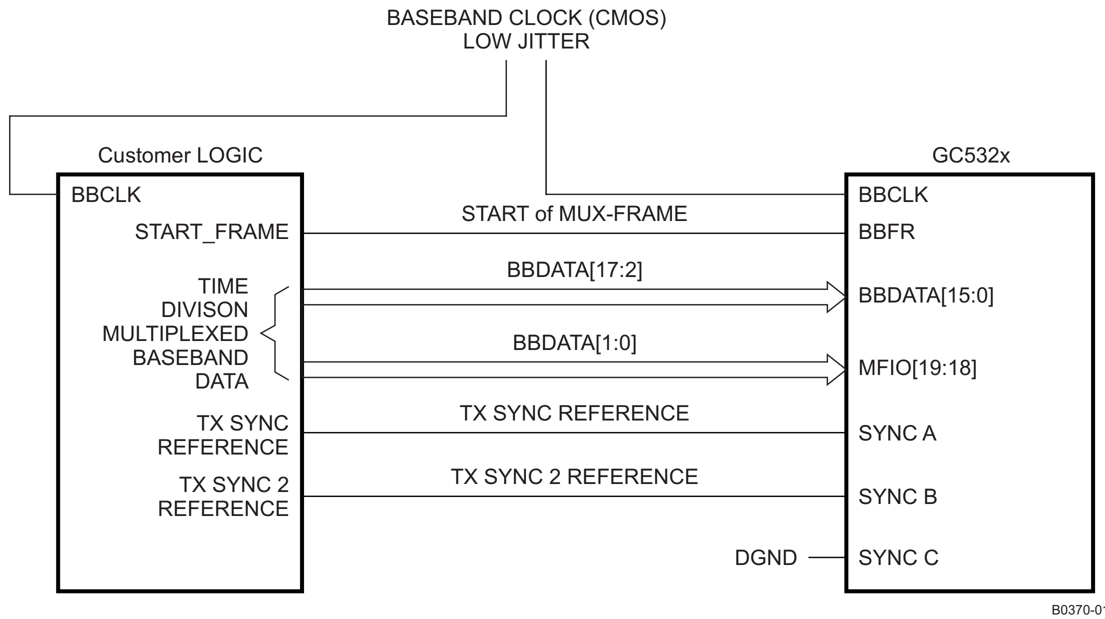


Figure 3. Baseband and Sync Interface to GC5322

BB Clock Input

The baseband clock input is a CMOS, low-jitter clock.

Gain/Pilot Insertion/AntCal Insertion/Power Meter

Baseband gain can be applied on a per-carrier basis to control the individual channel power accurately through the system. A UMTS pilot sequence at a programmable gain can be added for antenna calibration. Each individual baseband channel has an integrated $I^2 + Q^2$ power accumulator. There is a common control for the power meters.

Digital Upconverters (DUCs)

The GC5322 DUC block has interpolation filters, programmable delays, and complex mixers for each channel. There are two DUC blocks within the GC5322. The sum chain after the DUC channel combines the DUC channel streams or the bypass stream and sends the data to the CFR block. Each DUC can operate in one wide, two medium, or six CDMA channels. Each DUC has a PFIR for spectral shaping, a CFIR for interpolation and image rejection, and a bulk interpolation CIC. The two DUCs can support:

- (6-channel/DUC mode) up to 12 – 1.23(8) Mhz CDMA, 1xEVDO, or TDSCDMA carriers
- (2-channel/DUC mode) up to 4 – WCDMA or LTE-5 carriers
- (2-channel/DUC mode) up to 3 – WiBro, WiMAX-10 carriers
- (1-channel/DUC mode) up to 2 – WiBro, WiMAX, LTE-10 carriers
- (1-channel/DUC mode) 1 – WiMAX or LTE-20 carrier

Users can specify the filter characteristics of the DUC programmable finite impulse response (PFIR), compensating finite impulse response (CFIR), and cascade integrator comb (CIC) filters. Users can also specify the center frequencies of each carrier with a resolution of 0.25 μHz. Additional controls available in the DUCs include bulk and fractional time-delay adjustments, and phase adjustments. The maximum DUC output bandwidth is limited to the BB maximum rate, and the usable channel and phase adjustments.

Crest Factor Reduction (CFR)

The GC5322 CFR block selectively reduces the peak-to-average ratio (PAR) of wideband digital signals. There are four peak-detection cancellation sections in series in the CFR block. Each stage compares the estimated peak at the stage input with the target, and subtracts a scaled cancellation peak from the signal. There are 24 cancellers pooled among the four stages. The CFR interpolation filter must have at least 1.6× bandwidth, typical is 2× BBClock-to-signal bandwidth.

There are four canceller memories, and an update shadow memory, that can be used for the auto-IPDL UMTS select cancellation filter. The shadow memory allows the user to update one of the four filter banks during operation. The CFR block has a composite RMS meter that can monitor the CFR input.

The CFR block for WCDMA reduces TM1, TM3 signals for four adjacent carriers to 6.5 db PAR within the 3GPP limit. The WiMAX-10 reduction for two adjacent carriers is to 8.5 db PAR. TDSCDMA and CDMA performance are limited by the carrier allocations and carrier coding.

Fractional Farrow Resampler (FR)

The fractional resampler block takes the composite DUC signal from CFR and resamples this through fractional interpolation to the DPD clock / 2. The user-programmable Farrow resampler supports upsampling rates from 1× to 64×, with 16-bit precision on the interpolation ratio. After the fractional interpolation, a complex mixer is available to provide a composite carrier IF offset frequency. A peak I or Q monitor is provided.

Digital Predistortion (DPD)

The DPD block provides predistortion for up to Nth-order nonlinearities, and can correct multiple orders and lengths of PA memory effects. The circular hard limiter provides a circular clipper that limits the magnitude-squared value to –6 dbfs. This is optimized for hardware, and for the allowed gain expansion in the nonlinear DPD correction.

The DPD has an RMS power meter and a peak I or Q monitor.

The predistortion is performed for the nonlinear correction in the DPD section. The linear correction is performed in the TX equalizer. The predistortion correction terms are computed by an external processor (TMS320C6727 DSP) based on capture buffer information and the DPD software.

The DSP sets up the condition for collecting capture buffer data, retrieves the captured data over the EMIF bus, and then performs calculations to compute the error and corrections to be used for the transmit path.

The host interface controls the mode of operation of the software in the TI DSP. TI provides a base delivery of 'C6727 software to GC5322 customers that achieves a typical ACLR improvement of 20 dB or more when compared to a PA without DPD. The standard EMIF bus allows the user to provide an alternate DPD adaptation algorithm and DSP embodiment, if desired.

DPD Clock Input

The DPD clock input is an LVDS, low-jitter clock.

SyncD – DPD Clocked Sync Input

Sync D, DC (if used) is registered with the DPD clock.

Bulk Upconverter (BUC)

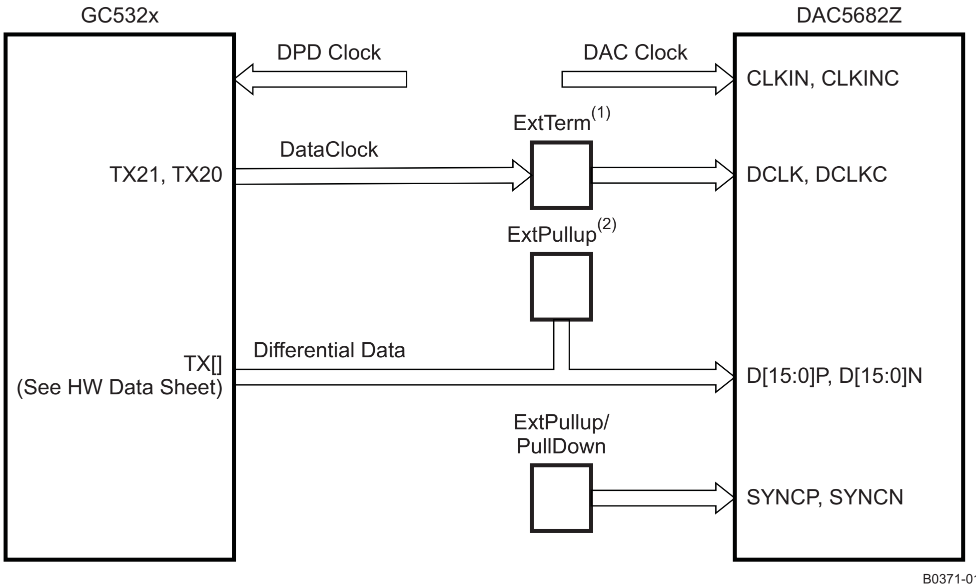
The bulk upconverter block can interpolate the DPD block output by 2× or 3× with a complex output. The BUC can also have no interpolation. The BUC interpolation, and the DAC interpolation are used to interpolate the DPD predistorted output. The BUC mixer can translate the composite IQ predistorted TX output if the BUC interpolation is > 1.

Output Formatter and DAC Interface (OFMT)

The output format and DAC interface presents the GC5322 output in the proper format for the different DAC output interfaces. The output formatter supports a test pattern for testing the DAC5682Z interface. The output interfaces supported for the GC5322 are:

- DAC5682 interleaved IQ

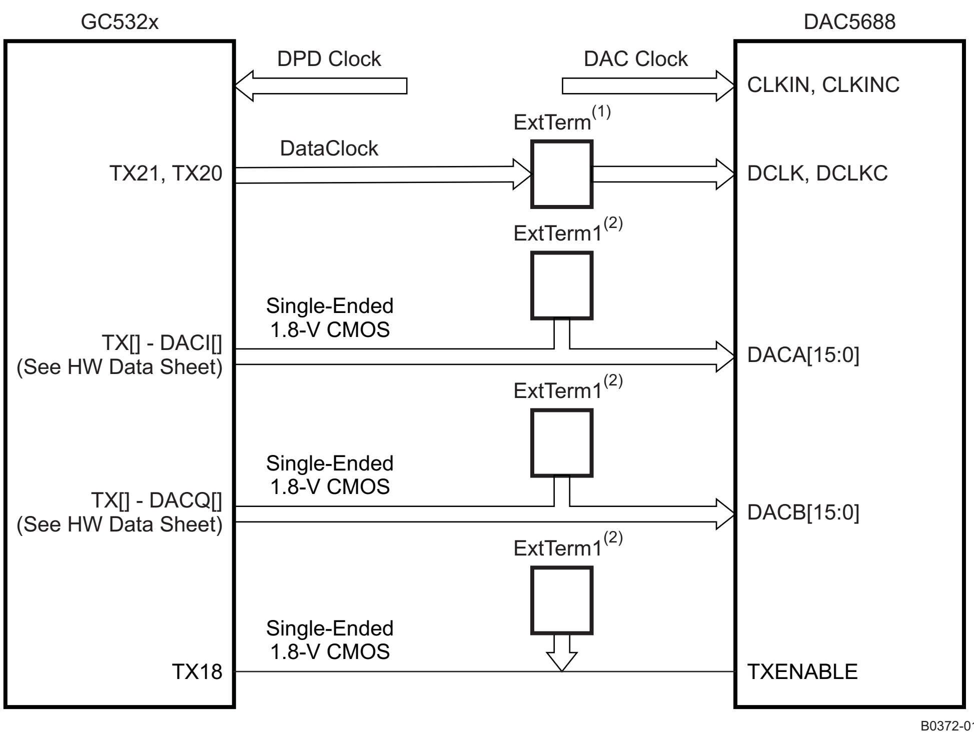
- DAC5688 parallel IQ !!!



(1) 100 Ω between P, N of series capacitor on DAC

(2) 500-Ω pullup to 1.8 V only required when DAC data clock is > 337.5 MHz

Figure 4. GC5322 to DAC5682Z Interface



(1) 100 Ω between P, N of series capacitor on DAC

(2) Tester uses 50 Ω to 0.9 V for data lines; TXENABLE 100 Ω to 1.8 V, 100 Ω to ground.

Figure 5. GC5322 to DAC5688 (Parallel IQ) Interface

Feedback Path (FB)

The feedback path has two LVDS input ports. The A port is preferred (it has better timing). The external ADC input is converted or processed to generate a complex signal. The feedback equalizer has eight complex taps as a receive equalizer. The feedback path has a mixer to translate the complex IF to the 0IF reference. The ADC feedback rate is at the same rate as the DPD clock (f_S). The typical feedback is $f_S/4$, $f_S3/4$(m), or $f_S5/4$ IF. The feedback equalizer can provide (m) inverted spectral output, if needed.

The FB complex mixer translates the frequency of the complex input signal to 0IF. The feedback path has the capability for nonlinear correction with a lookup table. TI ADCs that connect to the feedback path are the SDR type ADS5444, DDR type ADS5445 (6149, 5517), DDR with reversed-data-phase ADSC217 and ADS5463. The ADC feedback path has modified connections for shared feedback path operation (see Figure 2). The GC5322 simplifies timing by providing a FIFO for each ADC port.

NOTE

There are eight LVDS data lanes and one LVDS clock lane. If the ADC has < 8 LVDS data lanes, the MSB of the ADC is connected to LVDS lane 7 (MSB) of the A feedback port.

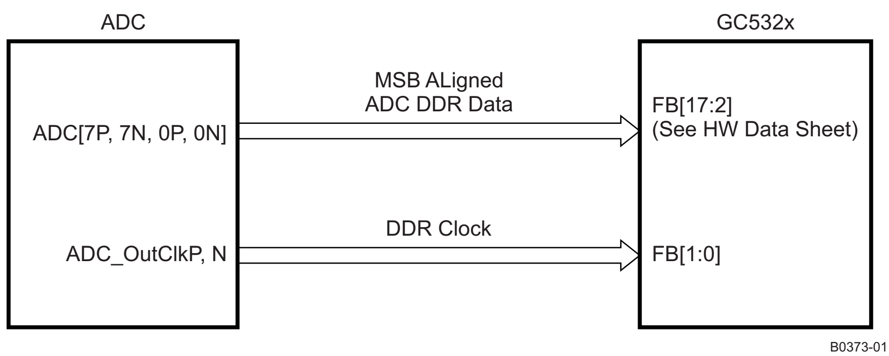


Figure 6. LVDS DDR ADC to GC5322 FB Interface

Microprocessor (MPU) Interface

The MPU interface is designed to interface with external memory interface (EMIF) ports on TI DSPs operating in asynchronous mode. It consists of a 16-bit bidirectional data bus, a 10-bit address bus, and RDB, WRB, OEB, and CEB control signals. There are EMIF control signals which are not directly connected to the DSP:

Table 1. EMIF to GC5322 Microprocessor Interface

6727 DSP EMIF	GC5322	Notes
EM_D[15.0]	UPDATA[15.0]	
EM_A[8.0]	UPADDR[9.1]	
EM_BA[1]	UPADDR[0]	
EM_CS2	CEB	DSP HD[22:20] are used for logic for multiple chip select, inverted output.
EM_RWB	OEB	Invert RWB, send to OEB
EM_WEB	WRB	
EM_OEB	RDB	

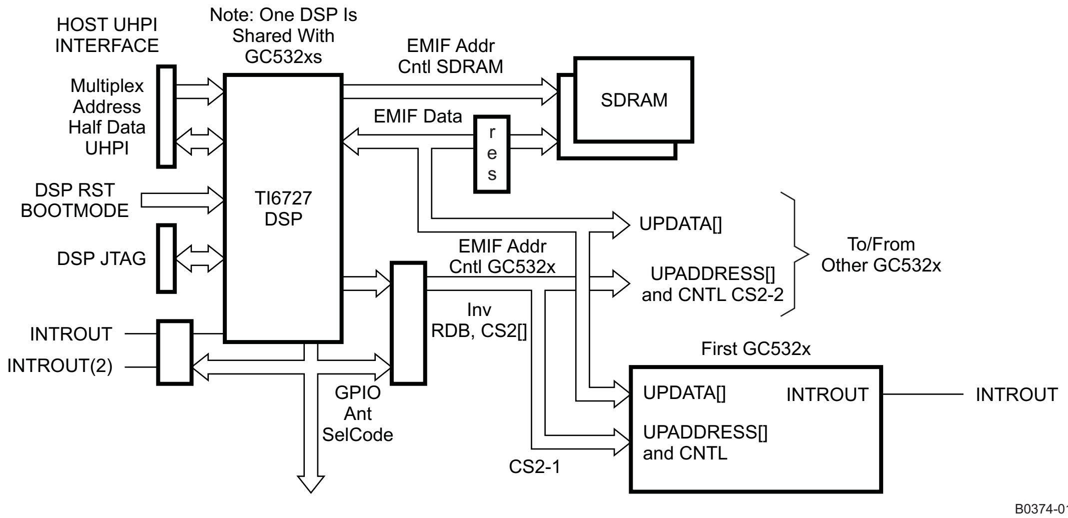


Figure 7. '6727 DSP to GC5322 EMIF Interface

Capture Buffers (CB)

The GC5322 has two capture buffers of 4096 complex words. The capture buffers are normally used to capture the TX reference signal and the feedback output signal. Other signals can be captured:

- The TX reference from the DPD after the circular hard limiter
- The feedback output; this represents the waveform as seen by the PA.
- The error output
- Testbus(31:16)
- QRD error output

The second capture buffer can be used to provide:

- The TX reference from the DPD after the circular hard limiter
- The feedback output; this represents the waveform as seen by the PA.
- The error output
- Testbus(15:0)

Standard capture mode – The capture buffers can be armed to collect the 4K complex samples after a programmable delay following a sync event.

Smart capture mode (SCB) – There are two trigger conditions that combine the number of samples greater than a threshold; these are used to find a number of peak events while the transmit signal is above a threshold. In this case, the magnitude and magnitude squared of the signal are compared against a threshold and counted. If the capture buffer finds the trigger condition, the capture logic captures the programmed capture-buffer depth after the trigger. This is a combination of DSP software and the GC5322 hardware.

NOTE

Capture buffer A has a special mode to source data for diagnostic testing.

The DSP host interface software has a function to select and get capture-buffer data. The complex data is passed from the GC5322 to the EMIF bus, to the DSP, and back to the host processor.

The DSP host software has a signal power monitoring function. This uses the capture-buffer data to perform special monitoring, power measurement, and error measurements.

NOTE

There are special DSP software PA protection modes that use the capture buffer to determine the DPD correction applied to the signal, the error between the DPD reference input and the feedback signal. The capture buffers are also used in the initial bulk delay and fractional delay alignment.

Input Syncs and Output Sync

The GC5322 features multiple user-programmable input syncs. There are three syncs sampled with the BBClock, (A, B, C), and the sync D, DC as an LVDS sync is sampled by the DPD clock. Internally, the GC5322 can also generate timed and software-controlled syncs. The sync A input is required for the GC5322 hardware to initialize. It should ideally be the start of the frame or frame down link. The output sync is a test signal used for debugging.

The input syncs can be used to trigger:

- Power measurements
- DUC channel delay, dither, and tuner alignment
- Initializing/loading the DUC,, feedback, equalizer, LUTs, etc.
- Feedback path tuner alignment
- Capturing and sourcing of data through SCBs

NOTE

The Sync A external synchronization should match the customer TX frame (total TX period – i.e., 5 ms). See Figure 3; these synchronization signals must meet the timing of the BBClk. Sync A should be aligned with the BBFR signal.

Power Meters and Peak I-or-Q Monitors

There are three integrated $I^2 + Q^2$ power meters in the GC5322:

- GPP – each baseband input channel
- CFR – the CFR input or output, and which antenna stream (0, 1)
- DPD – the input to the DPD nonlinear correction after the DPDL gain, and which antenna stream (0, 1)

There are several peak I or Q monitors within the GC5322:

- FRW – The resampled combined IQ interleaved input to the DPD
- DPD – The input to the DPD nonlinear correction after the DPDL gain
- DPD – After the nonlinear correction in DPD, and separately after the linear correction in DPD
- FDBK – There is a peak monitor at the output of the feedback path.

NOTE

The DSP host software has a HW POWER meter setup and Get(Monitor) function to configure and get data from the integrated $I^2 + Q^2$ values.

PIN ASSIGNMENT AND DESCRIPTIONS

ZND Package
(Bottom View)

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	VSS1	VSS1	VSS1	VSS1	FB1	FB5	FB9	FB11	FB15	FB17	FB21	FB25	FB27	VDD SHV	FB31	FB35	VSSA2	SYNC C	BB15	BB11	BB7	BB3	BB0	VSS1	VSS1	VSS1
B	VDD1	VSS1	VSS1	VSS1	FB0	FB4	FB8	FB10	FB14	FB16	FB20	FB24	FB26	VDD SHV	FB30	FB34	VDDA2	SYNC B	BBFR	BB12	BB8	BB4	BB1	VSS1	VSS1	VDD1
C	VSS1	VDD1	VSS1	VSS1	MFIO 0	FB3	FB7	VDD1	FB13	ADC IREF	FB19	FB23	VDD1	VDD SHV	FB29	FB33	VDD1	SYNC A	BBCLK	BB13	BB9	BB5	BB2	VSS1	VDD1	VSS1
D	VSS1	VSS1	VDD1	VSS1	MFIO 1	FB2	FB6	VDD1	FB12	ADC VREF	FB18	FB22	VDD1	VDD SHV	FB28	FB32	VSS1	SYNC OUT	VDD1	BB14	BB10	BB6	VSS1	VDD1	VSS1	VSS1
E	VSS1	VSS1	VSS1	VDD1																			VDD1	VSS1	VSS1	VSS1
F	VSS1	VSS1	VSS1	VDD1																			VDD1	VDD1	VSS1	VSS1
G	VSS1	VSS1	VSS1	VDD SHV																			VDD SHV	VSS1	VSS1	VSS1
H	MFIO 2	MFIO 3	VPP1	VDD1																			VDD1	UP ADDR2	UP ADDR1	UP ADDR0
J	VPP1	MFIO 4	MFIO 5	VDD1																			VDD1	UP ADDR5	UP ADDR4	UP ADDR3
K	MFIO 6	MFIO 7	VDD SHV	VDD1																			VDD1	UP ADDR8	UP ADDR7	UP ADDR6
L	MFIO 8	MFIO 9	MFIO 10	VDD1																			VDD1	VDD SHV	WRB	UP ADDR9
M	MFIO 11	MFIO 12	MFIO 13	VDD1																			VDD1	OEB	CEB	RDB
N	MFIO 14	MFIO 15	VDD SHV	VDD1																			VDD1	UP DATA2	UP DATA1	UP DATA0
P	MFIO 16	MFIO 17	MFIO 18	VDD1																			VDD1	VDD SHV	VSS1	VSS1
R	MFIO 19	MFIO 20	MFIO 21	VDD1																			VDD1	UP DATA5	UP DATA4	UP DATA3
T	MFIO 22	MFIO 23	MFIO 24	VDD1																			VDD1	VDD SHV	VPP2	UP DATA6
U	MFIO 25	MFIO 26	VDD SHV	VDD1																			VDD1	UP DATA8	UP DATA7	VPP2
V	MFIO 27	MFIO 28	MFIO 29	VDD1																			VDD1	UP DATA11	UP DATA10	UP DATA9
W	MFIO 30	MFIO 31	MFIO 32	VDD1																			VDD1	UP DATA14	UP DATA13	UP DATA12
Y	MFIO 33	VSS1	VSS1	VDD1																			VDD SHV	VSS1	VSS1	UP DATA15
AA	VSS1	VSS1	VSS1	VDD1																			VDD1	VSS1	VSS1	VSS1
AB	VSS1	VSS1	VSS1	VDD1																			VDD1	VDD1	VSS1	VSS1
AC	VSS1	VSS1	VDD1	RESET B	VDD SHV	DPD CLK	VSS1	VDD1	TX2	TX6	TX10	TX14	VDDS	VSS1	DAC REFP	TX25	TX29	TX33	TX37	VSS1	VDD1	VDD2	VSS1	VDD1	VSS1	VSS1
AD	VSS1	VDD1	VSS1	VSS1	DPD IREF	DPD CLKC	VSS1	VDDA1	TX3	TX7	TX11	TX15	VDDS	VSS1	DAC REFN	TX24	TX28	TX32	TX36	VDD SHV	VDD1	VSS2	VSS1	VSS1	VDD1	VSS1
AE	VDD1	VSS1	VSS1	VSS1	DPD VREF	SYNC D	VDD SHV	TX0	TX4	TX8	TX12	TX16	VDDS	TX19	TX21	TX23	TX27	TX31	TX35	TRSTB	TDI	INTER-RUPT	VSS1	VSS1	VSS1	VDD1
AF	VSS1	VSS1	VSS1	VSS1	VSS1	SYNC DC	VSSA1	TX1	TX5	TX9	TX13	TX17	VSS1	TX18	TX20	TX22	TX26	TX30	TX34	TMS	TCK	TDO	TEST MODE	VSS1	VSS1	VSS1

= Baseband Input
= Transmit Output
= Feedback Input
= Microprocessor Interface
= Miscellaneous
= Multi-Function Input/Output
= Power and Biasing
= JTAG Interface

P0077-01

PIN FUNCTIONS

PIN NAME	PIN NO.	I/O	DESCRIPTION
MICROPROCESSOR INTERFACE			
OEB	M3	I	Output enable
CEB	M2	I	Chip enable
RDB	M1	I	Read
WRB	L2	I	Write
UPADDR[9:0]	L1, K3, K2, K1, J3, J2, J1, H3, H2, H1	I	Microprocessor address
UPDATA[15:0]	Y1, W3, W2, W1, V3, V2, V1, U2, U1, T1, R3, R2, R1, N3, N2, N1	I/O	Microprocessor data
INTERRUPT	AE5	O	Microprocessor interrupt
POWER AND BIASING			
VDD1	B1, B26, C2, C10, C14, C19, C25, D3, D8, D14, D19, D24, E4, E23, F3, F4, F23, H4, H23, J4, J23, K4, K23, L4, L23, M4, M23, N4, N23, P4, P23, R4, R23, T4, T23, U4, U23, V4, V23, W4, W23, Y23, AA4, AA23, AB3, AB4, AB23, AC3, AC6, AC19, AC24, AD2, AD6, AD25, AE1, AE26	PWR	1.2-V supply
VSS1	A1, A2, A3, A23, A24, A25, A26, B2, B3, B23, B24, B25, C1, C3, C23, C24, C26, D1, D2, D4, D10, D23, D25, D26, E1, E2, E3, E24, E25, E26, F1, F2, F24, F25, F26, G1, G2, G3, G24, G25, G26, P1, P2, Y2, Y3, Y24, Y25, AA1, AA2, AA3, AA24, AA25, AA26, AB1, AB2, AB24, AB25, AB26, AC1, AC2, AC4, AC7, AC13, AC20, AC25, AC26, AD1, AD3, AD4, AD13, AD20, AD23, AD24, AD26, AE2, AE3, AE4, AE23, AE24, AE25, AF1, AF2, AF3, AF14, AF22, AF23, AF24, AF25, AF26	PWR	Ground
VDD2	AC5	NC	1.2-V monitor, no connect
VSS2	AD5	NC	GND monitor, no connect
VDDS	AC14, AD14, AE14	PWR	1.8-V supply
VDDSHV	A13, B13, C13, D13, G4, G23, K24, L3, N24, P3, T3, U24, Y4, AC22, AD7, AE20	PWR	3.3-V supply
VDDA1	AD19	PWR	1.2-V supply (requires filtering)
VSSA1	AF20	PWR	Ground (requires filtering)
VDDA2	B10	PWR	1.2-V supply (requires filtering)
VSSA2	A10	PWR	Ground (requires filtering)
VPP1	H24, J26	PWR	1.2-V supply
VPP2	T2, U1	PWR	1.2-V supply
DPDIREF	AD22	PWR	DPD bias, 1 kΩ to VSS
DPDVREF	AE22	PWR	DPD bias to VDD1
DACREFP	AC12	PWR	DAC bias, 50 Ω to VSS
DACREFN	AD12	PWR	DAC bias, 50 Ω to VDDS
ADCIREF	C17	PWR	ADC bias, 1 kΩ to VSS
ADCVREF	D17	PWR	ADC bias to VDD1
BASEBAND INPUT			
BB[15:0]	A8, D7, C7, B7, A7, D6, C6, B6, A6, D5, C5, B5, A5, C4, B4, A4	I	Baseband input signal
BBCLK	C8	I	Baseband input clock
BBFR	B8	I	Baseband frame for sample and channel timing
MFIO[19:18]	R26, P24	I	LSBs for 18-bit baseband input signal [-2, -1]
MISCELLANEOUS			
RESETB	AC23	I	Chip reset (active-low)
SYNCA	C9	I	Programmable general-purpose sync

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SYNCB	B9	I	Programmable general-purpose sync
SYNCC	A9	I	DPDI-purpose sync
SYNCD	AE21	I	Programmable general-purpose sync
SYNCDC	AF21	I	Complementary DPD-purpose sync
SYNCOUT	D9	O	Programmable general-purpose output sync
DPDCLK	AC21	I	Clock to DPD
DPDCLKC	AD21	I	Complementary clock to DPD
TESTMODE	AF4	I	Tie to ground
JTAG INTERFACE			
TCK	AF6	I	JTAG clock
TDI	AE6	I	JTAG data in
TDO	AF5	O	JTAG data out
TRSTB	AE7	I	JTAG reset (active-low); pull down if JTAG is not used.
TMS	AF7	I	JTAG mode select
SIGNALS (See mode selection guide for pin assignment)			
TX[37:0]	AC8, AD8, AE8, AF8, AC9, AD9, AE9, AF9, AC10, AD10, AE10, AF10, AC11, AD11, AE11, AF11, AE12, AF12, AE13, AF13, AF15, AE15, AD15, AC15, AF16, AE16, AD16, AC16, AF17, AE17, AD17, AC17, AF18, AE18, AD18, AC18, AF19, AE19	O	Transmit to DAC(s)
FB[35:0]	A11, B11, C11, D11, A12, B12, C12, D12, A14, B14, A15, B15, C15, D15, A16, B16, C16, D16, A17, B17, A18, B18, C18, D18, A19, B19, A20, B20, C20, D20, A21, B21, C21, D21, A22, B22	I	Feedback from ADC(s)
MFIO[33:0]	Y26, W24, W25, W26, V24, V25, V26, U25, U26, T24, T25, T26, R24, R25, R26, P24, P25, P26, N25, N26, M24, M25, M26, L24, L25, L26, K25, K26, J24, J25, H25, H26, D22, C22	I/O	MFIO

Special Power Supply Requirements for VDDA1, VSSA1, VDDA2, VSSA2

The two PLLs require a filtered supply. Each pair (VDDA1,VSSA1), (VDDA2,VSSA2) requires a separate filter. These can be generated by filtering the core digital supply (VDD1). A representative filter is shown in Figure 8. The filters should be located as close as reasonable to their respective pins (especially the bypass capacitors). The ferrite beads should be series 50R (similar to Murata P/N: BLM31P500SPT; Description: IND FB BLM31P500SPT 50R 1206). In particular, supply VDDA1 must be less than or equal to VDD1 when VDD1 is at the low end of the required range. The series resistor assures this condition is met.

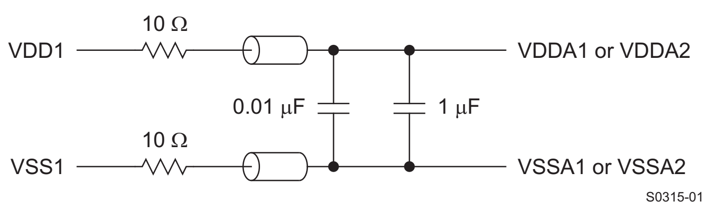


Figure 8. Recommended Filter for VDDA1, VDDA2 Power

TX Output to DAC5682Z and DAC5688

Figure 4 and Figure 5 show the GC5322-to-DAC data, sync, and clock signals. Table 2 and Table 4 list the specific GC5322-to-DAC TX connections.

Table 2. GC5322 TX Interface Options

PIN FUNCTION	PIN NAME	I/O	DESCRIPTION
GC5322 TX (Single-Channel Single-Ended HSTL – DAC5688 – 1.8-V CMOS)			
DACI[15:0]	TX15, TX14, TX11, TX10, TX7, TX6, TX3, TX2, TX1, TX0, TX4, TX5, TX8, TX9, TX12, TX13	O	DAC-I output
DACQ[15:0]	TX24, TX25, TX28, TX29, TX32, TX33, TX36, TX37, TX35, TX34, TX31, TX30, TX27, TX26, TX23, TX22	O	DAC-Q output
DACCLK	TX21	O	Clock to DAC
DACCLKC	TX20	O	Complementary clock to DAC
DACSYNC	TX18	O	Output data sync (TX enable)

Table 3. GC5322 TX (Single-Channel Differential HSTL – DAC5682Z)

PIN FUNCTION	PIN NAME	I/O	DESCRIPTION
GC5322 TX (Differential HSTL) – DAC 5682Z – 1.2-V LVDS			
DACI[15:0]P	TX10, TX6, TX2, TX0, TX4, TX8, TX12, TX16, TX23, TX27, TX31, TX35, TX32, TX36, TX29, TX25	O	DAC positive output
DACQ[15:0]N	TX11, TX7, TX3, TX1, TX5, TX9, TX13, TX17, TX22, TX26, TX30, TX34, TX33, TX37, TX28, TX24	O	DAC negative output
DACCLK	TX21	O	Clock to DAC
DACCLKC	TX20	O	Complementary clock to DAC
DACSYNCP	TX14	O	Positive output data sync
DACSYNCN	TX15	O	Negative output data sync

FB Input From LVDS ADC

There are several different ADC formats; these are formed from the possible combinations of DDR and SDR clocking modes with positive-clock-edge even bits and positive-clock-edge odd bits. Figure 6 shows the DDR-ADC data, and clock signals to the GC5322. Table 4 and Table 5 list the specific ADC to GC5322 FB connections. There are two feedback (FB) ports, A and B. Port A has faster timing and is preferred. There are several ADC styles:

- LVDS DDR – ADS5545 (ADS61x9, ADS5517); ADS5463 [(1)]
- LVDS DDR – ADS62C17 – reversed data alignment (same connections as ADS5545)
- LVDS SDR – ADS5544

(1) Clock aligns with data.

ADCs are typically connected to the GC5322 so the MSB of the ADC is connected to FB Port A MSB. The lower bit numbers follow until the ADC bits are all connected. Any remaining lower-order bits on the FB port should be terminated with a P connection to a series resistor to GND, N connection to a series resistor to 1.8 V as a logic 0. See the GC5325SEK schematic (reference 2 in the References section) for an example.

NOTE

There are special connections for shared-feedback ADCs between GC5322s. The *ADS6149 to GC5325 or GC5322 Shared Feedback Interface* application guide, available as a PDF file from a TI field application engineer, describes the special connections and routing.

Table 4. Single LVDS SDR ADC to FB Ports A and B

PIN FUNCTION	PIN NAME	I/O	DESCRIPTION
Feedback (Single-Channel SDR LVDS or DDR LVDS)			

Table 4. Single LVDS SDR ADC to FB Ports A and B (continued)

PIN FUNCTION	PIN NAME	I/O	DESCRIPTION
ADC[15:0]P	FB2, FB4, FB6, FB8, FB10, FB12, FB14, FB16, FB20, FB22, FB24, FB26, FB28, FB30, FB32, FB34	I	ADC positive feedback from PA output
ADC[15:0]N	FB3, FB5, FB7, FB9, FB11, FB13, FB15, FB17, FB21, FB23, FB25, FB27, FB29, FB31, FB33, FB35	I	ADC negative feedback from PA output
ADCCLK	FB0	I	Clock from ADC
ADCLKC	FB1	I	Complementary clock from ADC

Table 5. Single LVDS DDR ADC

PIN FUNCTION	PIN NAME	I/O	DESCRIPTION
To FB Port A (Preferred)			
ADCA[7:0]P	FB2, FB4, FB6, FB8, FB10, FB12, FB14, FB16	I	ADC-A positive feedback from PA output
ADCA[7:0]N	FB3, FB5, FB7, FB9, FB11, FB13, FB15, FB17	I	ADC-A negative feedback from PA output
ADCACLK	FB0	I	Clock from ADC-A
ADCACLKC	FB1	I	Complementary clock from ADC-A
To FB Port B			
ADCB[7:0]P	FB20, FB22, FB24, FB26, FB28, FB30, FB32, FB34	I	ADC-B positive feedback from PA output
ADCB[7:0]N	FB21, FB23, FB25, FB27, FB29, FB31, FB33, FB35	I	ADC-B negative feedback from PA output
ADCBCLK	FB18	I	Clock from ADC-B
ADCBCLKC	FB19	I	Complementary clock from ADC-B

Envelope Output

The GC5322 has a magnitude output and magnitude clock that can be delayed to align with the TX output after DPD. The envelope output is transmitted at the DPD clock rate / 2.

Table 6. Envelope Output

PIN FUNCTION	PIN NAME	I/O	DESCRIPTION
Envelope (Single-Ended 3.3-V CMOS)			
ENV[14:0]	MFIO33, MFIO32, MFIO28, MFIO27, MFIO26, MFIO25, MFIO17, MFIO16, MFIO15, MFIO14, MFIO9, MFIO8, MFIO7, MFIO6, MFIO3	O	Magnitude of the CFR output signal
ENVCLK	MFIO1	O	Clock to envelope modulator

MPU Interface Guidelines

This section describes the hardware interface between the recommended microprocessor and the GC5322. Users may select a microprocessor that meets their specific system requirements. Although the hardware can support multiple options, the recommended TMS320C6727 DSP is also fully supported with host control and adaptation software. Figure 7 and Figure 9 illustrate the hardware interface from the DSP to GC5322 and SDRAM. The external memory is required to accommodate the computational efforts of the adaptation algorithm. Reference to the SDRAM used is a 64-Mb/PC133; there are two memory devices for 32-bit SDRAM memory. The DSP timing is adjusted for the SDRAM; an example is Samsung K4S641632H-TC(L)75.

The use of an external inverter, with minimal propagation delay, is required for OEB of the GC5322; this device is necessary when using a TMS320C6727 DSP. Additional documentation for the hardware interface is available in the *Hardware Designer's Resource Guide* application report (SPRAA87) and *TMS320C672x DSP External Memory Interface (EMIF)* user's guide (SPRU711).

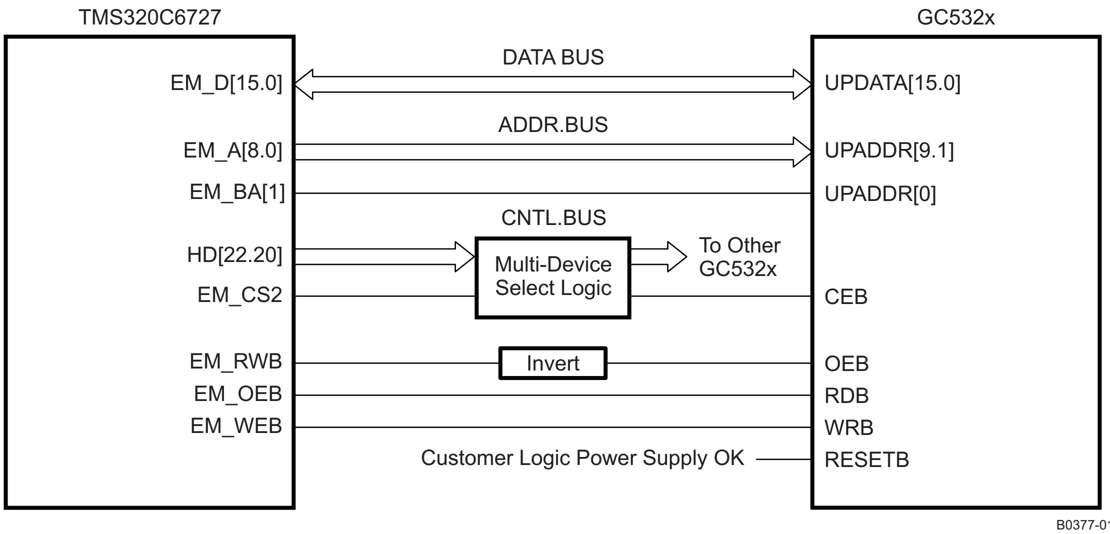


Figure 9. DSP to GC5322/SDRAM Interface Specifications

In a typical implementation, the system configuration software resides locally (in nonvolatile memory) to ensure proper operation at power up. The size of the software required to support the GC5322 and 'C6727 should be no more than 128 Mb (16 MB); however, this allocation is subject to change pending algorithm improvements. The suggested host-to-DSP interface is through the UHPI port. See reference 4 in the *References* section. The SDRAM used is a 64-Mb / PC133 SDRAM. There are two SDRAM devices for a 32-bit memory.

The port can be configured into multiple modes of data transfer; the *Multiplexed Host Address/Data Dual Halfword Mode* is suggested for this application.

Additional specifications and documents for the TMS320C6727 DSP are available from Texas Instruments at:

http://focus.ti.com/docs/prod/folders/print/tms320c6727b.html.

GENERAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

		VALUE	UNIT
V_{DD}, V_{DDA}	Core supply voltage	–0.3 to 1.32	V
V_{DDS}	Digital supply voltage for TX	–0.3 to 2	V
V_{DDSHV}	Digital supply voltage	–0.3 to 3.6	V
V_{IN}	Input voltage (under/overshoot)	–0.5 to V_{DDSHV}+ 0.5	V
	Clamp current for an input/output	–20 to 20	mA
T_{stg}	Storage temperature	–65 to 150	°C
	ESD classification Class 2 (Required 2-kV HBM, 500-V CDM) (Passed 2.5-kV HBM, 500-V CDM, 200-V MM)		
	Moisture sensitivity Class 3 (floor life at 30°C/60% H)	1	week
Latchup	JEDEC Level 2 per JEDEC 78 standard (at 90°C and 1.5 × Vmax)	±100	mA

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{DD}, V_{DDA2}, V_{PP}	Core supply voltages. Note $V_{DDA2} \le V_{DD}$		1.14	1.2	1.26	V
V_{DDA1}	Analog supply for DPD PLL	See(1)	1	1.1	VDD	V
V_{DDS}	Digital supply voltage for TX		1.71	1.8	1.89	V
V_{DDSHV}	Digital supply voltage		3.15	3.3	3.45	V
I_{DD}, I_{DDA1}, I_{DDA2}, I_{PP}	Combined supply current for Vdd, Vdda1, Vdda2, and V_{PP}				3	A
I_{DDS}	Digital supply current for TX				0.25	A
I_{DDSHV}	Digital supply current				0.3	A
T_C	Case temperature	See(2)	–40	30	85	°C
T_J	Junction temperature	See(3)			105	°C

(1) VDDA1 must be less than VDD1 when VDD is low. See recommended filtering circuit in Figure 8. Maximum observed current on VDDA1 is 8 mA.
(2) Chip specifications are production tested to 90°C case temperature. QA tests are performed at 85°C.
(3) Thermal management may be required for full-rate operation. Sustained operation at elevated temperatures reduces long-term reliability. Lifetime calculations are based on a maximum junction temperature of 105°C.

THERMAL INFORMATION

THERMAL METRIC(1)		GC5322 ZND 352 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	19	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	0.8	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	9	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	8	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

GENERAL ELECTRICAL CHARACTERISTICS

Describes the electrical characteristics for the baseband interface, multifunction I/O (MFIO), DPD clock and fast sync, MPU and JTAG interfaces over recommended operating conditions. Device is production tested at 90°C for the given specification and characterized at –40°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS INTERFACE						
V_{IL}	CMOS voltage input, low				0.8	V
V_{IH}	CMOS voltage input, high		2		V_{DDSHV}	V
V_{OL}	CMOS voltage output, low	I_{OL} = 2 mA			0.5	V
V_{OH}	CMOS voltage output, high	I_{OH} = –2 mA	2.4		V_{DDSHV}	V
$\|I_{PU}\|$	Pullup current	V_{IN} = 0 V	40	100	200	µA
$\|I_{IN}\|$	Leakage current	V_{IN} = 0 or V_{IN} = V_{DDSHV}			5	µA
DAC INTERFACE (DACP/N[15:0])						
$V_{o(diff)}$	Output differential swing	$\| V_{OD} \| = \| V_{OH} – V_{OL} \|$ (1)	250			mV
V_{comm}	Common mode	$(V_{OH} + V_{OL}) / 2$ (1)	1000			mV
LVDS INTERFACE (FB[35:0], DPDCLK/C, SYNCD/C)						
V_I	Input voltage range		0		2000	mV
$V_{I(diff)}$	Input differential voltage, |Vpos – Vneg|	0 < V_i < 2000 mV	250			mV
		1000 mV < V_I < 1400 mV, FB[35:0] only	90			
R_{IN}	Input differential impedance		80		120	Ω
POWER SUPPLY						
I_{dyn}	Core current	See (2)			2.2	A

(1) HSTL output levels measured at 675 Mb/s delay and with 100-Ω load from P to N. Drive strength set to 0x360. Contact TI for operations above 675 Mb/s.

(2) Operating at 280 MHz core, TX 840 MHz, maximum filtering, nominal supplies

GENERAL SWITCHING CHARACTERISTICS

Describes the electrical characteristics for the baseband interface, MFIO[19:18], Sync A, B, C, and BB clock over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
BASEBAND INTERFACE					
$f_{CLK(BB)}$	Baseband input clock frequency	GPP is ACTIVE.	25	93.3	MHz
		GPP is BYPASSED.	25	140	
$t_{su(BB)}$	Input data setup time before BBCLK↑	BB[15:0], BBFR, SYNCA, SYNCB, and SYNCC; MFIO18/19	1.3		ns
$t_{h(BB)}$	Input data hold time after BBCLK↑	BB[15:0], BBFR, MFIO18/19	1.5		ns
$t_{h(SYNCA, -B, -C)}$	Input data hold time after BBCLK↑	SYNCA, SYNCB, and SYNCC	2		ns
$Duty_{CLK(BB)}$	Duty cycle		30%	70%	

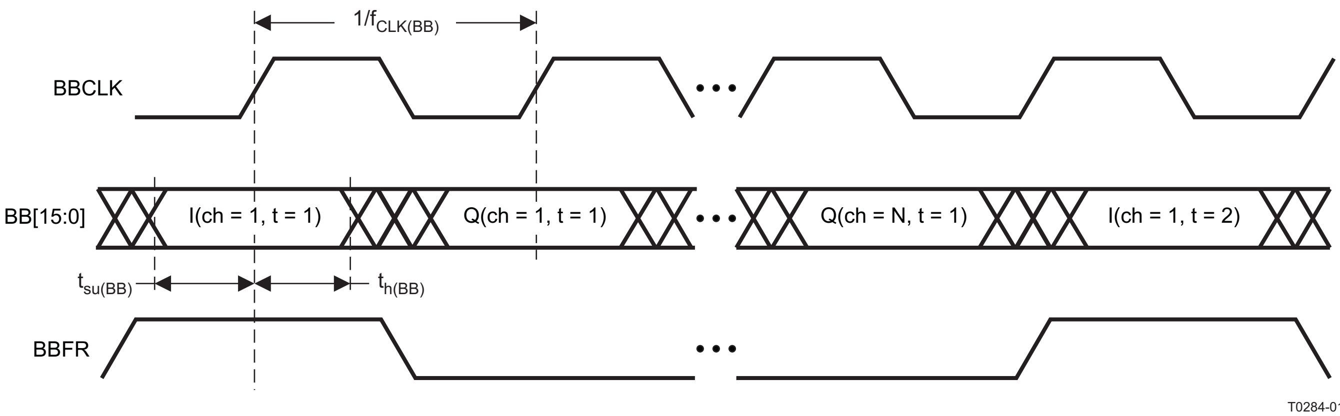


Figure 10. Baseband Timing Specifications (ex. Four Interleaved I/Q Channels)

DPD CLOCK AND FAST SYNC SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{CLK(DPD)}$	DPD input clock frequency		100	280	MHz
$Duty_{CLK(DPD)}$	DPD input clock duty cycle		30%	70%	
$t_{h(SYNCD)}$	Input hold time after DPDCLK↑		0.2		ns
$t_{su(SYNCD)}$	Input setup time after DPDCLK↑		0.4		ns
$t_{h(SYNCA, -B, -C)}$	Input hold time after DPDCLK↑		2		ns
$t_{su(SYNCA, -B, -C)}$	Input setup time after DPDCLK↑		0.4		ns
$t_{jCLK(DPD)}$	DPD output clock cycle-to-cycle jitter		–2.5%	2.5%	

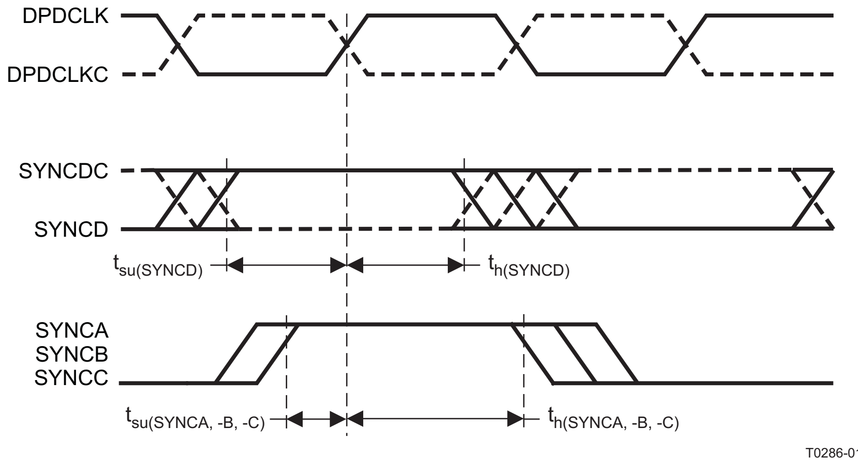


Figure 11. DPD Clock and Fast Sync Timing Specifications

MPU SWITCHING CHARACTERISTICS (READ)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{su(AD)}$	ADDR setup time to RDB↓	WRB is HIGH.	5		ns
$t_{su(CEB)}$	CEB setup time to RDB↓	WRB is HIGH.	7		ns
$t_{su(OEB)}$	OEB setup time to RDB↓	WRB is HIGH.	2		ns
$t_{d(RD)}$	DATA valid time after RDB↓	WRB is HIGH.		14	ns
$t_{h(RD)}$	ADDR hold time to RDB↑	WRB is HIGH.	2		ns
	OEB, CEB hold time to RDB↑		0		
$t_{HIGH(RD)}$	Time RDB must remain HIGH between READs.	WRB is HIGH[(1)].	7		ns
$t_{Z(RD)}$	DATA goes high-impedance after OEB↑ or RDB↑.	WRB is HIGH[(1)].		7	ns

(1) These values are obtained from testing during characterization.

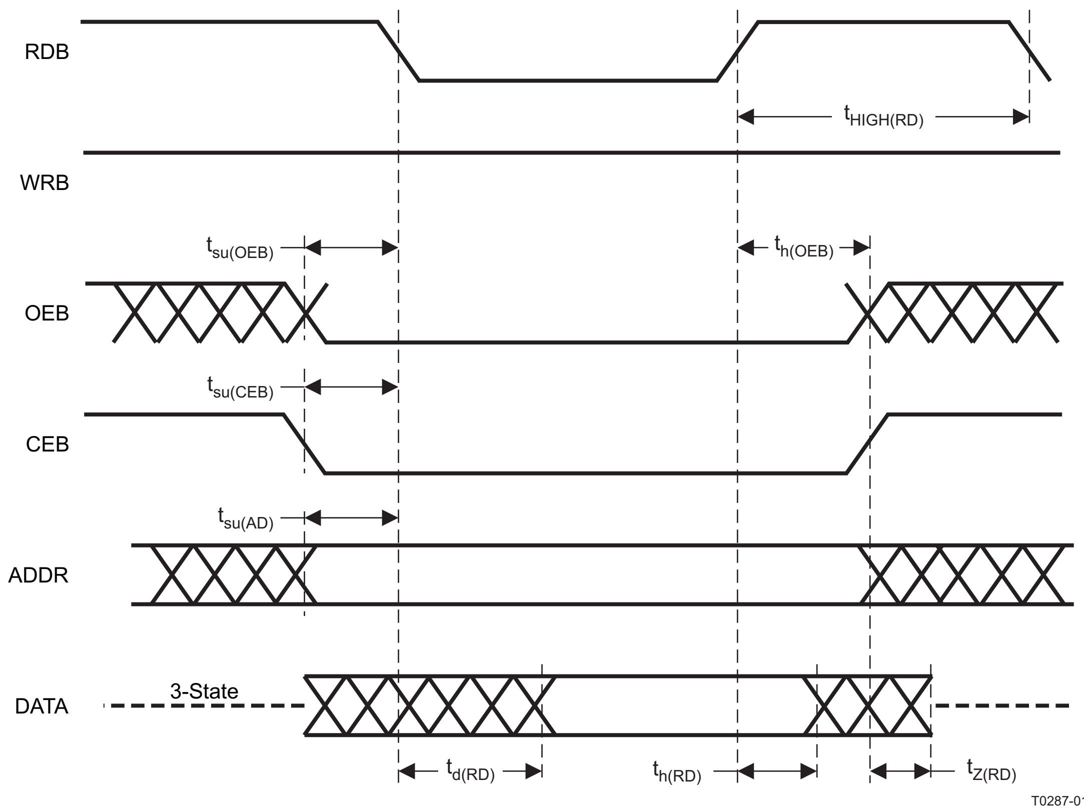


Figure 12. MPU READ Timing Specifications

MPU SWITCHING CHARACTERISTICS (WRITE)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{su(WR)}$	DATA and ADDR setup time to WRB↓	OEB and RDB are HIGH.	5		ns
	CEB setup time to WRB↓		7		
	OEB setup time to WRB↓		2		
$t_{h(WR)}$	DATA and ADDR hold time after WRB↑	OEB and RDB are HIGH.	2		ns
	OEB and CEB hold time after WRB↑		0		
$t_{low(WR)}$	Time WRB and CEB must remain simultaneously LOW	OEB and RDB are HIGH.	15		ns
$t_{high(WR)}$	Time CEB or WRB must remain HIGH between WRITEs.	OEB and RDB are HIGH.	10		ns

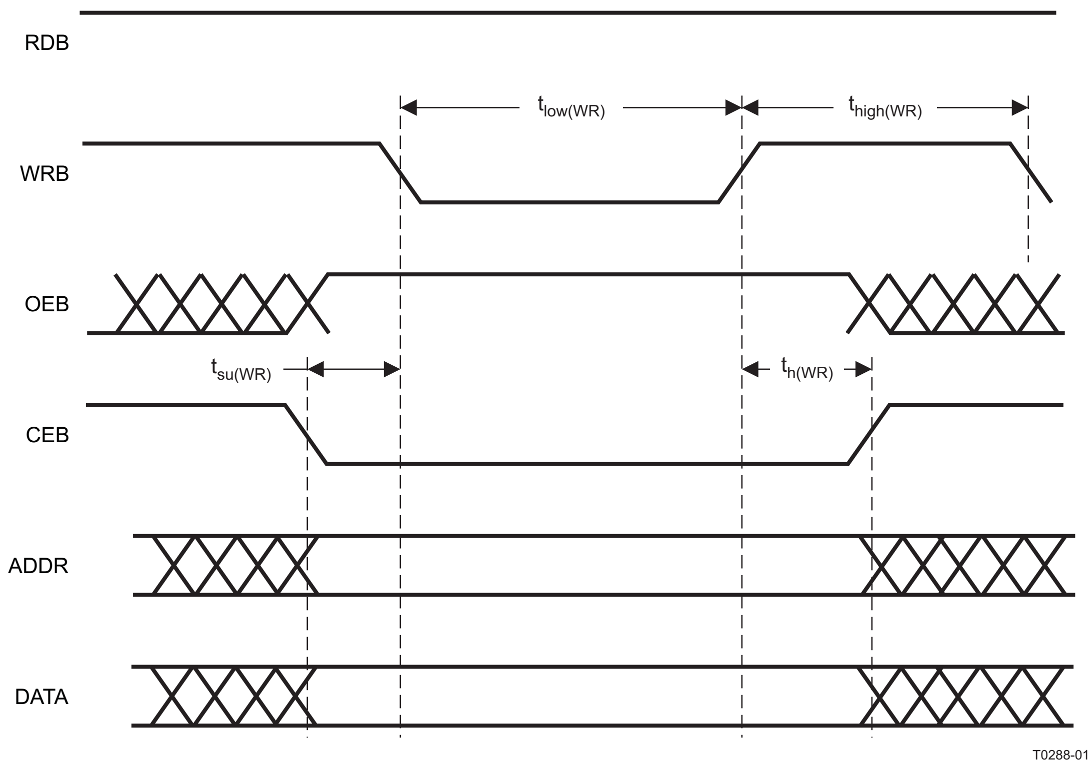


Figure 13. MPU WRITE Timing Specifications

JTAG SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{TCK}	JTAG clock frequency			50	MHz
$t_{p(TCKL)}$	JTAG clock low period		10		ns
$t_{p(TCKH)}$	JTAG clock high period		10		ns
$t_{su(TDI)}$	Input data setup time before TCK↑	Valid for TDI and TMS	1		ns
$t_{h(TDI)}$	Input data hold time after TCK↑	Valid for TDI and TMS	6		ns
$t_{d(TDO)}$	Output data delay from TCK↓			8	ns

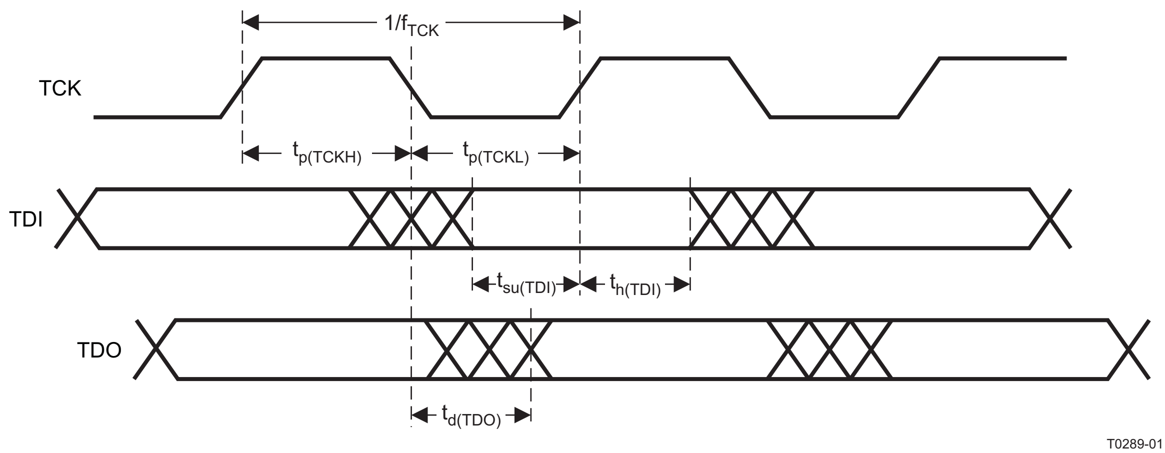


Figure 14. JTAG Timing Specifications

DIFFERENTIAL HSTL SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HSTL MODE – DDR ex. DAC5682						
$f_{CLK(DAC)}$	DAC output clock frequency	R_L= 100 Ω (1)			420	MHz
$t_{SKW(DAC)}$	DACCLK to DACData	R_L= 100 Ω			TBD	ps

(1) DDR interface; DAC clock is 1/2 DAC data rate.

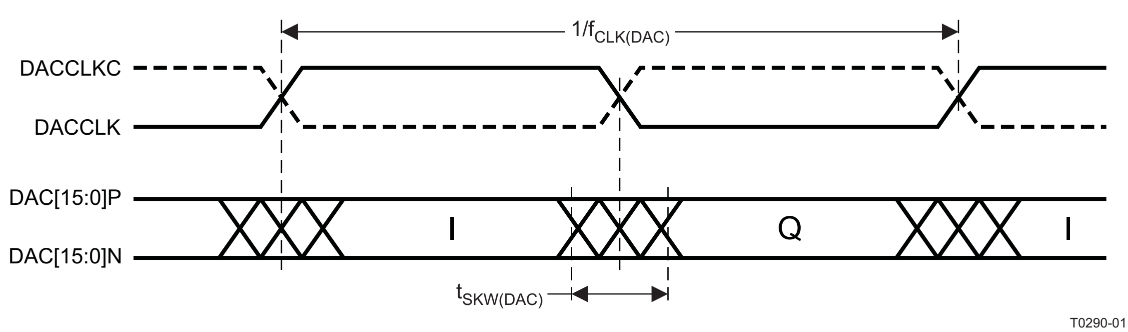


Figure 15. TX Timing Specifications (HSTL – DDR)

SINGLE-ENDED HSTL SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HSTL MODE – SDR ex. DAC5688						
$f_{CLK(DAC)}$	DAC output clock frequency	2-mA load (1)			200	MHz
t_d	DACCLK-to-DACData delay time	2-mA load (2)			1.5	ns
t_{ho}	DACCLK-to-DACData hold time	2-mA load (2)	1.5			ns

(1) Because the output clock is SDR, the positive edge of the clock is used to register the data at the DAC receiver. The clock rate is limited to 200 MHz.
(2) t_d and t_{ho} clock-to-data is measured during characterization.

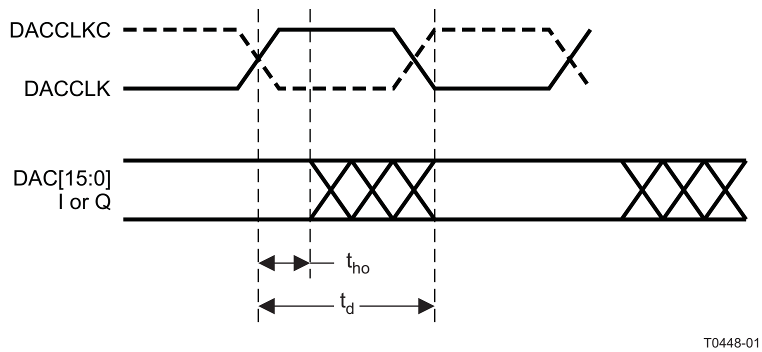


Figure 16. TX Timing Specifications (HSTL – SDR)

ENVELOPE SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MFIO CMOS – SDR to Envelope Modulator						
$f_{CLK(ENV)}$	ENVELOPE data output clock frequency	2-mA load (1)			140	MHz
t_d	ENVCLK-to-ENVData delay time	2-mA load (2)			1.5	ns
t_{ho}	ENVCLK-to-ENVData hold time	2-mA load (2)	1.5			ns

(1) Envelope output is magnitude; this is a real output at a DPDClk/2 (140-MHz) rate.
(2) t_d and t_{ho} clock-to-data is measured during characterization.

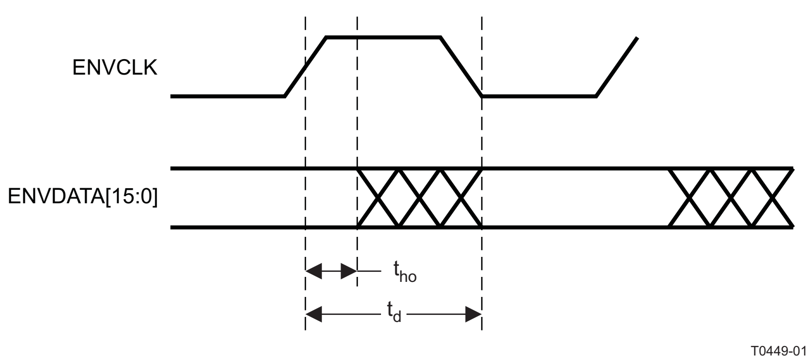


Figure 17. Envelope Timing (MFIO-CMOS 3.3 V)

LVDS SWITCHING CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted). The following table uses a shorthand nomenclature, NxM. N means the number of differential pairs used to transmit data from one ADC and M means the number of bits sent serially down each LVDS pair. Thus, 8x2 means 8 LVDS pairs each containing 2 bits of information sent serially.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
16 × 1 SDR LVDS MODE ex. ADS5444						
$f_{CLK(ADC)}$	ADC interface clock frequency	See (1)			280	MHz
$t_{su(ADC[\#]P)}$	Input data setup time before CLK↑	See (1)(2)	300			ps
$t_{h(ADC[\#]P)}$	Input data hold time after CLK↑	See (1)(2)	600			ps
16 × 1 DDR LVDS MODE ex. ADS5463						
$f_{CLK(ADC)}$	ADC interface clock frequency	See (1)			140	MHz
$t_{su(ADC[\#]P)}$	Input data setup time before CLK↑↓	See (1)(2)	100			ps
$t_{h(ADC[\#]P)}$	Input data hold time after CLK↑↓	See (1)(2)	1200			ps
8 × 2 DDR LVDS MODE ex. ADS5545, ADS6149						
$f_{CLK(ADCA)}$	ADCA interface clock frequency	See (1)			280	MHz
$t_{su(ADCA[\#/2]P)}$	Input data setup time before CLK↑↓	See (1)(3). For port A	430			ps
$t_{h(ADCA[\#/2]P)}$	Input data hold time after CLK↑↓	See (1)(3). For port A	260			ps
$f_{CLK(ADCB)}$	ADCB interface clock frequency	See (1)			280	MHz
$t_{su(ADCB[\#/2]P)}$	Input data setup time before CLK↑↓	See (1)(4). For port B	800			ps
$t_{h(ADCB[\#/2]P)}$	Input data hold time after CLK↑↓	See (1)(4). For port B	400			ps

(1) Specifications are limited by GC5322 performance and may exceed the example ADC capabilities for the given interface.
(2) Setup and hold measured for ADC[15:0]P, ADC[15:0]N valid for (V_{OD} > 250 mV) to/from ADCCLK and ADCCLKC clock crossing (V_{OD} = 0).
(3) Setup and hold measured for ADCA[7:0]P, ADCA[7:0]N valid for (V_{OD} > 250 mV) to/from ADCACLK and ADCACLKC clock crossing (V_{OD} = 0).
(4) Setup and hold measured for ADCB[7:0]P, ADCB[7:0]N valid for (V_{OD} > 250 mV) to/from ADCBCLK and ADCBCLKC clock crossing (V_{OD} = 0).

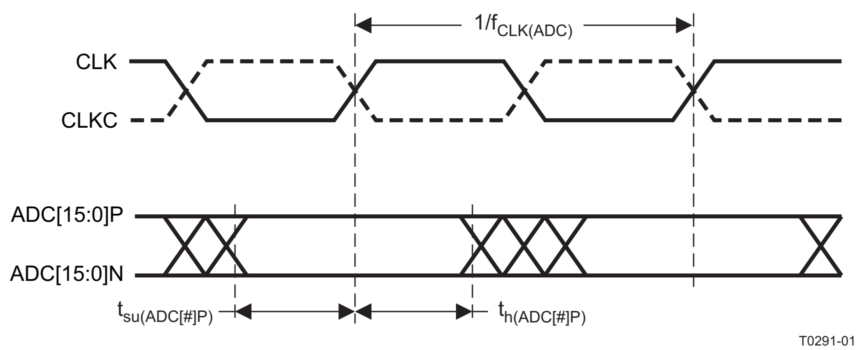


Figure 18. LVDS Timing Specifications (16 × 1 SDR LVDS)

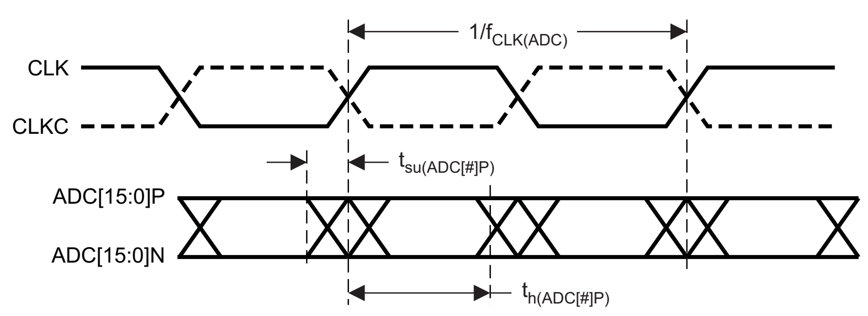


Figure 19. LVDS Timing Specifications (16 × 1 DDR LVDS)

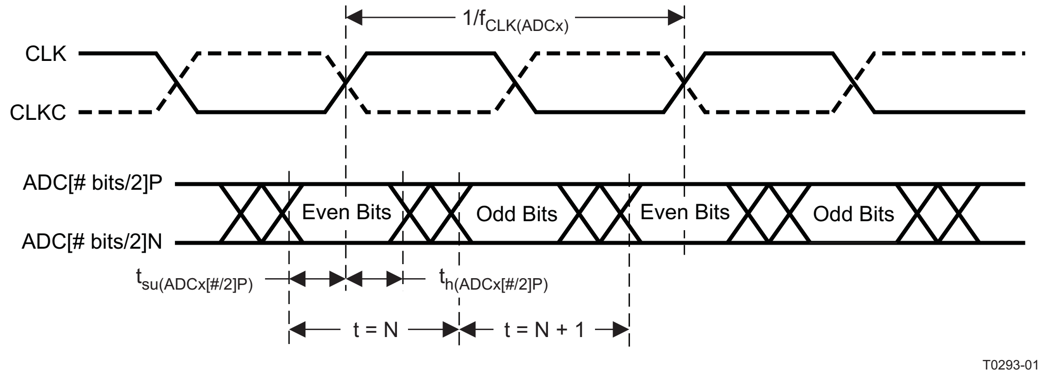


Figure 20. LVDS Timing Specifications (8 × 2 DDR LVDS)

GLOSSARY OF TERMS

3G	Third generation (refers to next-generation wideband cellular systems that use CDMA)
3GPP	Third generation partnership project (W-CDMA specification,www.3gpp.org)
3GPP2	Third generation partnership project 2 (cdma2000 specification,www.3gpp2.org)
ACLR	Adjacent channel leakage ratio (measure of out-of-band energy from one CDMA carrier)
ACPR	Adjacent channel power ratio
ADC	Analog-to-digital converter
BW	Bandwidth
CCDF	Complementary cumulative distribution function
CDMA	Code division multiple access (spread spectrum)
CEVM	Composite error vector magnitude
CFR	Crest factor reduction
CMOS	Complementary metal oxide semiconductor
DAC	Digital-to-analog converter
dB	Decibels
dBm	Decibels relative to 1 mW (30 dBm = 1 W)
DDR	Dual data rate (ADC output format)
DSP	Digital signal processing or digital signal processor
DUC	Digital upconverter (usually provides the GC5322 input)
EVM	Error vector magnitude
FIR	Finite impulse response (type of digital filter)
I/Q	In-phase and quadrature (signal representation)
IF	Intermediate frequency
IIR	Infinite impulse response (type of digital filter)
JTAG	Joint Test Action Group (chip debug and test standard 1149.1)
LO	Local oscillator
LSB	Least-significant bit
Mb	Megabits (divide by 8 for megabytes MB)

MSB	Most-significant bit
MSPS	Megasamples per second (1×10^6 samples/s)
PA	Power amplifier
PAR	Peak-to-average ratio
PCDE	Peak code domain error
PDC	Peak detection and cancellation (stage)
PDF	Probability density function
RF	Radio frequency
RMS	Root mean square (method to quantify error)
SDR	Single data rate (ADC output format)
SEM	Spectrum emission mask
SNR	Signal-to-noise ratio (usually measured in dB or dBm)
UMTS	Universal mobile telephone service
W-CDMA	Wideband code division multiple access (synonymous with 3GPP)
WiBro	Wireless broadband (Korean initiative IEEE 802.16e)
WiMAX	Worldwide Interoperability of Microwave Access (IEEE 802.16e)

REVISION HISTORY

- Inserted new *Output Formatter and DAC Interface (OFMT)* section 8
- Removed last bullet from OFMT list 9
- Deleted *GC5322 to Dual DAC5688 (Interleaved IQ) Interface* illustration 9
- Replaced all text of *Feedback Path (FB)* section and added an illustration 10
- Changed section title from *Smart Capture Buffers (SCB)* section to *Capture Buffers (CB)* 11
- Deleted existing paragraph; inserted two new paragraphs and four notes 11
- Revised title and first paragraph of the *Input Syncs and Output Sync* section; deleted a bullet from the list, and added a note 12
- Changed title and replaced all text of *Power Meters and Peak I-or-Q Monitors* section 12
- Changed names of some pins in the pinout diagram 13
- Changed package from GND to ZND on pinout drawing 13
- Made changes to *Terminal Functions* table in the areas of UPDATA, VSS1, VDD2, VSS2, RESETB, SYNCD, SYNCDC, SYNCOUT, and MFIO 14
- Made changes to *Terminal Functions* table in the areas of UPDATA, VSS1, VDD2, VSS2, RESETB, SYNCD, SYNCDC, SYNCOUT, and MFIO 15
- Added title for *Special Power Supply Requirements for VDDA1, VSSA1, VDDA2, VSSA2* section 15
- Inserted one sentence in this paragraph and revised another 15
- Changed analog supply to filtered supply 15
- Changed caption of Figure 8 and moved figure to the end of the section 15
- Added title and introductory paragraph to *TX Output to DAC5682Z and DAC5688* section; major overhaul of Table 2 and Table 4 16
- Changed to new figure reference as a result of deleted illustration 16
- Deleted Single- or Dual-Channel DDR LVDS section of table 16
- Added new *FB Input From LVDS ADC* section 16
- Added new *Envelope Output* section 17
- Revised the MPU Interface Guidelines section 17
- Replaced Figure 9 graphic 18
- Deleted sentence: "The adaptation algorithm..." 18
- Deleted *Typical Baseband Interface* section 18
- Changed $f_{CLK(ENV)}$ MAX value to 140 MHz 26
- Changed the LVDS 16 × 1 DDR timing digram 27

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
GC5322IZND	NRND	BGA	ZND	352	40	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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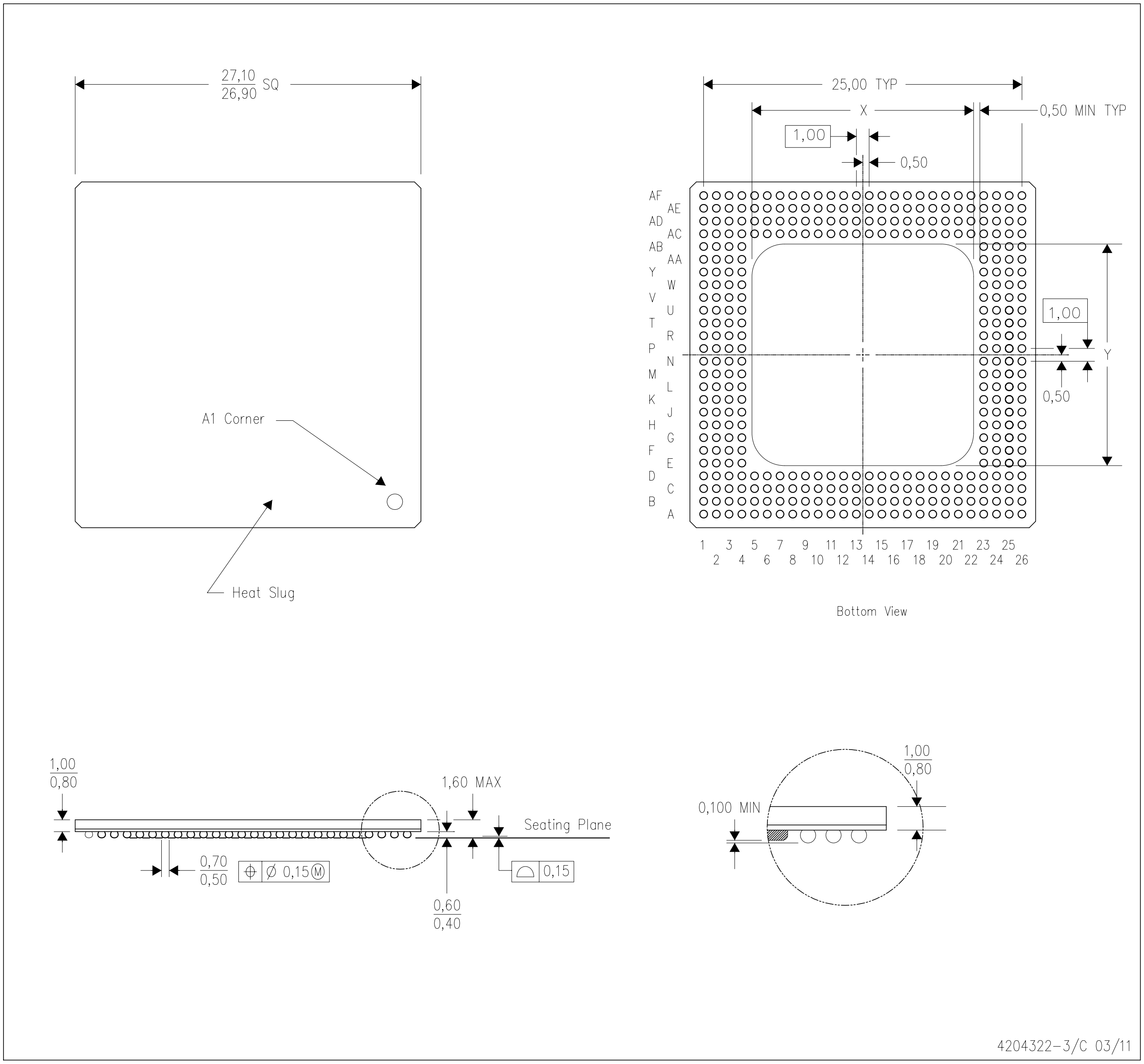
ZND (S-PBGA-N352) PLASTIC BALL GRID ARRAY (CAVITY DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Thermally enhanced plastic package with heat slug (HSL).
D. The encapsulation size (X,Y) will vary with cavity size. The distance from bond finger edge to encapsulation shall be min 0.5mm
E. This is a Pb-free solder ball design.

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