# Dual 1:4 Low Additive Jitter LVDS Buffer

Check for Samples: CDCLVD2104

## FEATURES

- Dual 1:4 Differential Buffer
- Low Additive Jitter <300 fs, RMS in 10 kHz to 20 MHz
- Low Within Bank Output Skew of 35ps (Max)
- Universal Inputs Accept LVDS, LVPECL, LVCMOS
- One Input Dedicated for Four Output Buffers
- 8 LVDS Outputs, ANSI EIA/TIA-644A Standard Compatible
- Clock Frequency up to 800 MHz
- 2.375–2.625V Device Power Supply
- LVDS Reference Voltage, $V_{AC\_REF}$, Available for Capacitive Coupled Inputs
- Industrial Temperature Range –40°C to 85°C
- Packaged in 5mm × 5mm 28-Pin QFN (RHD)
- ESD Protection Exceeds 3 kV HBM, 1 kV CDM

## APPLICATIONS

- Telecommunications/Networking
- Medical Imaging
- Test and Measurement Equipment
- Wireless Communications
- General Purpose Clocking

## DESCRIPTION

The CDCLVD2104 clock buffer distributes two clock inputs (IN0, IN1) to a total of 8 pairs of differential LVDS clock outputs (OUT0, OUT7). Each buffer block consists of one input and 4 LVDS outputs. The inputs can either be LVDS, LVPECL, or LVCMOS.

The CDCLVD2104 is specifically designed for driving 50-Ω transmission lines. If the input is in single ended mode, the appropriate bias voltage ($V_{AC\_REF}$) should be applied to the unused negative input pin.

Using the control pin (EN), outputs can be either disabled or enabled. If the EN pin is left open two buffers with all outputs are enabled, if switched to a logical "0" both buffers with all outputs are disabled (static logical "0"), if switched to a logical "1", one buffer with four outputs is disabled and another buffer with four outputs is enabled. The part supports a fail safe function. It incorporates an input hysteresis, which prevents random oscillation of the outputs in absence of an input signal.

The device operates in 2.5V supply environment and is characterized from –40°C to 85°C (ambient temperature). The CDCLVD2104 is packaged in small 28-pin, 5-mm × 5-mm QFN package.

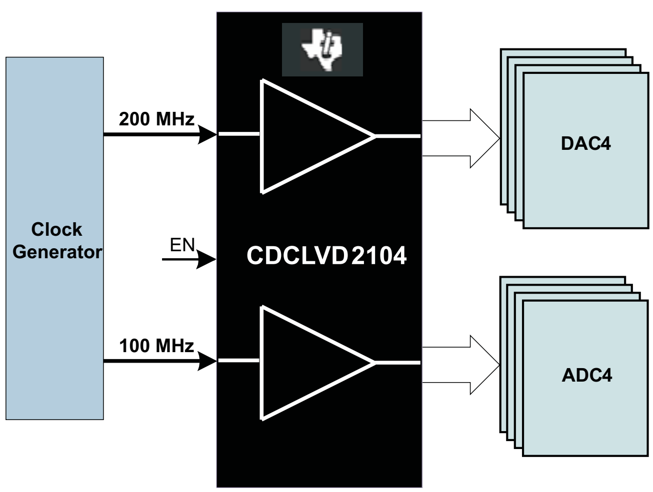



Figure 1. Application Example

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

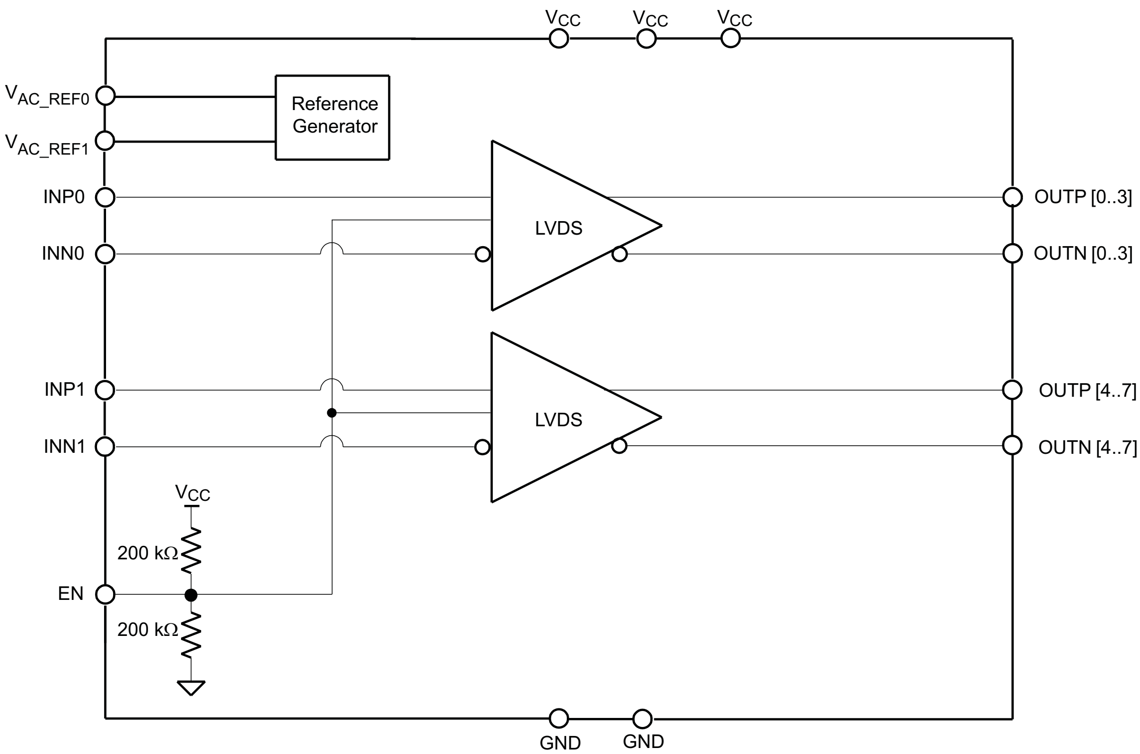
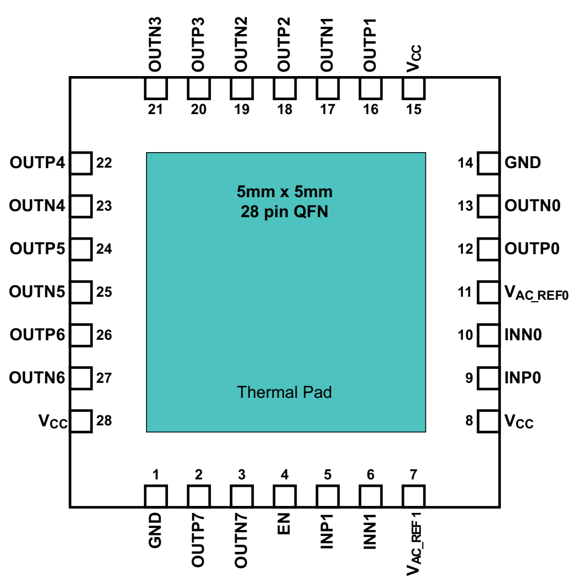



Figure 2. CDCLVD2104 Block Diagram



## PIN FUNCTIONS

| PIN | | TYPE | DESCRIPTION | |
|---|---|---|---|---|
| NAME | NO. | | | |
| VCC | 8,15,28 | Power | 2.5V supplies for the device | |
| GND | 1,14 | Ground | Device ground | |
| INP0, INN0 | 9,10 | Input | Differential input pair or single ended input | |
| INP1, INN1 | 5,6 | Input | Differential redundant input pair or single ended input | |
| OUTP0, OUTN0 | 12,13 | Output | Differential LVDS output pair no. 0 | INP0/INN0 is the input |
| OUTP1, OUTN1 | 16,17 | Output | Differential LVDS output pair no. 1 | |
| OUTP2, OUTN2 | 18,19 | Output | Differential LVDS output pair no. 2 | |
| OUTP3, OUTN3 | 20,21 | Output | Differential LVDS output pair no. 3 | |
| OUTP4, OUTN4 | 22,23 | Output | Differential LVDS output pair no. 4 | INP1/INN1 is the input |
| OUTP5, OUTN5 | 24,25 | Output | Differential LVDS output pair no. 5 | |
| OUTP6, OUTN6 | 26,27 | Output | Differential LVDS output pair no. 6 | |
| OUTP7, OUTN7 | 2,3 | Output | Differential LVDS output pair no. 7 | |
| $V_{AC\_REF0}$ | 11 | Output | Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1µF to GND on this pin. | |
| $V_{AC\_REF1}$ | 7 | Output | Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1µF to GND on this pin. | |
| EN | 4 | Input with an internal 200kΩ pull-up and pull-down | Control pin – enables or disables the outputs, (See Table 1) | |
| Thermal Pad | | | See thermal management recommendations | |

### Table 1. Output Control Table

| EN | CLOCK OUTPUTS |
|---|---|
| 0 | All outputs disabled (static "0") |
| OPEN | All outputs enabled |
| 1 | OUT0, OUT3 enabled and OUT4, OUT7 disabled (static "0") |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | VALUE / UNIT |
|---|---|---|
| $V_{CC}$ | Supply voltage range | –0.3 to 2.8 V |
| $V_I$ | Input voltage range | –0.2 to ($V_{CC}$ + 0.2) V |
| $V_O$ | Output voltage range | –0.2 to ($V_{CC}$ + 0.2) V |
| $I_{OSD}$ | Driver short circuit current | See Note (2) |
| ESD | Electrostatic discharge (HBM, 1.5 kΩ, 100 pF) | >3000 V |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) The outputs can handle permanent short.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{CC}$ | Device supply voltage | 2.375 | 2.5 | 2.625 | V |
| $T_A$ | Ambient temperature | -40 | | 85 | °C |

## THERMAL INFORMATION

| THERMAL METRIC(1) | | CDCLVD2104 QFN 28 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 34 | °C/W |
| $\theta_{JC(top)}$ | Junction-to-case(top) thermal resistance | 27 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 9 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 8 | |
| $\theta_{JC(bottom)}$ | Junction-to-case(bottom) thermal resistance | 4 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## ELECTRICAL CHARACTERISTICS

At $V_{CC}$ = 2.375 V to 2.625 V and $T_A$ = –40°C to 85°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **EN CONTROL INPUT CHARACTERISTICS** | | | | | | |
| $Vd_{I3}$ | 3-State | Open | | 0.5×$V_{CC}$ | | V |
| $Vd_{IH}$ | Input high voltage | | 0.7×$V_{CC}$ | | | V |
| $Vd_{IL}$ | Input low voltage | | | | 0.2×$V_{CC}$ | V |
| $Id_{IH}$ | Input high current | $V_{CC}$ = 2.625 V, $V_{IH}$ = 2.625 V | | | 30 | μA |
| $Id_{IL}$ | Input low current | $V_{CC}$ = 2.625 V, $V_{IL}$ = 0 V | | | –30 | μA |
| $R_{pull(EN)}$ | Input pull-up/ pull-down resistor | | | 200 | | kΩ |
| **2.5V LVCMOS (see Figure 7) INPUT CHARACTERISTICS** | | | | | | |
| $f_{IN}$ | Input frequency | | | | 200 | MHz |
| $V_{th}$ | Input threshold voltage | External threshold voltage applied to complementary input | 1.1 | | 1.5 | V |
| $V_{IH}$ | Input high voltage | | $V_{th}$ + 0.1 | | $V_{CC}$ | V |
| $V_{IL}$ | Input low voltage | | 0 | | $V_{th}$ – 0.1 | V |
| $I_{IH}$ | Input high current | $V_{CC}$ = 2.625 V, $V_{IH}$ = 2.625 V | | | 10 | μA |
| $I_{IL}$ | Input low current | $V_{CC}$ = 2.625 V, $V_{IL}$ = 0 V | | | –10 | μA |
| ΔV/ΔT | Input edge rate | 20% – 80% | 1.5 | | | V/ns |
| $C_{IN}$ | Input capacitance | | | 2.5 | | pF |
| **DIFFERENTIAL INPUT CHARACTERISTICS** | | | | | | |
| $f_{IN}$ | Input frequency | Clock input | | | 800 | MHz |
| $V_{IN, DIFF}$ | Differential input voltage peak-to-peak | $V_{ICM}$ = 1.25 V | 0.3 | | 1.6 | $V_{PP}$ |
| $V_{ICM}$ | Input common-mode voltage range | $V_{IN, DIFF, PP}$ > 0.4V | 1 | | $V_{CC}$ – 0.3 | V |
| $I_{IH}$ | Input high current | $V_{CC}$ = 2.625 V, $V_{IH}$ = 2.625 V | | | 10 | μA |
| $I_{IL}$ | Input low current | $V_{CC}$ = 2.625 V, $V_{IL}$ = 0 V | | | –10 | μA |
| ΔV/ΔT | Input edge rate | 20% to 80% | 0.75 | | | V/ns |
| $C_{IN}$ | Input capacitance | | | 2.5 | | pF |

## ELECTRICAL CHARACTERISTICS (continued)

At $V_{CC}$ = 2.375 V to 2.625 V and $T_A$ = –40°C to 85°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LVDS OUTPUT CHARACTERISTICS** | | | | | | |
| $\|V_{OD}\|$ | Differential output voltage magnitude | $V_{IN,\ DIFF,\ PP}$ = 0.3 V, $R_L$ = 100 Ω | 250 | | 450 | mV |
| $\Delta V_{OD}$ | Change in differential output voltage magnitude | | –15 | | 15 | mV |
| $V_{OC(SS)}$ | Steady-state common mode output voltage | | 1.1 | | 1.375 | V |
| $\Delta V_{OC(SS)}$ | Steady-state common mode output voltage | $V_{IN,\ DIFF,\ PP}$ = 0.6 V, $R_L$ = 100 Ω | –15 | | 15 | mV |
| $V_{ring}$ | Output overshoot and undershoot | Percentage of output amplitude $V_{OD}$ | | | 10% | |
| $V_{OS}$ | Output ac common mode | $V_{IN,\ DIFF,\ PP}$ = 0.6 V, $R_L$ = 100 Ω | | 40 | 70 | $mV_{PP}$ |
| $I_{OS}$ | Short-circuit output current | $V_{OD}$ = 0 V | | | ±24 | mA |
| $t_{PD}$ | Propagation delay | $V_{IN,\ DIFF,\ PP}$ = 0.3 V | | 1.5 | 2.5 | ns |
| $t_{SK,\ PP}$ | Part-to-part skew | | | | 600 | ps |
| $t_{SK,\ O\_WB}$ | Within bank output skew | | | | 35 | ps |
| $t_{SK,O\_BB}$ | Bank-to-bank output skew | both inputs are phase aligned | | | 100 | ps |
| $t_{SK,P}$ | Pulse skew(with 50% duty cycle input) | Crossing-point-to-crossing-point distortion | –50 | | 50 | ps |
| $t_{RJIT}$ | Random additive jitter (with 50% duty cycle input) | Edge speed 0.75V/ns<br>10 kHz – 20 MHz | | | 0.3 | ps, RMS |
| $t_R/t_F$ | Output rise/fall time | 20% to 80%,100 Ω, 5 pF | 50 | | 300 | ps |
| $I_{CCSTAT}$ | Static supply current | Outputs unterminated, f = 0 Hz | | 27 | 45 | mA |
| $I_{CC100}$ | Supply current | All outputs, $R_L$ = 100 Ω,<br>f = 100 MHz | | 74 | 108 | mA |
| $I_{CC800}$ | Supply current | All outputs, $R_L$ = 100 Ω,<br>f = 800 MHz | | 108 | 144 | mA |
| **$V_{AC\_REF}$ CHARACTERISTICS** | | | | | | |
| $V_{AC\_REF}$ | Reference output voltage | $V_{CC}$ = 2.5 V, $I_{load}$ = 100 µA | 1.1 | 1.25 | 1.35 | V |

## Typical Additive Phase Noise Characteristics for 100 MHz Clock

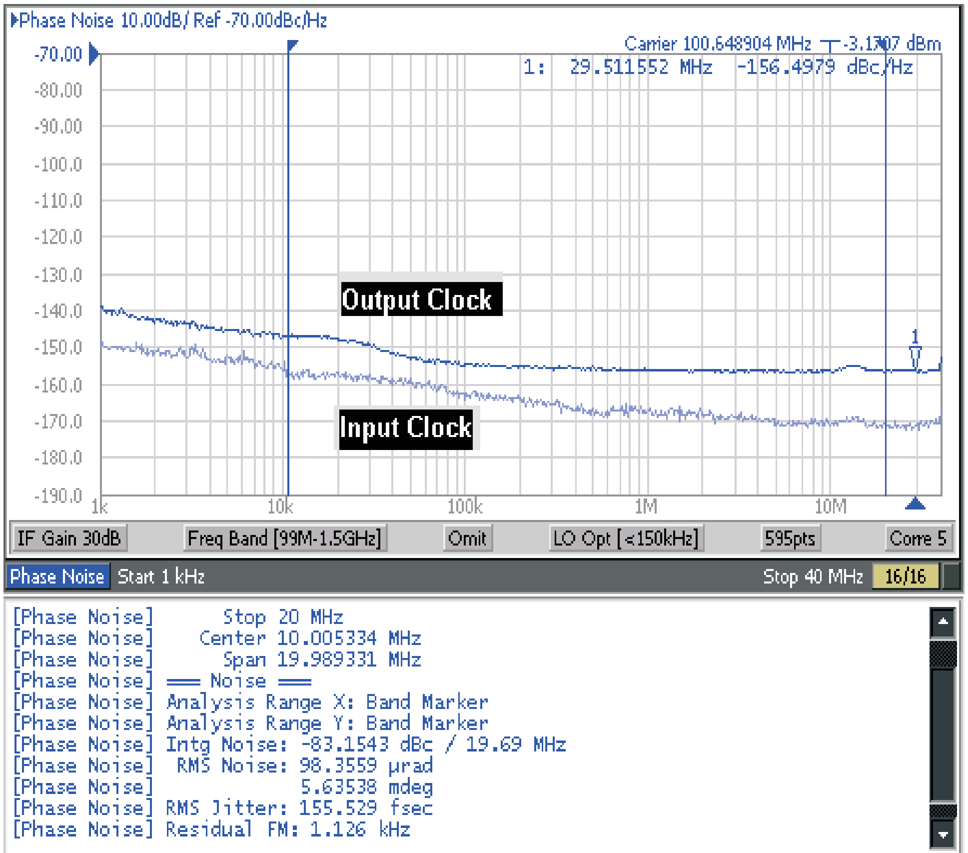
| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $phn_{100}$ | Phase noise at 100 Hz offset | | -132.9 | | dBc/Hz |
| $phn_{1k}$ | Phase noise at 1 kHz offset | | -138.8 | | dBc/Hz |
| $phn_{10k}$ | Phase noise at 10 kHz offset | | -147.4 | | dBc/Hz |
| $phn_{100k}$ | Phase noise at 100 kHz offset | | -153.6 | | dBc/Hz |
| $phn_{1M}$ | Phase noise at 1 MHz offset | | -155.2 | | dBc/Hz |
| $phn_{10M}$ | Phase noise at 10 MHz offset | | -156.2 | | dBc/Hz |
| $phn_{20M}$ | Phase noise at 20 MHz offset | | -156.6 | | dBc/Hz |
| $t_{RJIT}$ | Random additive jitter from 10 kHz to 20 MHz | | 171 | | fs, RMS |

## Typical Additive Phase Noise Characteristics for 737.27 MHz Clock

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $phn_{100}$ | Phase noise at 100 Hz offset | | -80.2 | | dBc/Hz |
| $phn_{1k}$ | Phase noise at 1 kHz offset | | -114.3 | | dBc/Hz |
| $phn_{10k}$ | Phase noise at 10 kHz offset | | -138 | | dBc/Hz |
| $phn_{100k}$ | Phase noise at 100 kHz offset | | -143.9 | | dBc/Hz |
| $phn_{1M}$ | Phase noise at 1 MHz offset | | -145.2 | | dBc/Hz |
| $phn_{10M}$ | Phase noise at 10 MHz offset | | -146.5 | | dBc/Hz |
| $phn_{20M}$ | Phase noise at 20 MHz offset | | -146.6 | | dBc/Hz |
| $t_{RJIT}$ | Random additive jitter from 10 kHz to 20 MHz | | 65 | | fs, RMS |

# TYPICAL CHARACTERISTICS

**INPUT CLOCK AND OUTPUT CLOCK PHASE NOISES**
**vs**
**FREQUENCY FROM THE CARRIER ($T_A$ = 25°C and $V_{CC}$ = 2.5V)**




Input clock RMS jitter is 32 fs from 10 kHz to 20 MHz and additive RMS jitter is 152 fs

**Figure 3. 100 MHz Input and Output Phase Noise Plot**

## TYPICAL CHARACTERISTICS (continued)

**Differential Output Voltage vs Frequency**

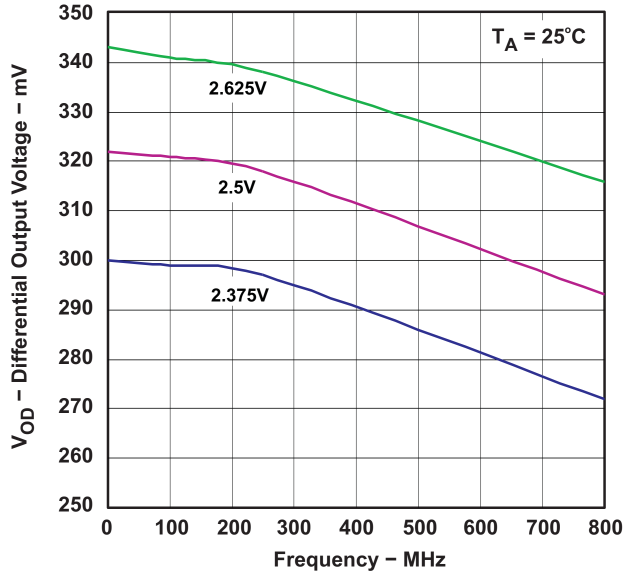



**Figure 4.**

## TEST CONFIGURATIONS

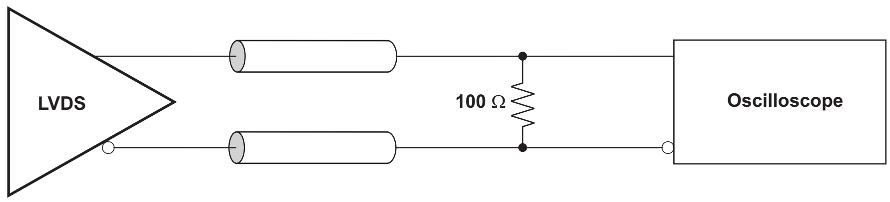



**Figure 5. LVDS Output DC Configuration During Device Test**

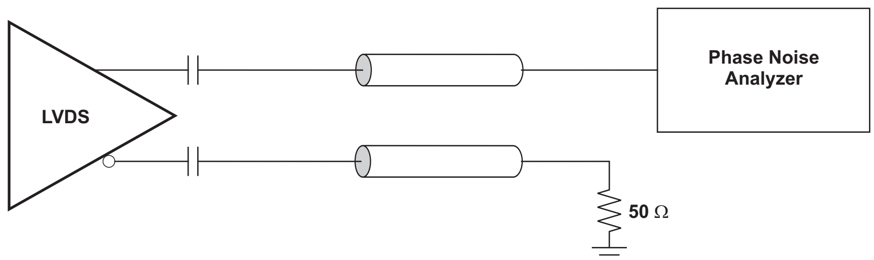



**Figure 6. LVDS Output AC Configuration During Device Test**

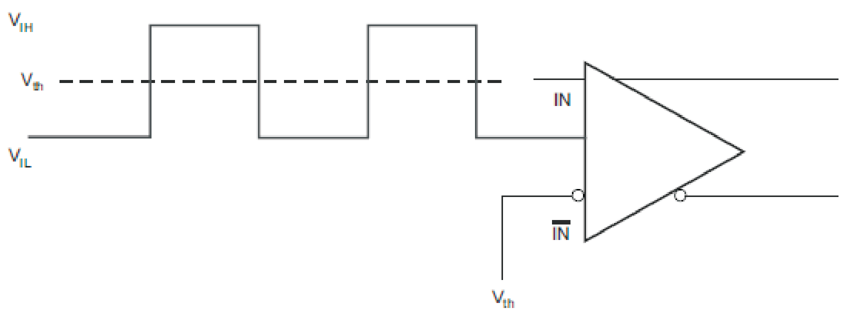



**Figure 7. DC Coupled LVCMOS Input During Device Test**

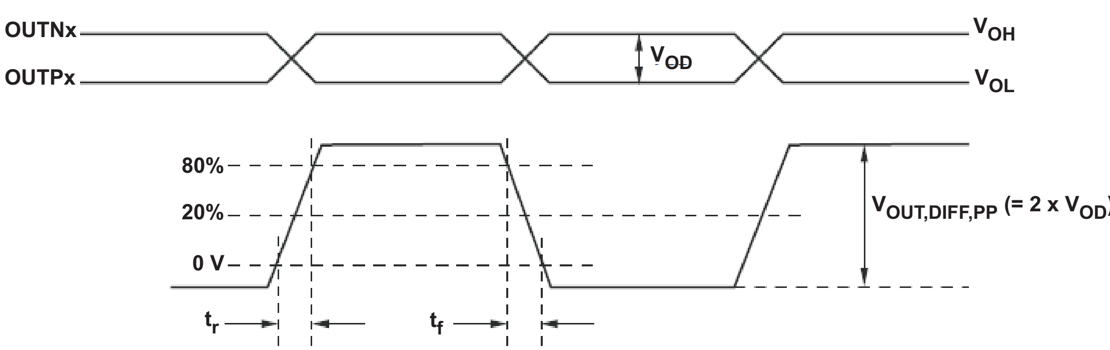
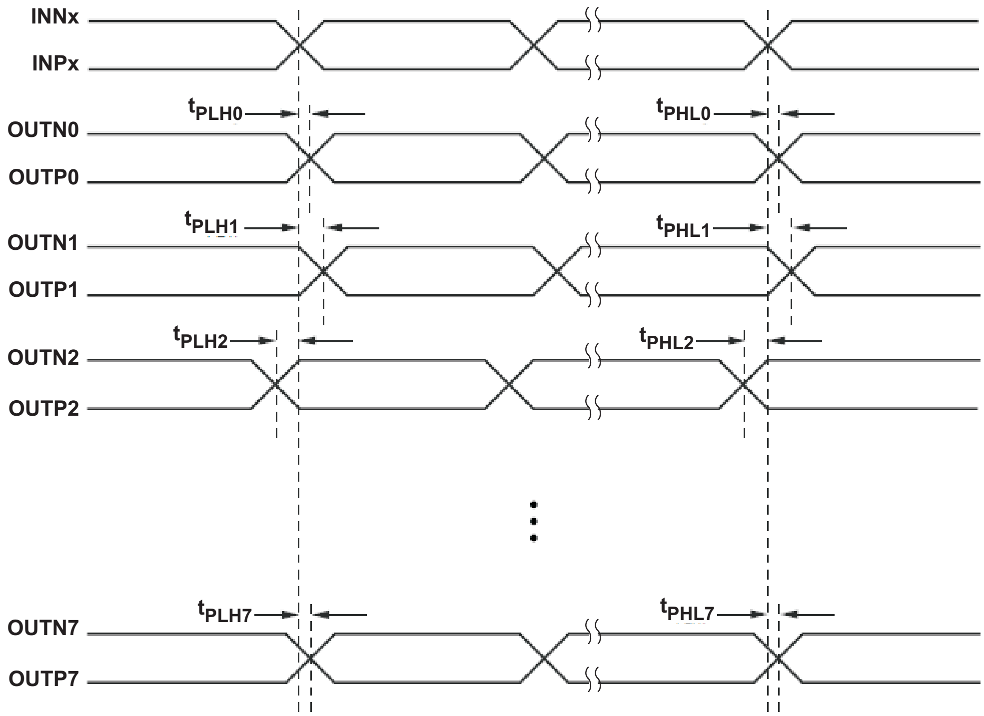



**Figure 8. Output Voltage and Rise/Fall Time**




A. Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest $t_{PLHn}$ or the difference between the fastest and the slowest $t_{PHLn}$ (n = 0, 1, 2, ..7).

B. Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest $t_{PLHn}$ or the difference between the fastest and the slowest $t_{PHLn}$ across multiple devices (n = 0, 1, 2, ..7).

C. Both inputs (IN0 and IN1) are phase aligned.

**Figure 9. Output Skew and Part-to-Part Skew**

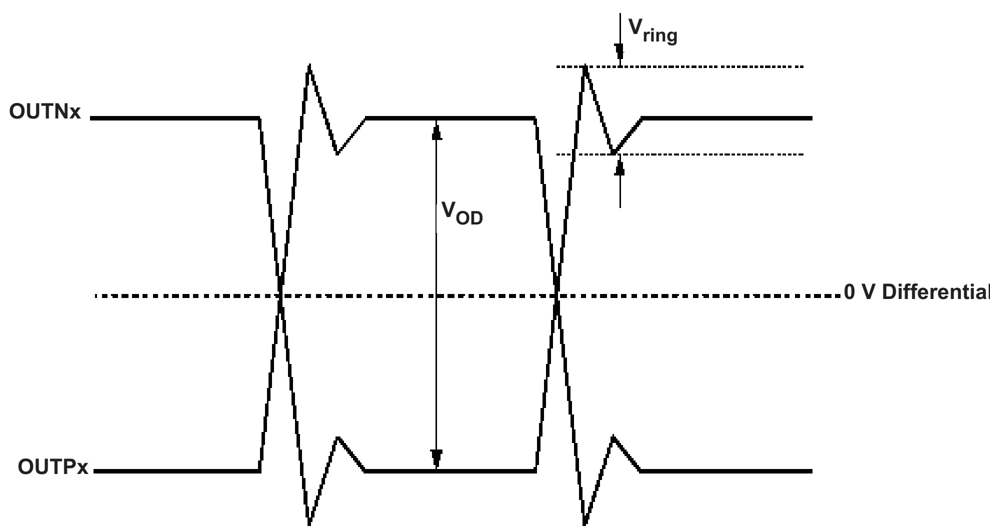



**Figure 10. Output Overshoot and Undershoot**

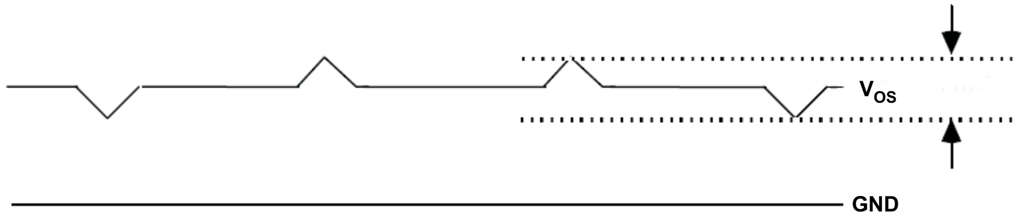



**Figure 11. Output AC Common Mode**

## APPLICATION INFORMATION

### THERMAL MANAGEMENT

For reliability and performance reasons, the die temperature should be limited to a maximum of 125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The Thermal Pad must be soldered down to ensure adequate heat conduction to of the package. Figure 12 shows a recommended land and via pattern.

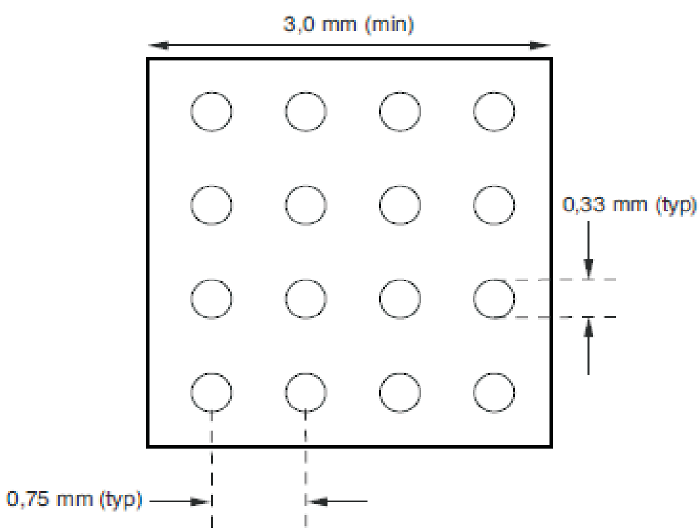



**Figure 12. Recommended PCB Layout**

### POWER-SUPPLY FILTERING

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply pins and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1 μF) bypass capacitors as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with very low dc resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

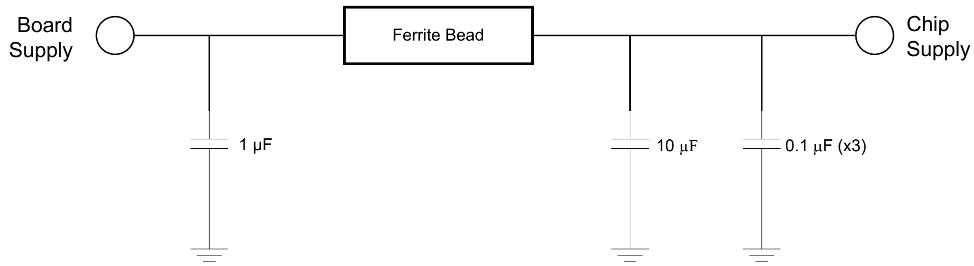



**Figure 13. Power-Supply Decoupling**

## LVDS OUTPUT TERMINATION

The proper LVDS termination for signal integrity over two 50 Ω lines is 100 Ω between the outputs on the receiver end. Either dc-coupled termination or ac-coupled termination can be used for LVDS outputs. It is recommended to place termination resister close to the receiver. If the receiver is internally biased to a voltage different than the output common mode voltage of the CDCLVD2104, ac-coupling should be used. If the LVDS receiver has internal 100 ohm termination, external termination must be omitted.

Unused outputs can be left open without connecting any trace to the output pins.

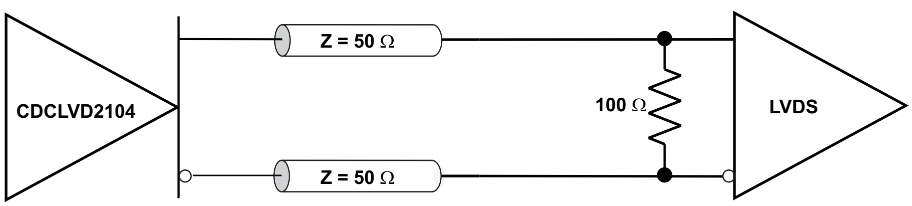



**Figure 14. LVDS Output DC Termination**

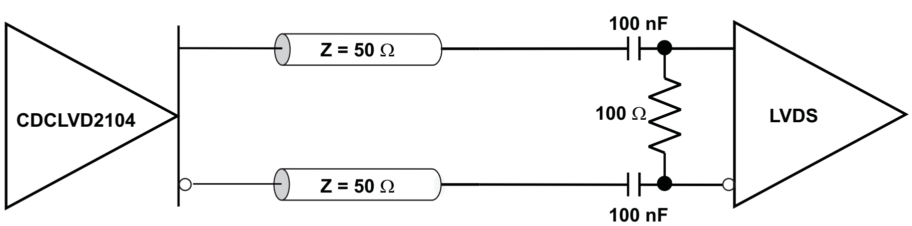



**Figure 15. LVDS Output AC Termination With Receiver Internally Biased**

## INPUT TERMINATION

The CDCLVD2104 inputs can be interfaced with LVDS, LVPECL, or LVCMOS drivers.

LVDS Driver can be connected to CDCLVD2104 inputs with dc or ac coupling as shown Figure 16 and Figure 17, respectively.

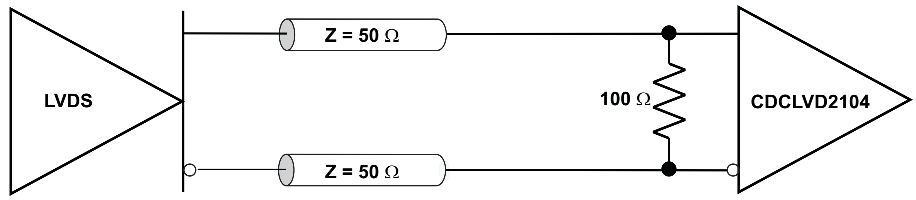



**Figure 16. LVDS Clock Driver Connected to CDCLVD2104 Input (AC Coupled)**

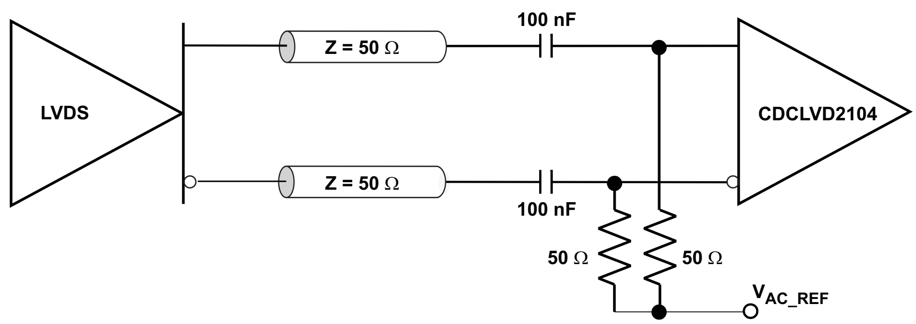



**Figure 17. LVDS Clock Driver Connected to CDCLVD2104 Input (DC Coupled)**

Figure 18 shows how to connect LVPECL inputs to the CDCLVD2104. The series resistors are required to reduce the LVPECL signal swing if the signal swing is >1.6 $V_{PP}$.

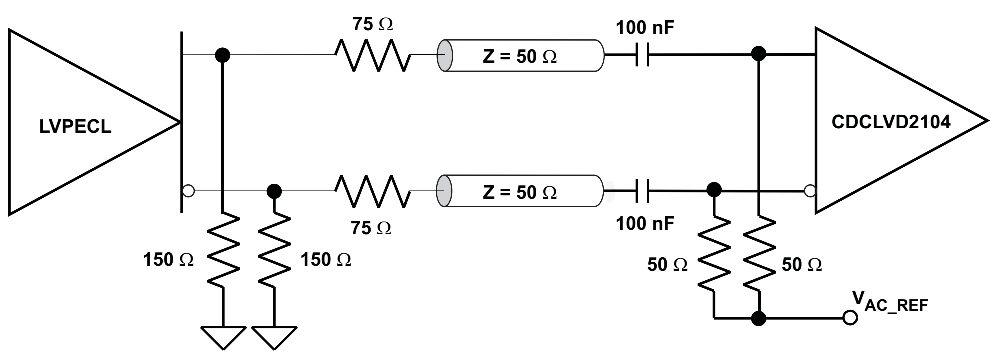



**Figure 18. LVPECL Clock Driver Connected to CDCLVD2104 Input**

Figure 19 illustrates how to couple a 2.5 V LVCMOS clock input to the CDCLVD2104 directly. The series resistance ($R_S$) should be placed close to the LVCMOS driver if needed. 3.3 V LVCMOS clock input swing needs to be limited to $V_{IH} \le V_{CC}$.

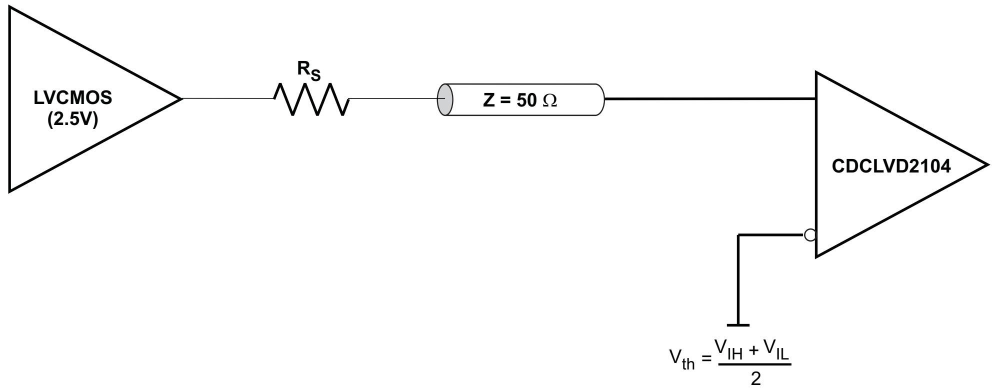



**Figure 19. 2.5V LVCMOS Clock Driver Connected to CDCLVD2104 Input**

If one of the input buffers is used, the other buffer should be disabled through the EN pin, and unused input pins should be grounded by 1 kΩ resistors.

## REVISION HISTORY

| Changes from Original (June 2010) to Revision A | Page |
| --- | --- |
| • Changed the data sheet from Product Preview to Production | 1 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CDCLVD2104RHDR | ACTIVE | VQFN | RHD | 28 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CDCLVD 2104 | Samples |
| CDCLVD2104RHDT | ACTIVE | VQFN | RHD | 28 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CDCLVD 2104 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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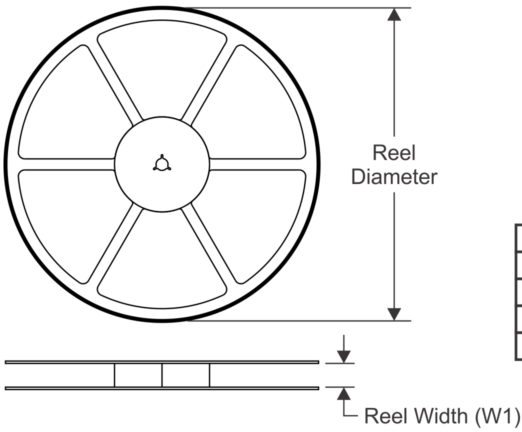
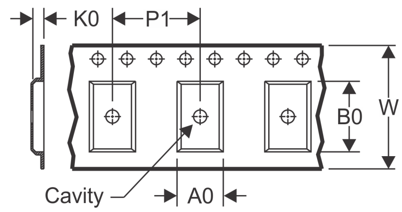
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

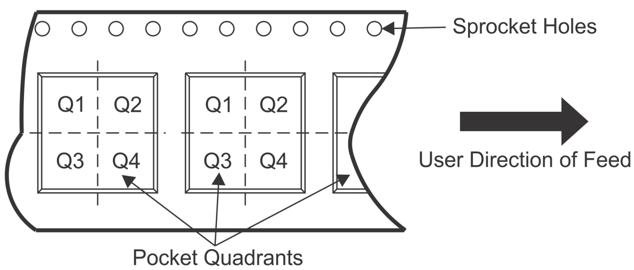



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

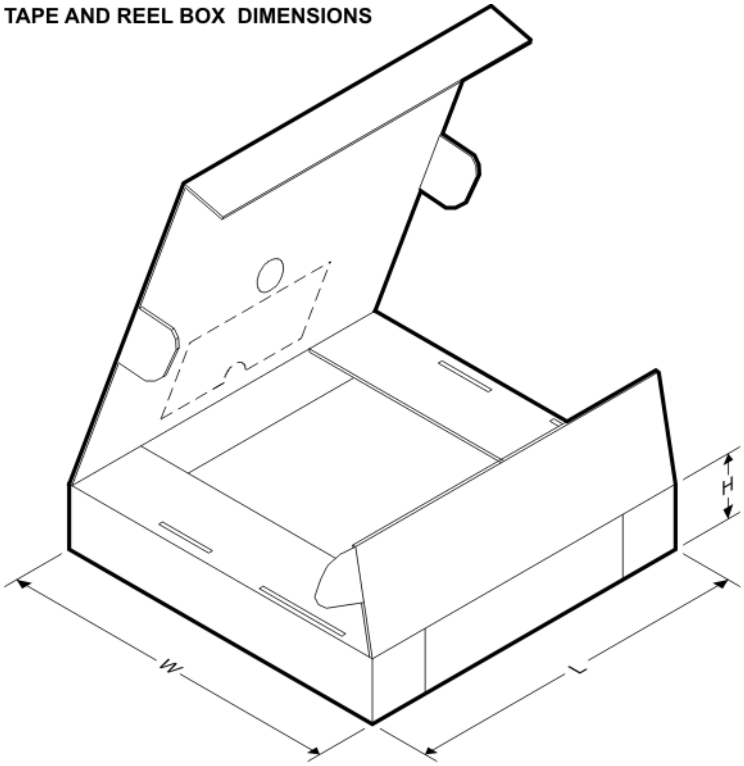
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CDCLVD2104RHDR | VQFN | RHD | 28 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| CDCLVD2104RHDT | VQFN | RHD | 28 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |

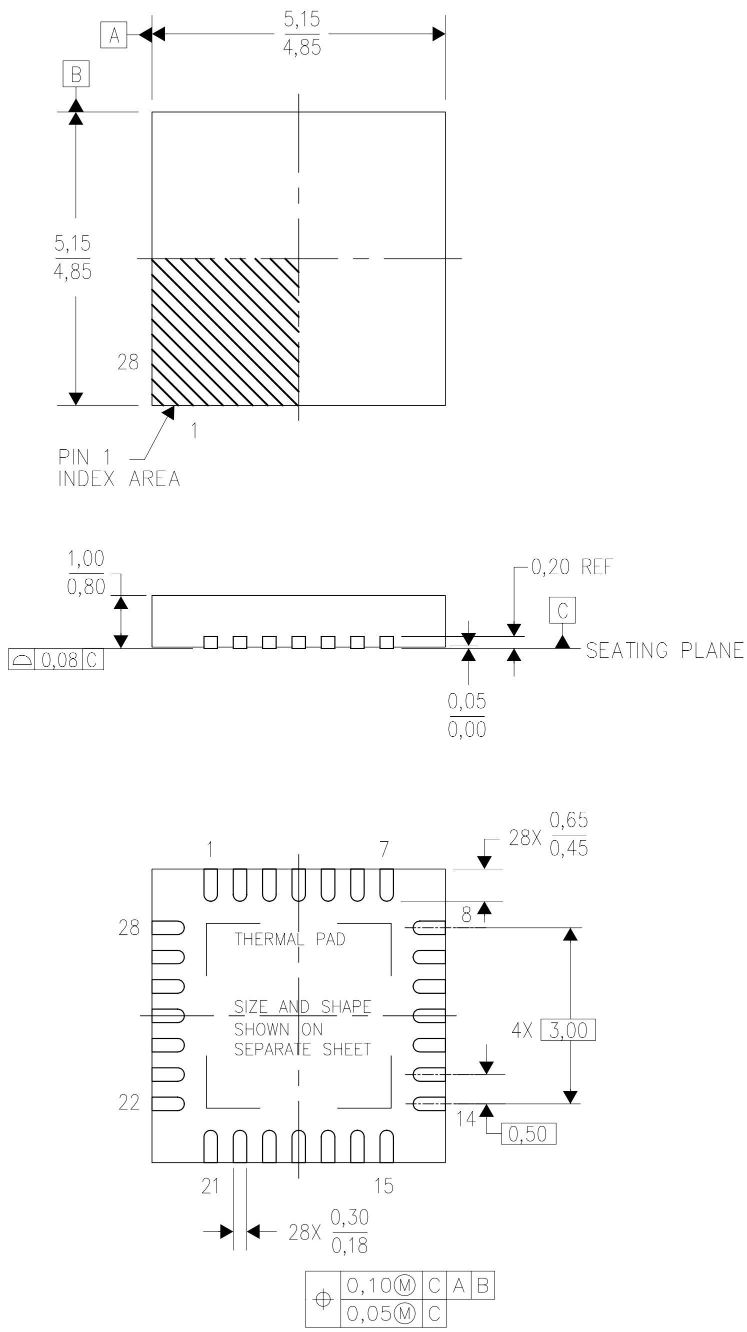
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CDCLVD2104RHDR | VQFN | RHD | 28 | 3000 | 338.1 | 338.1 | 20.6 |
| CDCLVD2104RHDT | VQFN | RHD | 28 | 250 | 210.0 | 185.0 | 35.0 |

RHD (S-PVQFN-N28) PLASTIC QUAD FLATPACK NO-LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.

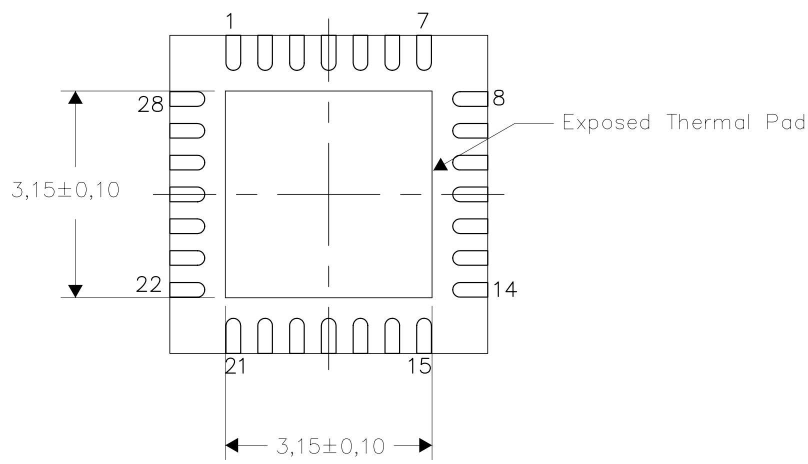
RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



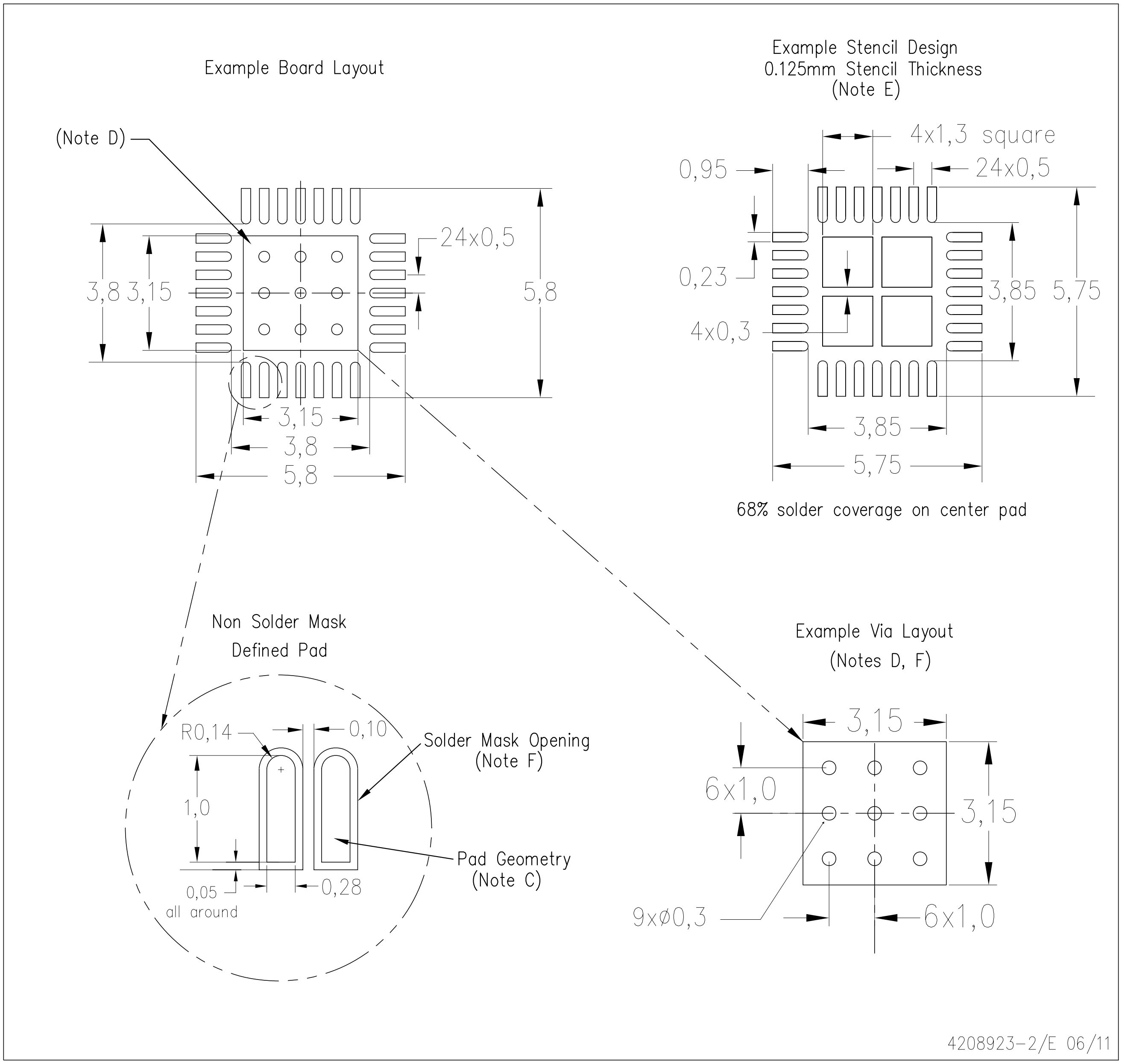

Bottom View

Exposed Thermal Pad Dimensions

4206358-2/I 05/11

NOTE: All linear dimensions are in millimeters

RHD (S-PVQFN-N28) PLASTIC QUAD FLATPACK NO-LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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