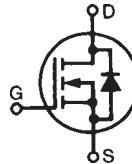


TrenchTTM Power MOSFET

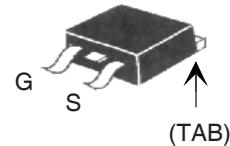
N-Channel Enhancement Mode
Avalanche Rated

IXTA110N055T2 IXTP110N055T2

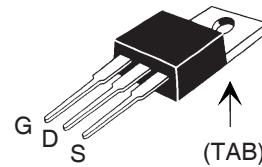
V_{DSS} = 55V
 I_{D25} = 110A
 $R_{DS(on)}$ ≤ 6.6mΩ



TO-263 (IXTA)



TO-220 (IXTP)



G = Gate D = Drain
S = Source TAB = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 175°C	55	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 175°C , $R_{GS} = 1\text{M}\Omega$	55	V
V_{GSM}	Transient	± 20	V
I_{D25}	$T_c = 25^\circ\text{C}$	110	A
I_{LRMS}	Lead Current Limit, RMS	75	A
I_{DM}	$T_c = 25^\circ\text{C}$, pulse width limited by T_{JM}	300	A
I_{AR}	$T_c = 25^\circ\text{C}$	50	A
E_{AS}	$T_c = 25^\circ\text{C}$	400	mJ
P_D	$T_c = 25^\circ\text{C}$	180	W
T_J		-55 ... +175	°C
T_{JM}		175	°C
T_{stg}		-55 ... +175	°C
T_L	1.6mm (0.062in.) from case for 10s Plastic body for 10 seconds	300 260	°C
M_d	Mounting torque (TO-220)	1.13 / 10	Nm/lb.in.
Weight	TO-263 TO-220	2.5 3.0	g

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$	55		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2.0		V
I_{GSS}	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$		±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$ $V_{GS} = 0\text{V}$ $T_J = 150^\circ\text{C}$		2 200	μA
$R_{DS(on)}$	$V_{GS} = 10\text{V}$, $I_D = 25\text{A}$, Notes 1, 2	5.5	6.6	mΩ

Features

- International standard packages
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
- 175°C Operating Temperature
- High current handling capability
- ROHS Compliant
- High performance Trench Technology for extremely low $R_{DS(on)}$

Advantages

- Easy to mount
- Space savings
- High power density
- Synchronous

Applications

- Automotive Engine Control
- Synchronous Buck Converter (for notebook system power & General purpose point & load.)
- DC/DC Converters
- High Current Switching Applications
- Power Train Management
- Distributed Power Architecture

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 0.5 \cdot I_{D25}$, Note 1	30	49	S
C_{iss}		3060		pF
C_{oss}		497		pF
C_{rss}		105		pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 30\text{V}$, $I_D = 25\text{A}$ $R_G = 5\Omega$ (External)	18	ns	
t_r		25	ns	
$t_{d(off)}$		40	ns	
t_f		23	ns	
$Q_{g(on)}$		57		nC
Q_{gs}		16		nC
Q_{gd}		11		nC
R_{thJC}			0.82	$^\circ\text{C}/\text{W}$
R_{thCH}	TO-220	0.50		$^\circ\text{C}/\text{W}$

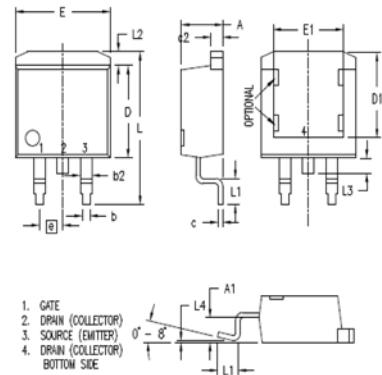
Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
I_s	$V_{GS} = 0\text{V}$		110	A
I_{SM}	Repetitive, Pulse width limited by T_{JM}		300	A
V_{SD}	$I_F = 25\text{A}$, $V_{GS} = 0\text{V}$, Note 1	0.84	1.0	V
t_{rr}	$I_F = 50\text{A}$, $V_{GS} = 0\text{V}$ $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 27\text{V}$	38		ns
I_{RM}		2.4		A
Q_{RM}		46		nC

Notes: 1. Pulse test, $t \leq 300\mu\text{s}$; duty cycle, $d \leq 2\%$.

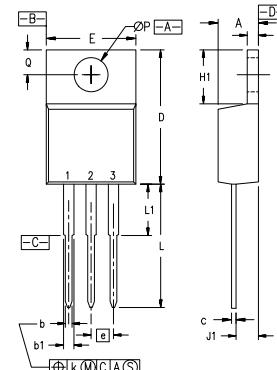
2. On through-hole packages, $R_{DS(on)}$ Kelvin test contact location must be 5mm or less from the package body.

TO-263 (IXTA) Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.160	.190	4.06	4.83
A1	.080	.110	2.03	2.79
b	.020	.039	0.51	0.99
b2	.045	.055	1.14	1.40
c	.016	.029	0.40	0.74
c2	.045	.055	1.14	1.40
D	.340	.380	8.64	9.65
D1	.315	.350	8.00	8.89
E	.380	.410	9.65	10.41
E1	.245	.320	6.22	8.13
e	.100	BSC	2.54	BSC
L	.575	.625	14.61	15.88
L1	.090	.110	2.29	2.79
L2	.040	.055	1.02	1.40
L3	.050	.070	1.27	1.78
L4	0	.005	0	0.13

TO-220 (IXTP) Outline



Pins: 1 - Gate 2 - Drain
3 - Source 4 - Drain

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b1	.045	.065	1.15	1.65
c	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
e	.100	BSC	2.54	BSC
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L1	.110	.230	2.79	5.84
ØP	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

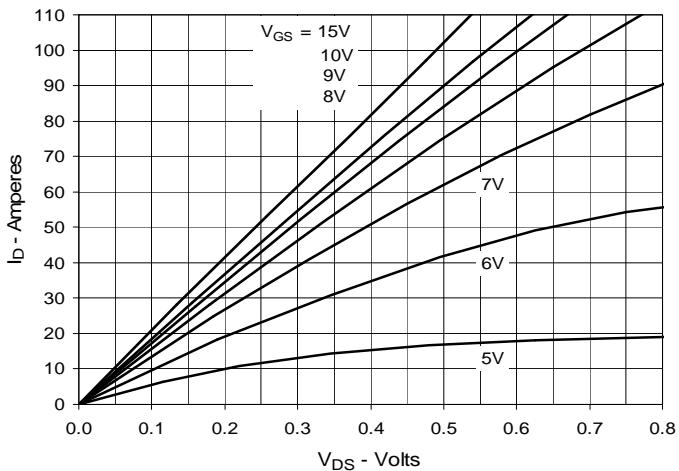
PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

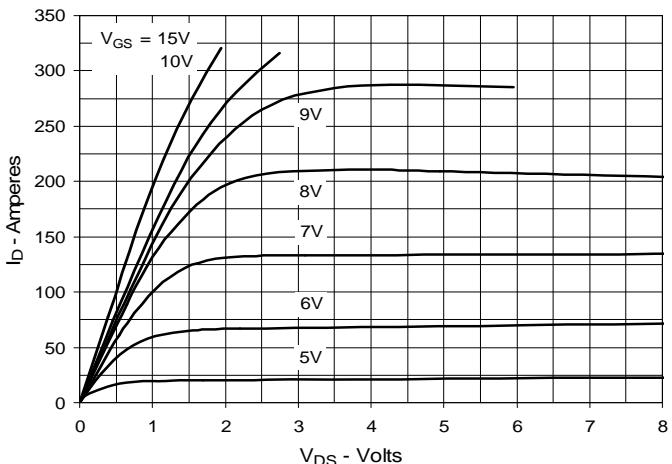
IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2 4,850,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2 4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

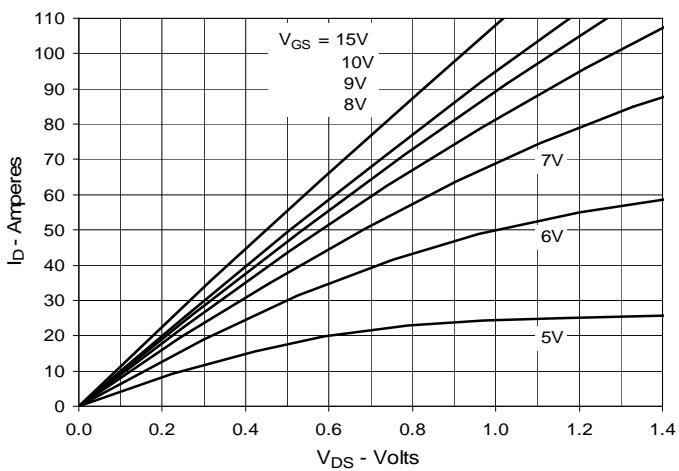
**Fig. 1. Output Characteristics
@ 25°C**



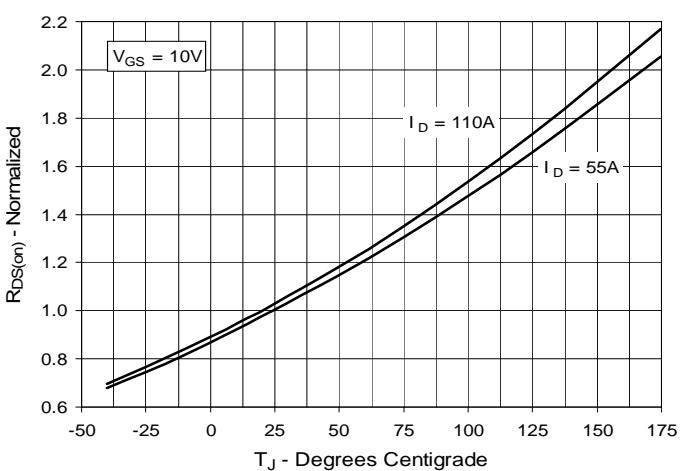
**Fig. 2. Extended Output Characteristics
@ 25°C**



**Fig. 3. Output Characteristics
@ 150°C**



**Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 55A$ Value
vs. Junction Temperature**



**Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 55A$ Value
vs. Drain Current**

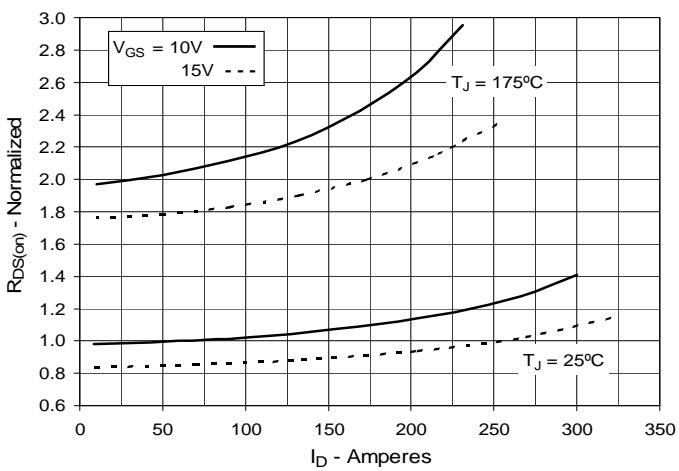


Fig. 6. Drain Current vs. Case Temperature

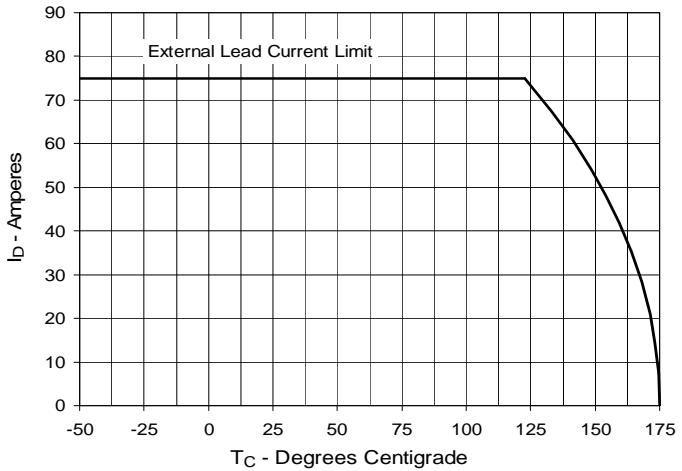


Fig. 7. Input Admittance

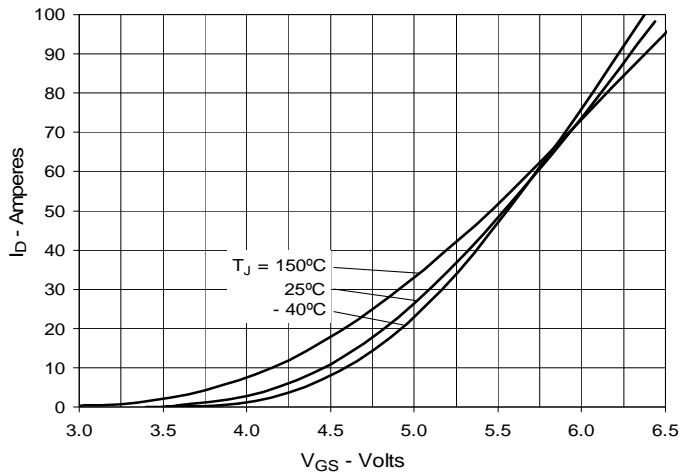


Fig. 8. Transconductance

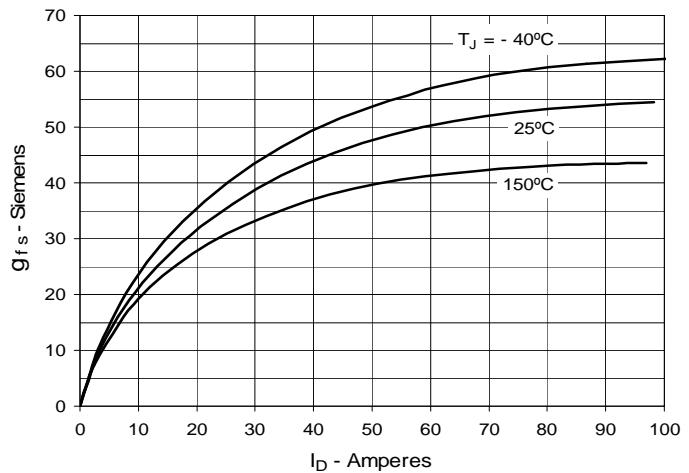


Fig. 9. Forward Voltage Drop of Intrinsic Diode

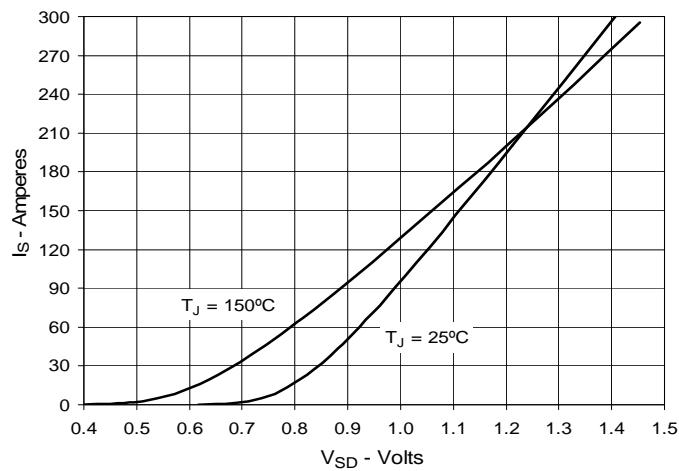


Fig. 10. Gate Charge

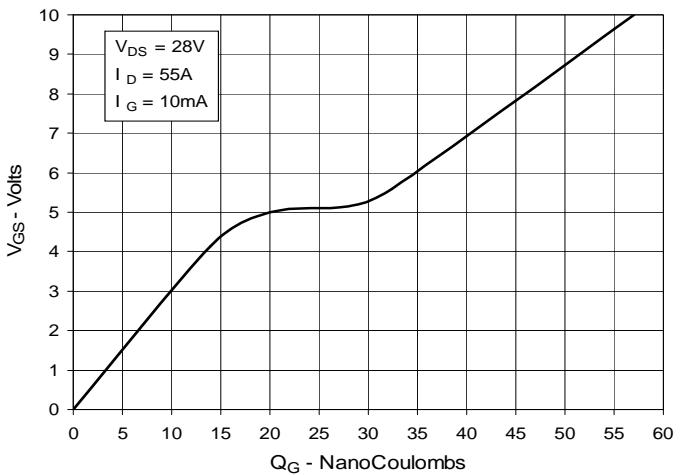


Fig. 11. Capacitance

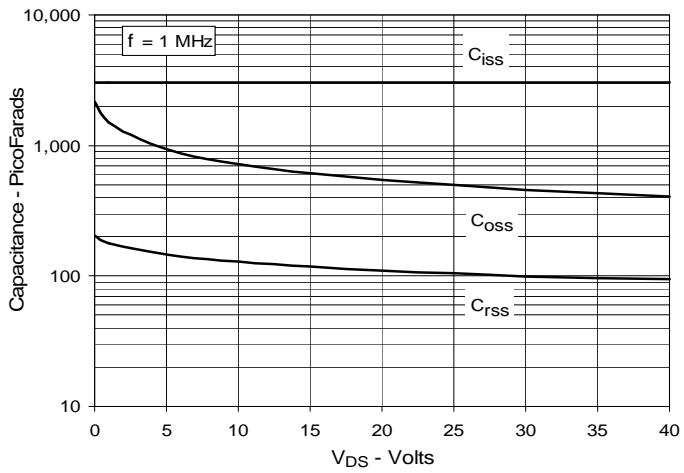
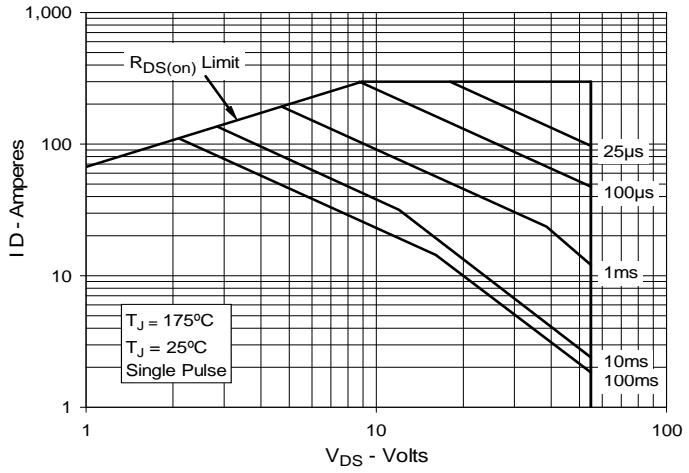
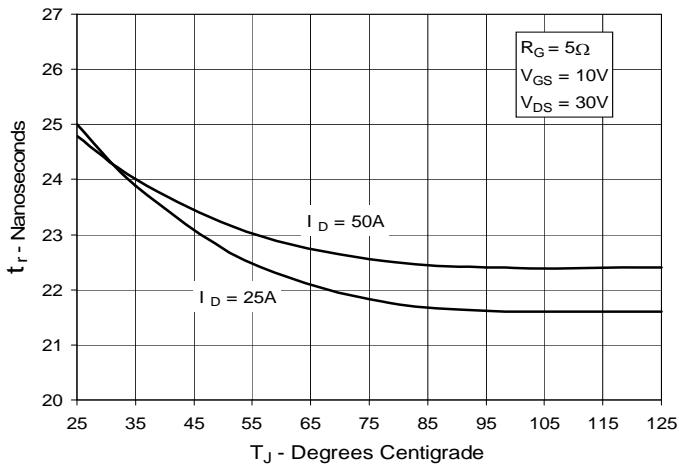


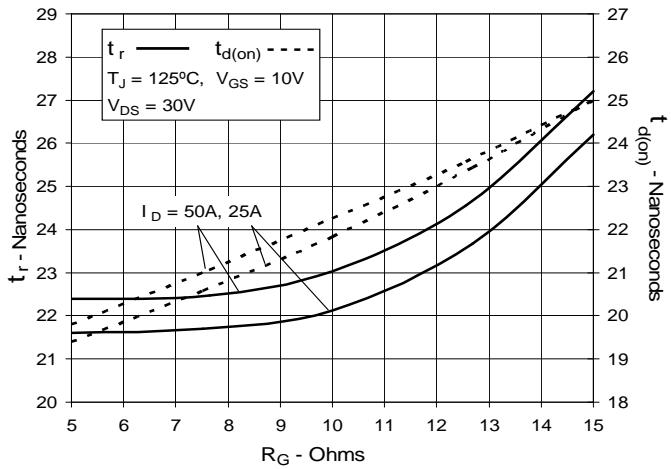
Fig. 12. Forward-Bias Safe Operating Area



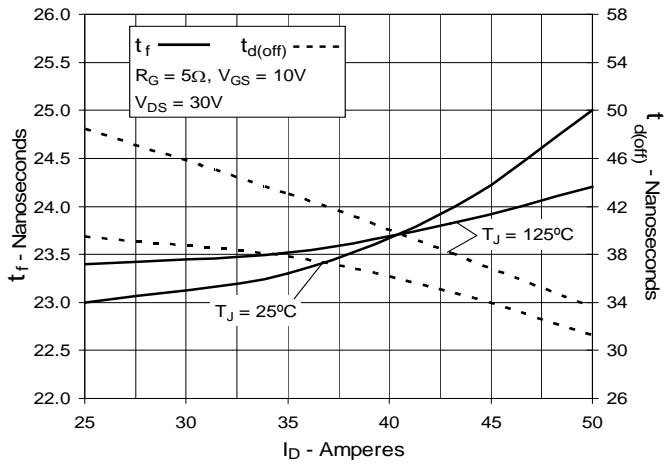
**Fig. 13. Resistive Turn-on
Rise Time vs. Junction Temperature**



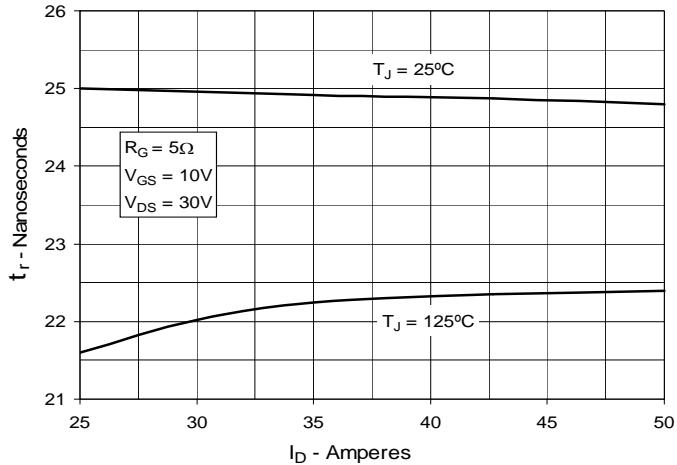
**Fig. 15. Resistive Turn-on
Switching Times vs. Gate Resistance**



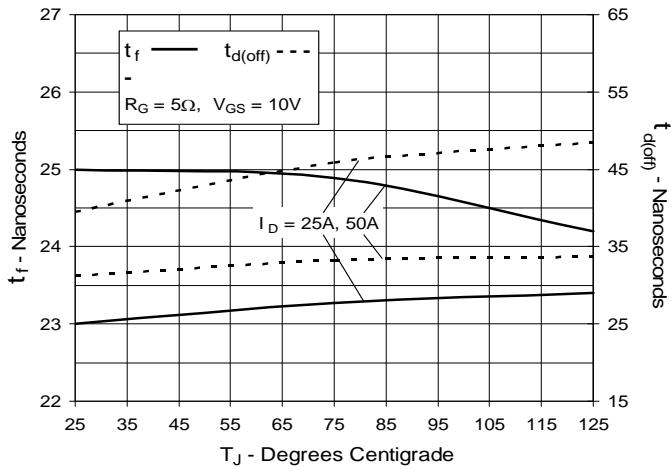
**Fig. 17. Resistive Turn-off
Switching Times vs. Drain Current**



**Fig. 14. Resistive Turn-on
Rise Time vs. Drain Current**



**Fig. 16. Resistive Turn-off
Switching Times vs. Junction Temperature**



**Fig. 18. Resistive Turn-off
Switching Times vs. Gate Resistance**

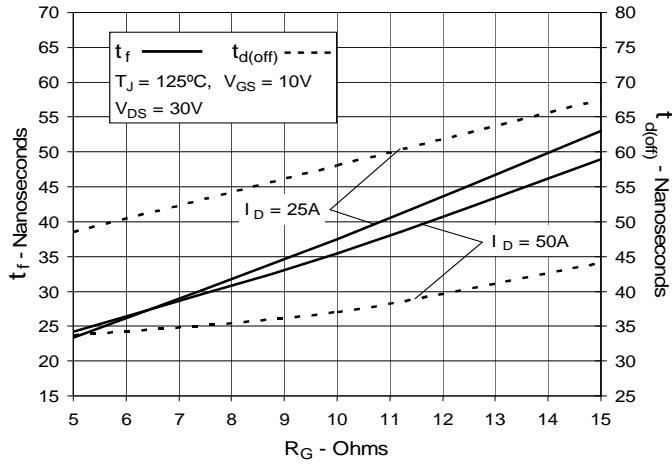
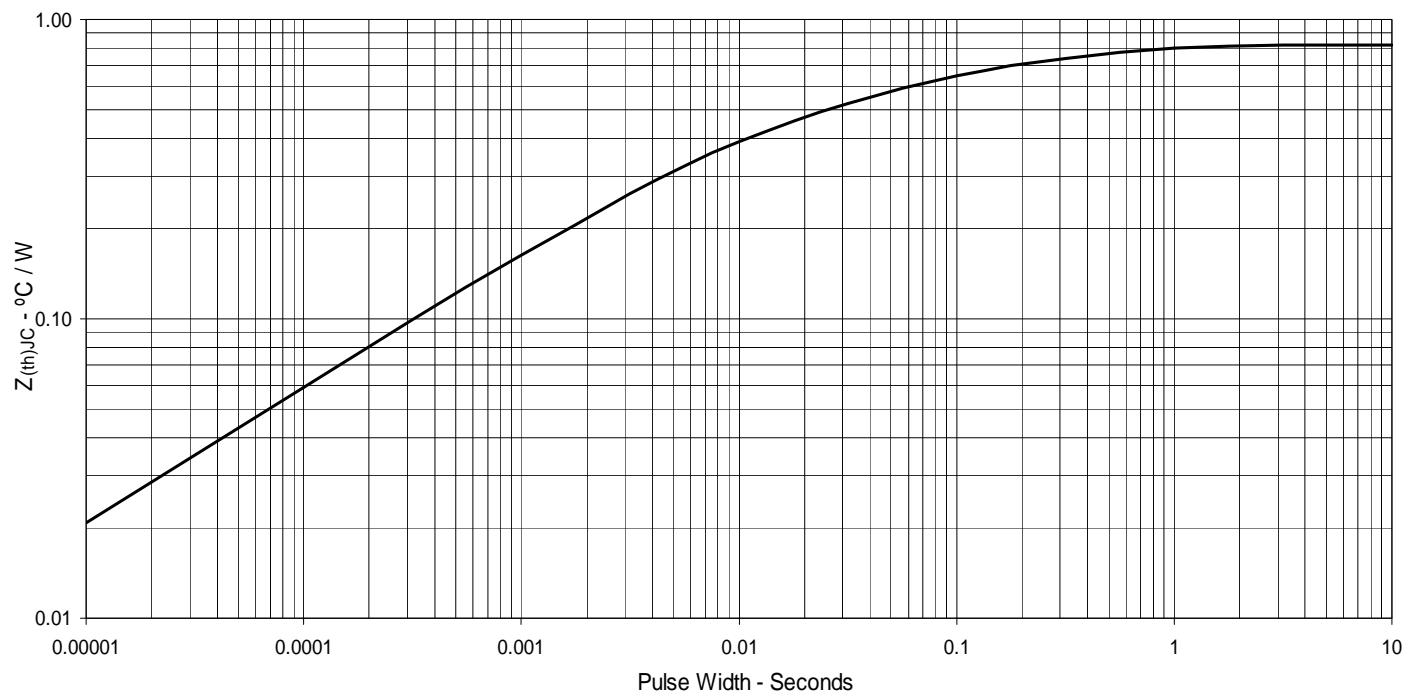


Fig. 19. Maximum Transient Thermal Impedance

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