

74ALVT16501

18-bit universal bus transceiver; 3-state

Rev. 04 — 8 August 2005

Product data sheet

1. General description

The 74ALVT16501 is a high-performance Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) product designed for V_{CC} operation at 2.5 V and 3.3 V with I/O compatibility up to 5 V. This device is an 18-bit universal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

Data flow in each direction is controlled by output enable ($OEAB$ and $\overline{OEBA}$), latch enable ($LEAB$ and $LEBA$), and clock ($CPAB$ and $CPBA$) inputs.

For A-to-B data flow, the device operates in the transparent mode when $LEAB$ is HIGH. When $LEAB$ is LOW, the A-bus data is latched if $CPAB$ is held at a HIGH or LOW level. If $LEAB$ is LOW, the A-bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of $CPAB$. When $OEAB$ is HIGH, the outputs are active. When $OEAB$ is LOW, the outputs are in the high-impedance state.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, $LEBA$ and $CPBA$. The output enables are complimentary ($OEAB$ is active HIGH and $\overline{OEBA}$ is active LOW).

2. Features

- 18-bit bidirectional bus interface
- 5 V I/O compatible
- 3-state buffers
- Output capability: +64 mA to –32 mA
- TTL and LVTTTL input and output switching levels
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Positive-edge triggered clock inputs
- Latch-up protection:
 - ◆ JESD78: exceeds 500 mA
- ESD protection:
 - ◆ MIL STD 883, method 3015: exceeds 2000 V
 - ◆ Machine model: exceeds 400 V

PHILIPS

3. Quick reference data

Table 1: Quick reference data

$GND = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

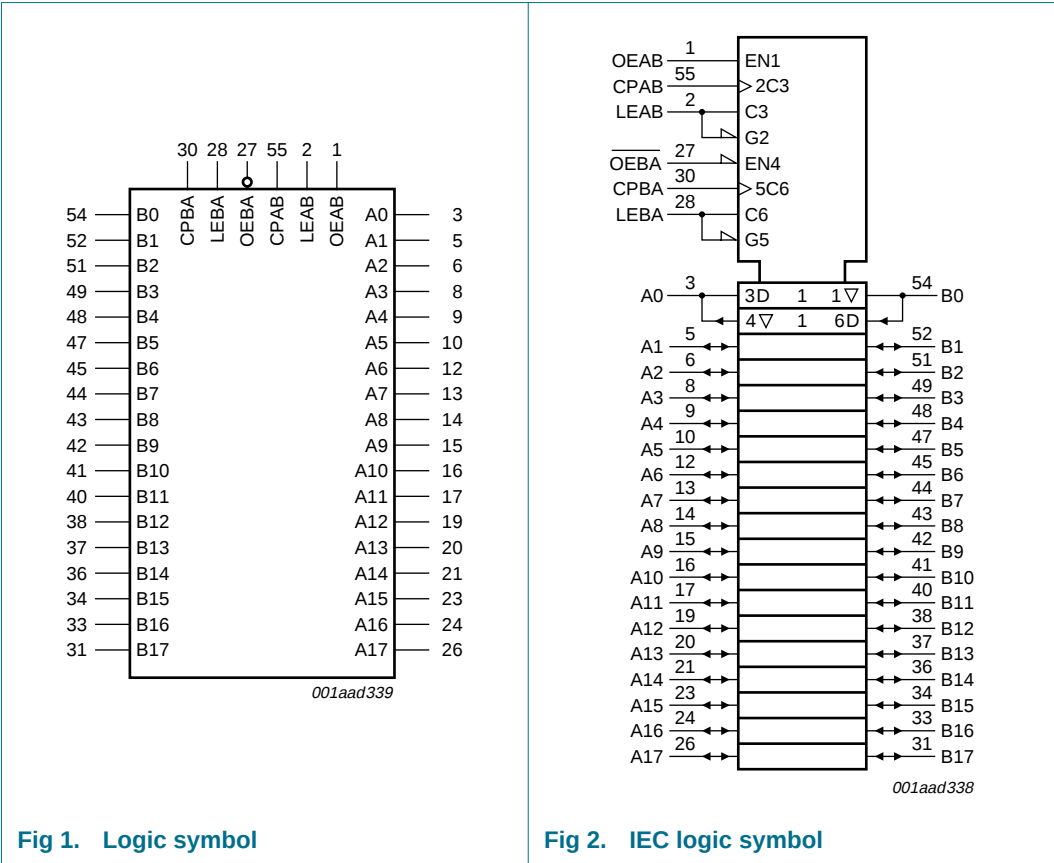
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC} = 2.5\text{ V}$						
t_{PLH}	propagation delay An to Bn or Bn to An	$C_L = 30\text{ pF}$	-	2.0	-	ns
t_{PHL}	propagation delay An to Bn or Bn to An	$C_L = 30\text{ pF}$	-	2.1	-	ns
C_i	input capacitance of control pins	$V_I = 0\text{ V}$ or V_{CC}	-	4	-	pF
C_{io}	input/output capacitance of I/O pins	$V_{IO} = 0\text{ V}$ or V_{CC}	-	8	-	pF
I_{CC}	quiescent supply current	outputs disabled	-	40	-	μA
$V_{CC} = 3.3\text{ V}$						
t_{PLH}	propagation delay An to Bn or Bn to An	$C_L = 50\text{ pF}$	-	1.8	-	ns
t_{PHL}	propagation delay An to Bn or Bn to An	$C_L = 50\text{ pF}$	-	1.9	-	ns
C_i	input capacitance of control pins	$V_I = 0\text{ V}$ or V_{CC}	-	4	-	pF
C_{io}	input/output capacitance of I/O pins	$V_{IO} = 0\text{ V}$ or V_{CC}	-	8	-	pF
I_{CC}	quiescent supply current	outputs disabled	-	60	-	μA

4. Ordering information

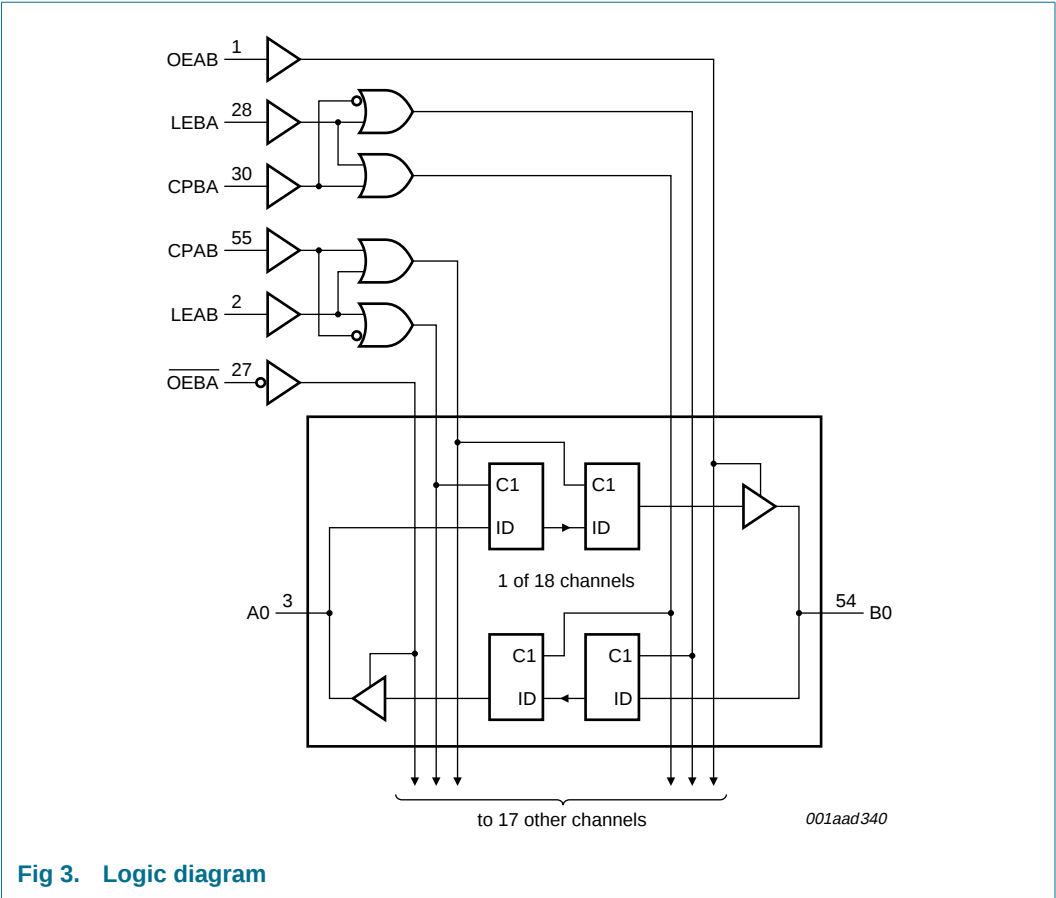
Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVT16501DL	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SSOP56	plastic shrink small outline package; 56 leads; body width 7.5 mm	SOT371-1
74ALVT16501DGG	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

5. Functional diagram

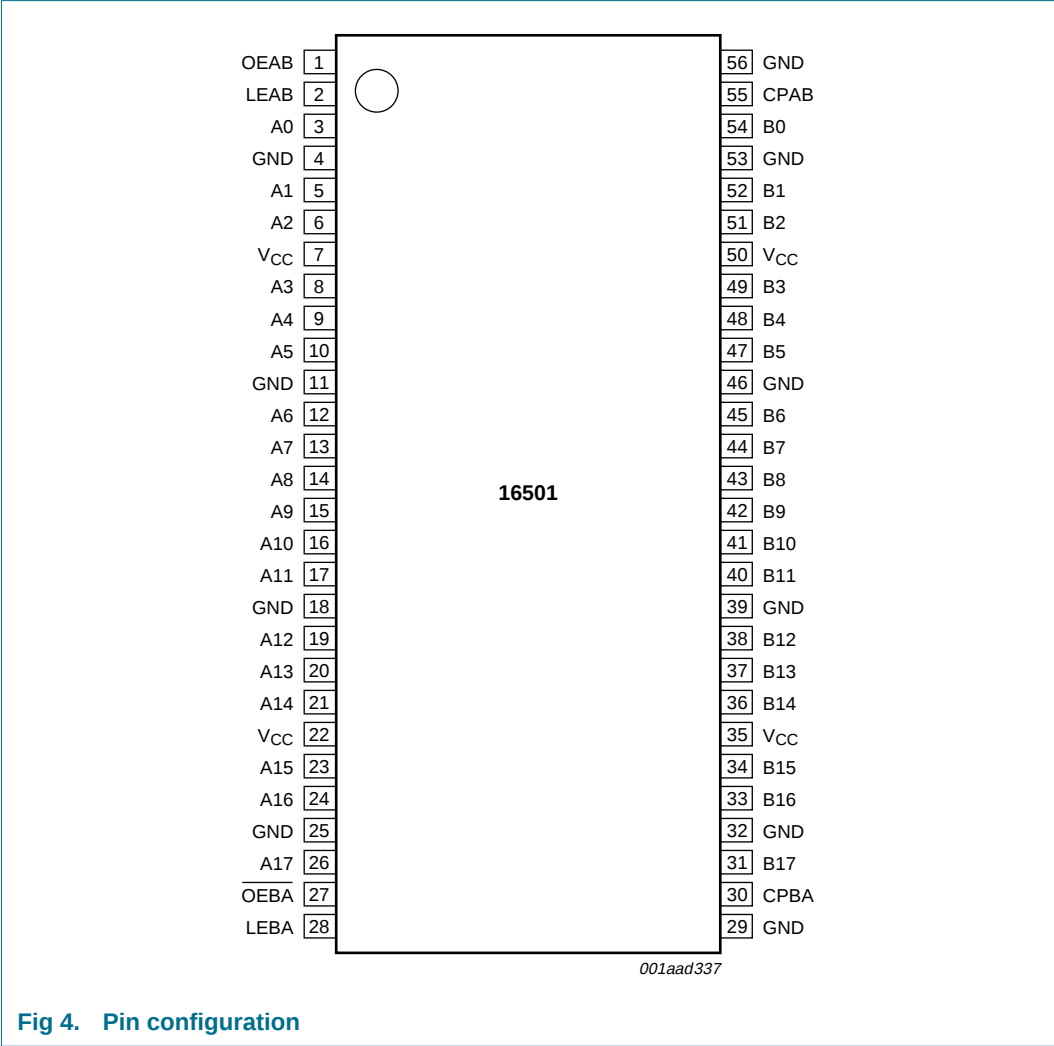


The IEC logic symbol for the 74ALVT16501 is a rectangular block with 18 pins on each side. The top pins are labeled B0 through B17 from left to right. The bottom pins are labeled A0 through A17 from left to right. On the left side, there are control pins: OEAB (pin 1), CPAB (pin 55), LEAB (pin 2), OEBA (pin 27), CPBA (pin 30), and LEBA (pin 28). On the right side, there are control pins: A0 (pin 3), A1 (pin 5), A2 (pin 6), A3 (pin 8), A4 (pin 9), A5 (pin 10), A6 (pin 12), A7 (pin 13), A8 (pin 14), A9 (pin 15), A10 (pin 16), A11 (pin 17), A12 (pin 19), A13 (pin 20), A14 (pin 21), A15 (pin 23), A16 (pin 24), and A17 (pin 26). The symbol is identified by the number 001aad338.



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
OEAB	1	A-to-B output enable input
LEAB	2	A-to-B latch enable input
A0	3	data input or output (A side)
GND	4	ground (0 V)
A1	5	data input or output (A side)
A2	6	data input or output (A side)
V _{CC}	7	voltage supply
A3	8	data input or output (A side)

Table 3: Pin description ...continued

Symbol	Pin	Description
A4	9	data input or output (A side)
A5	10	data input or output (A side)
GND	11	ground (0 V)
A6	12	data input or output (A side)
A7	13	data input or output (A side)
A8	14	data input or output (A side)
A9	15	data input or output (A side)
A10	16	data input or output (A side)
A11	17	data input or output (A side)
GND	18	ground (0 V)
A12	19	data input or output (A side)
A13	20	data input or output (A side)
A14	21	data input or output (A side)
V _{CC}	22	voltage supply
A15	23	data input or output (A side)
A16	24	data input or output (A side)
GND	25	ground (0 V)
A17	26	data input or output (A side)
OEBA	27	B-to-A output enable input (active LOW)
LEBA	28	B-to-A latch enable input
GND	29	ground (0 V)
CPBA	30	B-to-A clock input (active rising edge)
B17	31	data input or output (B side)
GND	32	ground (0 V)
B16	33	data input or output (B side)
B15	34	data input or output (B side)
V _{CC}	35	voltage supply
B14	36	data input or output (B side)
B13	37	data input or output (B side)
B12	38	data input or output (B side)
GND	39	ground (0 V)
B11	40	data input or output (B side)
B10	41	data input or output (B side)
B9	42	data input or output (B side)
B8	43	data input or output (B side)
B7	44	data input or output (B side)
B6	45	data input or output (B side)
GND	46	ground (0 V)
B5	47	data input or output (B side)
B4	48	data input or output (B side)
B3	49	data input or output (B side)

Table 3: Pin description ...continued

Symbol	Pin	Description
V _{CC}	50	voltage supply
B2	51	data input or output (B side)
B1	52	data input or output (B side)
GND	53	ground (0 V)
B0	54	data input or output (B side)
CPAB	55	A-to-B clock input (active rising edge)
GND	56	ground (0 V)

7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating mode	Control			Input	Internal registers	Output
	OEAB	LEAB	CPAB	A _n		B _n
	OEBA	LEBA	CPBA	B _n		A _n
Disabled	L	H	X	X	X	Z
Disabled, latch data	L	↓	X	h	H	Z
				l	L	Z
Disabled, hold data	L	L	H or L	X	NC	Z
Disabled, clock data	L	L	↑	h	H	Z
				l	L	Z
Transparent	H	H	X	H	H	H
				L	L	L
Latch data and display	H	↓	X	h	H	H
				l	L	L
Clock data and display	H	L	↑	h	H	H
				l	L	L
Hold data and display	H	L	H or L	X	H	H
				X	L	L

- [1] H = HIGH voltage level;
 h = HIGH voltage level one setup time prior to the enable or clock transition;
 L = LOW voltage level;
 l = LOW voltage level one setup time prior to the enable or clock transition;
 NC = no change;
 X = don't care;
 Z = high-impedance OFF-state;
 ↓ = HIGH-to-LOW enable or clock transition;
 ↑ = LOW-to-HIGH enable or clock transition.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage		[1] -0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+7.0	V
I_{IK}	input diode current	$V_I < 0$ V	-	-50	mA
I_{OK}	output diode current	$V_O < 0$ V	-	-50	mA
I_O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		[2] -	150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$						
V_{CC}	supply voltage		2.3	-	2.7	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		1.7	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.7	V
I_{OH}	HIGH-level output current		-	-	-8	mA
I_{OL}	LOW-level output current	none	-	-	8	mA
		current duty cycle ≤ 50 %; $f \geq 1$ kHz	-	-	24	mA
$\Delta t/\Delta V$	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
T_{amb}	ambient temperature	free air	-40	-	+85	°C
$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$						
V_{CC}	supply voltage		3.0	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-	-	-32	mA

Table 6: Recommended operating conditions ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f ≥ 1 kHz	-	-	64	mA
Δt/ΔV	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
T _{amb}	ambient temperature	free air	-40	-	+85	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

T_{amb} = -40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC} = 2.5 V ± 0.2 V [1]						
V _{IK}	input diode voltage	V _{CC} = 2.3 V; I _{IK} = -18 mA	-	-0.85	-1.2	V
V _{OH}	HIGH-level output voltage	V _{CC} = 2.3 V to 3.6 V; I _{OH} = -100 μA	V _{CC} - 0.2	-	-	V
		V _{CC} = 2.3 V; I _{OH} = -8 mA	1.8	-	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 2.3 V; I _{OL} = 100 μA	-	0.07	0.2	V
		V _{CC} = 2.3 V; I _{OL} = 24 mA	-	0.3	0.5	V
		V _{CC} = 2.3 V; I _{OL} = 8 mA	-	-	0.4	V
V _{RST}	power-up LOW-state output voltage	V _{CC} = 2.7 V; I _O = 1 mA; V _I = V _{CC} or GND	[2] -	-	0.55	V
I _{LI}	input leakage current control pins	V _{CC} = 2.7 V; V _I = V _{CC} or GND	-	0.1	±1	μA
		V _{CC} = 0 V or 2.7 V; V _I = 5.5 V	-	0.1	10	μA
	I/O data pins	V _{CC} = 2.7 V; V _I = V _{CC}	[3] -	0.1	1	μA
		V _{CC} = 2.7 V; V _I = 0 V	[3] -	+0.1	-5	μA
I _{OFF}	power-down leakage current	V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-	0.1	±100	μA
I _{HOLD}	bus hold current data inputs	V _{CC} = 2.3 V; V _I = 0.7 V	[4] -	90	-	μA
		V _{CC} = 2.3 V; V _I = 1.7 V	[4] -	-75	-	μA
I _{EX}	external current into output	output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 2.3 V	-	5	125	μA
I _{PU} , I _{PD}	power-up/down 3-state output current	V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; OEAB or OEBA don't care	[5] -	4	100	μA
I _{CC}	quiescent supply current	V _{CC} = 2.7 V; V _I = GND or V _{CC} ; I _O = 0 A				
		outputs HIGH-state	-	0.04	0.1	mA
		outputs LOW-state	-	2.5	4.5	mA
		outputs disabled	[6] -	0.04	0.1	mA
ΔI _{CC}	additional quiescent supply current per input pin	V _{CC} = 2.3 V to 2.7 V; one input at V _{CC} - 0.6 V, other inputs at V _{CC} or GND	[7] -	0.01	0.4	mA
C _i	input capacitance of control pins	V _I = 0 V or V _{CC}	-	4	-	pF

Table 7: Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

 $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{io}	input/output capacitance of I/O pins	$V_{I/O} = 0\text{ V}$ or V_{CC}	-	8	-	pF
$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ [8]						
V_{IK}	input diode voltage	$V_{CC} = 3.0\text{ V}$; $I_{IK} = -18\text{ mA}$	-	-0.85	-1.2	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 3.0\text{ V}$ to 3.6 V ; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	V_{CC}	-	V
		$V_{CC} = 3.0\text{ V}$; $I_{OH} = -32\text{ mA}$	2.0	2.3	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 3.0\text{ V}$; $I_{OL} = 100\text{ }\mu\text{A}$	-	0.07	0.2	V
		$V_{CC} = 3.0\text{ V}$; $I_{OL} = 16\text{ mA}$	-	0.25	0.4	V
		$V_{CC} = 3.0\text{ V}$; $I_{OL} = 32\text{ mA}$	-	0.3	0.5	V
		$V_{CC} = 3.0\text{ V}$; $I_{OL} = 64\text{ mA}$	-	0.4	0.55	V
V_{RST}	power-up LOW-state output voltage	$V_{CC} = 3.6\text{ V}$; $I_O = 1\text{ mA}$; $V_I = V_{CC}$ or GND	[2] -	-	0.55	V
I_{LI}	input leakage current					
	control pins	$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND	-	0.1	± 1	μA
		$V_{CC} = 0\text{ V}$ or 3.6 V ; $V_I = 5.5\text{ V}$	-	0.1	10	μA
	I/O data pins	$V_{CC} = 3.6\text{ V}$; $V_I = 5.5\text{ V}$	[3] -	0.1	20	μA
		$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$	[3] -	0.5	10	μA
		$V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V}$	[3] -	+0.1	-5	μA
I_{OFF}	power-down leakage current	$V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V}$ to 4.5 V	-	0.1	± 100	μA
I_{HOLD}	bus hold current data inputs	$V_{CC} = 3\text{ V}$; $V_I = 0.8\text{ V}$	[9] 75	130	-	μA
		$V_{CC} = 3\text{ V}$; $V_I = 2.0\text{ V}$	[9] -75	-140	-	μA
		$V_{CC} = 0\text{ V}$ to 3.6 V ; $V_I = 3.6\text{ V}$	[9] ± 500	-	-	μA
I_{EX}	external current into output	output in HIGH-state when $V_O > V_{CC}$; $V_O = 5.5\text{ V}$; $V_{CC} = 3.0\text{ V}$	-	10	125	μA
I_{PU}, I_{PD}	power-up/down 3-state output current	$V_{CC} \leq 1.2\text{ V}$; $V_O = 0.5\text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC} ; OEAB or OEBA don't care	[10] -	1.0	± 100	μA
I_{CC}	quiescent supply current	$V_{CC} = 3.6\text{ V}$; $V_I = \text{GND}$ or V_{CC} ; $I_O = 0\text{ A}$				
		outputs HIGH-state	-	0.06	0.1	mA
		outputs LOW-state	-	3.5	5	mA
		outputs disabled	[6] -	0.06	0.1	mA
ΔI_{CC}	additional quiescent supply current per input pin	$V_{CC} = 3\text{ V}$ to 3.6 V ; one input at $V_{CC} - 0.6\text{ V}$, other inputs at V_{CC} or GND	[7] -	0.04	0.4	mA
C_i	input capacitance of control pins	$V_I = 0\text{ V}$ or V_{CC}	-	4	-	pF
C_{io}	input/output capacitance of I/O pins	$V_{I/O} = 0\text{ V}$ or V_{CC}	-	8	-	pF

[1] All typical values are at $V_{CC} = 2.5\text{ V}$ and $T_{amb} = 25^{\circ}\text{C}$.

[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

[3] Unused pins at V_{CC} or GND.

[4] Not guaranteed.

[5] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms . From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ a transition time of $100\text{ }\mu\text{s}$ is permitted. This parameter is valid for $T_{amb} = 25^{\circ}\text{C}$ only.

- [6] I_{CC} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- [7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
- [8] All typical values are at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.
- [9] This is the bus hold overdrive current required to force the input to the opposite logic state.
- [10] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From $V_{CC} = 1.2$ V to $V_{CC} = 3.3$ V ± 0.3 V a transition time of 100 μ s is permitted. This parameter is valid for $T_{amb} = 25$ °C only.

11. Dynamic characteristics

Table 8: Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 11](#).

$T_{amb} = -40$ °C to $+85$ °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC} = 2.5$ V ± 0.2 V [4]; $C_L = 30$ pF						
t_{PLH}	propagation delay					
	An to Bn or Bn to An	see Figure 5	1.0	2.0	3.0	ns
	LEAB to Bn or LEBA to An	see Figure 6	1.5	2.4	4.0	ns
	CPAB to Bn or CPBA to An	see Figure 7	2.2	3.6	5.4	ns
t_{PHL}	propagation delay					
	An to Bn or Bn to An	see Figure 5	1.4	2.1	3.5	ns
	LEAB to Bn or LEBA to An	see Figure 6	1.5	2.3	4.0	ns
	CPAB to Bn or CPBA to An	see Figure 7	1.9	3.2	5.4	ns
t_{PZH}	output enable time to HIGH-level	see Figure 9	2.3	3.9	5.0	ns
t_{PZL}	output enable time to LOW-level	see Figure 10	1.9	3.3	4.4	ns
t_{PHZ}	output disable time from HIGH-level	see Figure 9	2.2	3.4	4.4	ns
t_{PLZ}	output disable time from LOW-level	see Figure 10	1.6	2.8	3.4	ns
$t_{h(H)}$	hold time HIGH					
	An to CPAB or Bn to CPBA	see Figure 8	0	-1.2	-	ns
	An to LEAB or Bn to LEAB	see Figure 8	+1.0	-0.5	-	ns
$t_{h(L)}$	hold time LOW					
	An to CPAB or Bn to CPBA	see Figure 8	+1.0	-0.4	-	ns
	An to LEAB or Bn to LEAB	see Figure 8	2.0	1.0	-	ns
$t_{su(H)}$	set-up time HIGH					
	An to CPAB or Bn to CPBA	see Figure 8	1.9	0.4	-	ns
	An to LEAB or Bn to LEBA	see Figure 8	0	-1.0	-	ns
$t_{su(L)}$	set-up time LOW					
	An to CPAB or Bn to CPBA	see Figure 8	2.5	1.2	-	ns
	An to LEAB or Bn to LEBA	see Figure 8	+1.0	-0.5	-	ns
t_{WH}	pulse width HIGH					
	CPAB or CPBA	see Figure 7	3.0	-	-	ns
	LEAB or LEBA	see Figure 6	1.5	-	-	ns
t_{WL}	pulse width LOW					
	CPAB or CPBA	see Figure 7	3.0	-	-	ns
f_{max}	maximum clock frequency	see Figure 7	150	-	-	MHz

Table 8: Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 11](#).

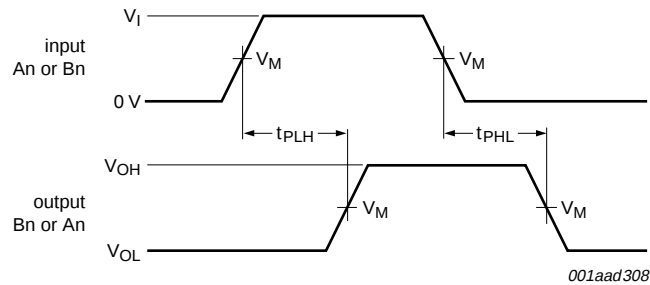
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ [2]; $C_L = 50\text{ pF}$						
t_{PLH}	propagation delay					
	An to Bn or Bn to An	see Figure 5	1.2	1.8	2.9	ns
	LEAB to Bn or LEBA to An	see Figure 6	1.5	2.4	3.5	ns
	CPAB to Bn or CPBA to An	see Figure 7	2.1	3.0	4.3	ns
t_{PHL}	propagation delay					
	An to Bn or Bn to An	see Figure 5	1.1	1.9	2.8	ns
	LEAB to Bn or LEBA to An	see Figure 6	1.4	2.1	3.6	ns
	CPAB to Bn or CPBA to An	see Figure 7	1.7	2.6	4.1	ns
t_{PZH}	output enable time to HIGH-level	see Figure 9	2.2	3.3	4.5	ns
t_{PZL}	output enable time to LOW-level	see Figure 10	1.6	2.5	3.6	ns
t_{PHZ}	output disable time from HIGH-level	see Figure 9	2.7	3.6	4.9	ns
t_{PLZ}	output disable time from LOW-level	see Figure 10	2.1	3.0	4.0	ns
$t_{h(H)}$	hold time HIGH					
	An to CPAB or Bn to CPBA	see Figure 8	+1.0	-0.6	-	ns
	An to LEAB or Bn to LEAB	see Figure 8	1.0	0.1	-	ns
$t_{h(L)}$	hold time LOW					
	An to CPAB or Bn to CPBA	see Figure 8	+1.0	-0.3	-	ns
	An to LEAB or Bn to LEAB	see Figure 8	1.5	0.6	-	ns
$t_{su(H)}$	set-up time HIGH					
	An to CPAB or Bn to CPBA	see Figure 8	2.0	0.5	-	ns
	An to LEAB or Bn to LEBA	see Figure 8	+1.0	-0.6	-	ns
$t_{su(L)}$	set-up time LOW					
	An to CPAB or Bn to CPBA	see Figure 8	2.0	0.7	-	ns
	An to LEAB or Bn to LEBA	see Figure 8	+1.0	-0.1	-	ns
t_{WH}	pulse width HIGH					
	CPAB or CPBA	see Figure 7	2.0	-	-	ns
	LEAB or LEBA	see Figure 6	1.5	-	-	ns
t_{WL}	pulse width LOW					
	CPAB or CPBA	see Figure 7	2.0	-	-	ns
f_{max}	maximum clock frequency	see Figure 7	150	-	-	MHz

[1] All typical values are measured at $V_{CC} = 2.5\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[2] All typical values are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$.

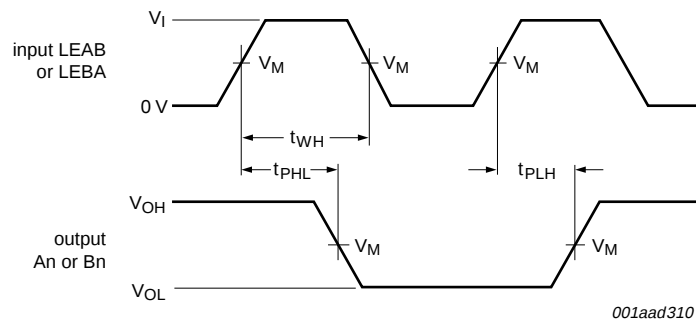
12. Waveforms



Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

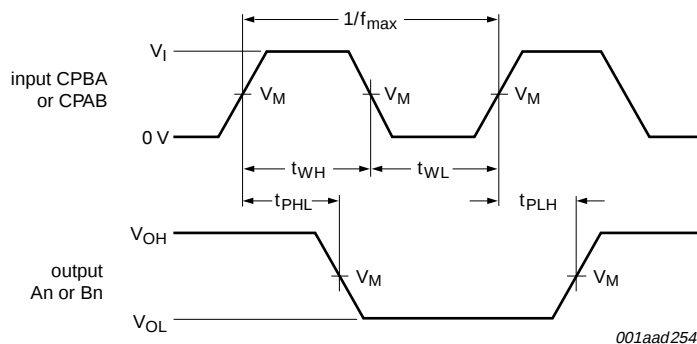
Fig 5. Propagation delay input (An, Bn) to output (Bn, An) in transparent mode



Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

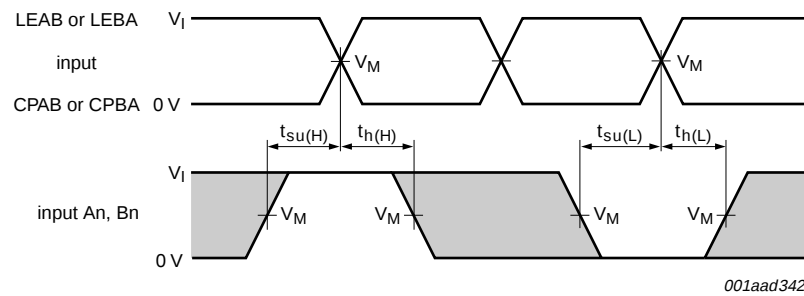
Fig 6. Propagation delay latch enable (LEAB, LEBA) to output (An, Bn) and latch enable (LEAB, LEBA) pulse width



Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

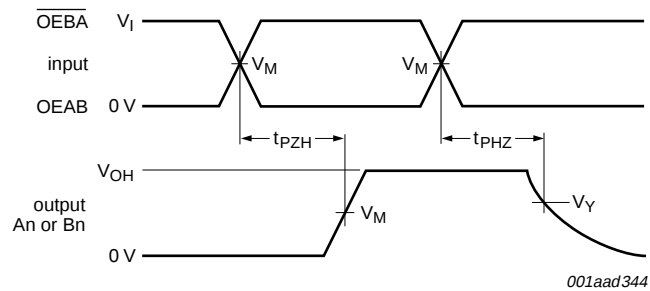
Fig 7. Propagation delay clock (CPAB, CPBA) to output (An, Bn), clock (CPAB, CPBA) pulse width and maximum clock frequency (CPAB, CPBA)



Measurement points are given in [Table 9](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

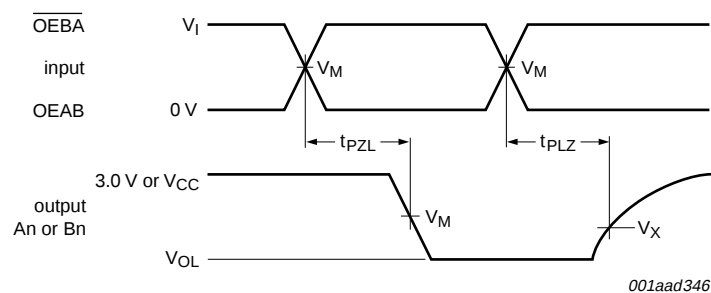
Fig 8. Data setup and hold times



Measurement points are given in [Table 9](#).

V_{OH} is typical voltage output drop that occur with the output load.

Fig 9. 3-state output enable time to HIGH-level and output disable time from HIGH-level



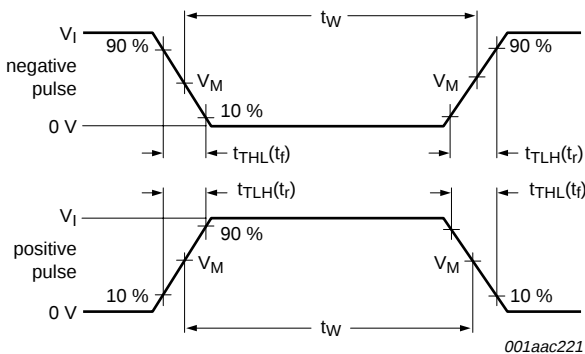
Measurement points are given in [Table 9](#).

V_{OL} is typical voltage output drop that occur with the output load.

Fig 10. 3-state output enable time to LOW-level and output disable time from LOW-level

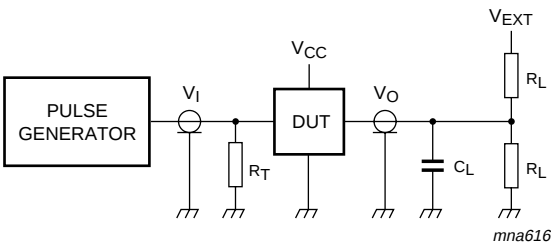
Table 9: Measurement points

Supply voltage	Input	Output		
	V _M	V _M	V _X	V _Y
≥ 3.0 V	1.5 V	1.5 V	V _{OL} + 0.30 V	V _{OH} - 0.30 V
≤ 2.7 V	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V



Measurement points are given in [Table 9](#).

a. Input pulse definition



Test data is given in [Table 10](#).

Definitions test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

b. Test circuit

Fig 11. Load circuitry for switching times

Table 10: Test data

Input				Load		V _{EXT}			
V _I	f _i	t _w	t _r , t _f	C _L	R _L	t _{PLZ} , t _{PZL}	t _{PLH} , t _{PHL}	t _{PHZ} , t _{PZH}	
3.0 V or V _{CC} whichever is less	≤ 10 MHz	500 ns	≤ 2.5 ns	30 pF or 50 pF	500 Ω	6 V or 2 × V _{CC}	open	GND	

13. Package outline

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

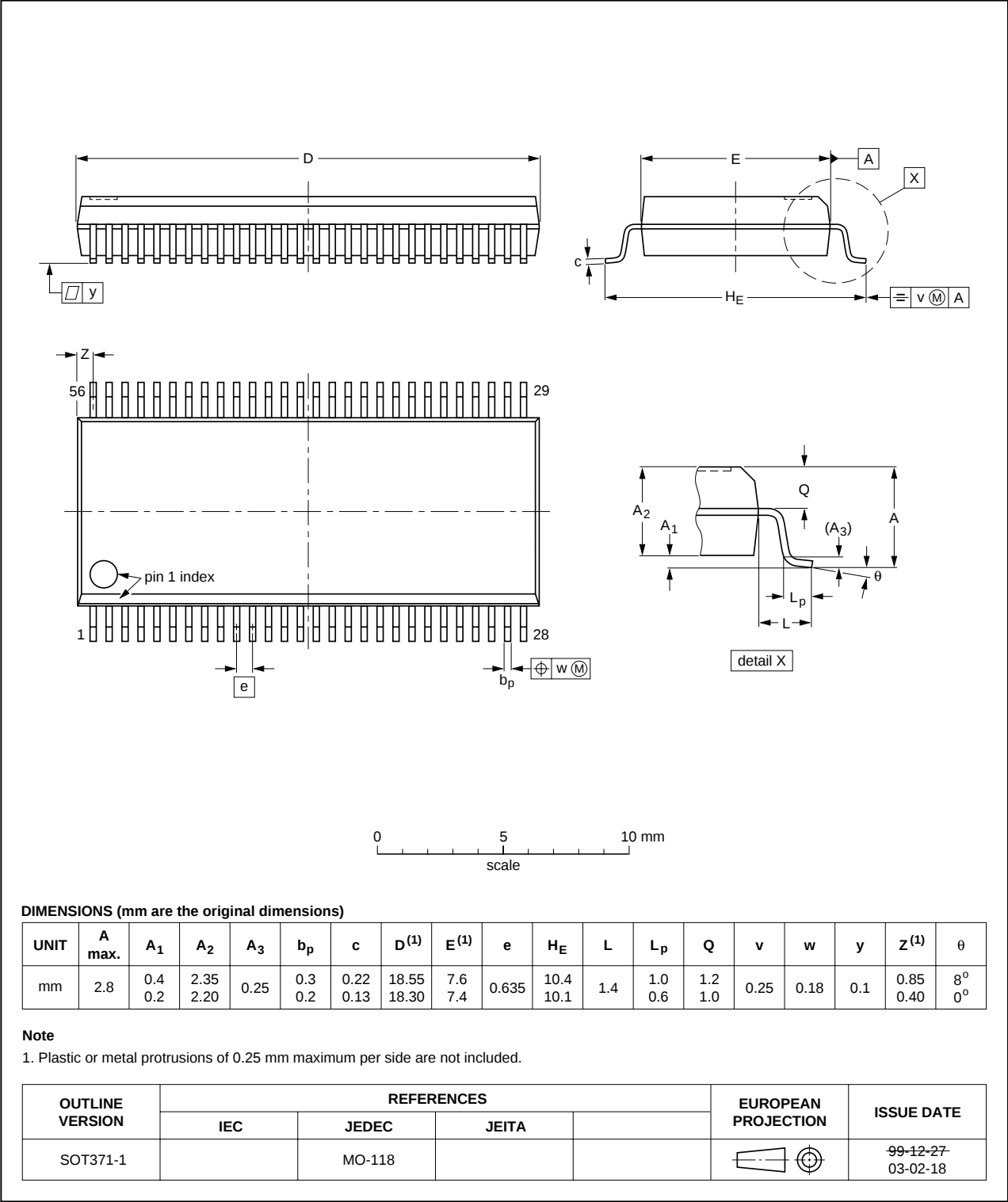


Fig 12. Package outline SOT371-1 (SSOP56)

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

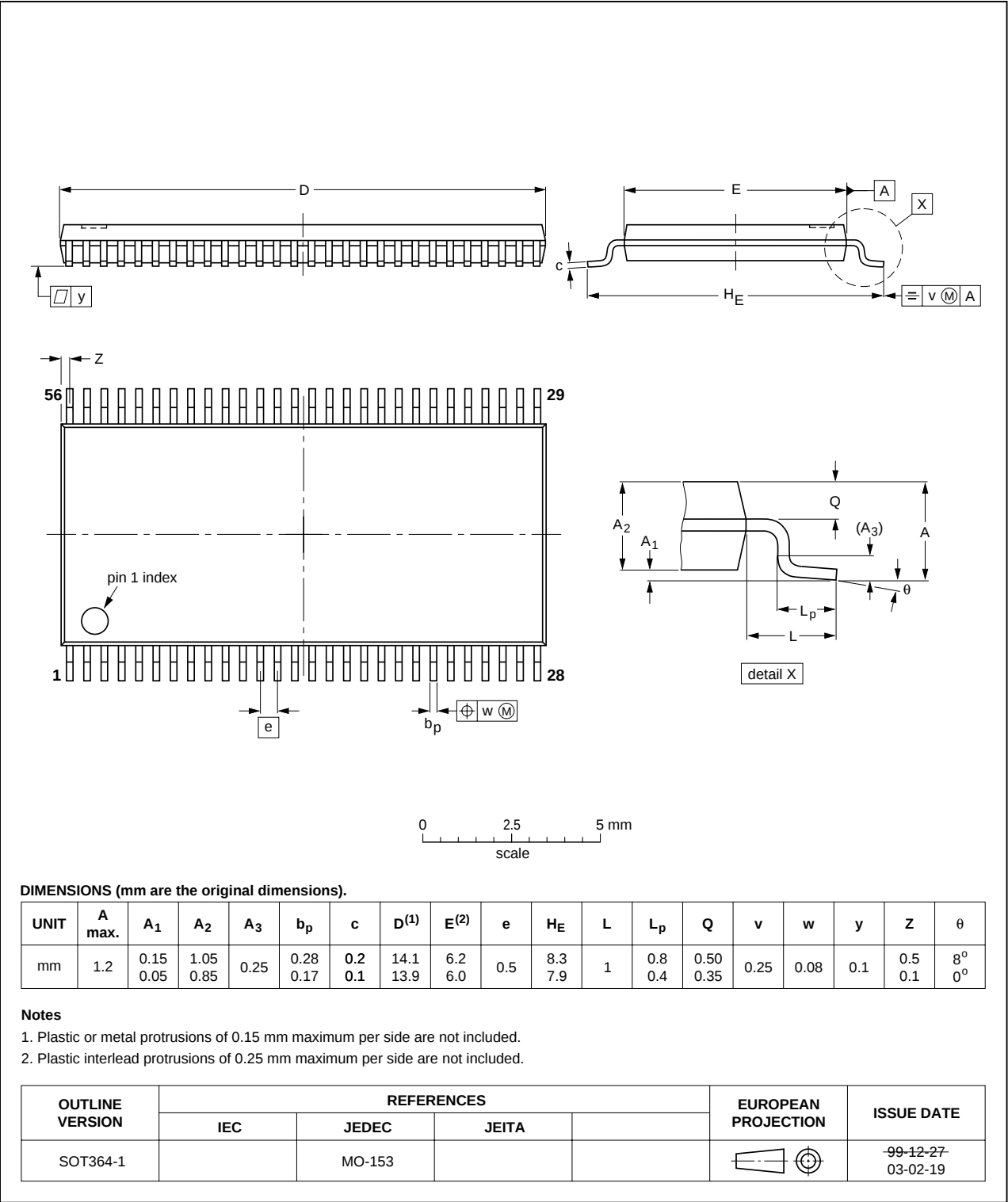


Fig 13. Package outline SOT364-1 (TSSOP56)

14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74ALVT16501_4	20050808	Product data sheet	-	-	74ALVT16501_3
Modifications:					
- The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Section 2 “Features”: modified ‘JEDEC Std. 17’ into ‘JESD78’. Table 8 “Dynamic characteristics”: changed maximum values of propagation delay, output enable time and output disable time.					
74ALVT16501_3	19980213	Product specification	-	9397 750 03567	74ALVT16501_2
74ALVT16501_2	-	-	-	-	74ALVT16501_1
74ALVT16501_1	-	-	-	-	-

15. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

18. Trademarks

Notice — All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors

19. Contact information

For additional information, please visit: <http://www.semiconductors.philips.com>

For sales office addresses, send an email to: sales.addresses@www.semiconductors.philips.com



20. Contents

1 General description 1

2 Features 1

3 Quick reference data 2

4 Ordering information 2

5 Functional diagram 3

6 Pinning information 5

6.1 Pinning 5

6.2 Pin description 5

7 Functional description 7

7.1 Function table 7

8 Limiting values 8

9 Recommended operating conditions 8

10 Static characteristics 9

11 Dynamic characteristics 11

12 Waveforms 13

13 Package outline 16

14 Revision history 18

15 Data sheet status 19

16 Definitions 19

17 Disclaimers 19

18 Trademarks 19

19 Contact information 19



© Koninklijke Philips Electronics N.V. 2005

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Date of release: 8 August 2005
Document number: 74ALVT16501_4

Published in The Netherlands

AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit www.ameya360.com

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com