SN74AVC4T774 4-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs

1 Features

- Each Channel Has an Independent DIR Control Input
- Control Inputs V_{IH}/V_{IL} Levels are Referenced to V_{CCA} Voltage
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- I/Os are 4.6-V Tolerant
- I_{off} Supports Partial Power-Down-Mode Operation
- Typical Data Rates
  - 380 Mbps (1.8-V to 3.3-V Translation)
  - 200 Mbps (<1.8-V to 3.3-V Translation)
  - 200 Mbps (Translate to 2.5 V or 1.8 V)
  - 150 Mbps (Translate to 1.5 V)
  - 100 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds the Following Levels (Tested Per JESD 22)
  - ±8000-V Human-Body Model (A114-A)
  - 250-V Machine Model (A115-A)
  - ±1500-V Charged-Device Model (C101)

2 Applications

- Personal Electronic
- Industrial
- Enterprise
- Telecom

3 Description

This 4-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2 to 3.6 V. The SN74AVC4T774 is optimized to operate with V_{CCA}/V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA}/V_{CCB} as low as 1.2 V. This allows for universal low-voltage bi-directional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

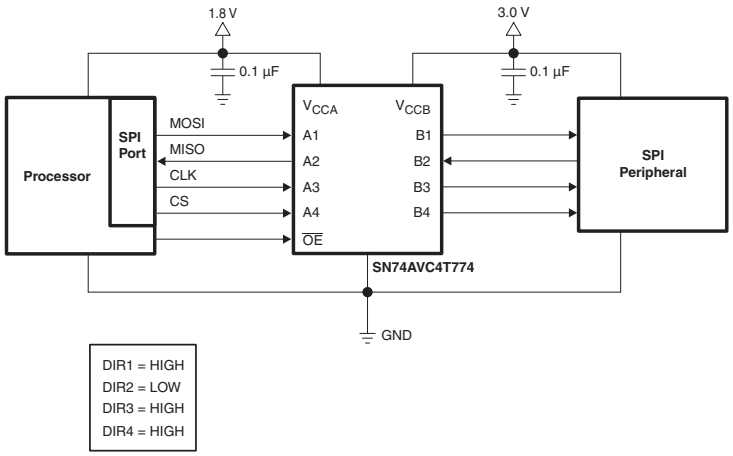
The SN74AVC4T774 is designed for asynchronous communication between data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports in the high-impedance mode. The device transmits data from the A bus to the B bus when the B outputs are activated, and from the B bus to the A bus when the A outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AVC4T774	TSSOP (16)	5.00 mm × 4.40 mm
	VQFN (16)	4.00 mm × 3.50 mm
	UQFN (16)	2.60 mm × 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



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4 Revision History

Changes from Revision C (December 2014) to Revision D **Page**

- Changed Pin Functions table order for Pins B4, B3, B2 and B1 ... 4

Changes from Revision B (May 2008) to Revision C **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

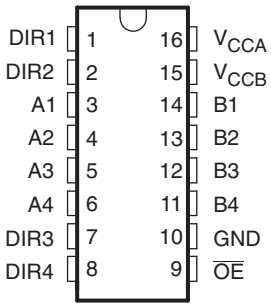
5 Description (continued)

The SN74AVC4T774 is designed so that the control pins (DIR1, DIR2, DIR3, DIR4, and $\overline{OE}$) are supplied by V_{CCA}. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

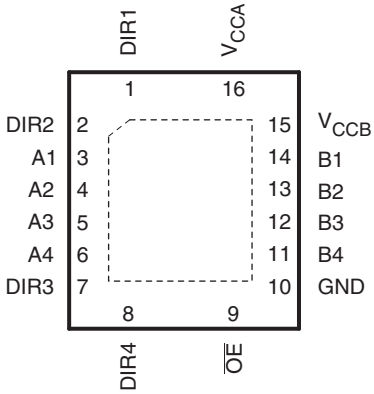
To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CCA} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Since this device has CMOS inputs, it is very important to not allow them to float. If the inputs are not driven to either a high V_{CC} state, or a low-GND state, an undesirable larger than expected I_{CC} current may result. Since the input voltage settlement is governed by many factors (for example, capacitance, board-layout, package inductance, surrounding conditions, and so forth), ensuring that they these inputs are kept out of erroneous switching states and tying them to either a high or a low level minimizes the leakage-current.

6 Pin Configuration and Functions

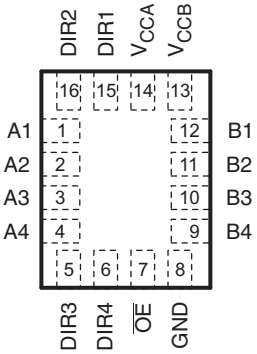
PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



RSV PACKAGE
(TOP VIEW)



(1) Shown for a single channel

Pin Functions

PIN			I/O	DESCRIPTION
NAME	PW RGY	RSV		
DIR1	1	15	I	Direction-control input for ‘1’ channel
DIR2	2	16	I	Direction-control input for ‘2’ channel
A1	3	1	I/O	Input/output A1. Referenced to V_{CCA}
A2	4	2	I/O	Input/output A2. Referenced to V_{CCA}
A3	5	3	I/O	Input/output A3. Referenced to V_{CCA}
A4	6	4	I/O	Input/output A4. Referenced to V_{CCA}
DIR3	7	5	I	Direction-control input for ‘3’ channel
DIR4	8	6	I	Direction-control input for ‘4’ channel
$\overline{OE}$	9	7	I	3-state output-mode enables. Pull $\overline{OE}$ high to place all outputs in 3-state mode. Referenced to V_{CCA}.
GND	10	8	G	Ground
B4	11	9	I/O	Input/output B4. Referenced to V_{CCB}
B3	12	10	I/O	Input/output B3. Referenced to V_{CCB}
B2	13	11	I/O	Input/output B2. Referenced to V_{CCB}
B1	14	12	I/O	Input/output B1. Referenced to V_{CCB}
V_{CCB}	15	13	P	B-port supply voltage. 1.2 V ≤ V_{CCB} ≤ 3.6 V
V_{CCA}	16	14	P	A-port supply voltage. 1.2 V ≤ V_{CCA} ≤ 3.6 V

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state(2)(3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
	Machine Model (A115-A)	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

See (1)(2)(3).

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs(4)	1.2 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs(4)	1.2 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V

Recommended Operating Conditions (continued)

See (1)(2)(3).

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})(5) (DIRx, $\overline{OE}$)	1.2 V to 1.95 V		V_{CCA} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})(5) (DIRx, $\overline{OE}$)	1.2 V to 1.95 V			V_{CCA} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.1 V to 1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.1 V to 1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(5) For V_{CCA} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V

7.4 Thermal Information

THERMAL METRIC(1)		SN74AVC4T774			UNIT
		PW	RGY	RSV	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.2	37.7	139.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	56.1	64.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	63.3	15.9	67.7	
ψ_{JT}	Junction-to-top characterization parameter	8.8	0.5	1.7	
ψ_{JB}	Junction-to-board characterization parameter	62.7	16.1	67.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics[1][2][3]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}		I_{OH} = –100 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				V_{CCO} – 0.2			V
		I_{OH} = –3 mA		1.2 V	1.2 V		0.95					
		I_{OH} = –6 mA		1.4 V	1.4 V				1.05			
		I_{OH} = –8 mA		1.65 V	1.65 V				1.2			
		I_{OH} = –9 mA		2.3 V	2.3 V				1.75			
		I_{OH} = –12 mA		3 V	3 V				2.3			
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V						0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V		0.25					
		I_{OL} = 6 mA		1.4 V	1.4 V						0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V						0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V						0.55	
		I_{OL} = 12 mA		3 V	3 V						0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25			±1	µA
I_{off}	A or B port	V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V		±0.1	±1			±5	µA
				0 V to 3.6 V	0 V		±0.1	±1			±5	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V		±0.5	±2.5			±5	µA
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V						8	µA
				0 V	0 V to 3.6 V						–2	
				0 V to 3.6 V	0 V						8	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V						8	µA
				0 V	0 V to 3.6 V						8	
				0 V to 3.6 V	0 V						–2	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V						16	µA
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		2.5				3	pF
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V		5				6	pF

(1) All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) V_{CCI} is the V_{CC} associated with the input port.

7.6 Switching Characteristics V_{CCA} = 1.2 V

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V	V_{CCB} = 2.5 V ± 0.2 V	V_{CCB} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	3.5	2.8	2.7	2.7	3.1	ns
t_{PHL}			3.5	2.8	2.7	2.7	3.1	
t_{PLH}	B	A	3.8	3.4	3.2	3	2.9	ns
t_{PHL}			3.8	3.4	3.2	3	2.9	
t_{PZH}	$\overline{OE}$	A	6	4.8	4.4	5.3	9.3	ns
t_{PZL}			6	4.8	4.4	5.3	9.3	
t_{PZH}	$\overline{OE}$	B	6.7	6.7	6.6	6.7	6.6	ns
t_{PZL}			6.7	6.7	6.6	6.7	6.6	
t_{PHZ}	$\overline{OE}$	A	4.3	3.6	3.7	3.3	4	ns
t_{PLZ}			4.3	3.6	3.7	3.3	4	
t_{PHZ}	$\overline{OE}$	B	4.4	4.4	4.4	4.4	4.4	ns
t_{PLZ}			4.4	4.4	4.4	4.4	4.4	

7.7 Switching Characteristics V_{CCA} = 1.5 V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.1	0.3	4.4	0.2	3.9	0.1	3.6	0.1	3.9	ns
t_{PHL}			3.1	0.3	4.4	0.2	3.9	0.1	3.6	0.1	3.9	
t_{PLH}	B	A	2.9	0.6	5.1	0.4	4.9	0.2	4.6	0.1	4.5	ns
t_{PHL}			2.9	0.6	5.1	0.4	4.9	0.2	4.6	0.1	4.5	
t_{PZH}	$\overline{OE}$	A	5.3	1.1	7.1	0.9	6.2	0.7	5.5	0.1	6.4	ns
t_{PZL}			5.3	1.1	7.1	0.9	6.2	0.7	5.5	0.1	6.4	
t_{PZH}	$\overline{OE}$	B	4.4	1.1	8.2	1.1	8.2	1.1	8.2	1.1	8.2	ns
t_{PZL}			4.4	1.1	8.2	1.1	8.2	1.1	8.2	1.1	8.2	
t_{PHZ}	$\overline{OE}$	A	3.6	1.2	4.8	0.8	5.4	0.4	5.1	1	5.4	ns
t_{PLZ}			3.6	1.2	4.8	0.8	5.4	0.4	5.1	1	5.4	
t_{PHZ}	$\overline{OE}$	B	3.1	0.3	5.6	0.2	5.7	0.3	5.6	0.3	56	ns
t_{PLZ}			3.1	0.3	5.6	0.2	5.7	0.3	5.6	0.3	5.6	

7.8 Switching Characteristics V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.8	0.1	4.1	0.1	3.6	0.1	3.1	0.1	3.3	ns
t_{PHL}			2.8	0.1	4.1	0.1	3.6	0.1	3.1	0.1	3.3	
t_{PLH}	B	A	2.6	0.4	4.3	0.1	4.1	0.1	3.8	0.1	3.7	ns
t_{PHL}			2.6	0.4	4.3	0.1	4.1	0.1	3.8	0.1	3.7	
t_{PZH}	$\overline{OE}$	A	5	0.8	6.7	0.6	5.8	0.4	4.8	0.3	4.6	ns
t_{PZL}			5	0.8	6.7	0.6	5.8	0.4	4.8	0.3	4.6	
t_{PZH}	$\overline{OE}$	B	3.3	0.2	6.7	0.2	6.6	0.2	6.7	0.2	6.7	ns
t_{PZL}			3.3	0.2	6.7	0.2	6.6	0.2	6.7	0.2	6.7	
t_{PHZ}	$\overline{OE}$	A	3.4	0.7	4.7	0.3	5.1	0.1	4.5	0.8	5	ns
t_{PLZ}			3.4	0.7	4.7	0.3	5.1	0.1	4.5	0.8	5	
t_{PHZ}	$\overline{OE}$	B	2.9	0.1	5.7	0.1	5.8	0.1	5.8	0.1	5.8	ns
t_{PLZ}			2.9	0.1	5.7	0.1	5.8	0.1	5.8	0.1	5.8	

7.9 Switching Characteristics V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.6	0.1	3.8	0.1	3.2	0.1	2.7	0.1	2.6	ns
t_{PHL}			2.6	0.1	3.8	0.1	3.2	0.1	2.7	0.1	2.6	
t_{PLH}	B	A	2.5	0.5	3.4	0.2	3.1	0.1	2.8	0.1	2.6	ns
t_{PHL}			2.5	0.5	3.4	0.2	3.1	0.1	2.8	0.1	2.6	
t_{PZH}	$\overline{OE}$	A	4.7	0.7	6.2	0.5	5.2	0.3	4.1	0.3	3.6	ns
t_{PZL}			4.7	0.7	6.2	0.5	5.2	0.3	4.1	0.3	3.6	
t_{PZH}	$\overline{OE}$	B	2.3	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns
t_{PZL}			2.3	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	
t_{PHZ}	$\overline{OE}$	A	3	0.2	4.3	0.1	4.9	0.1	4	0.7	4.3	ns
t_{PLZ}			3	0.2	4.3	0.1	4.9	0.1	4	0.7	4.3	
t_{PHZ}	$\overline{OE}$	B	1.9	01	4.7	0.1	4.6	0.1	4.7	0.1	4.7	ns
t_{PLZ}			1.9	01	4.7	0.1	4.6	0.1	4.7	0.1	4.7	

7.10 Switching Characteristics V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.5	0.1	3.6	0.1	3	0.1	2.6	0.1	2.4	ns
t_{PHL}			2.5	0.1	3.6	0.1	3	0.1	2.6	0.1	2.4	
t_{PLH}	B	A	2.6	0.5	3.4	0.2	2.9	0.1	2.5	0.1	2.3	ns
t_{PHL}			2.6	0.5	3.4	0.2	2.9	0.1	2.5	0.1	2.3	
t_{PZH}	$\overline{OE}$	A	4.5	0.9	5.9	0.5	5	0.3	3.8	0.3	3.3	ns
t_{PZL}			3.8	0.9	5.9	0.5	5	0.3	3.8	0.3	3.3	
t_{PZH}	$\overline{OE}$	B	1.9	0.4	3.6	0.4	3.6	0.4	3.6	0.4	3.6	ns
t_{PZL}			1.9	0.4	3.6	0.4	3.6	0.4	3.6	0.4	3.6	
t_{PHZ}	$\overline{OE}$	A	2.7	0.1	4.2	0.1	4.6	0.3	3.8	0.7	3.9	ns
t_{PLZ}			2.7	0.1	4.2	0.1	4.6	0.3	3.8	0.7	3.9	
t_{PHZ}	$\overline{OE}$	B	2.3	0.1	4.5	0.1	4.5	0.1	4.6	0.1	4.6	ns
t_{PLZ}			2.3	0.1	4.5	0.1	4.5	0.1	4.6	0.1	4.6	

7.11 Typical Characteristics

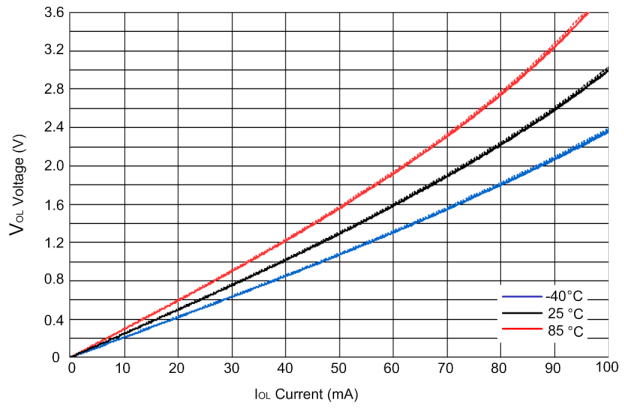


Figure 1. Low-Level Output Voltage (V_{OL}) vs Low-Level Current (I_{OL}) at V_{CCA} = V_{CCB} = 3.6 V

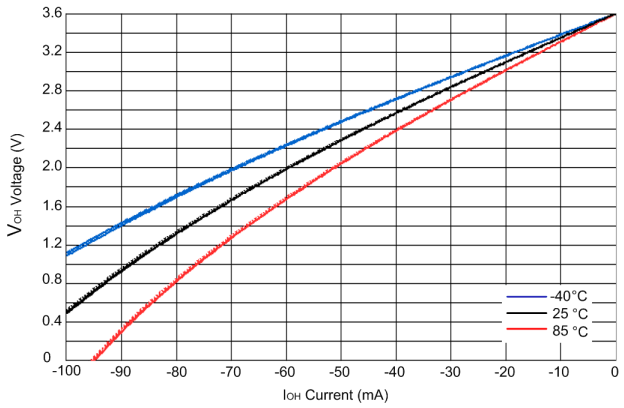
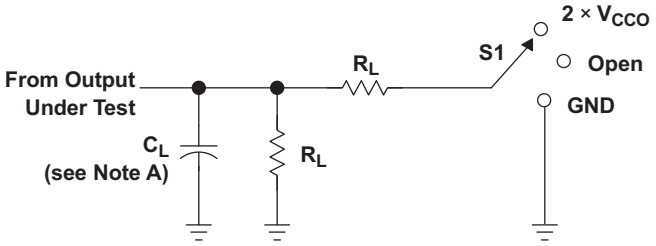


Figure 2. High-Level Output Voltage (V_{OH}) vs High-Level Current (I_{OH}) at V_{CCA} = V_{CCB} = 3.6 V

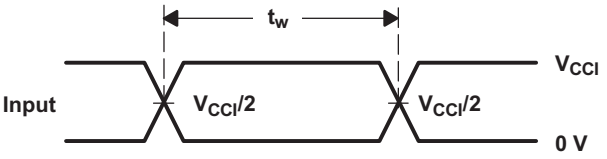
8 Parameter Measurement Information



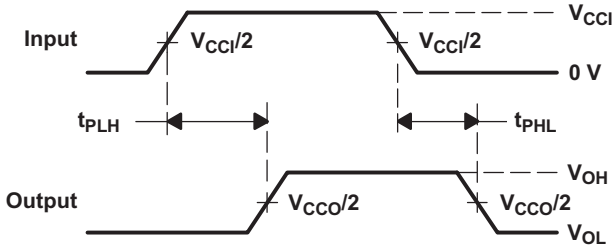
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

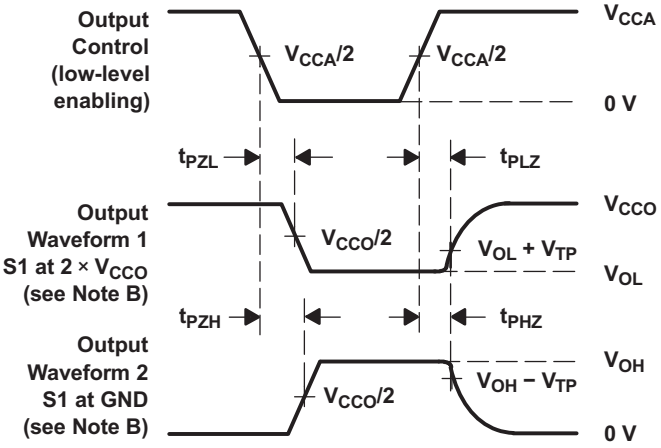
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 3. Load and Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN74AVC4T774 is a 4-bit, dual-supply, noninverting, bi-directional voltage level translation. Pins An and control pins (DIR1, DIR2, DIR3, DIR4 and $\overline{OE}$) are support by V_{CCA} and pins Bn are support by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from An to Bn and a low on DIR allows data transmission from B to A when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both An and Bn are in the high-impedance state.

9.2 Functional Block Diagram

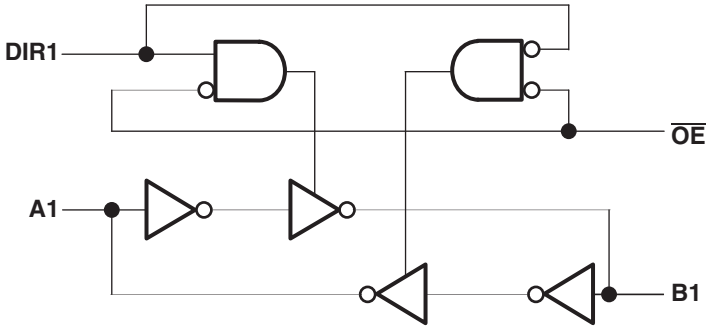


Figure 4. Logic Diagram (Positive Logic)

9.3 Feature Description

9.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.2 V and 3.6 V making the device suitable for translating between any of the low-voltage nodes (1.2 V, 1.8 V, 2.5 V and 3.3 V).

9.3.2 Support High-Speed Translation

SN74AVC4T774 can support high data rate application. The translated signal data rate can be up to 380 Mbps when signal is translated from 1.8 V to 3.3 V.

9.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} will prevent backflow current by disabling I/O output circuits when device is in partial-power-down mode.

9.4 Device Functional Modes

Table 1. Function Table (Each Bit)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74AVC4T774 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVC4T774 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. Its max data rate can be up to 380 Mbps when device translate signal from 1.8 V to 3.3 V.

10.2 Typical Application

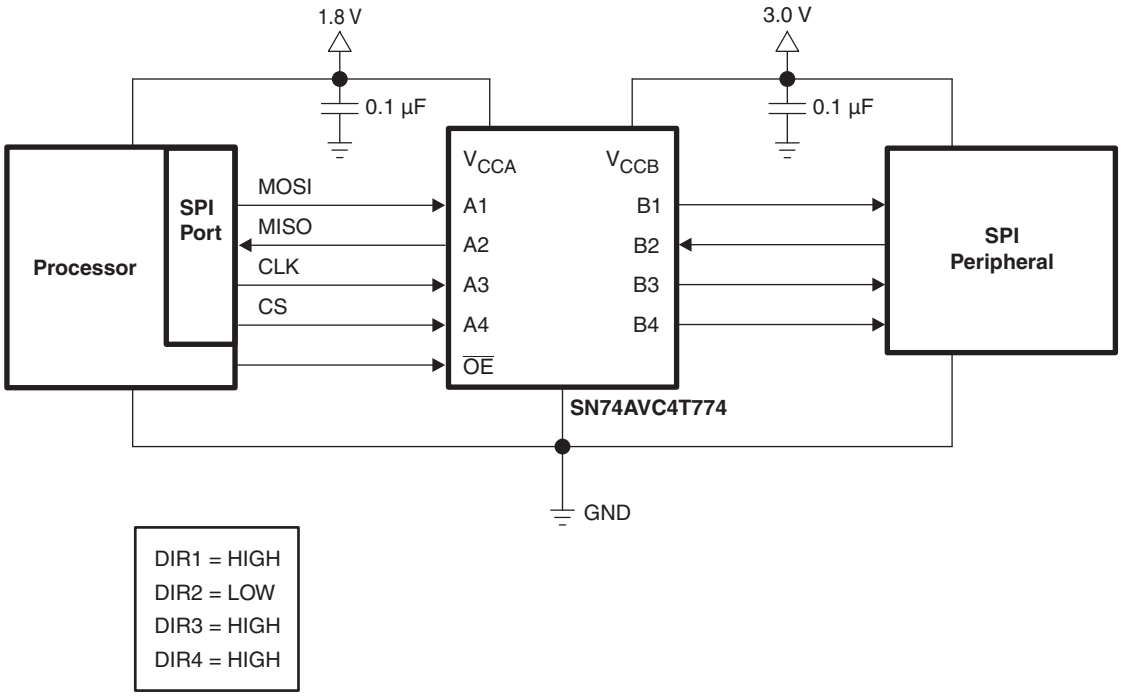


Figure 5. Typical Application of the SN74AVC4T774

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input Voltage Range	1.2 V to 3.6 V
Output Voltage Range	1.2 V to 3.6 V

10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC4T774 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC4T774 device is driving to determine the output voltage range.

10.2.3 Application Curve

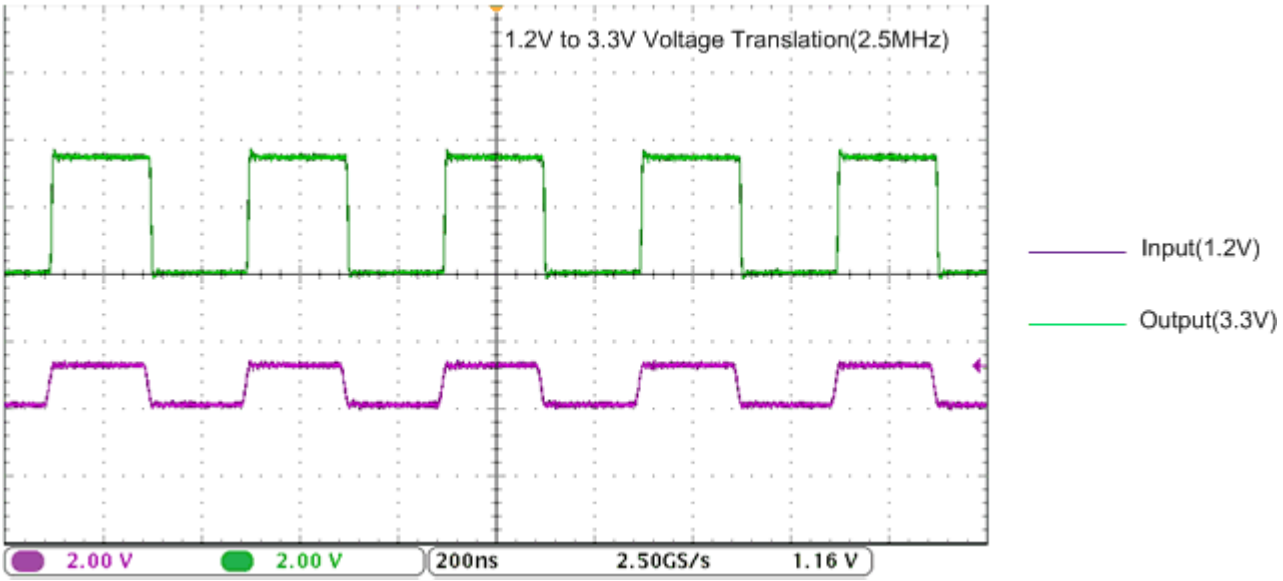


Figure 6. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

11 Power Supply Recommendations

The SN74AVC4T774 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V and V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage, bi-directional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.3-V voltage nodes.

The output-enable $\overline{OE}$ input circuit is designed so that it is supplied by V_{CCA} and when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power-up or power-down, the $\overline{OE}$ input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

12 Layout

12.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements

12.2 Layout Example

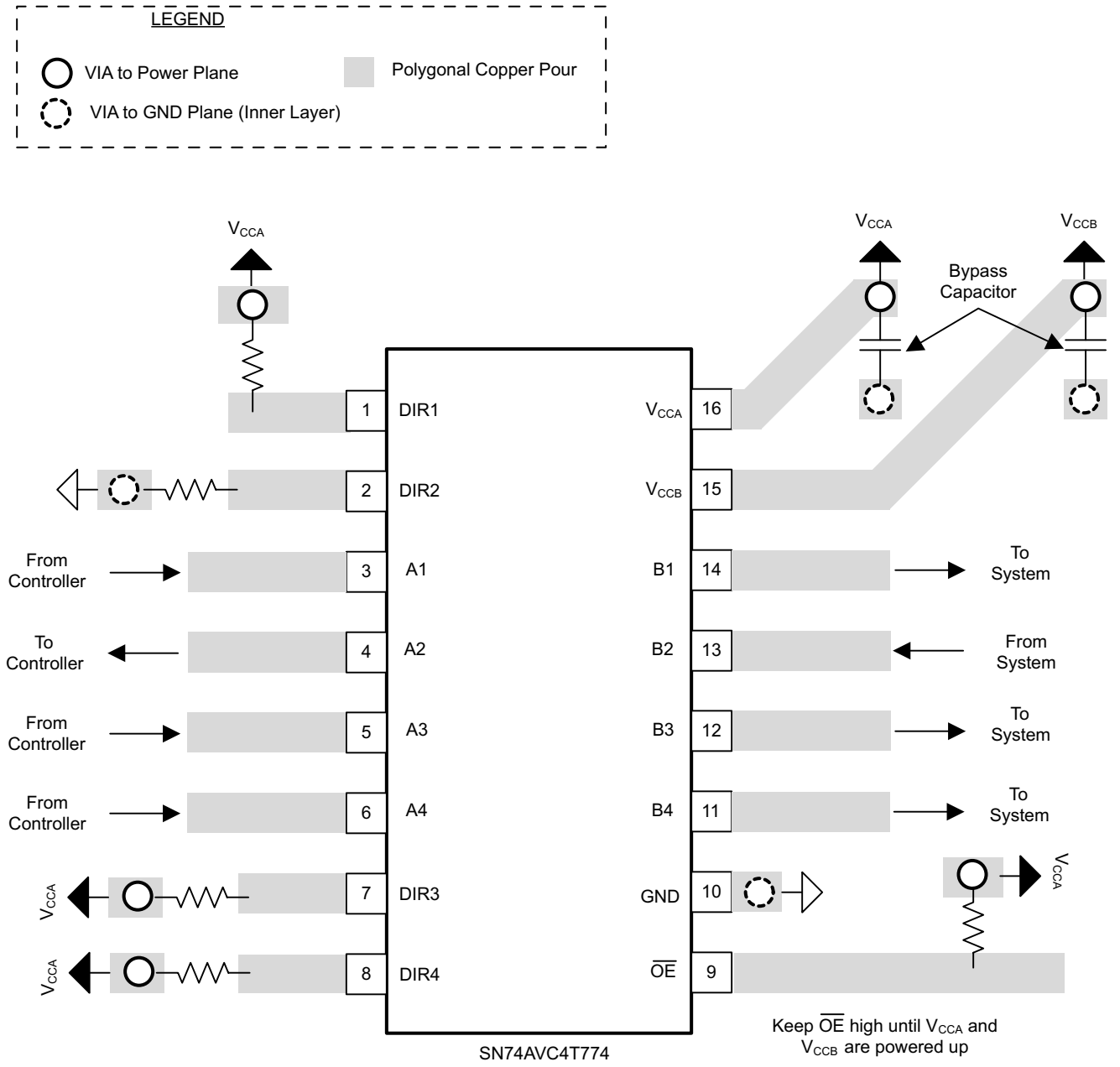


Figure 7. PCB Layout Example

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVC4T774RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT774	Samples
74AVC4T774RSVRG4	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK	Samples
SN74AVC4T774PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774	Samples
SN74AVC4T774PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774	Samples
SN74AVC4T774PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774	Samples
SN74AVC4T774PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774	Samples
SN74AVC4T774RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT774	Samples
SN74AVC4T774RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

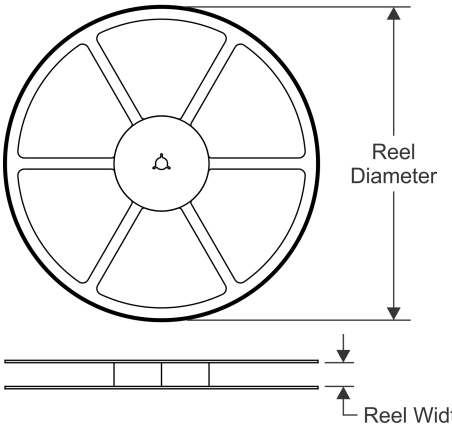
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

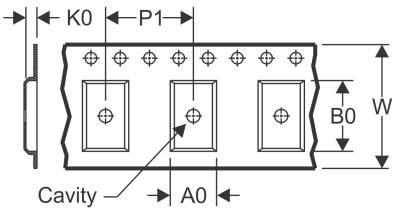
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

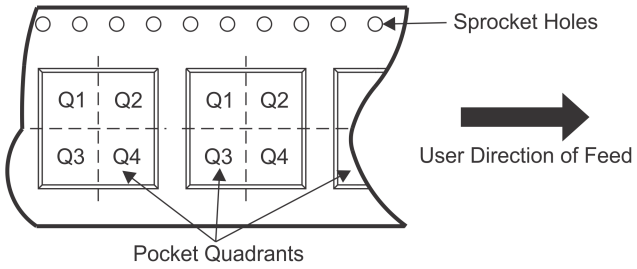


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

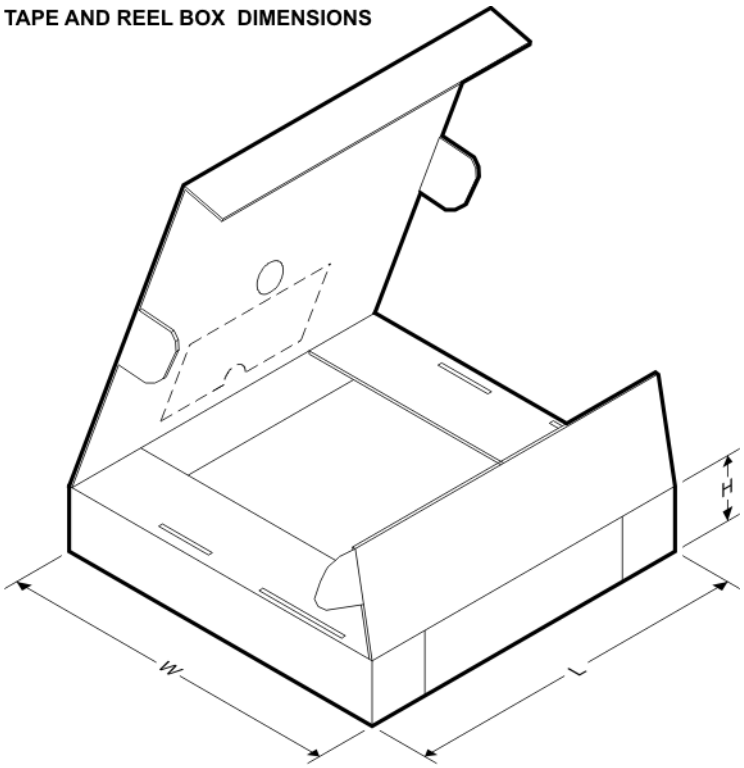
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC4T774PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC4T774RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74AVC4T774RSVR	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

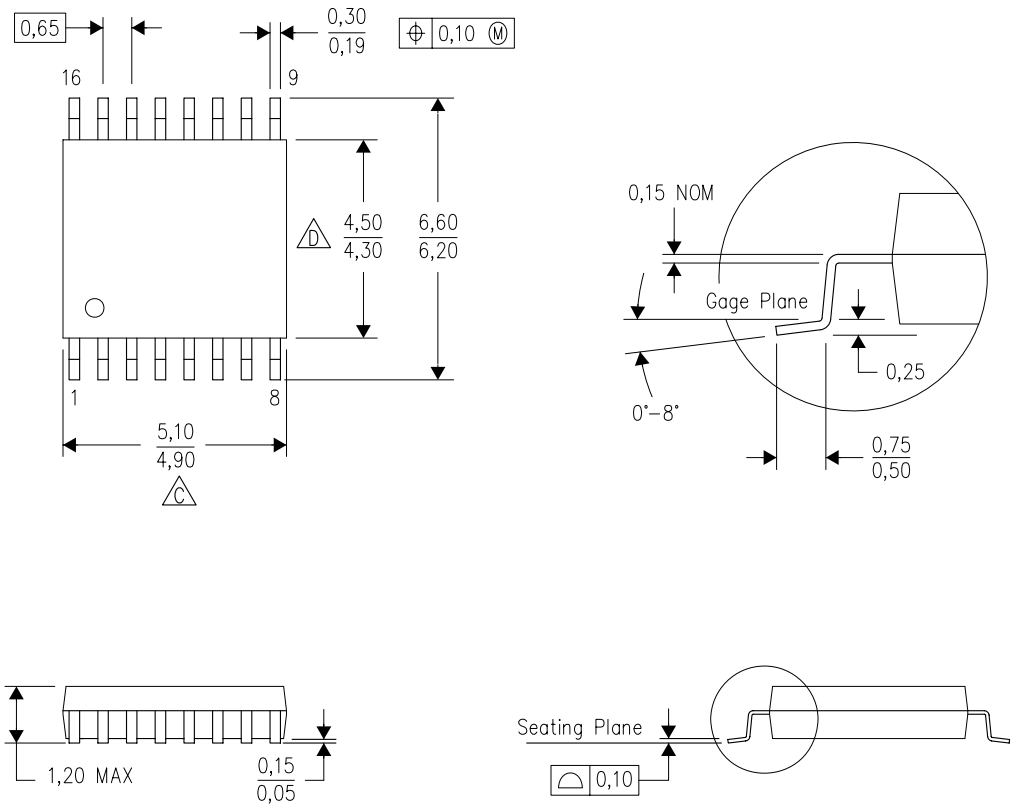
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC4T774PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74AVC4T774RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0
SN74AVC4T774RSVR	UQFN	RSV	16	3000	203.0	203.0	35.0

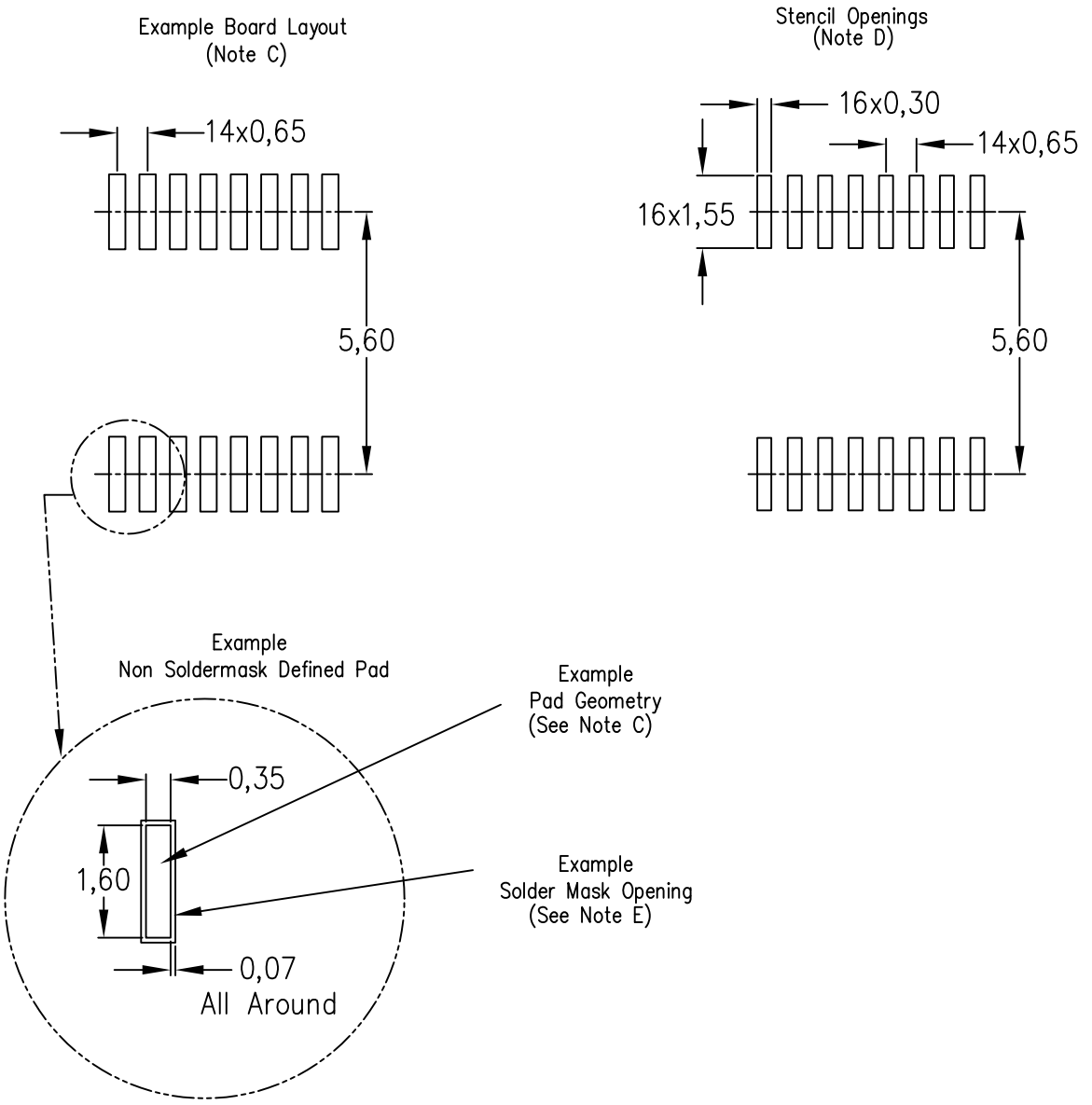
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

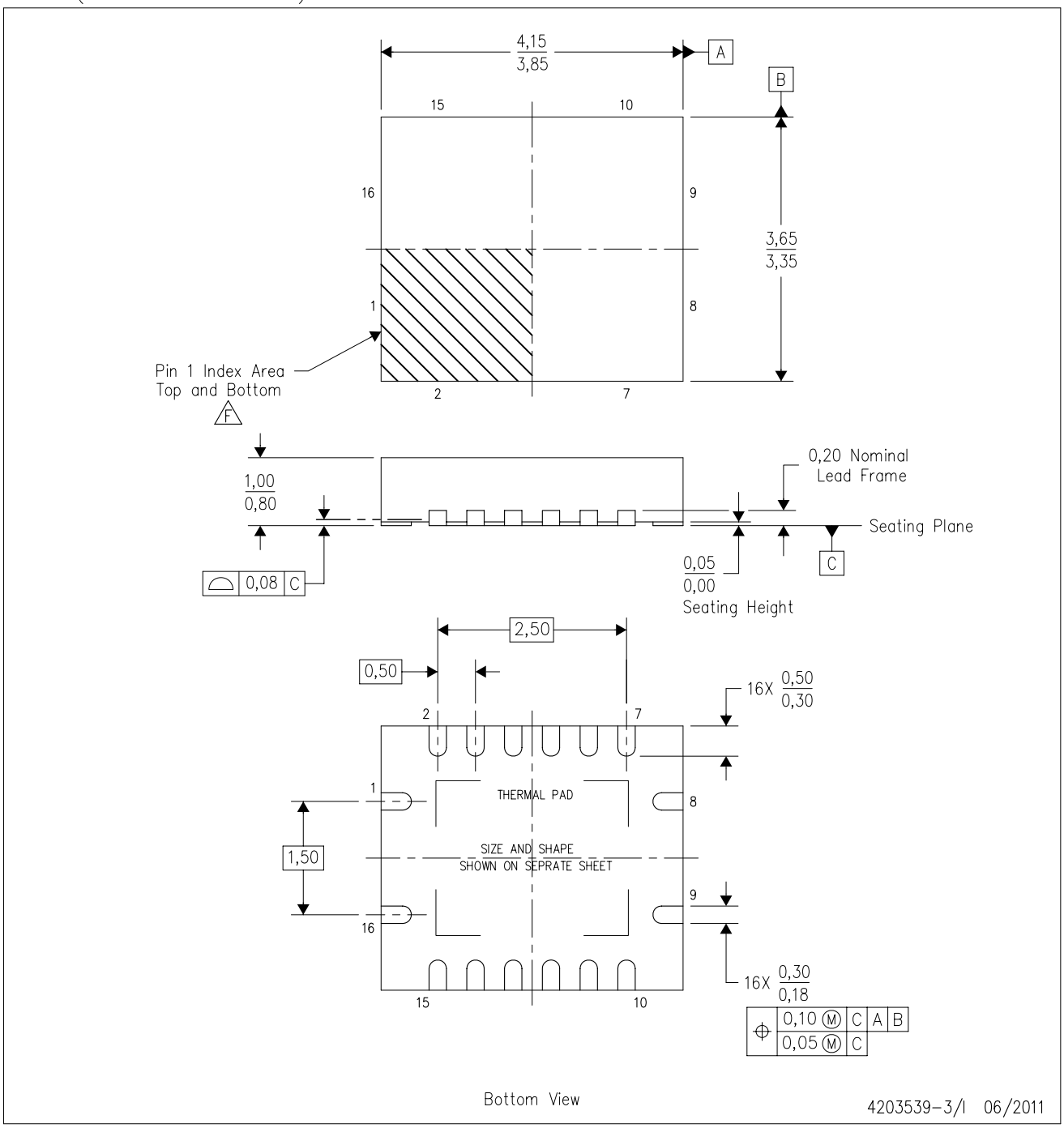
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

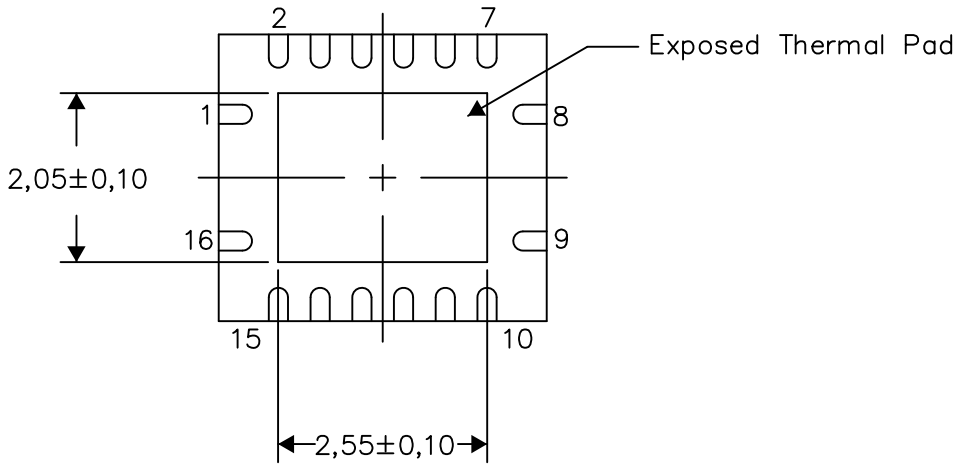
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



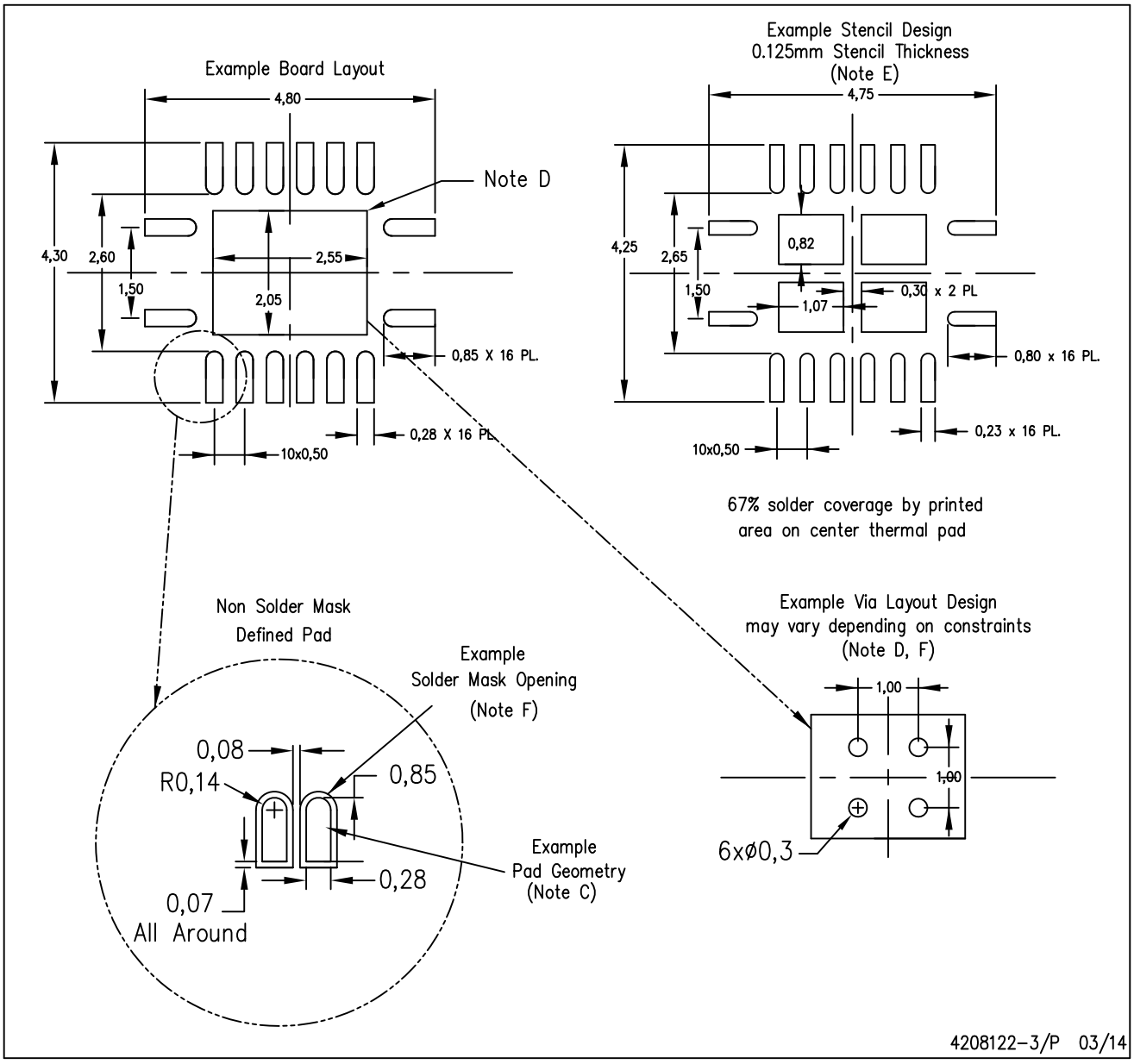
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

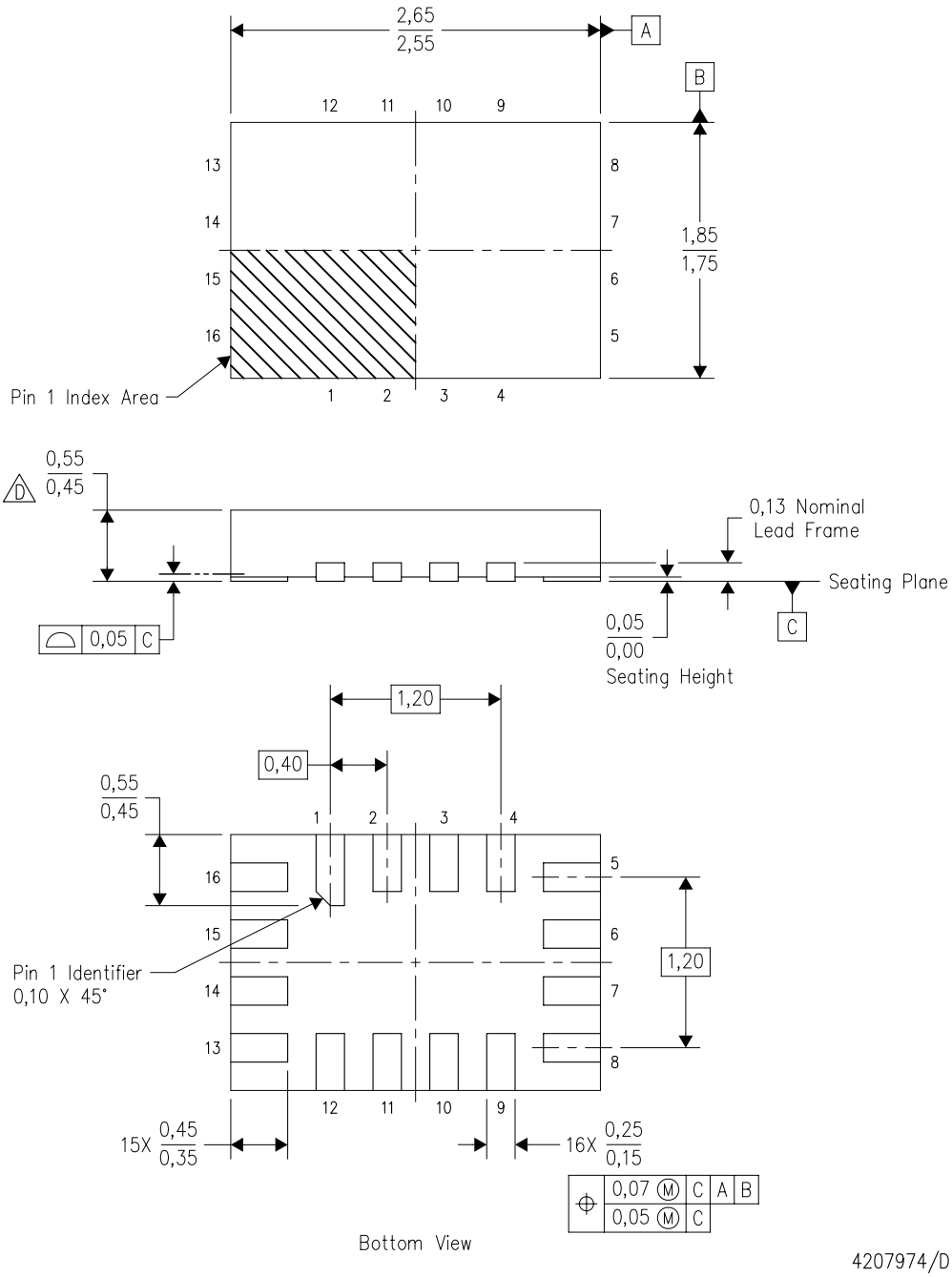
NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



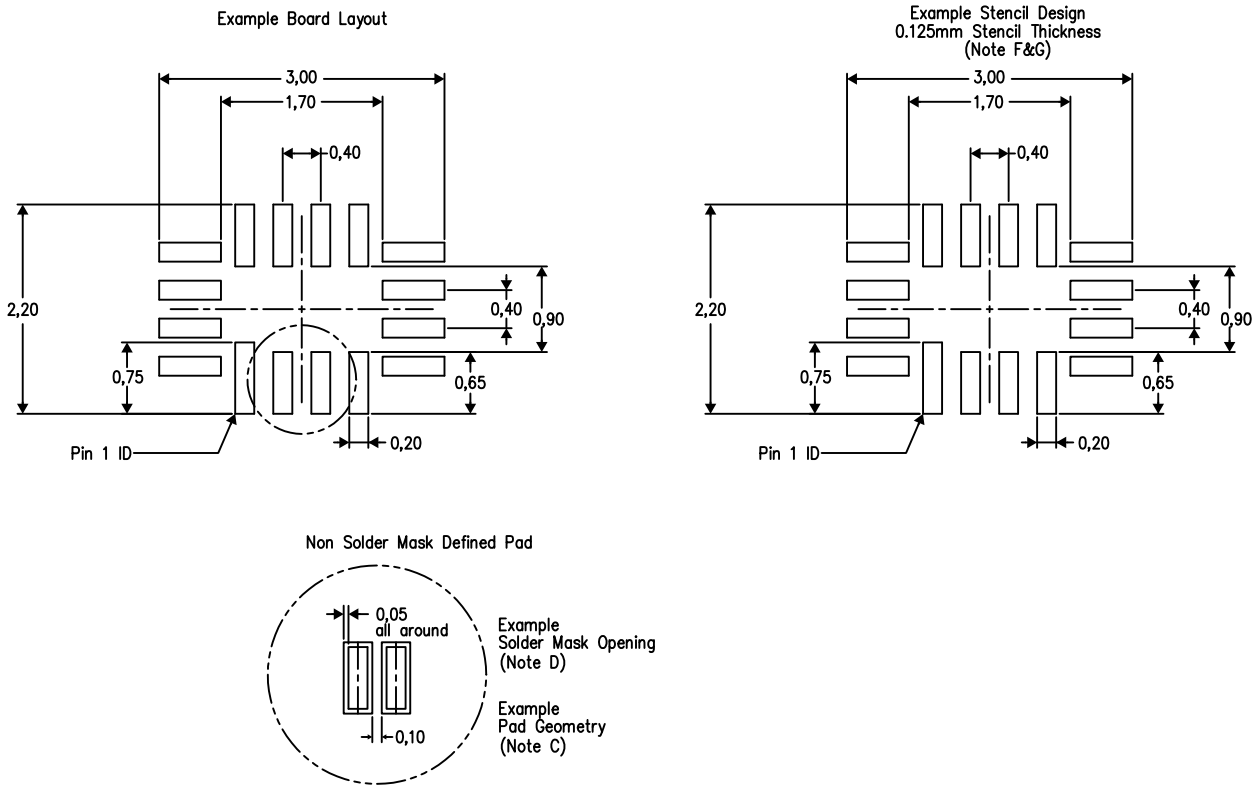
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UFHE, except minimum package thickness.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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