



# PSMN4R3-30BL

N-channel 30 V 4.1 mΩ logic level MOSFET in D2PAK

Rev. 1 — 22 March 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

### 1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

### 1.4 Quick reference data

Table 1. Quick reference data

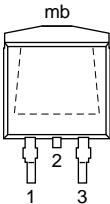
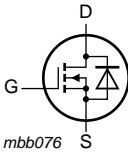
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	30	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> <sup>[1]</sup>	-	-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	103	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 15\text{ A}$ ; $T_j = 100\text{ °C}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	4.9	5.8	mΩ
		$V_{GS} = 10\text{ V}$ ; $I_D = 15\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 13</a>	-	3.5	4.1	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 15\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	5	-	nC
$Q_{G(tot)}$	total gate charge		-	19	-	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $I_D = 100\text{ A}$ ; $V_{sup} \leq 30\text{ V}$ ; $R_{GS} = 50\text{ Ω}$ ; unclamped	-	-	74	mJ

[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain <sup>[1]</sup>		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

[1] It is not possible to make connection to pin 2

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN4R3-30BL	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN4R3-30BL	PSMN4R3-30BL

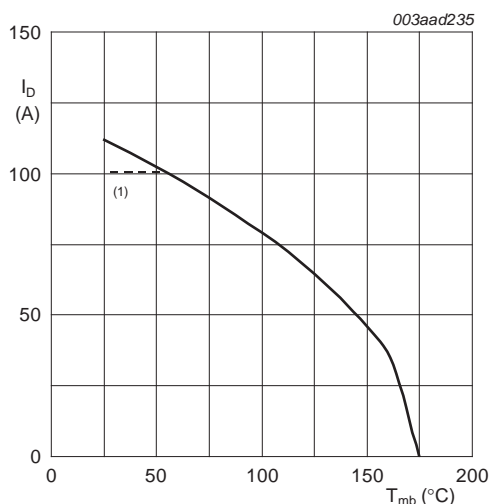
## 5. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

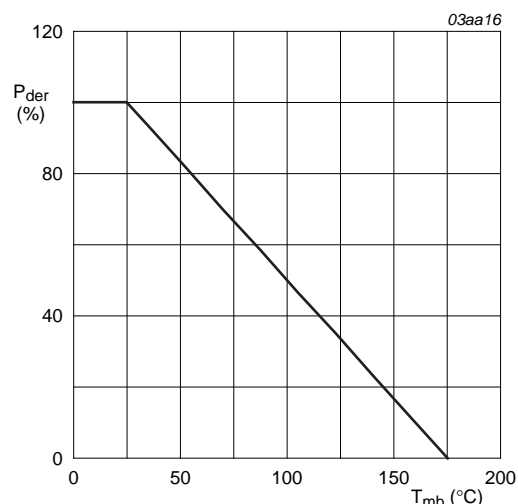
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a> <sup>[1]</sup>	-	80	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> <sup>[1]</sup>	-	100	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	465	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	103	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$ <sup>[1]</sup>	-	100	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	465	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 100\text{ A}$ ; $V_{sup} \leq 30\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped	-	74	mJ

[1] Continuous current is limited by package.



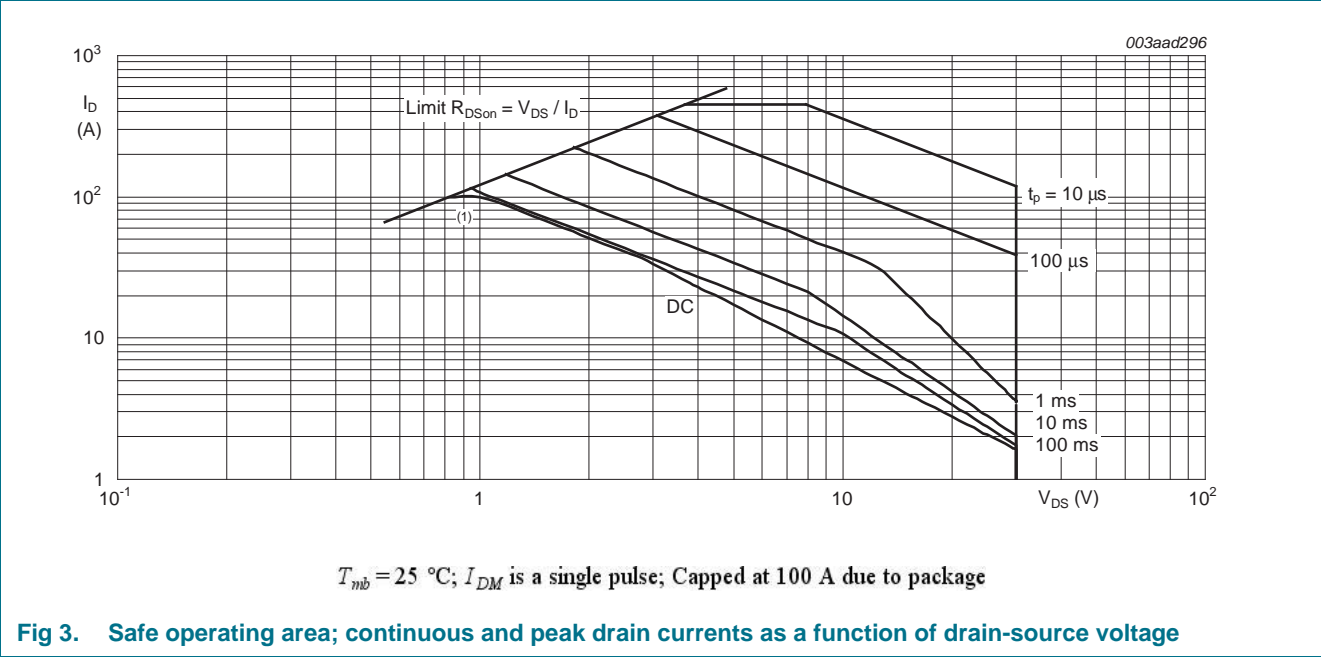
$V_{GS} \geq 10\text{ V}$ ; (1) Capped at 100A due to package

**Fig 1. Continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ °C})}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	1	1.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W

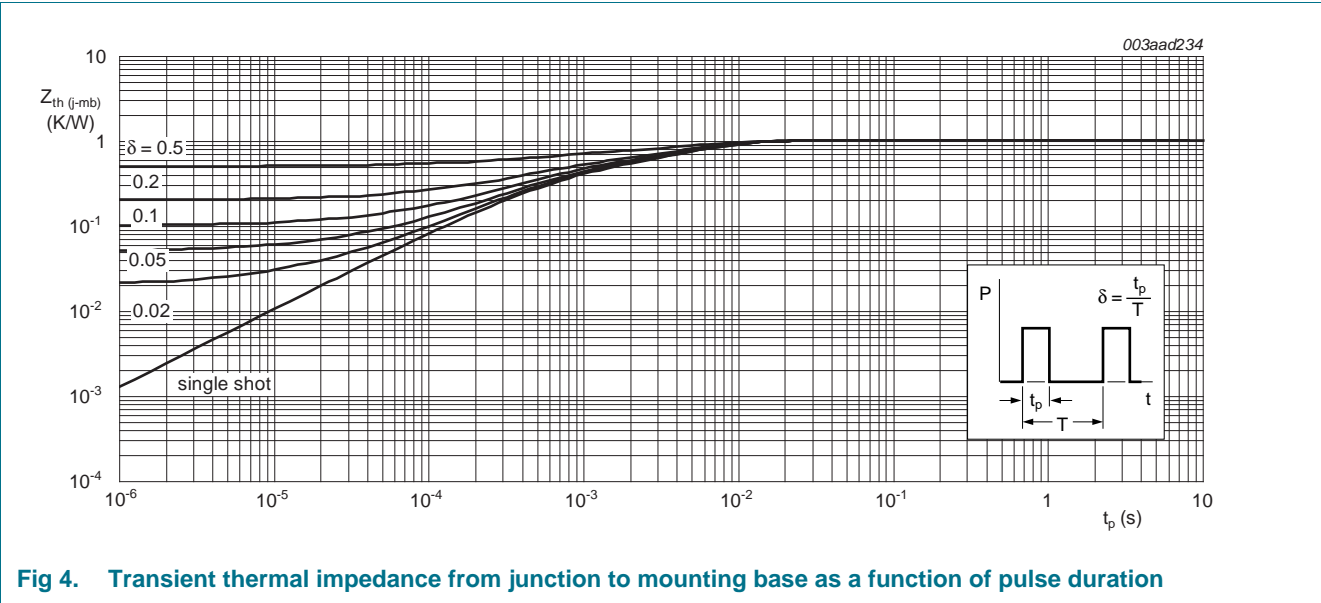


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 7. Characteristics

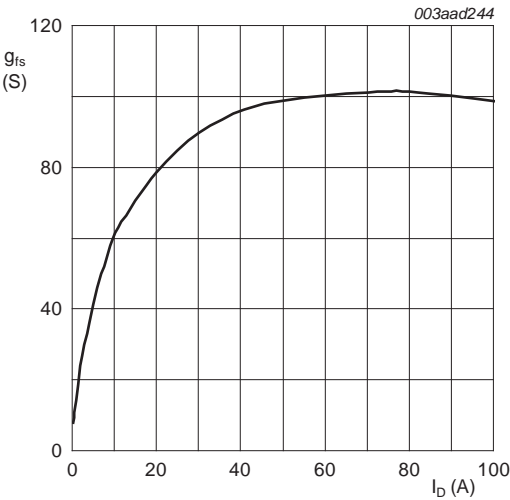
**Table 7. Characteristics**

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$ ; $V_{GS} = 0\ V$ ; $T_j = 25\ ^\circ C$	30	-	-	V
		$I_D = 250\ \mu A$ ; $V_{GS} = 0\ V$ ; $T_j = -55\ ^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$ ; $V_{DS} = V_{GS}$ ; $T_j = 25\ ^\circ C$ ; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	1.3	1.7	2.15	V
		$I_D = 1\ mA$ ; $V_{DS} = V_{GS}$ ; $T_j = 175\ ^\circ C$ ; see <a href="#">Figure 11</a>	0.5	-	-	V
		$I_D = 1\ mA$ ; $V_{DS} = V_{GS}$ ; $T_j = -55\ ^\circ C$ ; see <a href="#">Figure 11</a>	-	-	2.45	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30\ V$ ; $V_{GS} = 0\ V$ ; $T_j = 25\ ^\circ C$	-	0.02	1	$\mu A$
		$V_{DS} = 30\ V$ ; $V_{GS} = 0\ V$ ; $T_j = 125\ ^\circ C$	-	-	40	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16\ V$ ; $V_{DS} = 0\ V$ ; $T_j = 25\ ^\circ C$	-	10	100	nA
		$V_{GS} = -16\ V$ ; $V_{DS} = 0\ V$ ; $T_j = 25\ ^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ V$ ; $I_D = 15\ A$ ; $T_j = 175\ ^\circ C$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	6.65	7.8	mΩ
		$V_{GS} = 4.5\ V$ ; $I_D = 15\ A$ ; $T_j = 25\ ^\circ C$ ; see <a href="#">Figure 13</a>	-	4.46	5.2	mΩ
		$V_{GS} = 10\ V$ ; $I_D = 15\ A$ ; $T_j = 100\ ^\circ C$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	4.9	5.8	mΩ
		$V_{GS} = 10\ V$ ; $I_D = 15\ A$ ; $T_j = 25\ ^\circ C$ ; see <a href="#">Figure 13</a>	-	3.5	4.1	mΩ
$R_G$	gate resistance	$f = 1\ MHz$	-	1	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 15\ A$ ; $V_{DS} = 15\ V$ ; $V_{GS} = 4.5\ V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	19	-	nC
		$I_D = 15\ A$ ; $V_{DS} = 15\ V$ ; $V_{GS} = 10\ V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	41.5	-	nC
		$I_D = 0\ A$ ; $V_{DS} = 0\ V$ ; $V_{GS} = 10\ V$	-	30	-	nC
$Q_{GS}$	gate-source charge	$I_D = 15\ A$ ; $V_{DS} = 15\ V$ ; $V_{GS} = 4.5\ V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	8	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	4	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	4	-	nC
$Q_{GD}$	gate-drain charge		-	5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 15\ A$ ; $V_{DS} = 15\ V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	2.7	-	V
$C_{iss}$	input capacitance	$V_{DS} = 15\ V$ ; $V_{GS} = 0\ V$ ; $f = 1\ MHz$ ; $T_j = 25\ ^\circ C$ ; see <a href="#">Figure 16</a>	-	2400	-	pF
$C_{oss}$	output capacitance		-	500	-	pF
$C_{rss}$	reverse transfer capacitance		-	240	-	pF

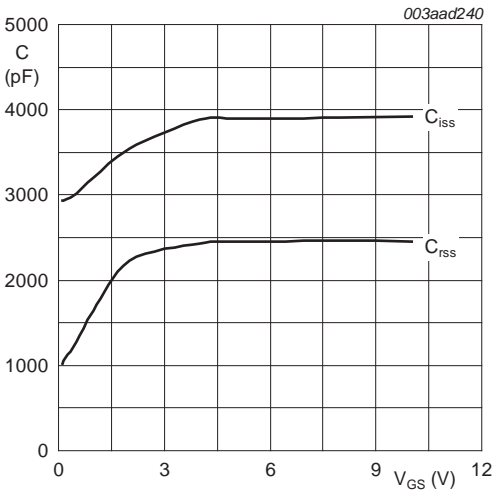
Table 7. Characteristics ...continued  
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 15 V; R <sub>L</sub> = 0.5 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 5.6 Ω	-	28	-	ns
t <sub>r</sub>	rise time		-	58	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	44	-	ns
t <sub>f</sub>	fall time		-	21	-	ns
Source-drain diode						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 15 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 17</a>	-	0.81	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 15 A; dI <sub>S</sub> /dt = -100 A/μs;	-	35	-	ns
Q <sub>r</sub>	recovered charge	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 15 V	-	30	-	nC



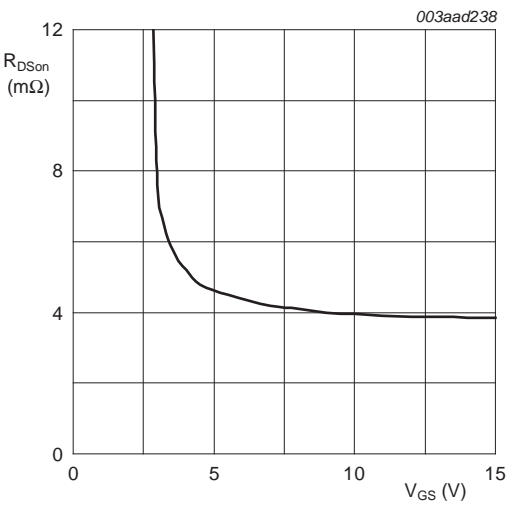
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 15\text{ V}$

Fig 5. Forward transconductance as a function of drain current; typical values



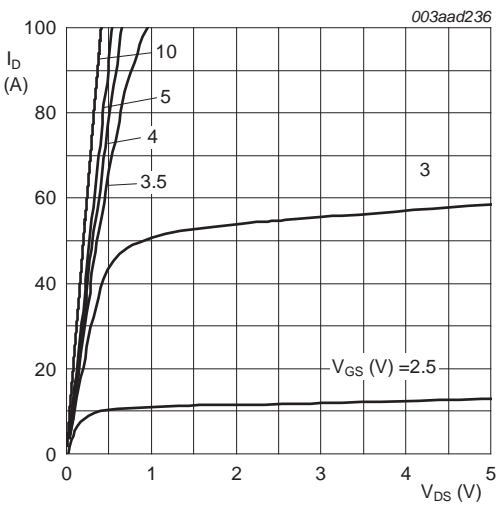
$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



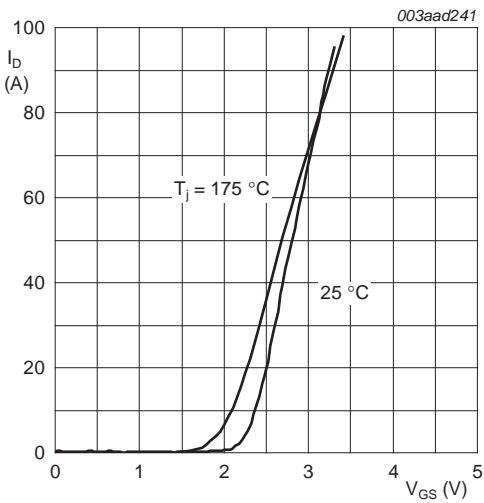
$T_j = 25\text{ °C}; I_D = 15\text{ A}$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



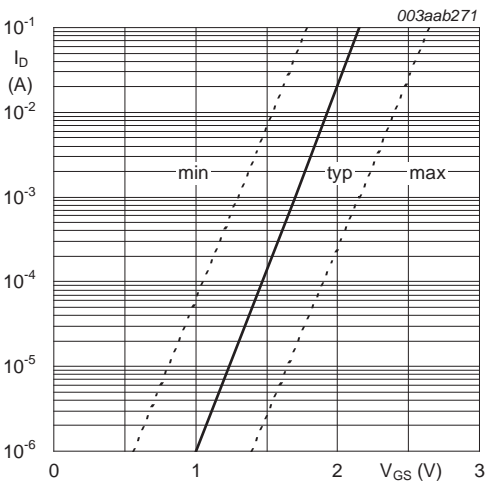
$T_j = 25\text{ °C}$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



$V_{DS} > I_D \times R_{DS(on)}$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



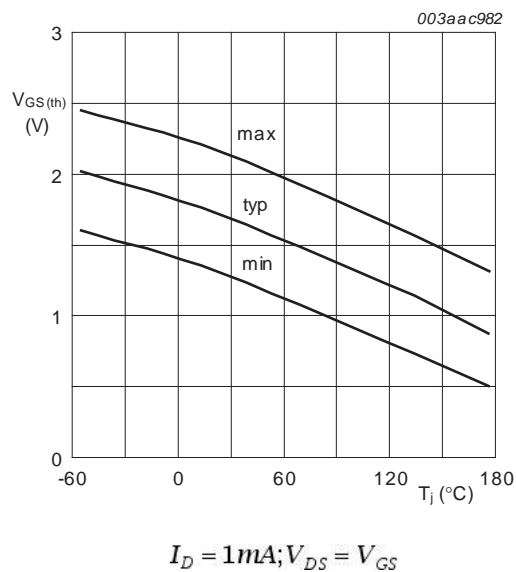


Fig 11. Gate-source threshold voltage as a function of junction temperature

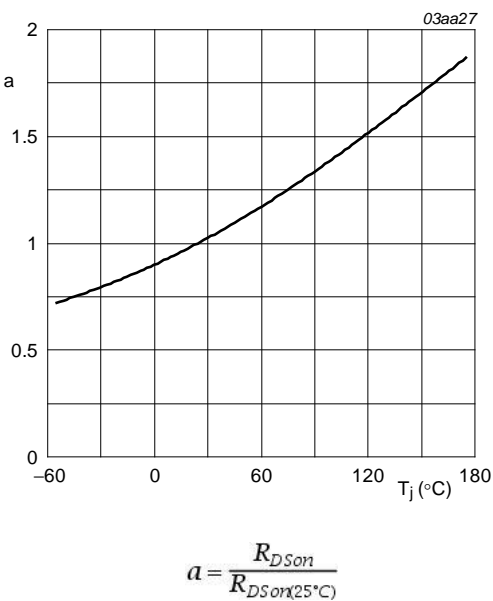


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

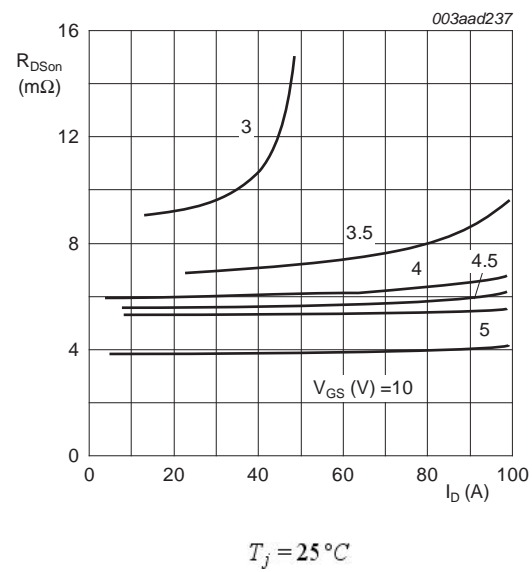


Fig 13. Drain-source on-state resistance as a function of drain current; typical values

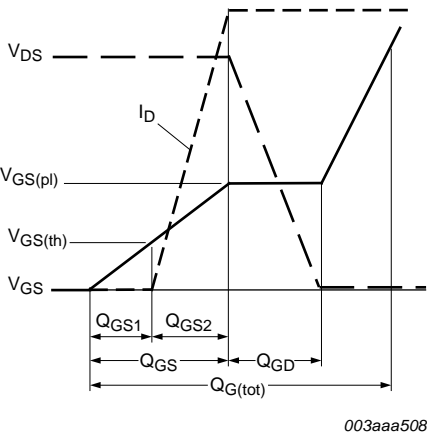


Fig 14. Gate charge waveform definitions

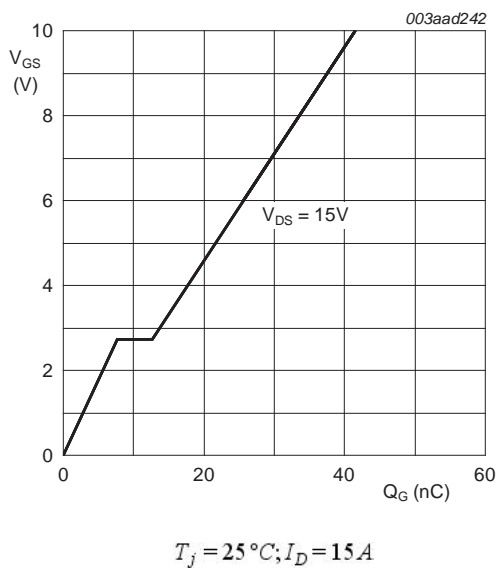


Fig 15. Gate-source voltage as a function of gate charge; typical values

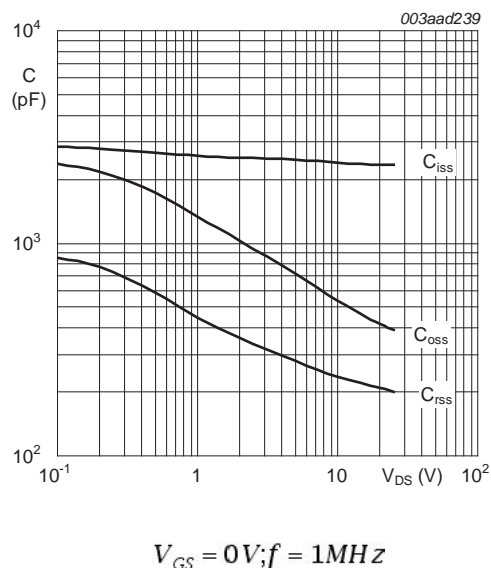


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

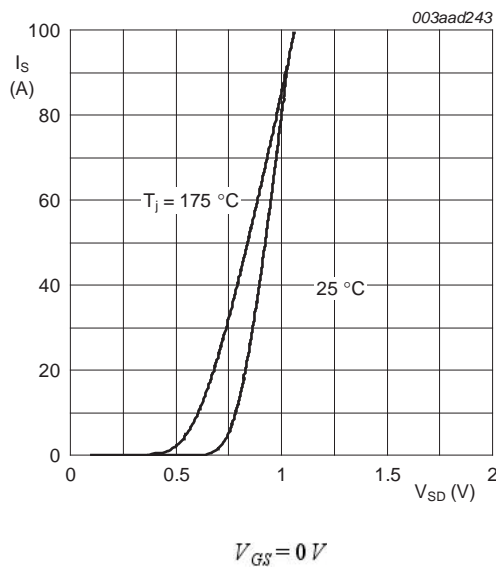


Fig 17. Source current as a function of source-drain voltage; typical values

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404

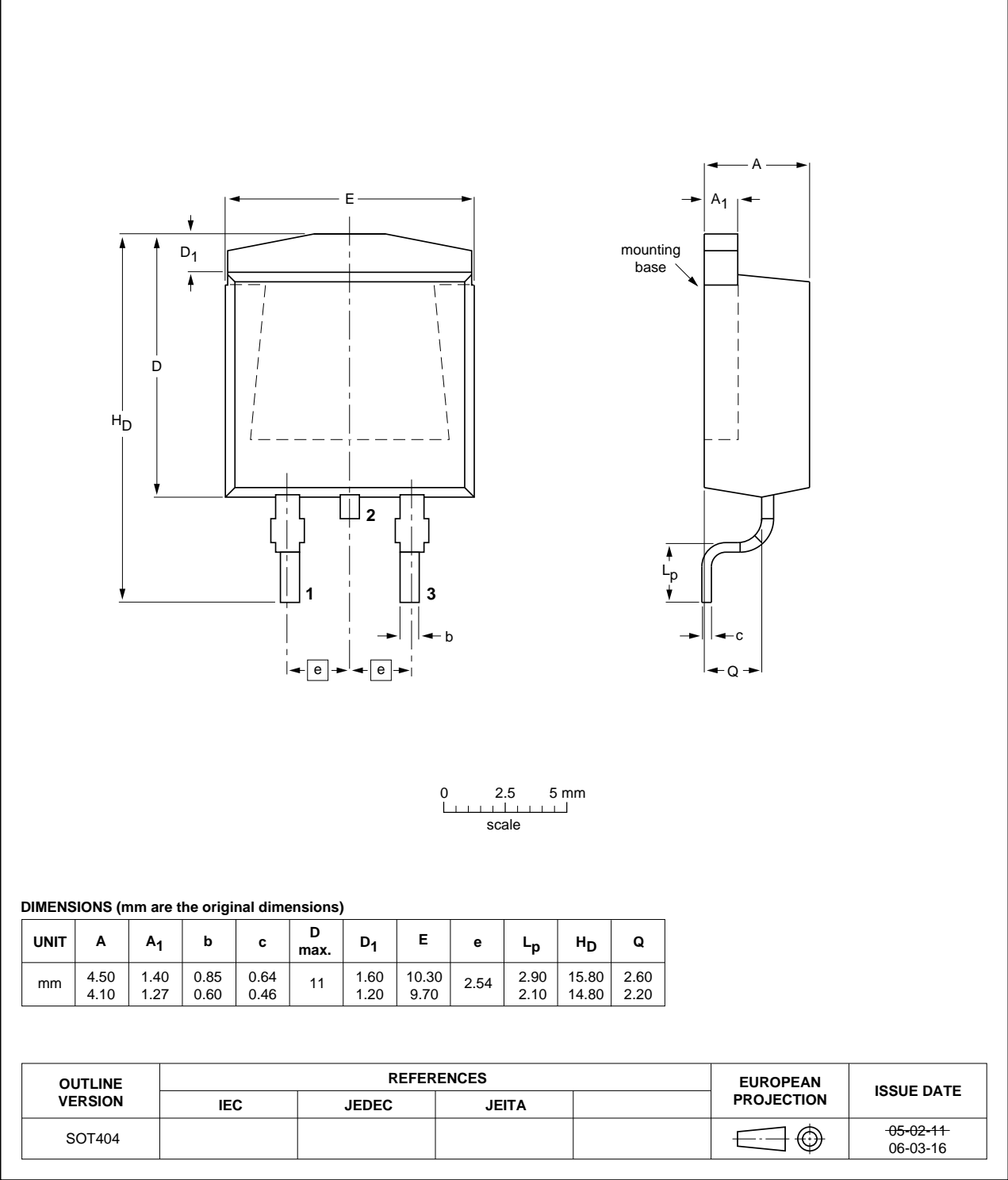


Fig 18. Package outline SOT404 (D2PAK)

## 9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN4R3-30BL v.1	20120322	Product data sheet	-	-

## 10. Legal information

### 10.1 Data sheet status

Document status <sup>[1] [2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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## 12. Contents

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