P-Channel 80 V (D-S) MOSFET

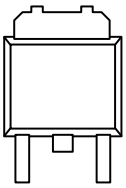
PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[b]	Q_g (Typ)
- 80	0.0112 at V_{GS} = - 10 V	- 110	85 nC
	0.0145 at V_{GS} = - 4.5 V	- 109	

FEATURES

- TrenchFET® Power MOSFET
- Material categorization:
  For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

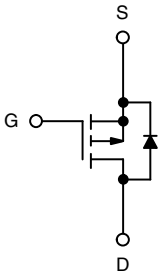
TO-263



Drain Connected to Tab

Top View

Ordering Information: SUM110P08-11L-E3 (Lead (Pb)-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 80	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)	T_C = 25 °C	I_D	- 110[a]	A
	T_C = 125 °C		- 71	
	T_A = 25 °C		- 23.5[b, c]	
	T_A = 125 °C		- 13.6[b, c]	
Pulsed Drain Current		I_{DM}	- 120	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 110	
	T_A = 25 °C		- 9[b, c]	
Avalanche Current	L = 0.1 mH	I_{AS}	- 75	
Single-Pulse Avalanche Energy		E_{AS}	281	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	375	W
	T_C = 125 °C		125	
	T_A = 25 °C		13.6[b, c]	
	T_A = 125 °C		4.5[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, d]	t ≤ 10 s	R_{thJA}	8	11	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	0.33	0.4	

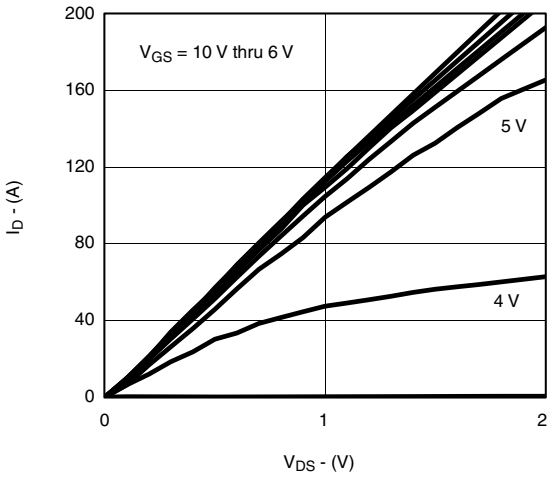
Notes:
a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under steady state conditions is 40 °C/W.

SPECIFICATIONS (T_A = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 80			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 1 µA		- 85		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 1		- 3	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 80 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 80 V, V_{GS} = 0 V, T_J = 175 °C			- 500	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 10 V, V_{GS} = - 10 V	- 120			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 20 A		0.0093	0.0112	Ω
		V_{GS} = - 4.5 V, I_D = - 15 A		0.0120	0.0145	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 20 A		85		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 40 V, V_{GS} = 0 V, f = 1 MHz		10850		pF
Output Capacitance	C_{oss}			800		
Reverse Transfer Capacitance	C_{rss}			700		
Total Gate Charge	Q_g	V_{DS} = - 40 V, V_{GS} = - 10 V, I_D = - 110 A		180	270	nC
		V_{DS} = - 40 V, V_{GS} = - 4.5 V, I_D = - 110 A		85	130	
Gate-Source Charge	Q_{gs}			35		
Gate-Drain Charge	Q_{gd}			42		
Gate Resistance	R_g	f = 1 MHz		3.6		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 40 V, R_L = 0.36 Ω I_D ≅ - 110 A, V_{GEN} = - 10 V, R_g = 1 Ω		20	30	ns
Rise Time	t_r			330	500	
Turn-Off Delay Time	$t_{d(off)}$			135	205	
Fall Time	t_f			550	825	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 110	A
Pulse Diode Forward Current[a]	I_{SM}				- 120	
Body Diode Voltage	V_{SD}	I_S = - 20 A		- 0.8	- 1.5	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 20 A, di/dt = 100 A/µs, T_J = 25 °C		65	100	ns
Body Diode Reverse Recovery Charge	Q_{rr}			135	205	nC
Reverse Recovery Fall Time	t_a			43		ns
Reverse Recovery Rise Time	t_b			22		

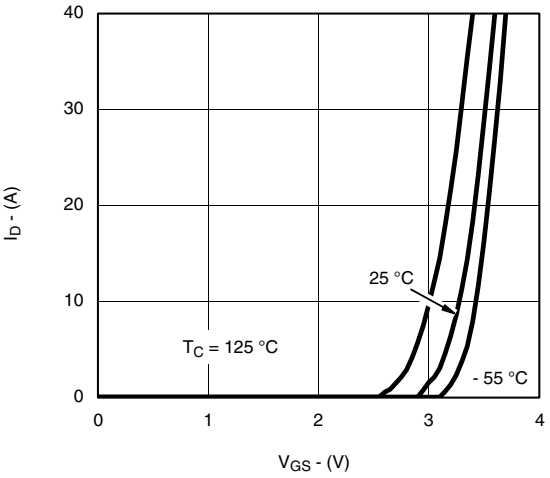
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

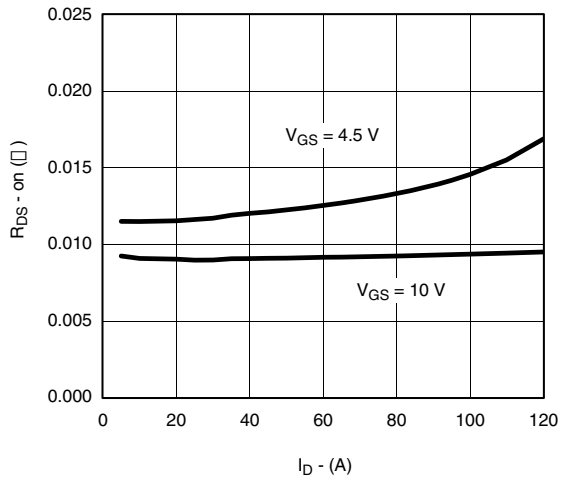
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



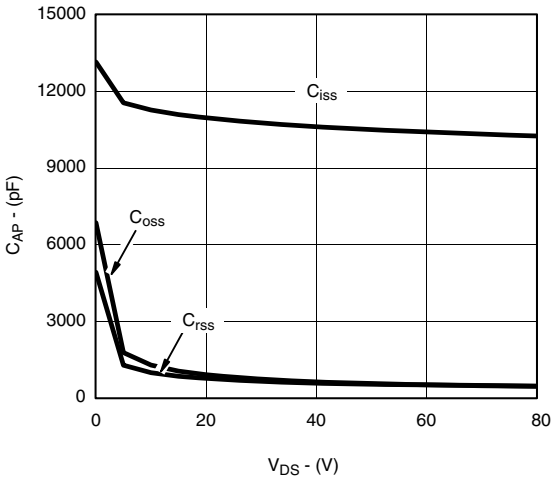
Output Characteristics



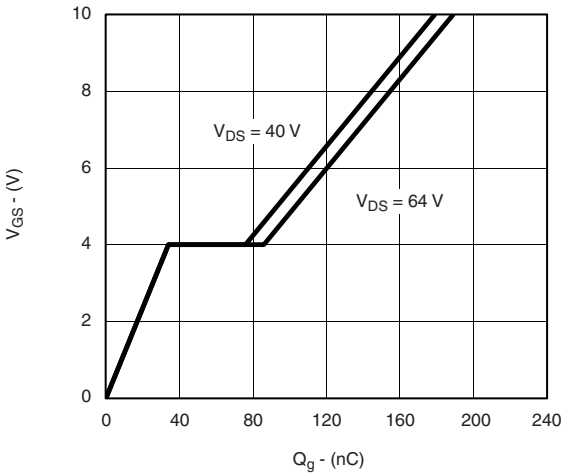
Transfer Characteristics



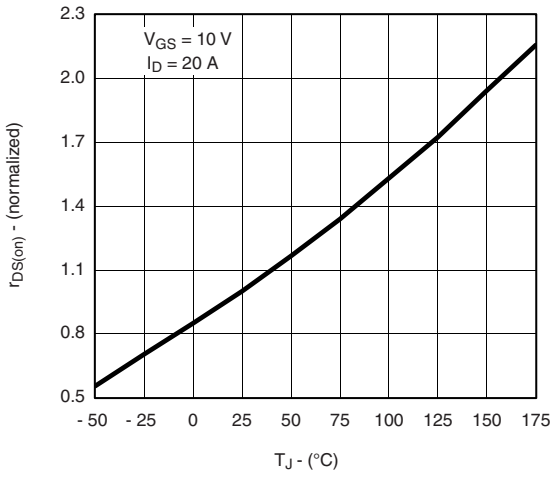
On-Resistance vs. Drain Current



Capacitance

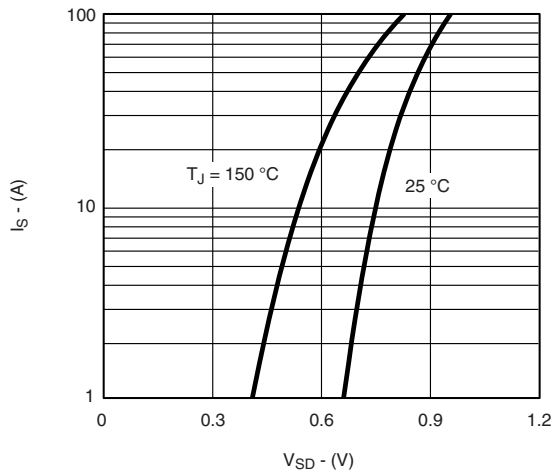


Gate Charge

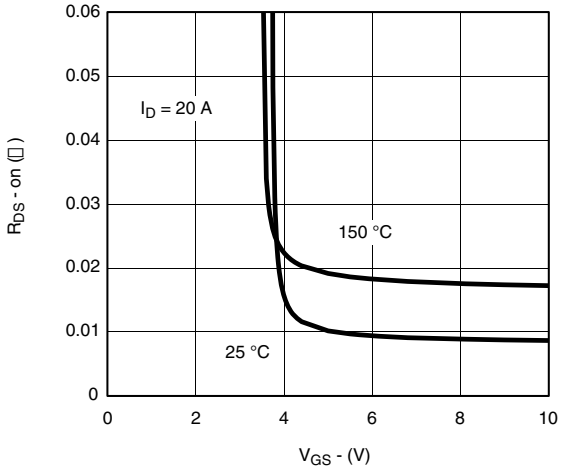


On-Resistance vs. Junction Temperature

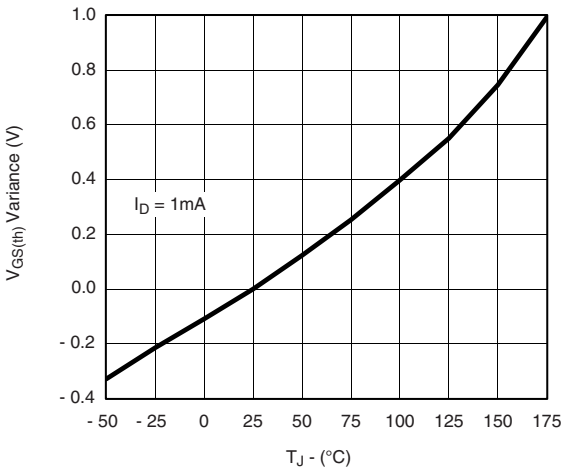
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



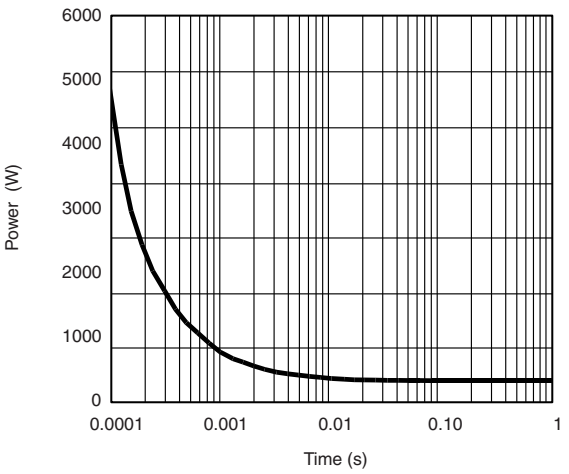
Source-Drain Diode Forward Voltage



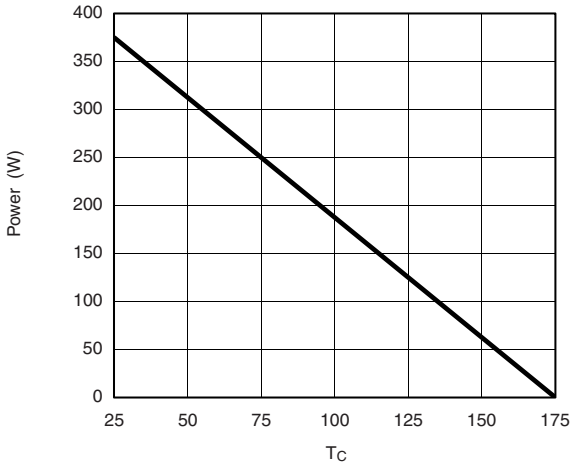
On-Resistance vs. Gate-to-Source Voltage



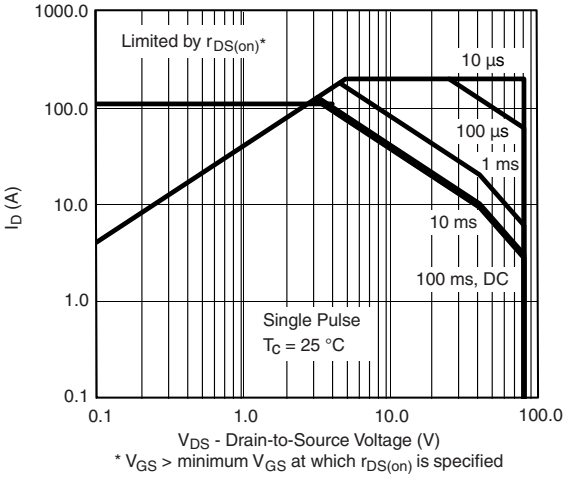
Threshold Voltage



Single Pulse Power, Junction-to-Case (T_C = 25 °C)



Power Derating, Junction-to-Case



Safe Operating Area

For technical questions, contact: pmostechsupport@vishay.com

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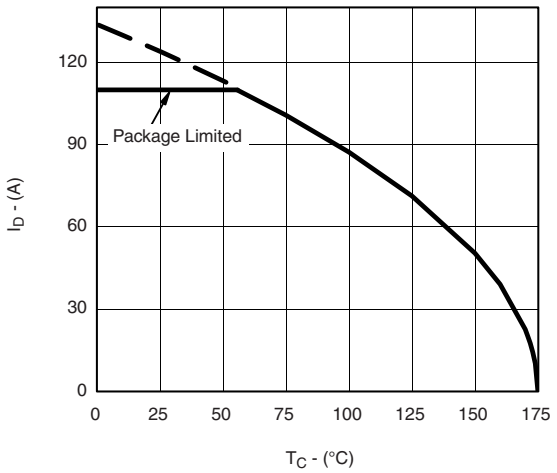
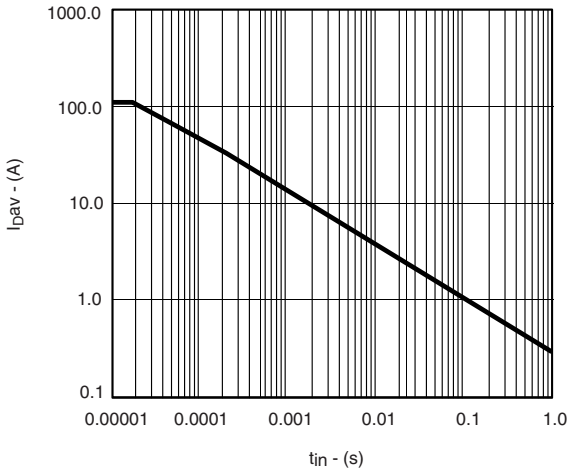
S12-3071-Rev. C, 24-Dec-12

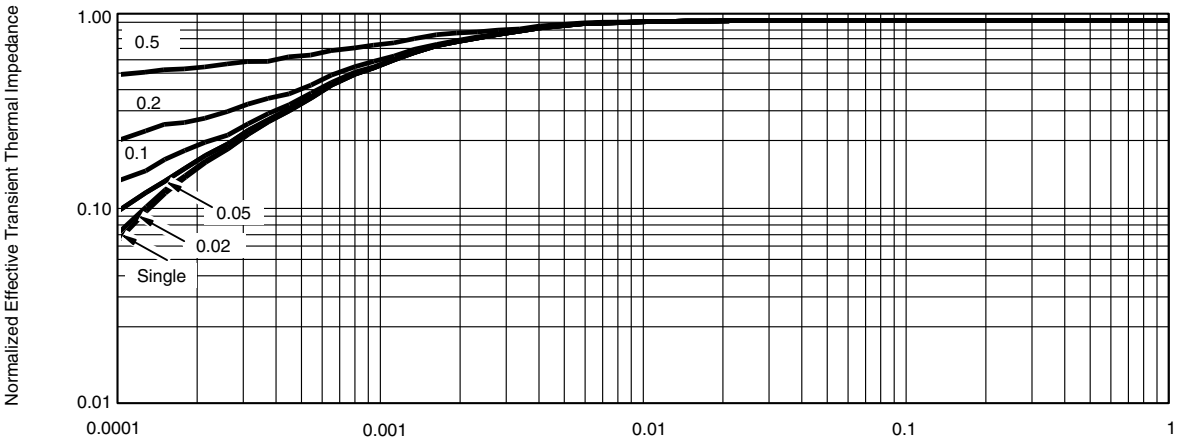
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Max. Avalanche and Drain Current vs. Case Temperature



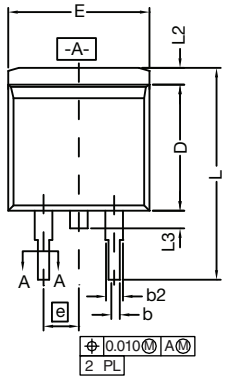
Avalanche Current vs. Time

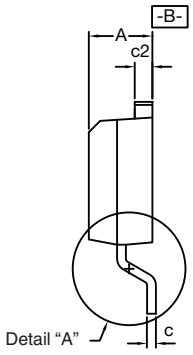


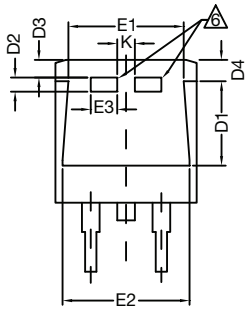
Normalized Thermal Transient Impedance, Junction-to-Case

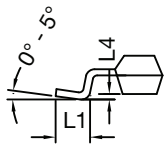
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73471.

TO-263 (D²PAK): 3-LEAD

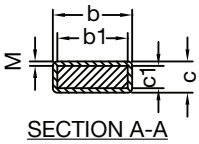








DETAIL A (ROTATED 90°)



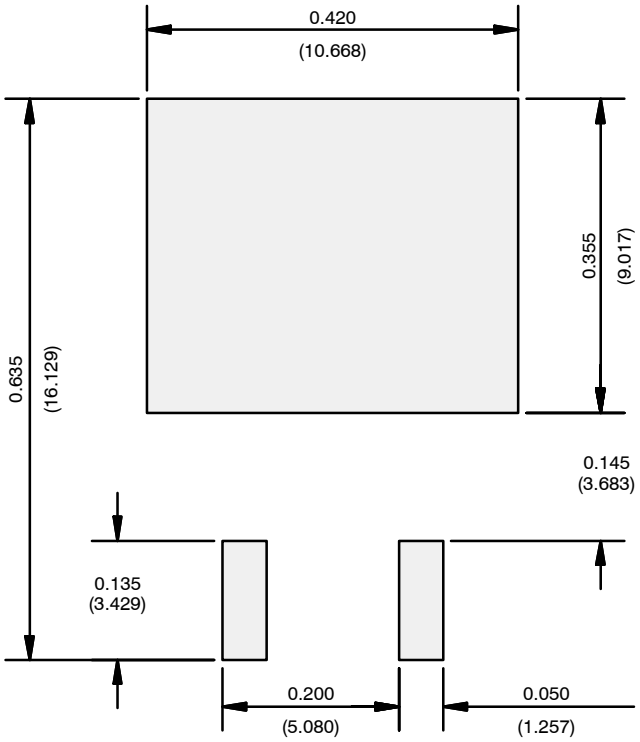
SECTION A-A

DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050
ECN: T13-0707-Rev. K, 30-Sep-13 DWG: 5843					

Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
   Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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Components Supply Platform

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