

SLLSEB2C-FEBRUARY 2012-REVISED FEBRUARY 2013

Single Channel ESD Protection Device in 0201 Package

Check for Samples: TPD1E6B06

FEATURES

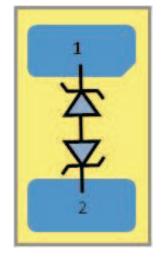
- Provides System Level ESD Protection for Low-voltage IO Interface
- IEC 61000-4-2 Level 4
 - ±15kV (Air Discharge),
 - ±15kV (Contact Discharge)
- IO Capacitance 6pF (Typ)
- R_{DYN} 0.55Ω (Typ)
- DC Breakdown Voltage ±6V (Min)
- Ultra Low Leakage Current 10nA (Typ)
- Low ESD Clamping Voltage
- Industrial Temperature Range: -40°C to 125°C
- IEC 61000-4-5 (Surge): 3.8A (8/20 µs Pulse)
- Space Saving 0201 Footprint (0.6mm x 0.3mm x 0.3mm)

APPLICATIONS

- Cell Phones
- eBook
- Portable Media Players
- Digital Camera

DEVICE CONFIGURATION

0.6 mm × 0.3 mm x 0.3 mm (0.35-mm pitch)



DESCRIPTION

The TPD1E6B06 is a single channel ESD protection device in a small 0201 package. The device offers ±15kV IEC air-gap, ±15kV contact ESD protection, and has an ESD clamp circuit with a back-to-back diode for bipolar or bidirectional signal support. The 6pF line capacitance is suitable for a wide range of applications supporting data rates up to 800Mbps .Typical application areas for the TPD1E6B06 are audio lines (microphone, earphone, and speakerphone), SD interfacing, keypad or other buttons, VBUS pin and ID pin of USB ports.

The 0201 package is industry standard and convenient for component placement in space saving applications. The TPD1E6B06 is characterized for operation over ambient air temperature of -40°C to 125°C.

ORDERING INFORMATION

T _A	PACKA	GE ⁽¹⁾⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 125°C	15000	Tape and reel	TPD1E6B06DPLR	Н	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.



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TPD1E6B06

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TEXAS INSTRUMENTS

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

		MIN	MAX	UNIT
	Operating temperature range	-40	125	°C
	Storage temperature	-65	155	°C
	IEC 61000-4-2 contact ESD		±15	kV
	IEC 61000-4-2 air-gap ESD		±15	kV
I_{PP}	Peak pulse current (tp = 8/20 μs)		3.8	А
P_PP	Peak pulse power (tp = 8/20 µs)		50	W

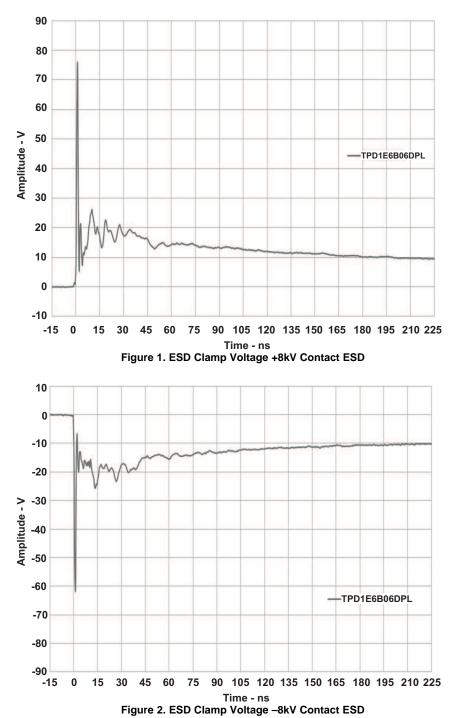
ELECTRICAL CHARACTERISTICS

	PARAMETER	TEST CONDITION	MIN TYP	MAX	UNIT		
V _{RWM}	Reverse stand-off voltage	I _{LEAK} = 100 nA		±5	V		
I _{LEAK}	Leakage Current	Pin 1 = 5 V, Pin 2 = 0 V		100	nA		
V	Clamp voltage with ESD strike on pin 1, pin 2	$I_{PP} = 1 \text{ A}, \text{ tp} = 8/20 \mu\text{s}$	10		V		
V _{Clamp1,2}	grounded.	$I_{PP} = 5 \text{ A}, \text{ tp} = 8/20 \ \mu\text{s}$		14	V		
V _{Clamp2,1}	Clamp voltage with ESD strike on pin 2, pin 1	$I_{PP} = 1 \text{ A}, \text{ tp} = 8/20 \mu\text{s}$		10	V		
	grounded.	$I_{PP} = 5 \text{ A}, \text{ tp} = 8/20 \mu\text{s}$		14	v		
R _{DYN}		Pin 1 to Pin 2 ⁽¹⁾	0.55		0		
	Dynamic resistance	Pin 2 to Pin 1 ⁽¹⁾	0.55		Ω		
C _{IO}	IO capacitance	V _{IO} = 2.5 V	6		pF		
V _{BR1,2}	Break-down voltage, pin 1 to pin 2	I _{IO} = 1 mA	6		V		
V _{BR2,1}	Break-down voltage, pin 2 to pin 1	I _{IO} = 1 mA	6		V		

(1) Extraction of R_{DYN} using least squares fit of TLP characteristics between $I_{PP} = 10A$ and $I_{PP} = 20A$.

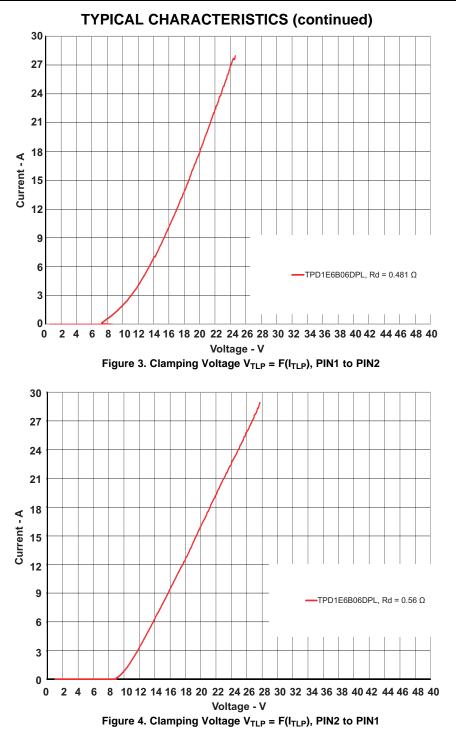


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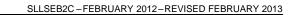


TYPICAL CHARACTERISTICS

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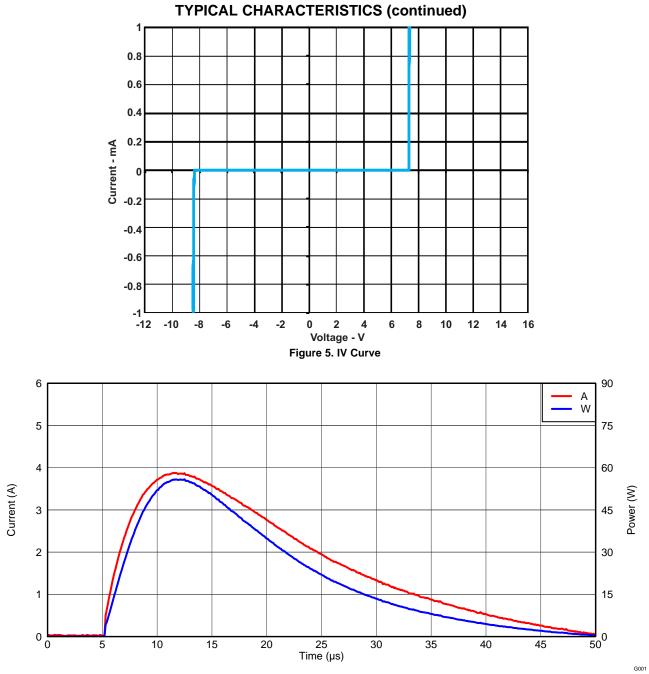


Figure 6. Surge Graph, Pin 1 to Pin 2

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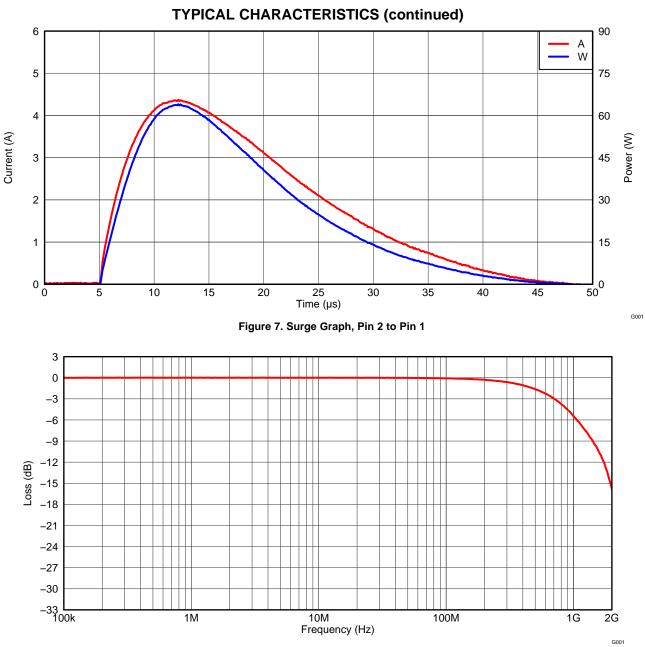


Figure 8. Insertion Loss, Pin 1 to Pin 2



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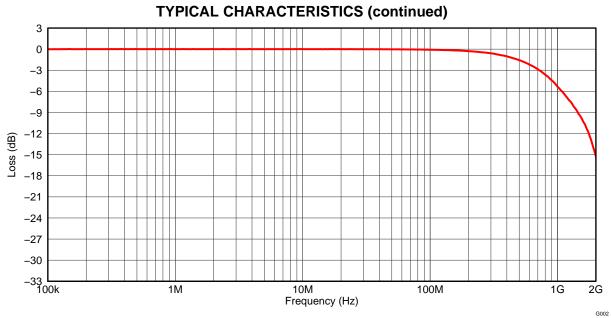


Figure 9. Insertion Loss, Pin 2 to Pin 1

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REVISION HISTORY

Changes from Original (February 2012) to Revision A						
Changed 0402 Package to 0201 Package in title.	1					
Added R _{DYN} to FEATURES.	1					
Changed supporting data rates from 150Mbps to 800Mbps in the DESCRIPTION section	1					
Added I _{LEAK} parameter to the ELECTRICAL CHARACTERISTICS table.	2					
Changes from Revision A (April 2012) to Revision B	Page					
Indated P value in EEATURES	1					

•	Updated R _{DYN} value in FEATURES.	1
•	Updated IEC 61000-4-5 (Surge) value in FEATURES.	1
•	Updated ABSOLUTE MAXIMUM RATINGS.	2
•	Updated TYPICAL CHARACTERISTICS section.	3

Changes from Revision B (August 2012) to Revision C

Updated TOP-SIDE MARKING in the ORDERING INFORMATION table. 1

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11-Apr-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	•	Pins	•	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing		Qty	(2)		(3)		(4)	
TPD1E6B06DPLR	ACTIVE	X2SON	DPL	2	15000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Н	Samples
TPD1E6B06DPLT	ACTIVE	X2SON	DPL	2	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Н	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

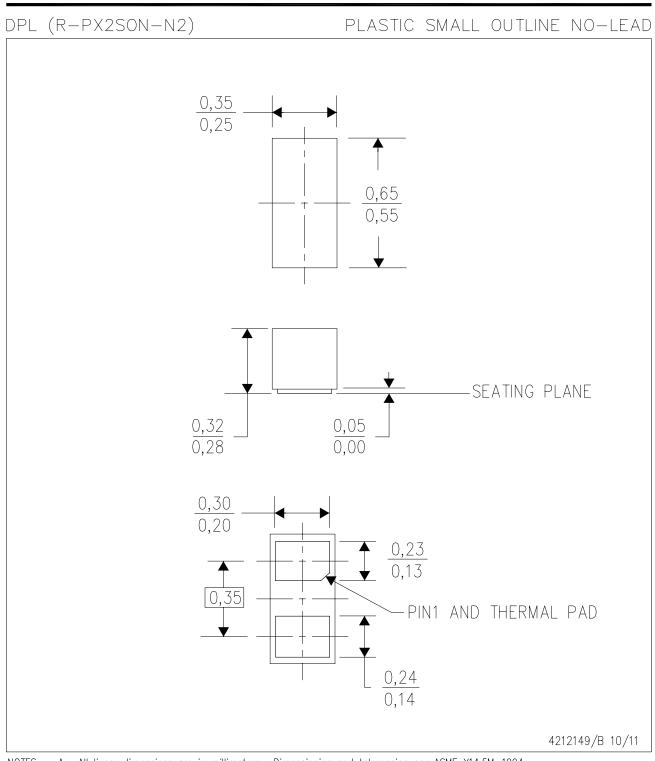
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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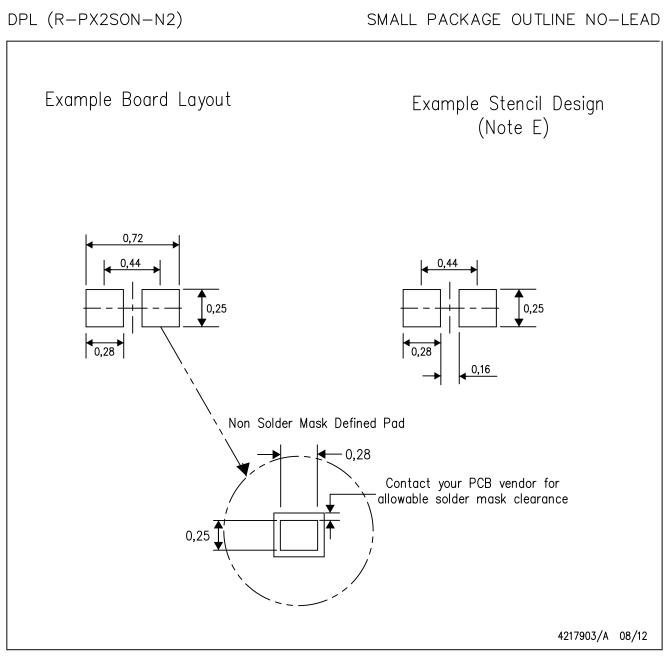
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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.





- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



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