

BUK7K6R2-40E

Dual N-channel 40 V, 5.8 mΩ standard level MOSFET

6 November 2013

Product data sheet

1. General description

Dual standard level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with $V_{GS(th)}$ of greater than 1 V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 1	[1]	-	-	40	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2		-	-	68	W
Static characteristics FET1 and FET2							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11		-	4.8	5.8	mΩ
Dynamic characteristics FET1 and FET2							
Q_{GD}	gate-drain charge	$I_D = 20\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14		-	10.5	-	nC

[1] Continuous current is limited by package.

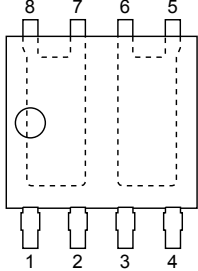
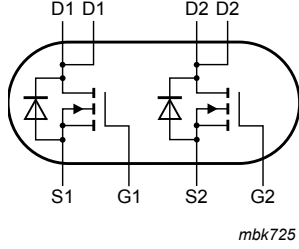


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LFPAK56D (SOT1205)	 mbk725
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7K6R2-40E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7K6R2-40E	76E240

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

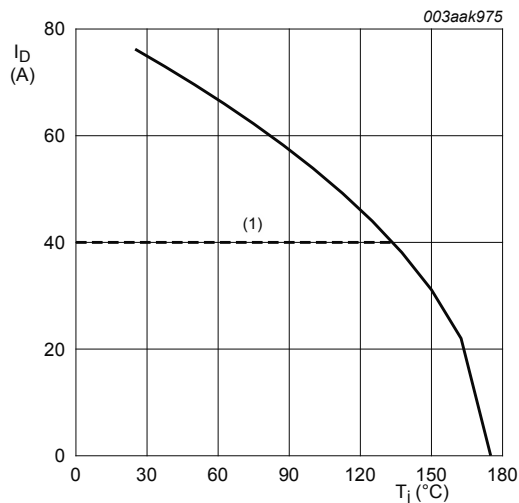
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$		-	40	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	40	V
V_{GS}	gate-source voltage	$T_j \leq 175\text{ °C}$; DC		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 1	[1]	-	40	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 1	[1]	-	40	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 4		-	308	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2		-	68	W

Symbol	Parameter	Conditions		Min	Max	Unit
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I_S	source current	$T_{\text{mb}} = 25\text{ °C}$	[1]	-	40	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{\text{mb}} = 25\text{ °C}$		-	308	A
Avalanche Ruggedness FET1 and FET2						
$E_{\text{DS(AL)S}}$	non-repetitive drain-source avalanche energy	$I_D = 40\text{ A}$; $V_{\text{sup}} \leq 40\text{ V}$; $V_{\text{GS}} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; Fig. 3	[2][3]	-	157	mJ

[1] Continuous current is limited by package.

[2] Refer to application note AN10273 for further information

[3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



(1) Capped at 40A due to package

Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{\text{GS}} \geq 10\text{ V}$$

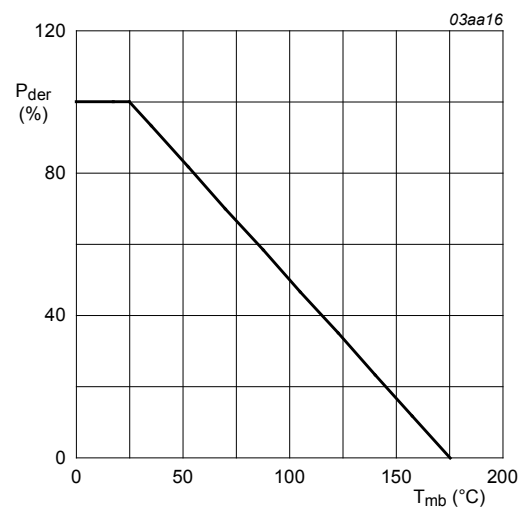
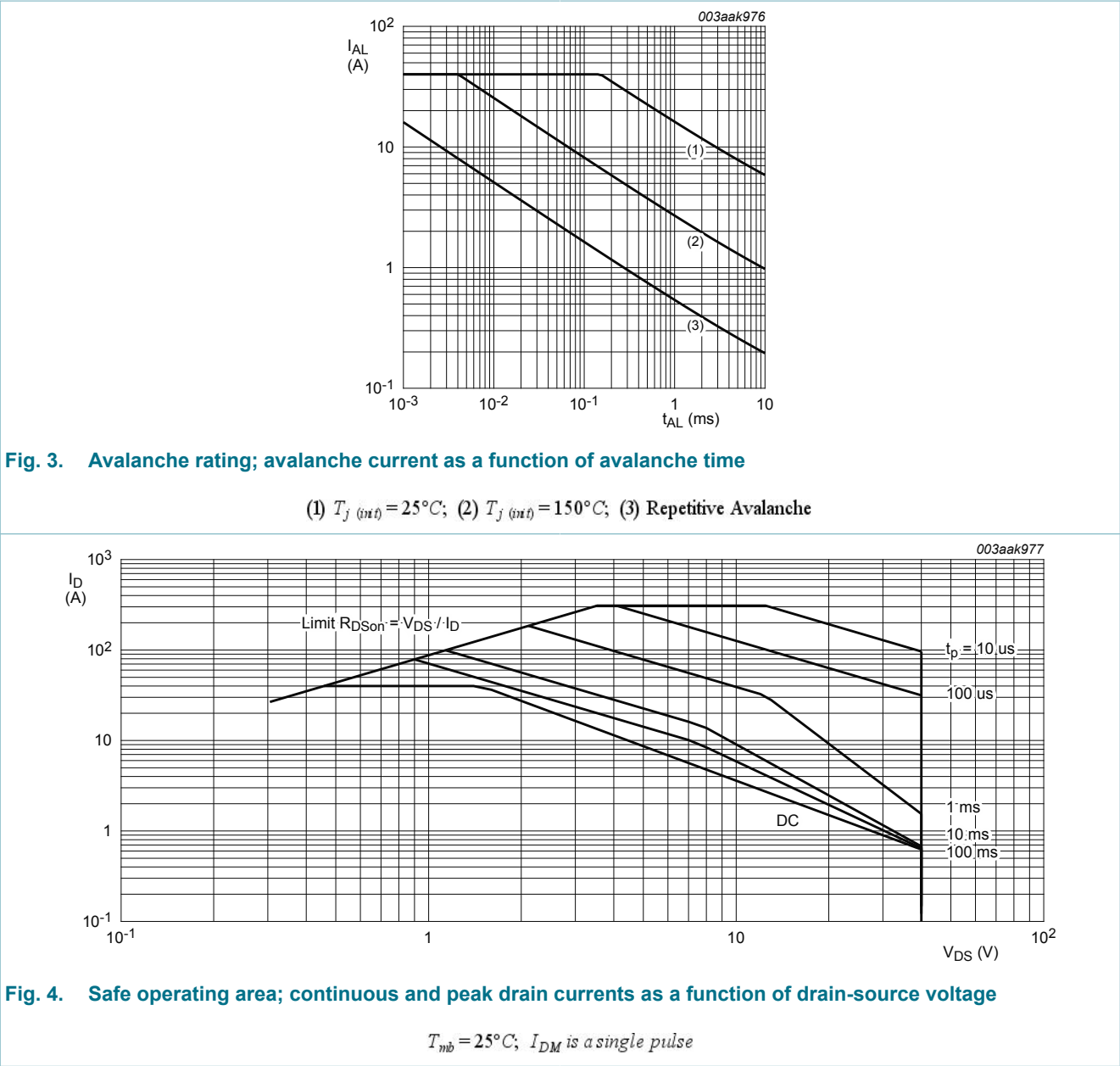


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{\text{der}} = \frac{P_{\text{tot}}}{P_{\text{tot}(25\text{ °C})}} \times 100\%$$



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	2.21	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

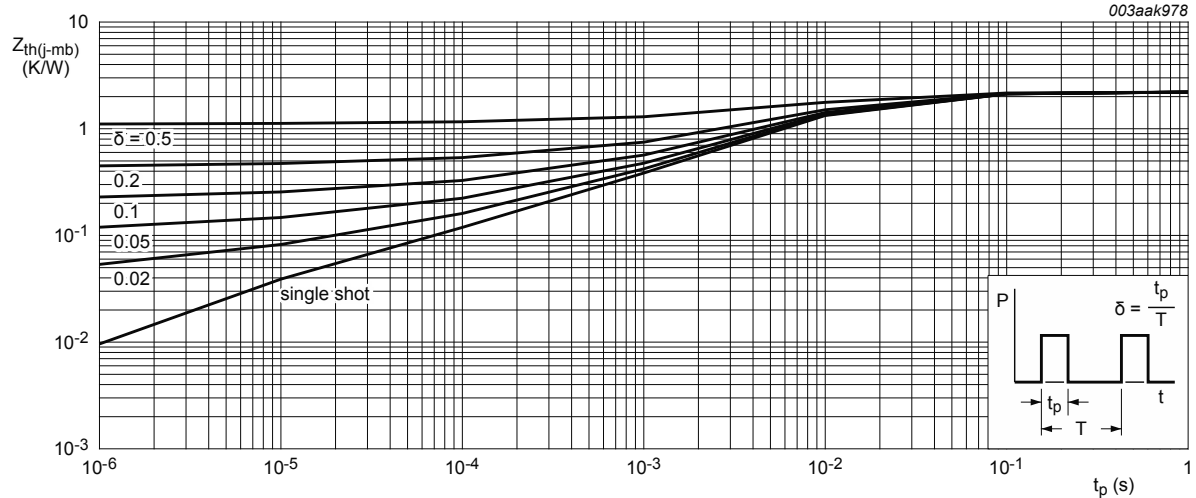


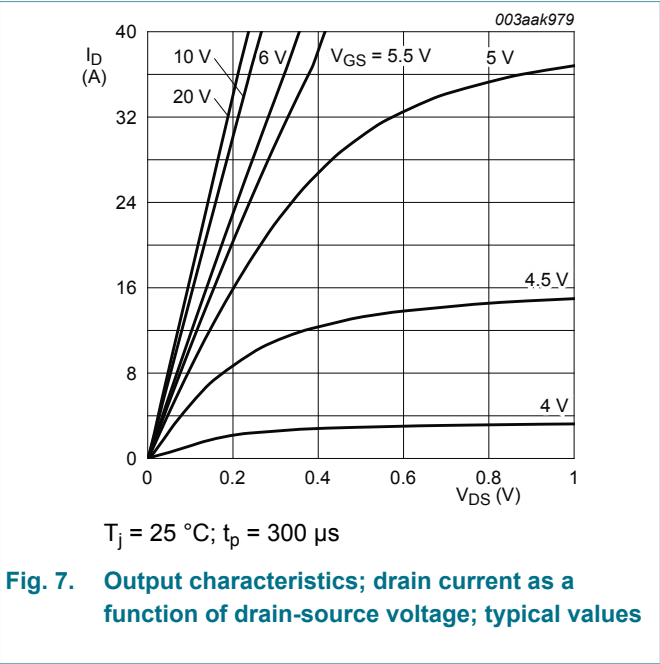
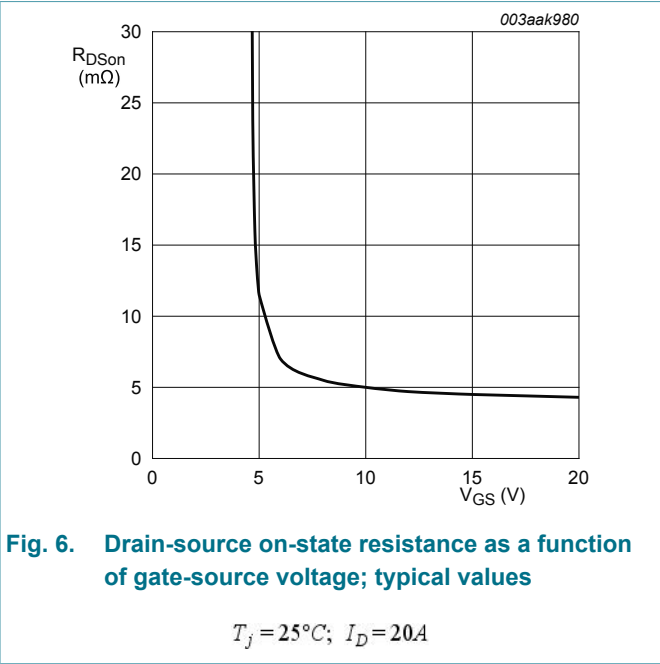
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^{\circ}C$		36	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^{\circ}C$		40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^{\circ}C;$ Fig. 9; Fig. 10		2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^{\circ}C;$ Fig. 9; Fig. 10		1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^{\circ}C;$ Fig. 9; Fig. 10		-	-	4.5	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 \text{ }^{\circ}C$		-	0.02	1	μA
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 \text{ }^{\circ}C$		-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^{\circ}C$		-	2	100	nA
		$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^{\circ}C$		-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 20 A; T_j = 25 \text{ }^{\circ}C;$ Fig. 11		-	4.8	5.8	m Ω
		$V_{GS} = 10 V; I_D = 20 A; T_j = 175 \text{ }^{\circ}C;$ Fig. 11; Fig. 12		-	9.5	11.4	m Ω
Dynamic characteristics FET1 and FET2							
$Q_{G(tot)}$	total gate charge	$I_D = 20 A; V_{DS} = 32 V; V_{GS} = 10 V;$ $T_j = 25 \text{ }^{\circ}C;$ Fig. 13; Fig. 14		-	32.3	-	nC
Q_{GS}	gate-source charge			-	7.2	-	nC
Q_{GD}	gate-drain charge			-	10.5	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; Fig. 15		-	1657	2210	pF
C _{oss}	output capacitance			-	354	425	pF
C _{rss}	reverse transfer capacitance			-	208	285	pF
t _{d(on)}	turn-on delay time	V _{DS} = 32 V; R _L = 1.6 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C; I _D = 20 A		-	9.5	-	ns
t _r	rise time			-	16	-	ns
t _{d(off)}	turn-off delay time			-	21	-	ns
t _f	fall time			-	17	-	ns
Source-drain diode FET1 and FET2							
V _{SD}	source-drain voltage	I _S = 15 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16		-	0.78	1.2	V
t _{rr}	reverse recovery time	I _S = 5 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _j = 25 °C		-	25	-	ns
Q _r	recovered charge			-	18	-	nC



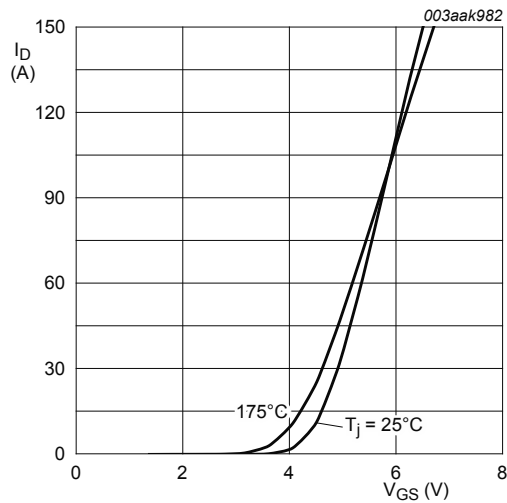


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

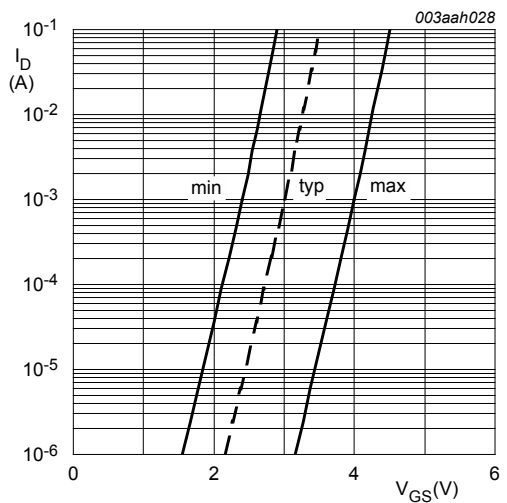


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5V$

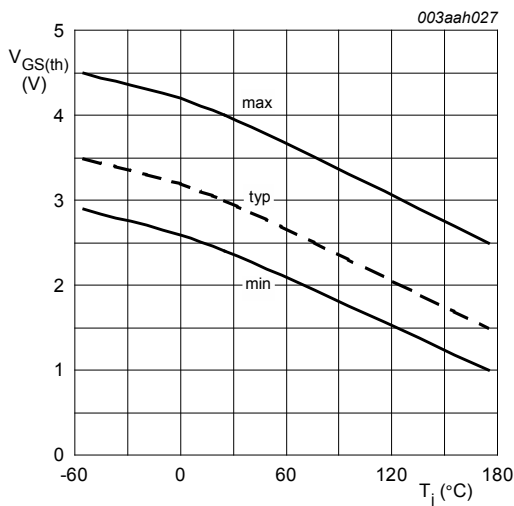


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

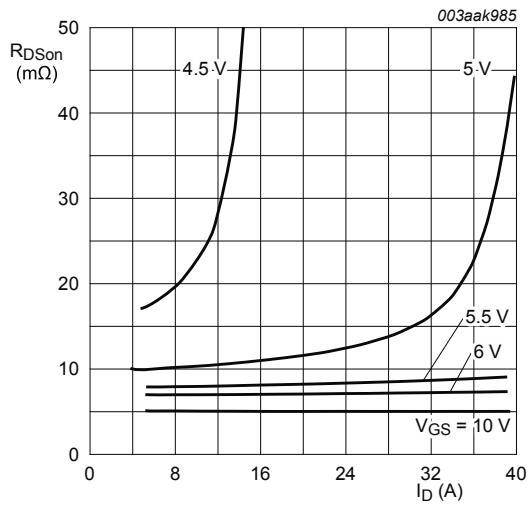


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

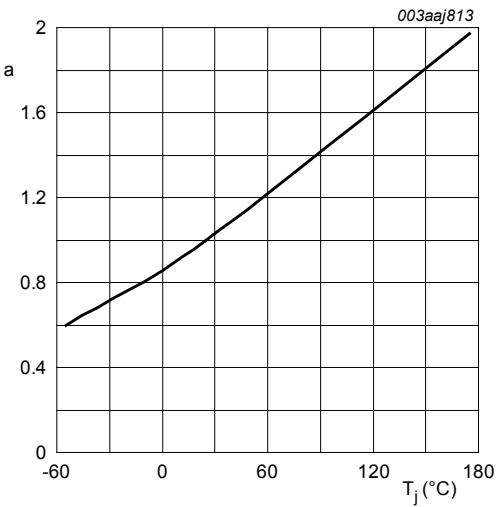


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^{\circ}\text{C})}$$

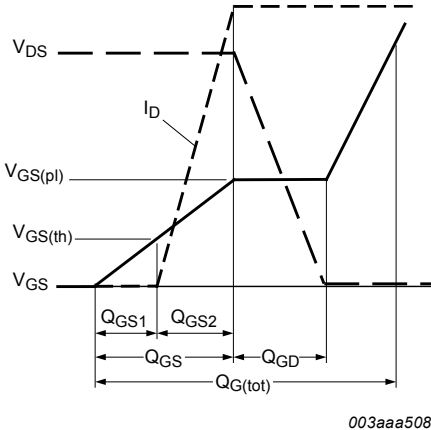


Fig. 13. Gate charge waveform definitions

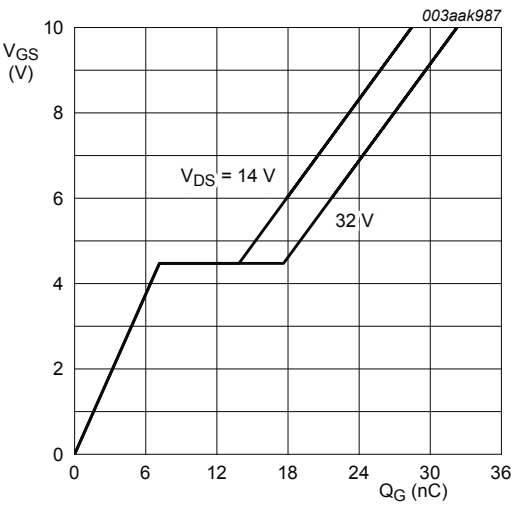


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}\text{C}; I_D = 20\text{ A}$$

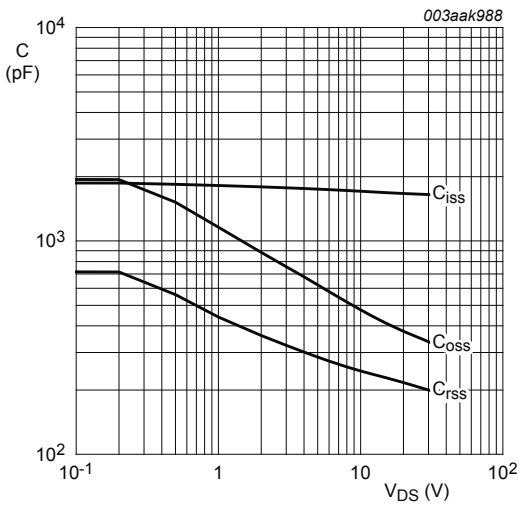


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$

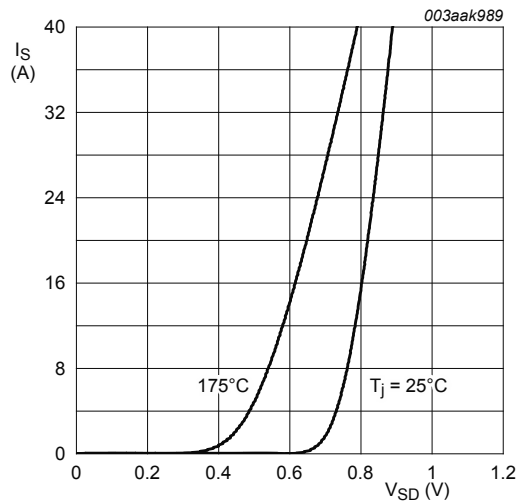


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0V$

11. Package outline

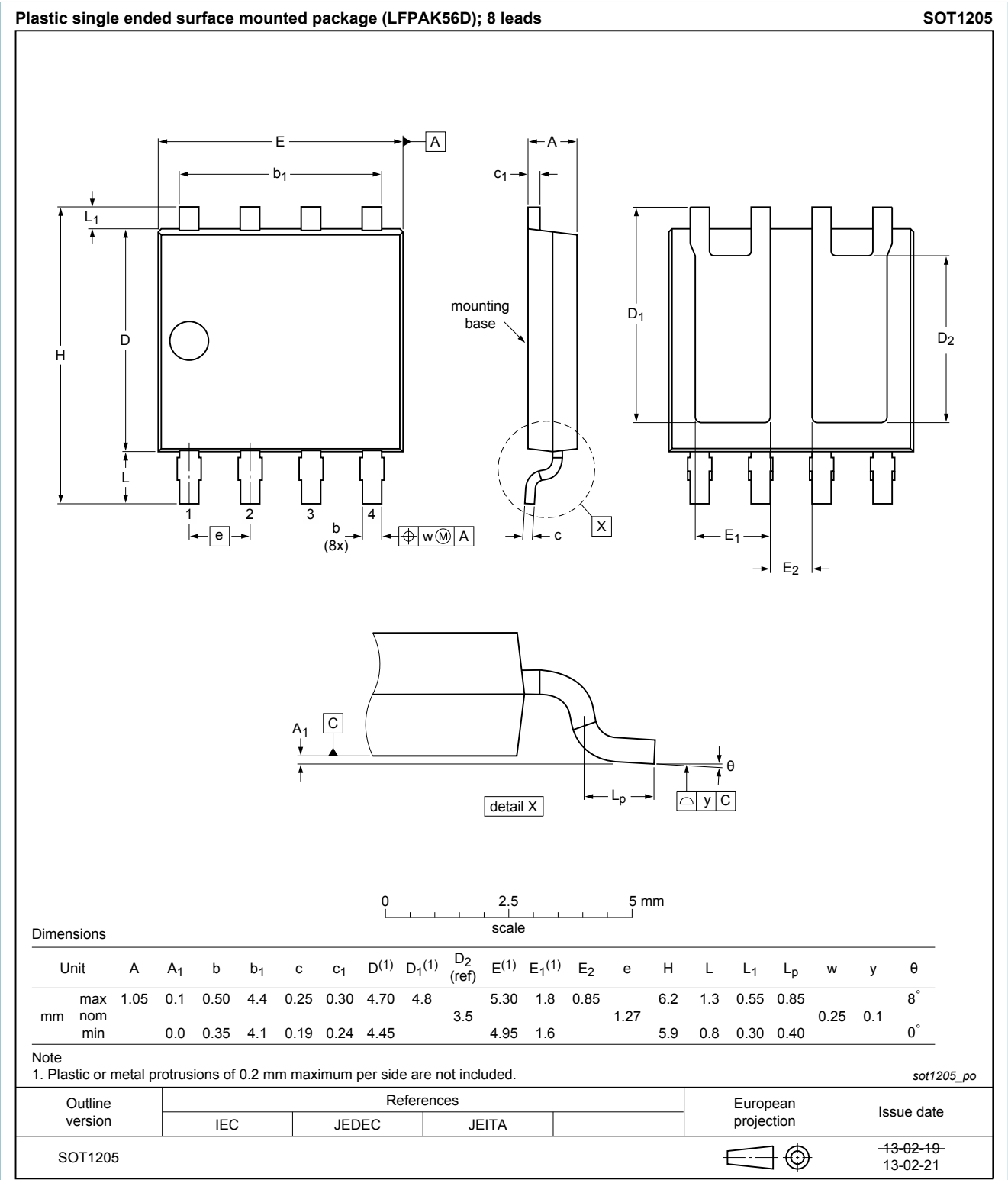


Fig. 17. Package outline LPAK56D (SOT1205)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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13. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	2
9	Thermal characteristics	4
10	Characteristics	5
11	Package outline	10
12	Legal information	11
12.1	Data sheet status	11
12.2	Definitions	11
12.3	Disclaimers	11
12.4	Trademarks	12

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