

# IRFS4115PbF IRFSL4115PbF

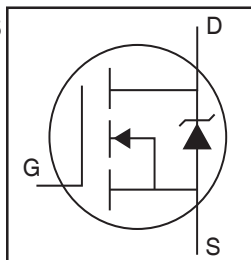
HEXFET® Power MOSFET

## Applications

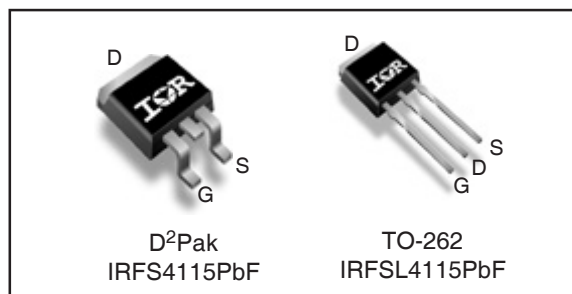
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

## Benefits

- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode  $dV/dt$  and  $dI/dt$  Capability
- Lead-Free



|                          |               |
|--------------------------|---------------|
| $V_{DSS}$                | <b>150V</b>   |
| $R_{DS(on)}$ <b>typ.</b> | <b>10.3mΩ</b> |
| <b>max.</b>              | <b>12.1mΩ</b> |
| $I_D$ (Silicon Limited)  | <b>99A ①</b>  |
| $I_D$ (Package Limited)  | <b>195A</b>   |



|          |          |          |
|----------|----------|----------|
| <b>G</b> | <b>D</b> | <b>S</b> |
| Gate     | Drain    | Source   |

## Absolute Maximum Ratings

| Symbol                            | Parameter                                                    | Max.             | Units |
|-----------------------------------|--------------------------------------------------------------|------------------|-------|
| $I_D$ @ $T_C = 25^\circ\text{C}$  | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited)   | 99①              | A     |
| $I_D$ @ $T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited)   | 70 ①             |       |
| $I_D$ @ $T_C = 25^\circ\text{C}$  | Continuous Drain Current, $V_{GS}$ @ 10V (Wire Bond Limited) | 195              |       |
| $I_{DM}$                          | Pulsed Drain Current ②                                       | 396              |       |
| $P_D$ @ $T_C = 25^\circ\text{C}$  | Maximum Power Dissipation                                    | 375              | W     |
|                                   | Linear Derating Factor                                       | 2.5              | W/°C  |
| $V_{GS}$                          | Gate-to-Source Voltage                                       | ± 20             | V     |
| $dv/dt$                           | Peak Diode Recovery ④                                        | 18               | V/ns  |
| $T_J$                             | Operating Junction and                                       | -55 to + 175     | °C    |
| $T_{STG}$                         | Storage Temperature Range                                    |                  |       |
|                                   | Soldering Temperature, for 10 seconds<br>(1.6mm from case)   | 300              |       |
|                                   | Mounting torque, 6-32 or M3 screw                            | 10lb·in (1.1N·m) |       |

## Avalanche Characteristics

|                              |                                 |                            |    |
|------------------------------|---------------------------------|----------------------------|----|
| $E_{AS}$ (Thermally limited) | Single Pulse Avalanche Energy ③ | 830                        | mJ |
| $I_{AR}$                     | Avalanche Current ②             | See Fig. 14, 15, 22a, 22b, | A  |
| $E_{AR}$                     | Repetitive Avalanche Energy ⑤   |                            | mJ |

## Thermal Resistance

| Symbol          | Parameter              | Typ. | Max. | Units |
|-----------------|------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case ⑧⑩    | —    | 0.4  | °C/W  |
| $R_{\theta JA}$ | Junction-to-Ambient ⑧⑨ | —    | 40   |       |

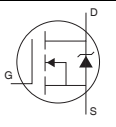
Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

| Symbol                          | Parameter                            | Min. | Typ. | Max. | Units               | Conditions                                               |
|---------------------------------|--------------------------------------|------|------|------|---------------------|----------------------------------------------------------|
| $V_{(BR)DSS}$                   | Drain-to-Source Breakdown Voltage    | 150  | —    | —    | V                   | $V_{GS} = 0V, I_D = 250\mu A$                            |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient  | —    | 0.18 | —    | V/ $^\circ\text{C}$ | Reference to $25^\circ\text{C}$ , $I_D = 3.5\text{mA}$ ② |
| $R_{DS(on)}$                    | Static Drain-to-Source On-Resistance | —    | 10.3 | 12.1 | m $\Omega$          | $V_{GS} = 10V, I_D = 62A$ ③                              |
| $V_{GS(th)}$                    | Gate Threshold Voltage               | 3.0  | —    | 5.0  | V                   | $V_{DS} = V_{GS}, I_D = 250\mu A$                        |
| $I_{DSS}$                       | Drain-to-Source Leakage Current      | —    | —    | 20   | $\mu A$             | $V_{DS} = 150V, V_{GS} = 0V$                             |
|                                 |                                      | —    | —    | 250  |                     | $V_{DS} = 150V, V_{GS} = 0V, T_J = 125^\circ\text{C}$    |
| $I_{GSS}$                       | Gate-to-Source Forward Leakage       | —    | —    | 100  | nA                  | $V_{GS} = 20V$                                           |
|                                 | Gate-to-Source Reverse Leakage       | —    | —    | -100 |                     | $V_{GS} = -20V$                                          |
| $R_G$                           | Internal Gate Resistance             | —    | 2.3  | —    | $\Omega$            |                                                          |

Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

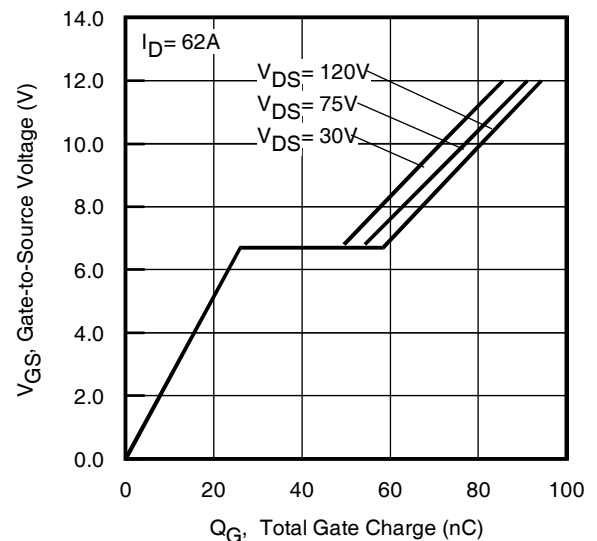
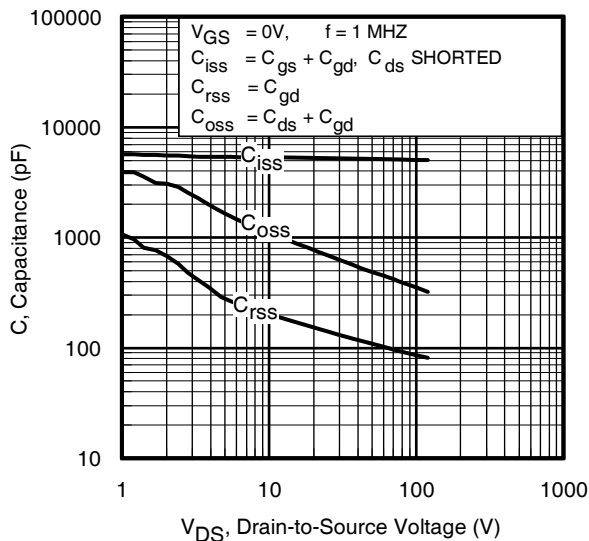
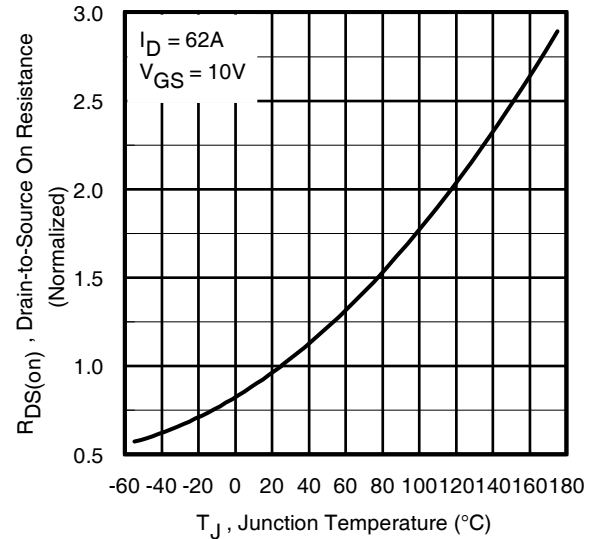
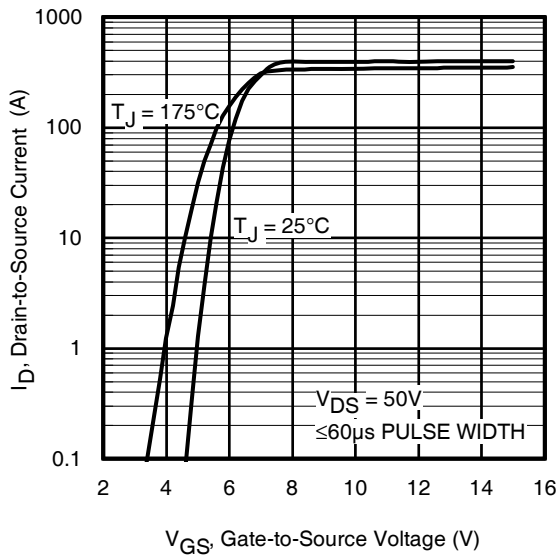
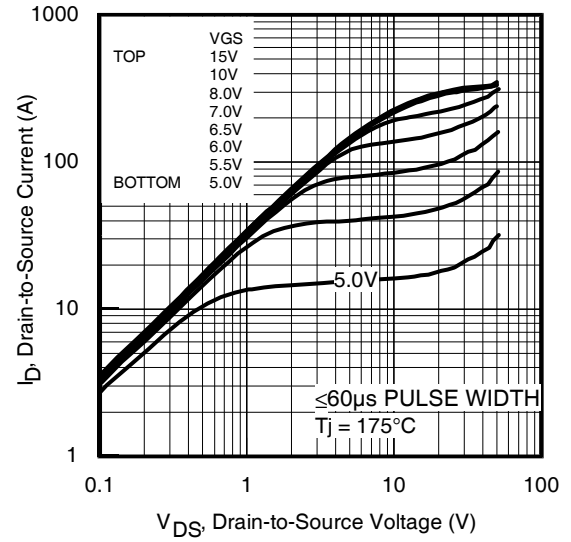
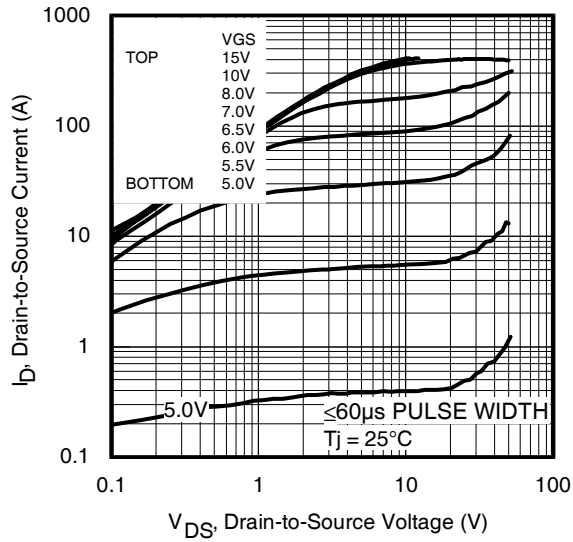
| Symbol                      | Parameter                                     | Min. | Typ. | Max. | Units | Conditions                                                 |
|-----------------------------|-----------------------------------------------|------|------|------|-------|------------------------------------------------------------|
| $g_{fs}$                    | Forward Transconductance                      | 97   | —    | —    | S     | $V_{DS} = 50V, I_D = 62A$                                  |
| $Q_g$                       | Total Gate Charge                             | —    | 77   | 120  | nC    | $I_D = 62A$                                                |
| $Q_{gs}$                    | Gate-to-Source Charge                         | —    | 28   | —    |       | $V_{DS} = 75V$                                             |
| $Q_{gd}$                    | Gate-to-Drain ("Miller") Charge               | —    | 26   | —    |       | $V_{GS} = 10V$ ⑤                                           |
| $Q_{sync}$                  | Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )    | —    | 51   | —    |       | $I_D = 62A, V_{DS} = 0V, V_{GS} = 10V$                     |
| $t_{d(on)}$                 | Turn-On Delay Time                            | —    | 18   | —    | ns    | $V_{DD} = 98V$                                             |
| $t_r$                       | Rise Time                                     | —    | 73   | —    |       | $I_D = 62A$                                                |
| $t_{d(off)}$                | Turn-Off Delay Time                           | —    | 41   | —    |       | $R_G = 2.2\Omega$                                          |
| $t_f$                       | Fall Time                                     | —    | 39   | —    |       | $V_{GS} = 10V$ ⑤                                           |
| $C_{iss}$                   | Input Capacitance                             | —    | 5270 | —    | pF    | $V_{GS} = 0V$                                              |
| $C_{oss}$                   | Output Capacitance                            | —    | 490  | —    |       | $V_{DS} = 50V$                                             |
| $C_{rss}$                   | Reverse Transfer Capacitance                  | —    | 105  | —    |       | $f = 1.0\text{ MHz}$ , See Fig. 5                          |
| $C_{oss \text{ eff. (ER)}}$ | Effective Output Capacitance (Energy Related) | —    | 460  | —    |       | $V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V$ ⑦, See Fig. 11 |
| $C_{oss \text{ eff. (TR)}}$ | Effective Output Capacitance (Time Related)   | —    | 530  | —    |       | $V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V$ ⑥              |

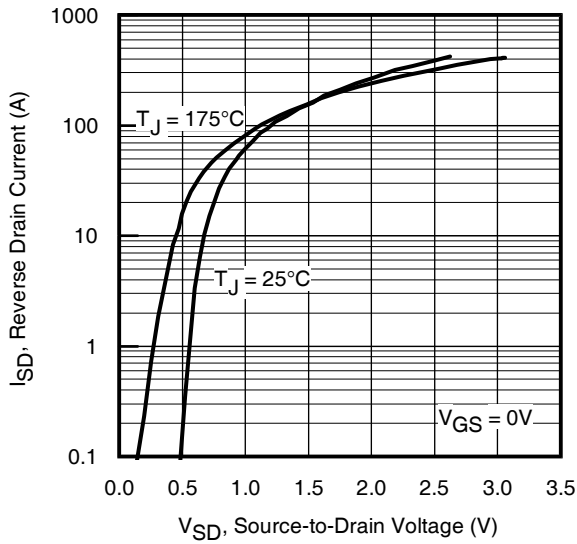
## Diode Characteristics

| Symbol    | Parameter                              | Min.                                                                 | Typ. | Max. | Units | Conditions                                                                                                                                           |
|-----------|----------------------------------------|----------------------------------------------------------------------|------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| $I_S$     | Continuous Source Current (Body Diode) | —                                                                    | —    | 99   | A     | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$  | Pulsed Source Current (Body Diode) ②   | —                                                                    | —    | 396  | A     |                                                                                                                                                      |
| $V_{SD}$  | Diode Forward Voltage                  | —                                                                    | —    | 1.3  | V     | $T_J = 25^\circ\text{C}, I_S = 62A, V_{GS} = 0V$ ③                                                                                                   |
| $t_{rr}$  | Reverse Recovery Time                  | —                                                                    | 86   | —    | ns    | $T_J = 25^\circ\text{C}$ $V_R = 130V,$                                                                                                               |
|           |                                        | —                                                                    | 110  | —    |       | $T_J = 125^\circ\text{C}$ $I_F = 62A$                                                                                                                |
| $Q_{rr}$  | Reverse Recovery Charge                | —                                                                    | 300  | —    | nC    | $T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ⑤                                                                                                      |
|           |                                        | —                                                                    | 450  | —    |       | $T_J = 125^\circ\text{C}$                                                                                                                            |
| $I_{RRM}$ | Reverse Recovery Current               | —                                                                    | 6.5  | —    | A     | $T_J = 25^\circ\text{C}$                                                                                                                             |
| $t_{on}$  | Forward Turn-On Time                   | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) |      |      |       |                                                                                                                                                      |

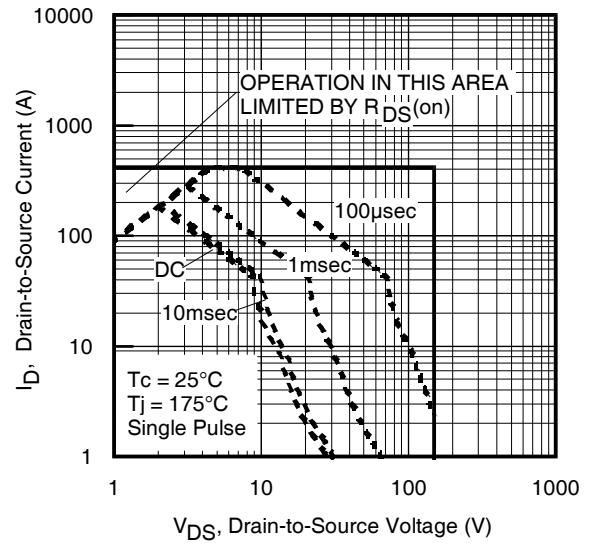
## Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Recommended max EAS limit, starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.17\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 100A$ ,  $V_{GS} = 15V$ .
- ④  $I_{SD} \leq 62A$ ,  $di/dt \leq 1040A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ⑤ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑥  $C_{oss \text{ eff. (TR)}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $C_{oss \text{ eff. (ER)}}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑩  $R_{\theta JC}$  value shown is at time zero.

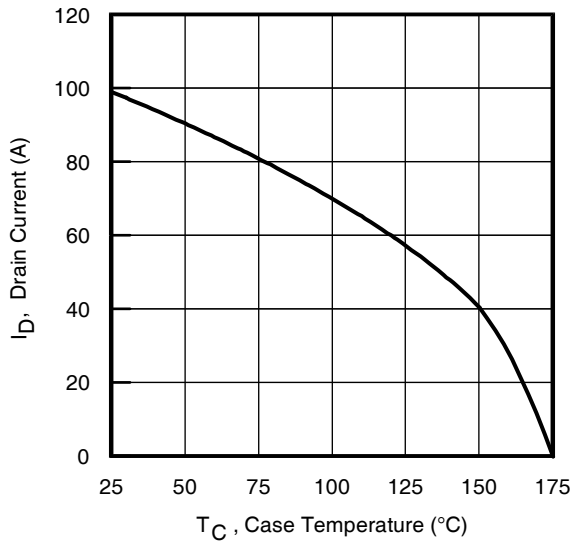




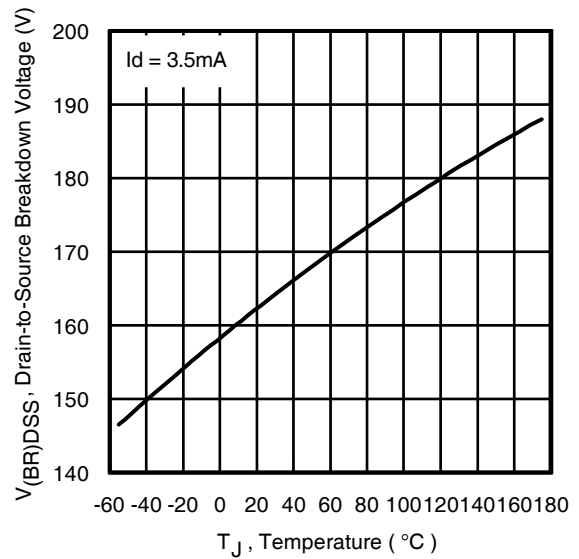
**Fig 7.** Typical Source-Drain Diode Forward Voltage



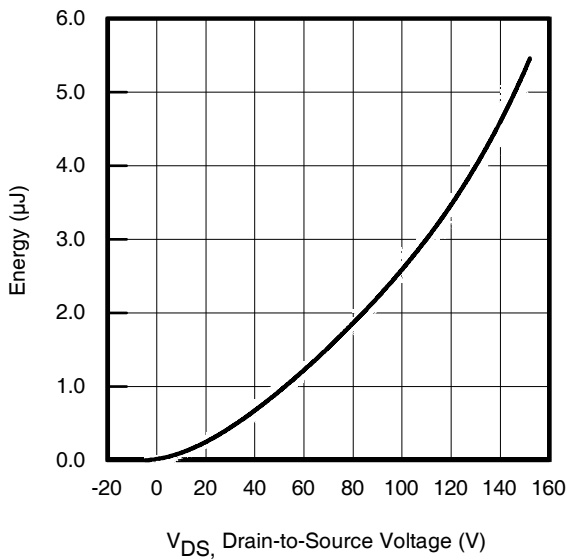
**Fig 8.** Maximum Safe Operating Area



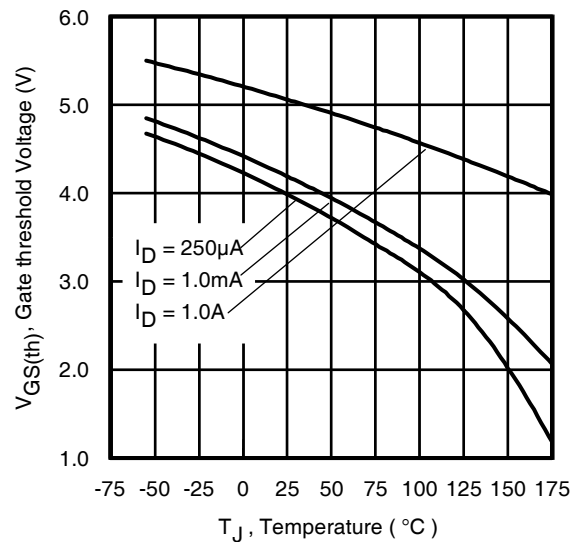
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Drain-to-Source Breakdown Voltage



**Fig 11.** Typical  $C_{OSS}$  Stored Energy



**Fig 12.** Threshold Voltage vs. Temperature

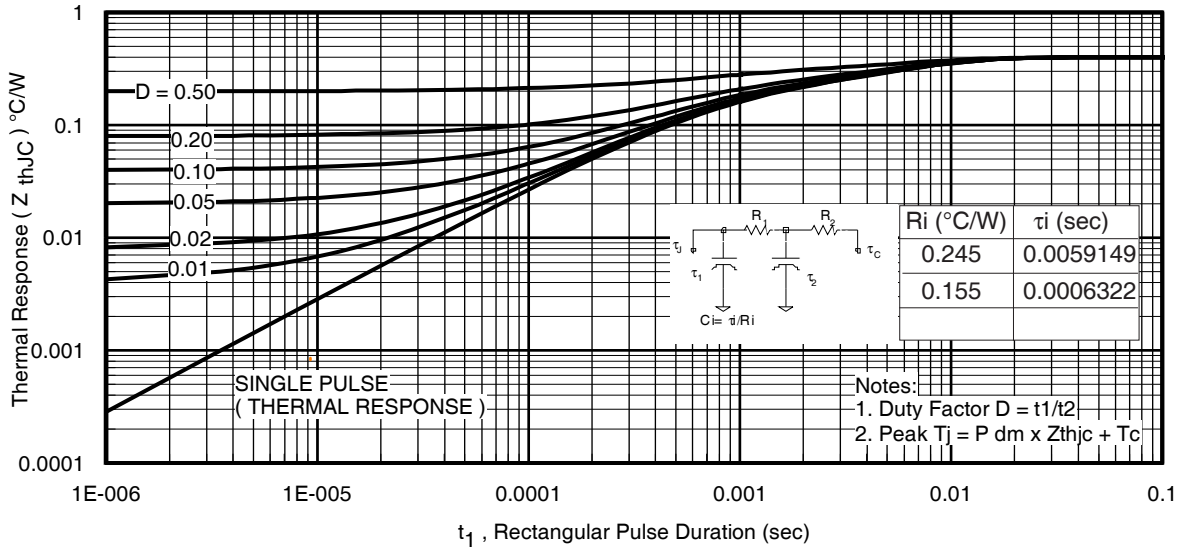


Fig. 13 Maximum Effective Transient Thermal Impedance, Junction-to-Case

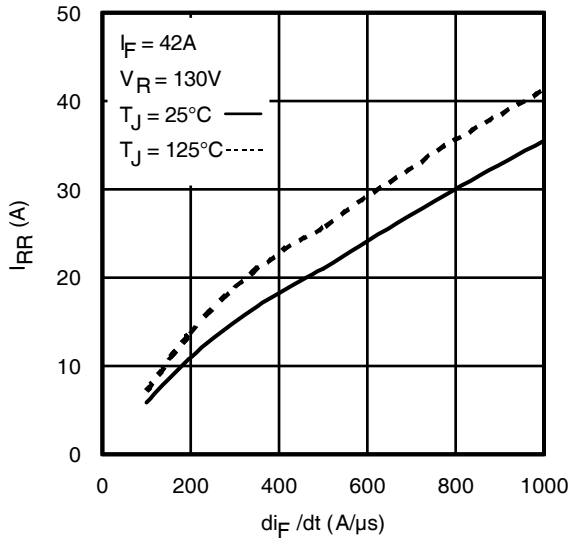


Fig. 14 - Typical Recovery Current vs.  $di_F/dt$

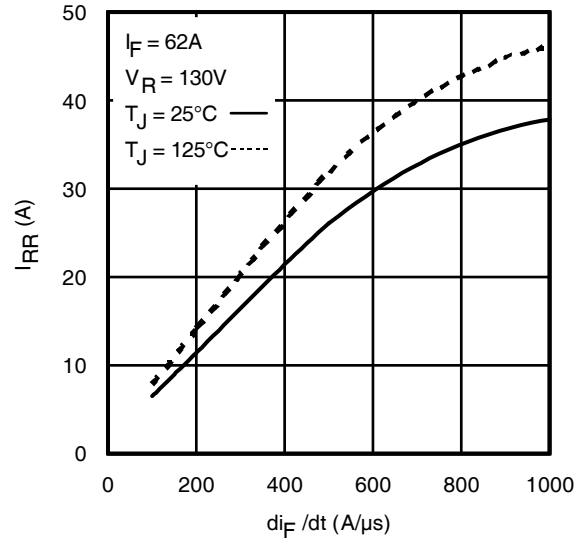


Fig. 15 - Typical Recovery Current vs.  $di_F/dt$

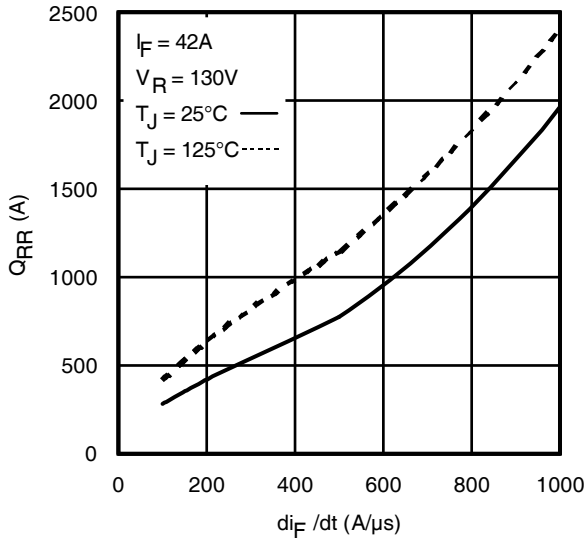


Fig. 16 - Typical Stored Charge vs.  $di_F/dt$

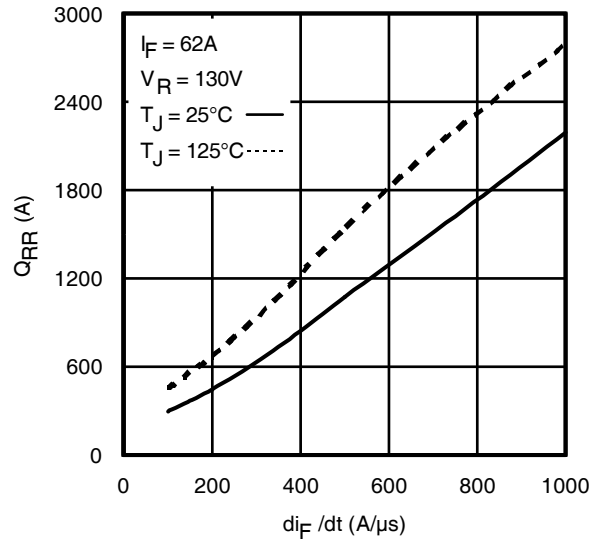
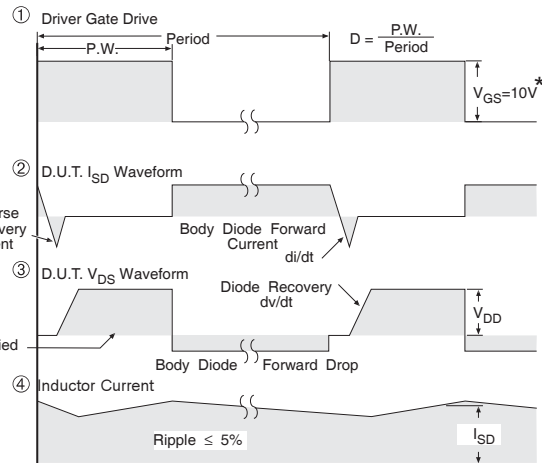
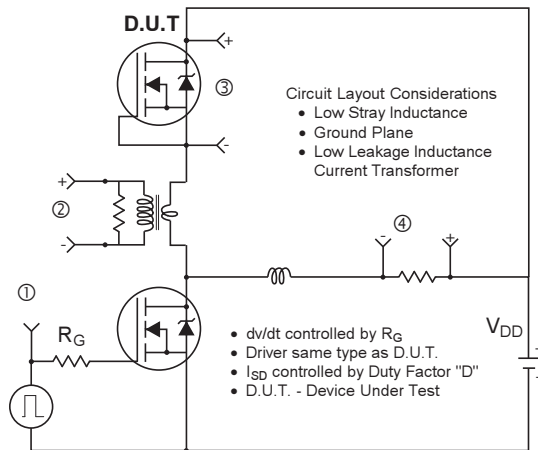
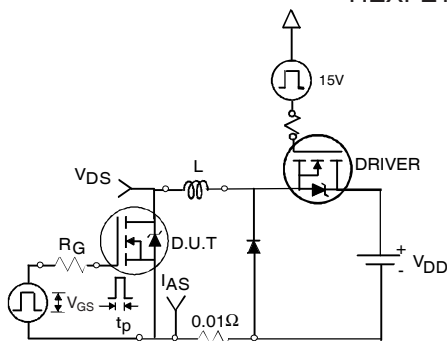


Fig. 17 - Typical Stored Charge vs.  $di_F/dt$

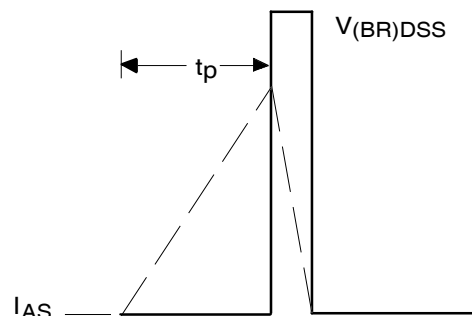


\*  $V_{GS} = 5V$  for Logic Level Devices

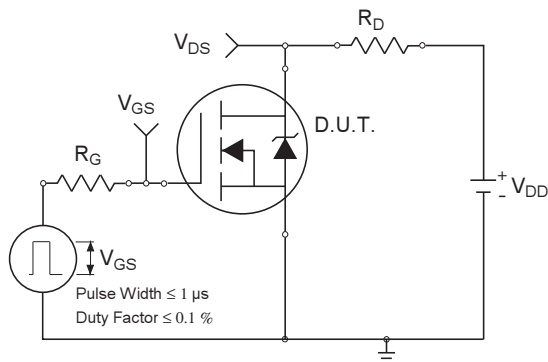
**Fig 18. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



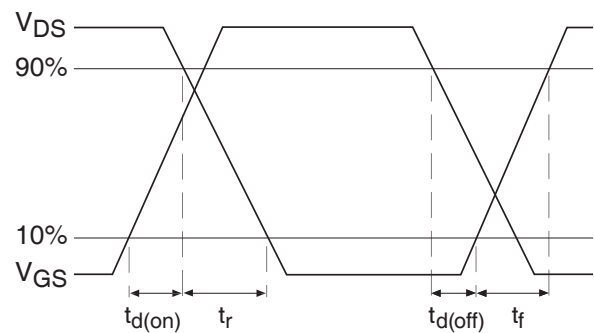
**Fig 19a. Unclamped Inductive Test Circuit**



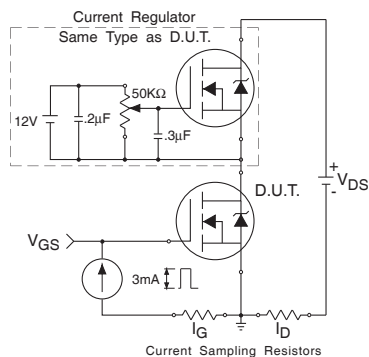
**Fig 19b. Unclamped Inductive Waveforms**



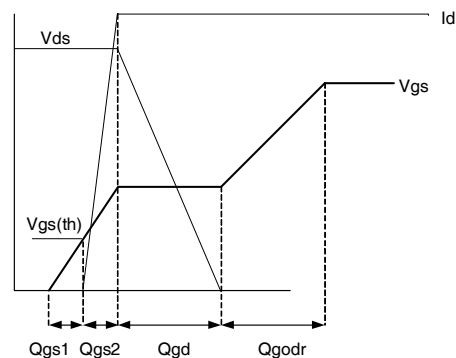
**Fig 20a. Switching Time Test Circuit**



**Fig 20b. Switching Time Waveforms**



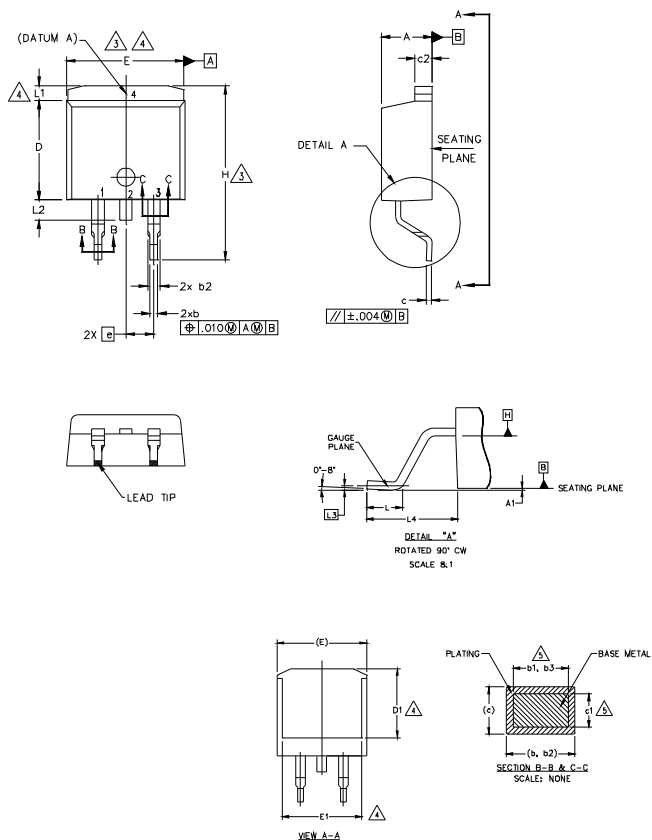
**Fig 21a. Gate Charge Test Circuit**



**Fig 21b. Gate Charge Waveform**

## D<sup>2</sup>Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

| SYMBOL | DIMENSIONS  |       |          |      | NOTES |
|--------|-------------|-------|----------|------|-------|
|        | MILLIMETERS |       | INCHES   |      |       |
|        | MIN.        | MAX.  | MIN.     | MAX. |       |
| A      | 4.06        | 4.83  | .160     | .190 | 5     |
| A1     | 0.00        | 0.254 | .000     | .010 |       |
| b1     | 0.51        | 0.99  | .020     | .039 |       |
| b2     | 0.51        | 0.89  | .020     | .035 | 5     |
| b3     | 1.14        | 1.78  | .045     | .070 |       |
| c      | 1.14        | 1.73  | .045     | .068 |       |
| c1     | 0.38        | 0.74  | .015     | .029 | 5     |
| c2     | 0.38        | 0.58  | .015     | .023 |       |
| D      | 1.14        | 1.65  | .045     | .065 |       |
| D1     | 8.38        | 9.65  | .330     | .380 | 3     |
| E      | 6.86        | —     | .270     | —    | 4     |
| E1     | 9.65        | 10.67 | .380     | .420 | 3,4   |
| e      | 6.22        | —     | .245     | —    | 4     |
| H      | 2.54 BSC    |       | .100 BSC |      | 4     |
| L      | 14.61       | 15.88 | .575     | .625 |       |
| L1     | 1.78        | 2.79  | .070     | .110 |       |
| L2     | —           | 1.65  | —        | .066 |       |
| L3     | 1.27        | 1.78  | —        | .070 |       |
| L4     | 0.25 BSC    |       | .010 BSC |      |       |
| L4     | 4.78        | 5.28  | .188     | .208 |       |

### LEAD ASSIGNMENTS

HEXFET

- 1.- GATE  
2, 4.- DRAIN  
3.- SOURCE

IGBTs, CoPACK

- 1.- GATE  
2, 4.- COLLECTOR  
3.- EMITTER

## DIODES

- 1.- ANODE \*  
2, 4.- CATHODE  
3.- ANODE

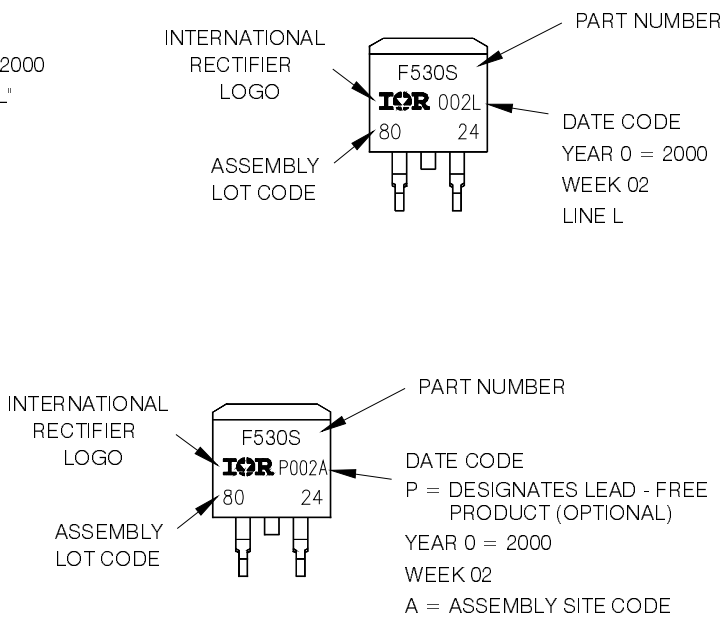
\* PART DEPENDENT.

## D<sup>2</sup>Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead - Free"

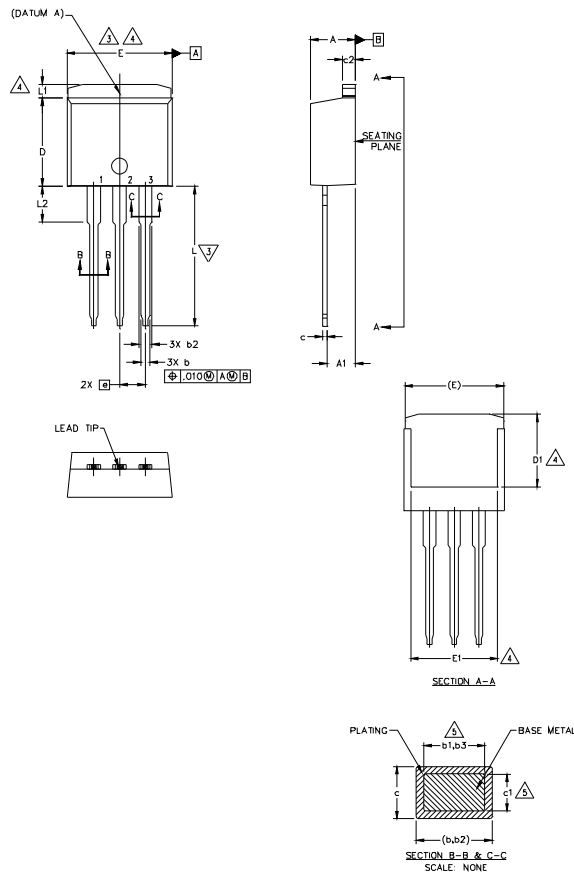
OR



**Note:** For the most current drawing please refer to IR website at <http://www.irf.com/package/www.irf.com>

## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

| SYMBOL | DIMENSIONS  |       |          |      | NOTES |
|--------|-------------|-------|----------|------|-------|
|        | MILLIMETERS |       | INCHES   |      |       |
|        | MIN.        | MAX.  | MIN.     | MAX. |       |
| A      | 4.06        | 4.83  | .160     | .190 |       |
| A1     | 2.03        | 3.02  | .080     | .119 |       |
| b      | 0.51        | 0.99  | .020     | .039 |       |
| b1     | 0.51        | 0.89  | .020     | .035 | 5     |
| b2     | 1.14        | 1.78  | .045     | .070 |       |
| b3     | 1.14        | 1.73  | .045     | .068 | 5     |
| c      | 0.38        | 0.74  | .015     | .029 |       |
| c1     | 0.38        | 0.58  | .015     | .023 | 5     |
| c2     | 1.14        | 1.65  | .045     | .065 |       |
| D      | 8.38        | 9.65  | .330     | .380 | 3     |
| D1     | 6.86        | —     | .270     | —    | 4     |
| E      | 9.65        | 10.67 | .380     | .420 | 3,4   |
| E1     | 6.22        | —     | .245     | —    | 4     |
| e      | 2.54 BSC    |       | .100 BSC |      |       |
| L      | 13.46       | 14.10 | .530     | .555 |       |
| L1     | —           | 1.65  | —        | .065 | 4     |
| L2     | 3.56        | 3.71  | .140     | .146 |       |

## LEAD ASSIGNMENTS

## HEXFET

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

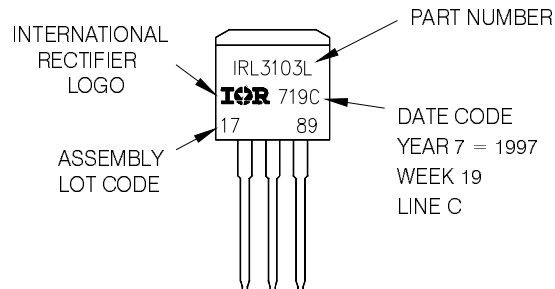
## IGBTs, CoPACK

1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

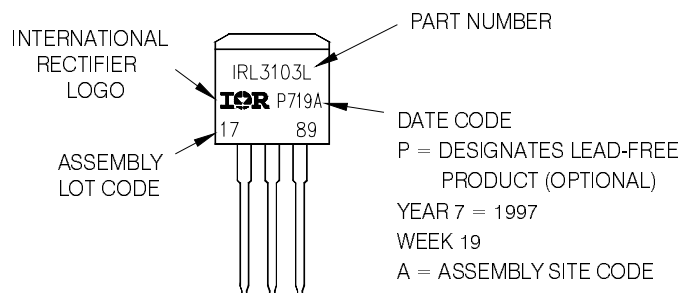
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



OR

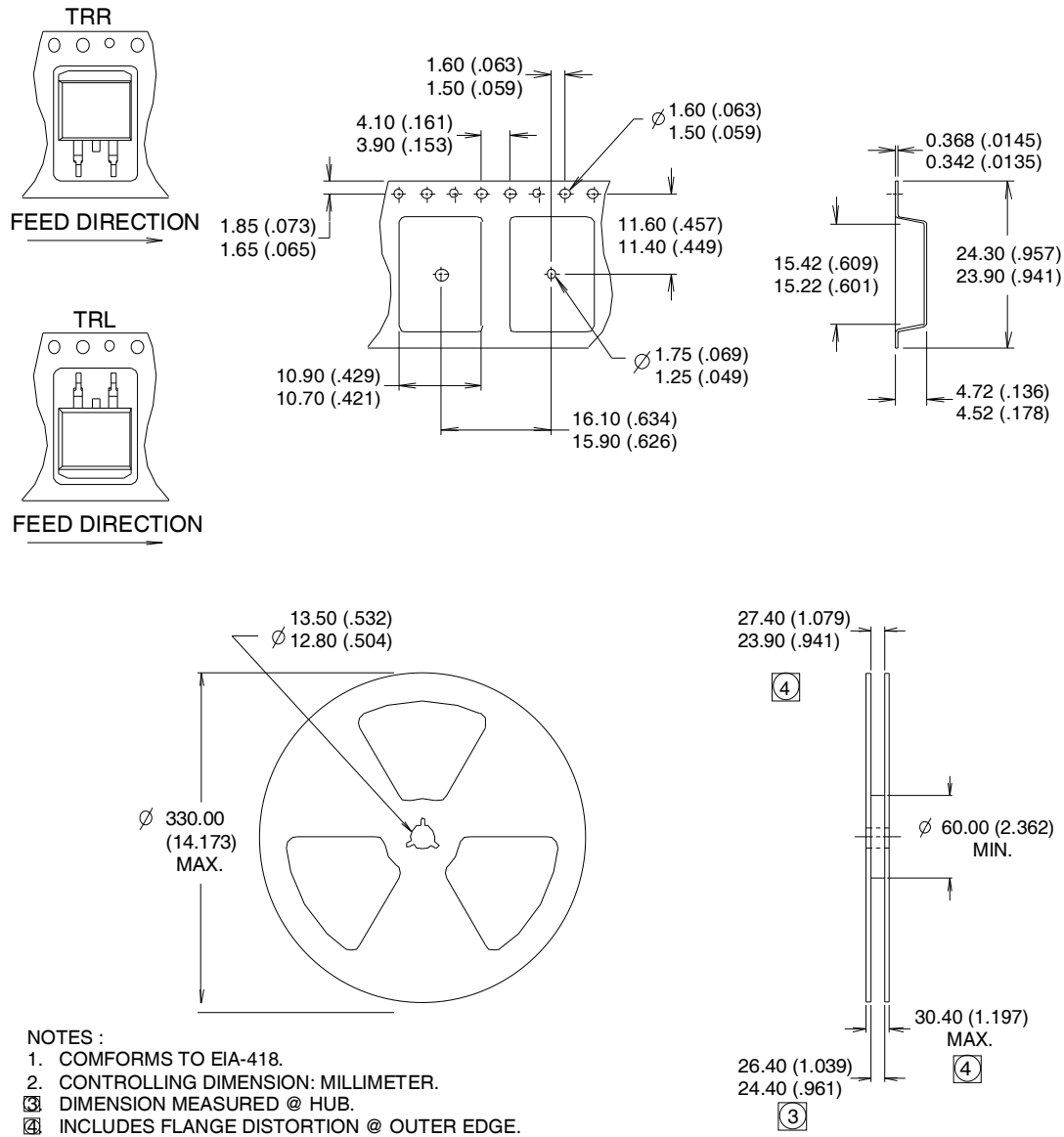


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



## D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IOR** Rectifier

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