

Advance Information

MC92460EC/D
Rev. 1.0, 5/2002

MC92460 HDLC Controller
Hardware Specifications



NCSD Applications

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MC92460 Multichannel HDLC Controller.

The following topics are addressed:

Topic	Page
Section 1.1, "Features"	2
Section 1.2, "Electrical and Thermal Characteristics"	4
Section 1.2.1, "DC Electrical Characteristics"	4
Section 1.2.2, "Thermal Characteristics"	6
Section 1.2.3, "Power Considerations"	6
Section 1.2.4, "Power Dissipation"	6
Section 1.2.5, "AC Specifications"	7
Section 1.2.5.1, "SYSCLK Timing"	7
Section 1.2.5.2, "EXCLK Timing"	7
Section 1.2.5.3, "AC Timing"	8
Section 1.3, "Pinout"	11

Features

Figure 1 shows a block diagram of the MC92460.

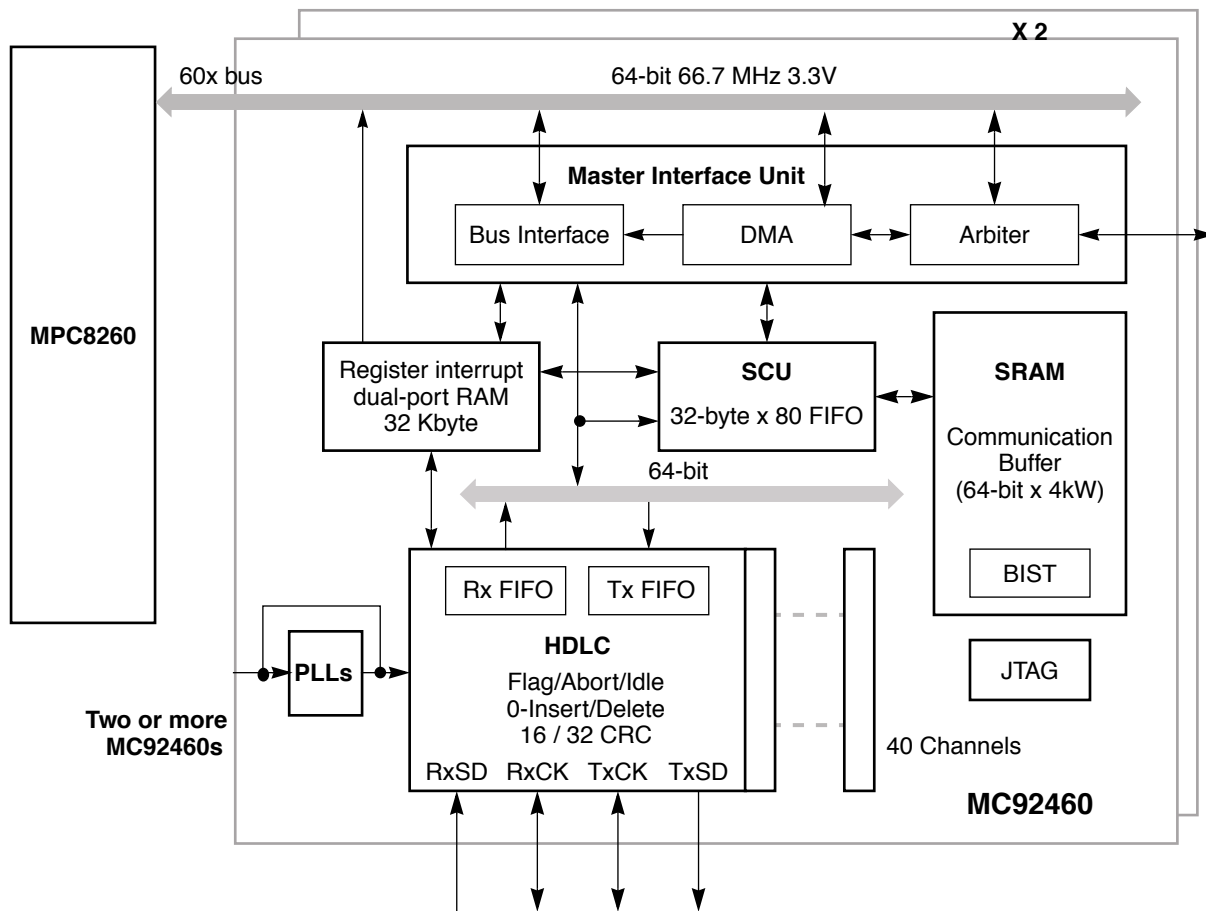


Figure 1. MC92460 Block Diagram

1.1 Features

The following is an overview of the MC92460 feature set:

- Channels
 - 40 full-duplex HDLC channels
 - Programmable channel assignment (any logical channel to any signal)
 - Each channel has a default of 64 buffer descriptors (Rx and Tx) but the number of buffer descriptors per channel is configurable
- Controllers
 - Maximum throughput of 1919 Mbps; individual controllers operate up to 66.7 Mbps
 - All communication controllers operate asynchronously
 - Programmable frame size (maximum 65,535 bytes)
 - Transparent memory access with internal memory controller
- 60x Bus
 - MC92460 directly connects with a 64-bit data and 32-bit address 60x bus
 - Supports 66.7 MHz 60x bus speed, with aggregate bandwidth of up to 1919 Mbps depending

- on the type of main memory used
- Up to four MC92460's may be connected in parallel on the 60x bus
- Bus supports multiple master design
- Communication Buffers
 - Data Buffer
 - 256 Kbits on-chip memory for data buffers
 - 256 Kbit communication buffer can store up to 819 bytes per frame.
 - 80 channel virtual DMA functionality executes between off-chip memory and the communication buffer
 - BD Buffer
 - 32 Kbyte on-chip dual-port RAM for buffer descriptors
 - A total of 4096 buffer descriptors (2048 TxBD and 2048 RxBD)
- JTAG Support
 - Supports the IEEE1149.1 JTAG controller standard
- Power and Clocks
 - Supports single-beat and burst accesses
 - On-chip PLL for baud rate generator (maximum of 66.7 MHz)
 - Separate power supplies for core internal logic (1.8V) and for I/O (3.3V)
- Package
 - 480 pin TPGA, 1.27 mm pitch

1.2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MC92460.

1.2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MC92460. Table 1 shows the maximum electrical ratings.

Table 1. Maximum Temperatures and Voltages

Rating	Symbol	Value Name	Unit
Core supply voltage	VDD	-0.3 – 2.5	V
I/O supply voltage	VDDH	-0.3 – 3.6	V
Input voltage	VIN	GND-0.3 – 3.6	V
Junction temperature	T _J	120	°C
Storage temperature range	T _{STG}	-55 – 150	°C
Ambient temperature	T _A	-40 – 85	°C

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.65 – 1.95	V
I/O supply voltage	VDDH	3.15 – 3.465	V
Input voltage	VIN	GND -0.3 – 3.6	V
Junction temperature	T _J	105	°C

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Table 3 shows DC electrical characteristics.

Table 3. DC Electrical Characteristics

TA=0 to 85°C; VDD=2.0±5% Vdc; VDDH=3.3±5% Vdc; GND=0Vdc; Load Capacitance < 10pF

Characteristics	Conditions	Symbol	Min	Max	Unit
Input high voltage		V _{IH}	2.0	3.465	V
Input low voltage		V _{IL}	GND	0.8	V
Input leakage current	V _{IN} =VDDH	I _{IN}	–	10	μA
HI-Z leakage current	V _{IN} =VDDH, GND	I _{OZ}	–10	+10	μA
Signal low input current	V _{IL} =0.8V	I _{IL}	–	60	μA
Signal high input current	V _{IH} =2.0V	I _{IH}	–	60	μA
Output high voltage	I _{OH} =-7.0mA	V _{OH}	2.4	-	V

Table 3. DC Electrical Characteristics (continued)

TA=0 to 85°C; VDD=2.0±5% Vdc; VDDH=3.3±5% Vdc; GND=0Vdc; Load Capacitance < 10pF

Output low voltage • BR • BG • ABB • TS • A[0-31] • AP[0-3] • APE • TT[0-4] • TBST • TSIZ[0-2] • GBL • CI • WT • LBCLAIM • BTO • INT • TC[0-1] • AACK • ARTRY • DBG • DBWO • DBB • DH[0-31],DL[0-31] • DP[0-7] • DPE • DBDIS • TA • DRTRY • TEA	$I_{OL}=7.0\text{mA}$	V_{OL}		0.4	V
Output low voltage • Rx CLK[0-39] • Tx CLK[0-39] • Tx SD[0-39] • TDO • SBG • SDBG • SBR • SIRQ • CS0 • CS1 • CS2	$I_{OL}=5.0\text{mA}$	V_{OL}		0.4	V

1.2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Maximum Temperatures and Voltages

Characteristics	Symbol	Thermal Resistance Value	Unit	Air Flow
Thermal resistance for 480 TBGA	θ_{JA}	10.48	°C/W	0 LFM
		8.61	°C/W	100 LFM
		7.78	°C/W	200 LFM
		6.89	°C/W	400 LFM
		5.52	°C/W	800 LFM

LFM = Linear Feet per Minute

1.2.3 Power Considerations

The average chip-junction temperature, T_J , can be obtained from the following:

$$T_J = T_A + (P_D \cdot \theta_{JA})$$

where

θ_{JA} = package thermal resistance, junction to ambient, °C/W

T_A = ambient temperature, °C

Power equations are the following:

$P_D = P_{VDD} + P_{VDDH}$ = chip total power dissipation, W

$P_{VDD} = I_{VDD} \times VDD$ = chip core power, W

$P_{VDDH} = I_{VDDH} \times VDDH$

= user-determined power dissipation on input/output pins, W

1.2.4 Power Dissipation

Table 5 describes maximum chip core power dissipation.

Table 5. Maximum Core Power Dissipation (PVDD)

VDD(V)	SYSCLK Frequency (MHz)	I _{VDD} (mA)	P _{VDD} (mW)	P _{VDDH} (mW)
1.95	66.7	650	980	920

1.2.5 AC Specifications

These AC specifications are target specifications.

1.2.5.1 SYSCLK Timing

Table 6 shows the system clock timing.

Table 6. Clock Timing

Characteristics	Symbol	Min	Max	Unit
Operation Frequency	f	60.0	66.7	MHz
Clock period		15.0	16.7	nS
Clock pulse width	t_{CL}, t_{CH}	7	8	nS
SYSCLK input high voltage	V_{IHC}	2.4	3.465	V
SYSCLK input low voltage	V_{ILC}	GND	0.4	V
SYSCLK Jitter			± 200	pS

Figure 2 shows the SYSCLK.

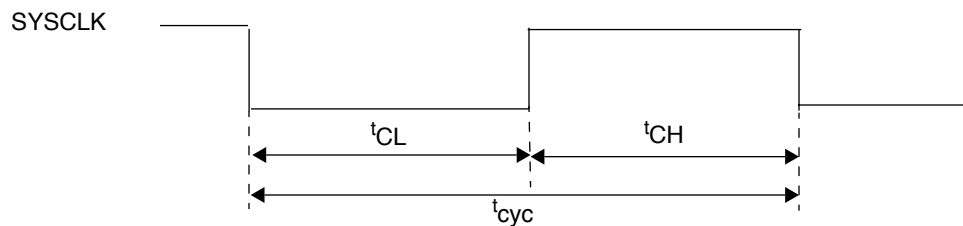


Figure 2. SYSCLK

1.2.5.2 EXCLK Timing

Table 7 shows the external clock timing.

Table 7. Clock Timing

Characteristics	Symbol	Min	Max	Unit
Operation Frequency	f	14.0	16.0	MHz
Clock duty		40	60	%
Clock Pulse width	t_{CL}, t_{CH}	25	42.8	nS
EXCLK input high voltage	V_{IHC}	2.4	3.465	V
EXCLK input low voltage	V_{ILC}	GND	0.4	V
EXCLK Jitter			± 200	pS

Electrical and Thermal Characteristics

Figure 3 shows the EXCLK.

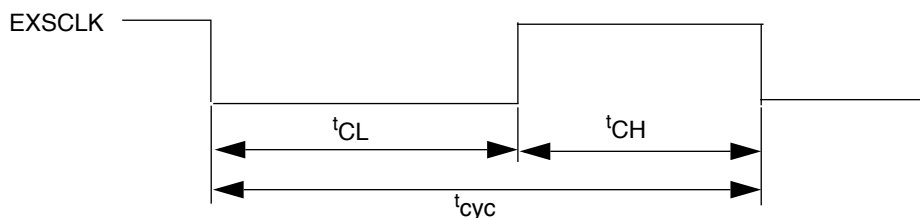


Figure 3. EXCLK

1.2.5.3 AC Timing

Figure 4 shows the HDLC external clock with polarity not inverted. All time specifications were measured at expected load capacitance $C_L=8\text{pF}$.

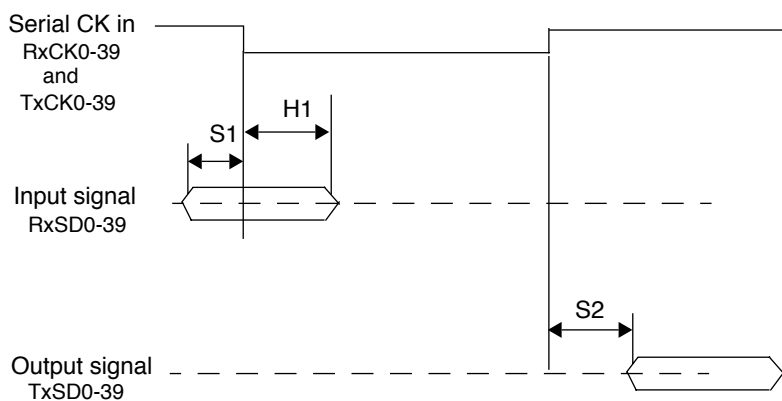


Figure 4. HDLC External Clock

Figure 5 shows an HDLC internal clock (TxCK/RxCK output mode) whose polarity is not inverted.

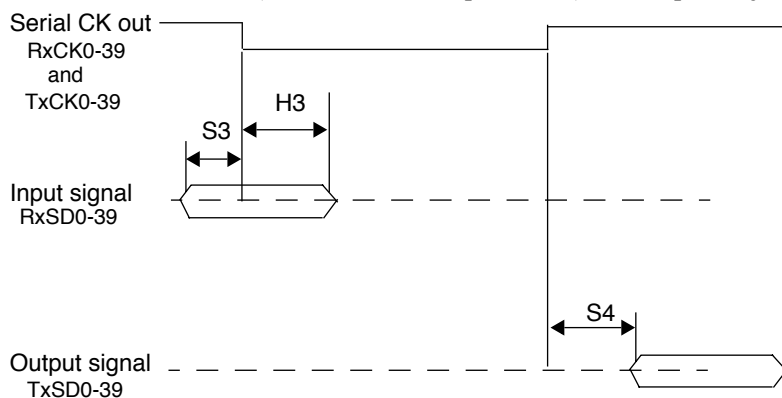


Figure 5. HDLC Internal Clock

Table 8 shows the AC electrical characteristics. The frequency is 20 MHz.

Table 8. AC Electrical Characteristics

Spec Num	Characteristic	Min	Max	Unit
S1	HDLC input- external clock setup time	2		nS
H1	HDLC input -external clock hold time	1		nS
S2	HDLC output- external clock setup time		14	nS
S3	HDLC input- internal clock setup time	12		nS
H3	HDLC input- internal clock hold time	0		nS
S4	HDLC output- internal clock setup time		4	nS

Figure 6 shows the interaction of several bus signals.

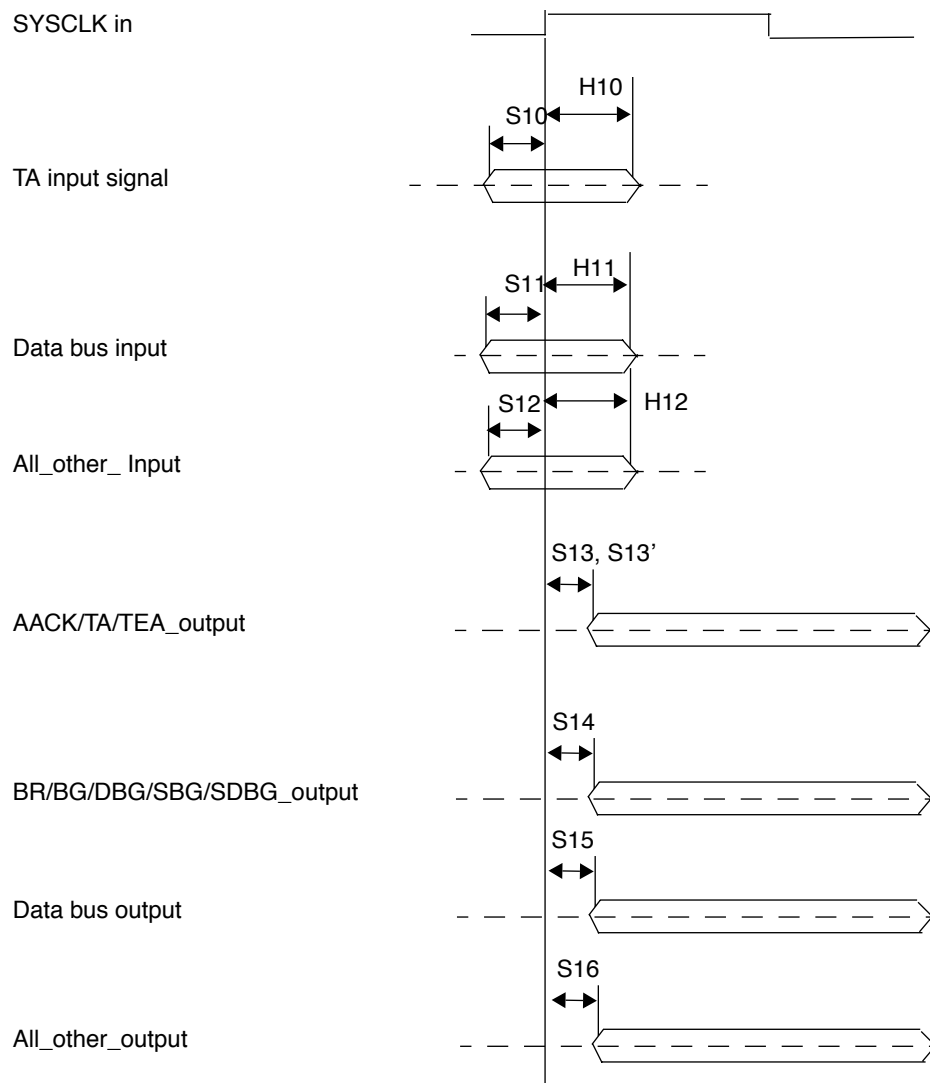


Figure 6. Bus Signals

Electrical and Thermal Characteristics

Table 9 shows the bus signal I/O characteristics. The frequency is 20 MHz.

Table 9. Bus Input/Output Characteristics

Spec Num	Characteristic	Min	Max	Unit
S10	TA/TEA input	6		nS
H10	TA/TEA input		1	nS
S11	Data bus input signals	7		nS
H11	Data bus input signals		1	nS
S12	All other input signals	7		nS
H12	All other input signals		1	nS
S13	AACK/TEA output	1	7	nS
S13'	TA output	1	8.5	nS
S14	BR/BG/DBG/SBG/SDBG output	1	7	nS
S15	Data bus output signals	1	8.5	nS
S16	All other output signals	1	7	nS

1.3 Pinout

Table 10. Pin Assignments

	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ball		
A	PwV6526 PwV6557 PwV6555	PwV6528 TEST0 PwV6525	PwV6528 TEST0 PwV6525	scan_out_e scan_out_h scan_out_g	PwV6523 CoreV6515 scan_out_j	PwV6523 CoreV6515 scan_out_j	PwV6523 CoreV6515 scan_out_j	D9 D1 D56	CoreV6523 D25 PwV6525	D57 D25 D49	D32 CoreV6516 D49	D32 D10 CoreV6516	D42 PwV6527 D54	D11 D3 D58	D55 PwV6528 CoreV6524	D59 CoreV6517 PwV6529	CoreV6517 D20 D4	D28 PwV6530 D56	D52 D60 D5	D21 DP7 D29	D45 PwV6532 D53	D61 D6 D14	PwV6533 CoreV6525 PwV6526	D54 D62 CoreV6525	CoreV6519 D31 CoreV6525	D54 D38 D47	D54 D38 D47	PwV6529 PwV6554 DP1	PwV656 PwV658 PwV6530	B		
B	PwV6527 PwV6525 TEST2	PwV6527 TEST2 PwV6525	PwV6527 TEST2 PwV6525	scan_out_h scan_out_g scan_out_e	CoreV6515 scan_out_j scan_out_e	CoreV6515 scan_out_j scan_out_e	CoreV6515 scan_out_j scan_out_e	D1 D56 D56	D25 D49 D49	CoreV6516 D49 D49	D10 CoreV6516 D49	D32 D10 CoreV6516	PwV6527 D54 D54	D3 D58 D58	PwV6528 CoreV6524 D27	CoreV6517 PwV6529 D43	D20 D4 D40	PwV6530 D56 D44	D60 D5 PwV6531	DP7 D29 CoreV6518	PwV6532 D53 CoreV6518	D38 D14 CoreV6518	CoreV6525 PwV6526 CoreV6518	D54 D62 CoreV6525	CoreV6519 D31 CoreV6525	D54 D38 D47	PwV6529 PwV6554 DP1	PwV656 PwV658 PwV6530	C			
D	SEN CSA5	FOR CSA3	SMOD0 CSA3	PwV6523 scan_out_e	PwV6523 scan_out_e	CSA2 scan_out_l	CSA2 scan_out_l	D48 D17	D41 D17	D2 D41	D2 D41	D26 D26	CoreV6524 D18	D27 D19	D43 D51	D40 D12	D44 scan_out_j	PwV6531 D13	PwV6531 D13	CoreV6518 D37	CoreV6518 DP6	D22 D38	D46 D7	D15 CoreV6519	PwV6535 D63	PwV652 TS20	DP2 PwV640	DP3 CoreV640	D			
E	CSA5	CSA3	TEST3	SMODE1	PwV6522	CS2	CS0	D24	D16	D33	PwV6526	D18	D50	D19	D51	D12	scan_out_j	D13	D37	DP6	D38	D7	CoreV6519	D63	PwV6541	TR	TS20	PwV640	CoreV640	E		
F	CSA1	PwV6521	DEW0	scan_out_d	AMODE																				TEST	TS21	DEG	TS	CoreV650	F		
G	PCMD	TEST1	DEW5	CoreV6514	CoreV6514																				TS22	CT360	AB	XCK	XTYPP	G		
H	TCK	TEST	TD1	RESET	CSA0																				ERG	PwV651	TT0	DPE	TT2	H		
J	PLL20	ACoreV652	EXCLK	TDO	TMS																				TT1	TT3	TT4	SDSG	PwV652	J		
K	scan_out_c	RcS39	CoreV6513	RcK39	ACoreV652																				DBB	A0	CoreV651	A1	SEG	K		
L	RcS39	RcK38	TS309	CoreV6513	TxCK38																				A2	A3	CoreV651	A4	PwV653	L		
M	RcS37	RcK37	TxS308	PwV6520	TxCK38																				A5	A6	ERR	A7	AI	M		
N	TxCK38	RcS36	RcK36	TxS37	TxCK37																				A9	PwV654	A10	A11	ERR	N		
P	CoreV6512	TxS306	TxCK35	RcS35	RcK35																				A13	A14	PwV655	A12	A15	P		
R	TxS35	CoreV6512	scan_out_b	RcS34	RcK34																				CoreV6520	A16	A17	CoreV652	CoreV652	R		
T	TxCK34	RcS33	TxS324	PwV6519	RcK33																				A20	PwV656	A19	A21	A18	T		
U	TxCK33	TxS333	RcK32	RcS32	TxCK32																				PwV657	A24	A23	CoreV6520	A22	U		
V	TxS32	RcK31	RcS31	TxCK31	TxS31																				TEFA	A28	A27	A26	A25	V		
W	RcK30	scan_out_a	RcS30	CoreV6511	TxCK30																				CoreV658	A31	PwV658	A30	A29	W		
Y	CoreV6511	TxS300	PwV6518	RcK29	TxCK29																				DRYR	DECTM	SRD	CoreV653	INT	Y		
AA	RcS29	TxS29	RcK28	RcS28	RcK27																				AP3	PwV659	AP0	CSA6	B10	AA		
AB	TxCK28	TxS208	RcS27	TxCK27	scan_in_k																				CI	WT	XPE	AP2	AP1	AB		
AC	TxS27	RcK26	RcS26	CoreV6510	CoreV6510																				TC0	DE	MODE	PwV6510	CSA4	AC		
AD	TxCK26	PwV6517	TxS206	TxCK25	TxCK24																				PLL10	TxCK0	CoreV654	TC1	CSA7	AD		
AE	RcK25	TxS225	TxS224	PwV6515	PwV6515																				PwV658	RcS30	ACoreV651	SYSLK	CoreV654	AE		
AF	RcS24	RcK24	RcK23	PwV6516	RcK22																					RcK1	PwV659	RcK0	ACoreV651	TxS30	AF	
AG	PwV6534	RcS23	PwV6517	TxS23	TxS22																						CSA8	RcS31	PwV6510	TxS31	PwV6531	AG
AH	PwV6521	PwV6518	TxCK23	TxCK22	RcK21																							TxCK2	TxCK1	PwV6511	PwV6513	AH
AJ	PwV6519	PwV6520	PwV6533	scan_in_j	RcS21																							TxS32	PwV652	PwV6514	PwV6512	AJ
29																															1	

HOW TO REACH US:**USA/EUROPE/LOCATIONS NOT LISTED:**

Motorola Literature Distribution
P.O. Box 5405, Denver, Colorado 80217
1-303-675-2140 or 1-800-441-2447

JAPAN:

Motorola Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu Minato-ku
Tokyo 106-8573 Japan
81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.
Silicon Harbour Centre, 2 Dai King Street
Tai Po Industrial Estate, Tai Po, N.T., Hong Kong
852-26668334

TECHNICAL INFORMATION CENTER:

1-800-521-6274

HOME PAGE:

<http://www.motorola.com/semiconductors>

DOCUMENT COMMENTS:

FAX (512) 933-2625
Attn: NCSD Applications Engineering

Information in this document is provided solely to enable system and software implementers to use Motorola products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein.

Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.

**MOTOROLA**

Motorola and the Stylized M Logo are registered in the U.S. Patent and Trademark Office. digital dna is a trademark of Motorola, Inc. All other product or service names are the property of their respective owners. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

© Motorola, Inc. 2002

MC92460EC/D

AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit www.ameya360.com

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com