TUSB8040A1 Four-Port USB 3.0 Hub

1 Device Overview

1.1 Features

- USB 3.0 Compliant Hub, TID #330000037
  - Upstream Port Supports SuperSpeed USB, High-Speed and Full-Speed Connections
  - Supports Four Downstream Ports
  - Each of the Four Downstream Ports Support SuperSpeed USB, High-Speed, Full-Speed, or Low-Speed Connections
- USB 2.0 Hub Features
  - Multiple Transaction Translator (MTT) Hub: Four Transaction Translators, One Per Port
  - Four Asynchronous Endpoint Buffers Per Transaction Translator (TT) for Better Throughput Than the USB-Required Minimum of Two Buffers Per TT
- Supports Battery Charging Applications
  - Battery Charging 1.2 Charging Downstream Port (CDP) When Upstream Port is Connected
  - Battery Charging 1.2 and Chinese Telecommunications Industry Standard YD/T 1591-2009 Dedicated Charging Port (DCP) When Upstream Port Is Disconnected
- Supports Operation as a USB 3.0 or USB 2.0 Compound Device
- Supports Per Port or Ganged Power Switching and Overcurrent Notification Inputs
- Provides the Following Status Outputs:
  - High-Speed Upstream Connection
  - High-Speed Upstream Port Suspended
  - SuperSpeed USB Upstream Connection
  - SuperSpeed USB Upstream Port Suspended
- Optional Serial EEPROM or SMBus Slave Interface for Custom Configurations:
  - VID or PID
  - Manufacturer and Product Strings
  - Serial Number
- Using Pin Selection or EEPROM and SMBus Slave Interface, Each Downstream Port Can Be Independently:
  - Enabled or Disabled
  - Marked as Removable or Permanently Attached (for Compound Applications)
  - Have Battery Charging Enabled or Disabled
- Provides 128-Bit Universally Unique Identifier (UUID)
- Optionally Supports USB 2.0 Compliant Port Indicator LEDs
- Configurable SMBus Address to Support Multiple Devices on the Same SMBus Segment
- Supports Onboard and In-System EEPROM Programming Through the USB 2.0 Upstream Port
- Single Clock Input, 24-MHz Crystal or Oscillator
- No Special Driver Requirements; Works Seamlessly With Any Operating System With USB Stack Support

1.2 Applications

- Computer Systems
- Docking Stations
- Monitors
- Set-top Boxes

1.3 Description

The TUSB8040A1 is a four-port USB 3.0 compliant hub and is available in a 100-pin WQFN package. The device is designed for operation over the commercial temperature range of 0°C to 70°C.

The TUSB8040A1 provides simultaneous SuperSpeed USB and high-speed or full-speed connections on the upstream port and provides SuperSpeed USB, high-speed, full-speed, or low-speed connections on the downstream ports. When the upstream port is connected to an electrical environment that only supports high-speed, full-speed, or low-speed connections, SuperSpeed USB connectivity is disabled on the downstream ports. When the upstream port is connected to an electrical environment that only supports full-speed or low-speed connections, SuperSpeed USB and high-speed connectivity are disabled on the downstream ports.

The TUSB8040A1 supports up to four downstream ports. The device may be configured to report one to four downstream ports by pin selection or by an attached EEPROM or SMBus controller. The configuration options provide the ability to scale the device by application.

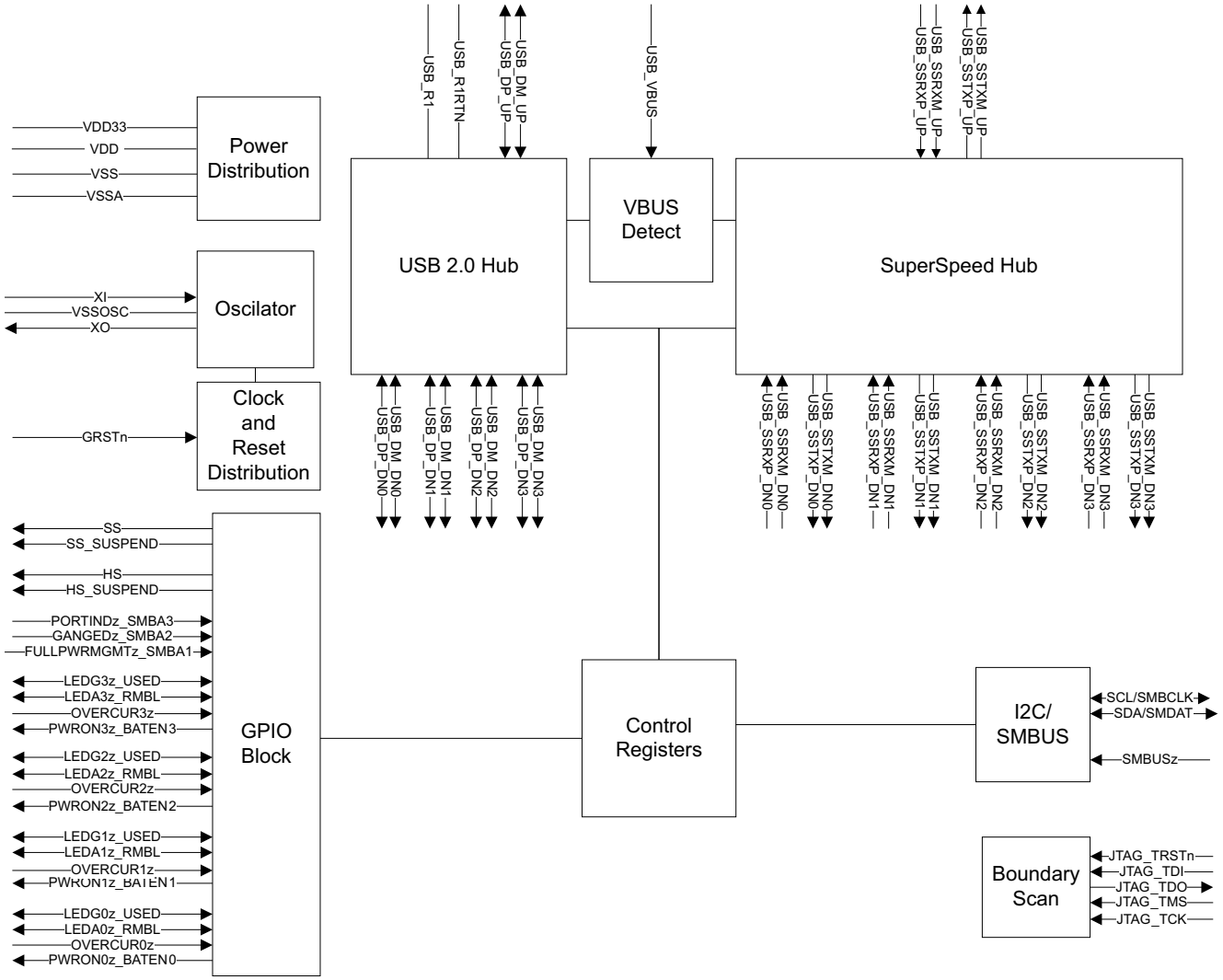
Figure 6-1 shows a typical view of the TUSB8040A1.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB8040A1	WQFN (100)	9.00 mm x 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

1.4 Functional Block Diagram



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2 Revision History

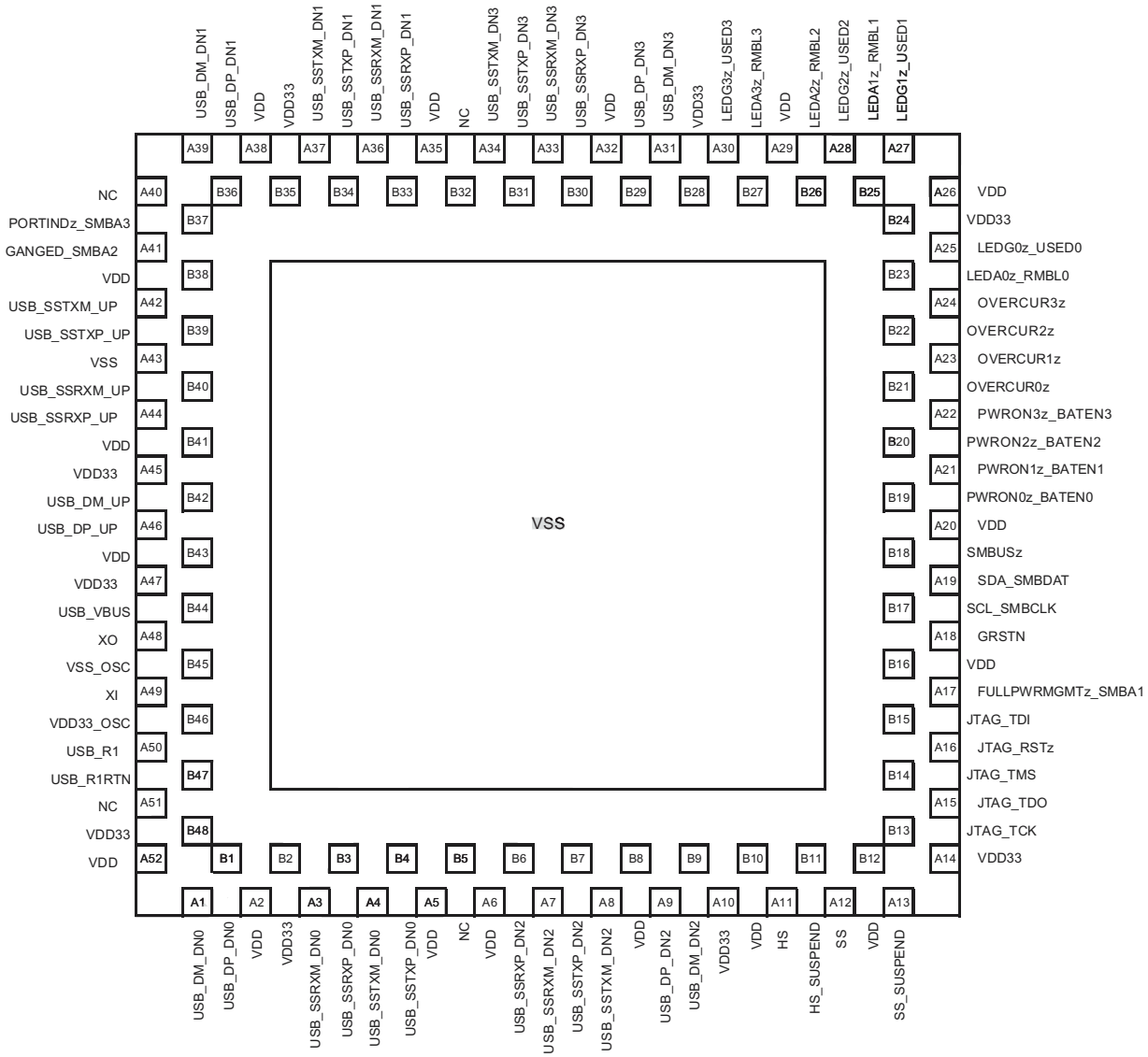
Changes from Revision B (September 2013) to Revision C **Page**

- Added *Terminal Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Updated GANGED_SMBA2 Signal description. 10
- Updated Downstream Port 1 Implementation section. 30
- Updated Downstream Port 2 Implementation section. 31
- Updated Downstream Port 3 Implementation section. 31
- Updated Downstream Port 4 Implementation section. 32

3 Pin Configuration and Functions

Pin Diagram

100-Pin TUSB8040A1
RKM Package
TUSB8040A1RKM (Top View)



3.1 Pin Descriptions

3.1.1 Signal Descriptions

Table 3-1. Signal Descriptions

TYPE	DESCRIPTION
I	Input
O	Output
I/O	Input/output
PD, PU	Internal pull-down/pull-up
PT	Passive pass through
P	Power Supply
G	Ground

3.1.2 Clock and Reset Signals

Table 3-2. Clock and Reset Signals

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
GRSTz	I, PU	A18	Global power reset. This reset brings all of the TUSB8040A1 internal registers to their default states. When GRSTz is asserted, the device is completely nonfunctional. GRSTz should be asserted a minimum of 3 ms after all power rails are valid at the device.
XI	I	A49	Crystal input. This pin is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
XO	O	A48	Crystal output. This pin is crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
VSSOSC	I	B45	Oscillator return. If using a crystal, the load capacitors should use this signal as the return path and it should not be connected to the PCB ground. If using an oscillator, this terminal should be connected to PCB Ground.

3.1.3 USB Upstream Signals

Table 3-3. USB Upstream Signals

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
USB_SSTXP_UP	O	B39	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_UP	O	A42	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_UP	I	A44	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_UP	I	B40	USB SuperSpeed receiver differential pair (negative)
USB_DP_UP	I/O	A46	USB high-speed differential transceiver (positive)
USB_DM_UP	I/O	B42	USB high-speed differential transceiver (negative)
USB_R1	PT	A50	Precision resistor reference. A 9.09-kΩ ±1% resistor should be connected between USB_R1 and USB_R1RTN.
USB_R1RTN	PT	B47	Precision resistor reference return
USB_VBUS	I	B44	USB Upstream port power monitor. The USB_VBUS input is a 1.2-V I/O cell and requires a voltage divider to prevent damage to the input. The signal USB_VBUS must be connected to VBUS through a 90.9-kΩ ±1% resistor, and to signal ground through a 10-kΩ ±1% resistor. This allows the input to detect VBUS present from a minimum of 4 V and sustain a maximum VBUS voltage up to 10 V (applied to the voltage divider).

3.1.4 USB Downstream Signals

Table 3-4. USB Downstream Signals

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
USB_SSTXP_DN0	O	B4	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN0	O	A4	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN0	I	B3	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN0	I	A3	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN0	I/O	B1	USB high-speed differential transceiver (positive)
USB_DM_DN0	I/O	A1	USB high-speed differential transceiver (negative)
PWRON0z_BATEN0	I/O, PD	B19	USB Port 0 Power On Control for Downstream Power/Battery Charging Enable. The pin is used for control of the downstream power switch; in addition, the value of the pin is sampled at the de-assertion of reset to determine the value of the battery charger support for the port as indicated in the Battery Charger Support register: 0 = Battery charging not supported 1 = Battery charging supported This pin provides the port power control for all downstream ports if GANGED_SMBA2 = 1. This pin also determines the battery charging support of all downstream ports if GANGED_SMBA2 = 1.
OVERCUR0z	I, PU	B21	USB Port 0 overcurrent detection. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred This pin should be pulled high using a 10-kΩ resistor if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power switch.
USB_SSTXP_DN1	O	B34	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN1	O	A37	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN1	I	B33	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN1	I	A36	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN1	I/O	B36	USB High-speed differential transceiver (positive)
USB_DM_DN1	I/O	A39	USB High-speed differential transceiver (negative)
PWRON1z_BATEN1	I/O, PD	A21	USB Port 1 Power On Control for Downstream Power/Battery Charging Enable. The terminal is used for control of the downstream power switch for Port 1. In addition, the value of the pin is sampled at the de-assertion of reset to determine the value of the battery charger support for Port 1 as indicated in the Battery Charger Support register: 0 = Battery Charging Not Supported 1 = Battery Charging Supported
OVERCUR1z	I, PU	A23	USB Downstream Port 1 Overcurrent Detection. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred This pin should be pulled high using a 10-kΩ resistor if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power management device.
USB_SSTXP_DN2	O	B7	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN2	O	A8	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN2	I	B6	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN2	I	A7	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN2	I/O	A9	USB High-speed differential transceiver (positive)
USB_DM_DN2	I/O	B9	USB High-speed differential transceiver (negative)

Table 3-4. USB Downstream Signals (continued)

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
PWRON2z_BATEN2	I/O, PD	B20	USB Port 2 Power On Control for Downstream Power/Battery Charging Enable. The pin is used for control of the downstream power switch for Port 2. In addition, the value of the pin is sampled at the de-assertion of reset to determine the value of the battery charger support for Port 2 as indicated in the Battery Charger Support register: 0 = Battery Charging Not Supported 1 = Battery Charging Supported
OVERCUR2z	I, PU	B22	USB Downstream Port 2 Overcurrent Detection. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred This pin should be pulled high using a 10-kΩ resistor if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power management device.
USB_SSTXP_DN3	O	B31	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN3	O	A34	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN3	I	B30	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN3	I	A33	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN3	I/O	B29	USB High-speed differential transceiver (positive)
USB_DM_DN3	I/O	A31	USB High-speed differential transceiver (negative)
PWRON3z_BATEN3	I/O, PD	A22	USB Port 3 Power On Control for Downstream Power/Battery Charging Enable. The pin is used for control of the downstream power switch for Port 3. In addition, the value of the pin is sampled at the de-assertion of reset to determine the value of the battery charger support for Port 3 as indicated in the Battery Charger Support register: 0 = Battery Charging Not Supported 1 = Battery Charging Supported
OVERCUR3z	I, PU	A24	USB Downstream Port 3 Overcurrent Detection. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred This pin should be pulled high using a 10K resistor if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power management device.
LEDA0z_RMBL0	I, PU	B23	USB Port 0 Amber LED Indicator & Device Removable Configuration Bit 1 = Device is Removable 0 = Device is NOT Removable
LEDA1z_RMBL1	I/O, PU	B25	USB Port 1 Amber LED Indicator & Device Removable Configuration Bit 1 = Device is Removable 0 = Device is NOT Removable
LEDA2z_RMBL2	I/O, PU	B26	USB Port 2 Amber LED Indicator & Device Removable Configuration Bit 1 = Device is Removable 0 = Device is NOT Removable
LEDA3z_RMBL3	I/O, PU	B27	USB Port 3 Amber LED Indicator & Device Removable Configuration Bit 1 = Device is Removable 0 = Device is NOT Removable
LEDG0z_USED0	I/O, PU	A25	USB Port 0 Green LED Indictor & Port Used Configuration Bit 1 = Port Used 0 = Port is NOT Used
LEDG1z_USED1	I/O, PU	A27	USB Port 1 Green LED Indictor & Port Used Configuration Bit 1 = Port Used 0 = Port is NOT Used

Table 3-4. USB Downstream Signals (continued)

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
LEDG2z_USED2	I/O, PU	A28	USB Port 2 Green LED Indictor & Port Used Configuration Bit 1 = Port Used 0 = Port is NOT Used
LEDG3z_USED3	I/O, PU	A30	USB Port 3 Green LED Indictor & Port Used Configuration Bit 1 = Port Used 0 = Port is NOT Used

3.1.5 I^2C/SMBUS Signals

Table 3-5. I^2C/SMBUS Signals

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
SCL/SMBCLK	I/O, PD	B17	I^2C clock/SMBus clock. Function of pin depends on the setting of the SMBUSz input. When SMBUSz = 1, this pin acts as the serial clock interface for an I^2C EEPROM. When SMBUSz = 0, this pin acts as the serial clock interface for an SMBus host. The SCL_SMBCLK pin is sampled at the deassertion of reset to determine if SuperSpeed USB low power states U1 and U2 are initiated. If SCL_SMBCLK is low, (default), U1 / U2 power states are enabled. If SCL_SMBCLK is high, entry to U1 / U2 power states is not initiated by the hub downstream ports, but is accepted. This input is over-ridden if SDA_SMBDAT is sampled as a '1'. If an EEPROM is installed, U1/U2 power state support is controlled by the Device Configuration Register. Can be left unconnected if external interface not implemented.
SDA/SMBDAT	I/O, PD	A19	I^2C data/SMBus data. Function of pin depends on the setting of the SMBUSz input. When SMBUSz = 1, this pin acts as the serial data interface for an I^2C EEPROM. When SMBUSz = 0, this pin acts as the serial data interface for an SMBus host. The SDA_SMBDAT pin is sampled at the deassertion of reset to determine if SuperSpeed USB low power states U1 and U2 are disabled. If SDA_SMBDAT is high, U1 and U2 low power states are disabled. If SDA_SMBDAT is low, U1 and U2 low power states are enabled. If the optional EEPROM or SMBUS is implemented, the value of the u1u2Disable bit of the Device Configuration Register determines if the low power states U1 and U2 are enabled. Can be left unconnected if external interface not implemented and U1 and U2 are to be enabled.
SMBUSz	I, PU	B18	I^2C/SMBus mode select. 1 = I^2C Mode Selected 0 = SMBus Mode Selected Can be left unconnected if external interface not implemented.

3.1.6 Test and Miscellaneous Signals

Table 3-6. Test and Miscellaneous Signals

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
JTAG_TCK	I/O, PD	B13	JTAG test clock. Can be left unconnected.
JTAG_TDI	I/O, PU	B15	JTAG test data in. Can be left unconnected.
JTAG_TDO	I/O, PD	A15	JTAG test data out. Can be left unconnected.
JTAG_TMS	I/O, PU	B14	JTAG test mode select. Can be left unconnected.
JTAG_RSTz	I/O, PD	A16	JTAG reset. Pull down using an external 1-kΩ resistor for normal operation.
HS_SUSPEND	I/O, PD	B11	High-speed suspend status output. 0 = High-speed upstream port not suspended 1= High-speed upstream port suspended The value of the pin is sampled at the deassertion of reset to determine the polarity of the PWRONxz_BATENx pins. If it is sampled as a '0' (default), the polarity is active low. If it is sampled as a '1', the polarity is active high. Can be left unconnected.
SS_SUSPEND	I/O, PD	A13	SuperSpeed USB suspend status output. 0 = SuperSpeed USB upstream port not suspended 1= SuperSpeed USB upstream port suspended The value of the pin is sampled at the deassertion of reset to determine if spread spectrum clocking is enabled or disabled. If it is sampled as a '0' (default), SSC is enabled. If it is sampled as a '1', SSC is disabled. Can be left unconnected.
HS	O, PU	A11	High-speed status. The pin is to indicate the connection status of the upstream port as documented below: 0 = Hub in low/full speed mode 1 = Hub in high-speed mode Can be left unconnected.
SS	O, PU	A12	SuperSpeed USB status. The pin is to indicate the connection status of the upstream port as documented below: 0 = Hub not in SuperSpeed USB mode 1 = Hub in SuperSpeed USB mode Can be left unconnected.
FULLPWRMGMTz_ SMBA1	I, PU	A17	Full power management enable/SMBus address bit 1. The value of the pin is sampled at the de-assertion of reset to set the power switch control follows: 0 = Full power management supported 1 = Full Power management not supported Full power management is the ability to control power to the downstream ports of the TUSB8040A1 using the PWRON0z_BATEN0 terminal. When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus slave address bit 1. SMBus slave address bits 2 and 3 are always 1 for the TUSB8040A1. When SMBus mode is enabled using SMBUSz, this pin sets the value of the SMBus slave address bit 1. Can be left unconnected if full power management and SMBus are not implemented.
GANGED_SMBA2	I, PU	A41	Ganged operation enable/SMBus Address bit 2. The value of the pin is sampled at the deassertion of reset to set the power switch and over current detection mode as follows: 0 = Power Gangs not supported 1 = Power Gangs supported When SMBus mode is enabled using SMBUSz, this pin sets the value of the SMBus slave address bit 2 .

Table 3-6. Test and Miscellaneous Signals (continued)

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
PORTINDz_SMBA3	I, PU	B37	Port Indicator LED Status/SMBus Address bit 3. The value of the pin is sampled at the deassertion of reset to determine the port indicator support for the hub as follows: 0 = Port Indicator LEDs are enabled 1 = Port Indicator LEDs are not enabled When SMBus mode is enabled using SMBUSz, this pin sets the value of the SMBus slave address bit 3.

3.1.7 Power Signals

Table 3-7. Power Signals

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
VDD33	P	B2, A10, A14, B24, B28, B35, A45, A47, B46, B48	3.3-V power rail
VDD	P	A2, A5, A6, B8, B10, B12, B16, A20, A26, A29, A32, A35, A38, B38, B41, B43, A52	1.1-V power rail
GND	G	A43, A53	Ground, Power Pad
GND_NC	G	C1, C2, C3, C4	The corner pins, which are for mechanical stability of the package, are connected to ground internally. These pins may be connected to GND or left unconnected.
NC	NC	A40, A51, B5, B32,	No connect

4 Specifications

4.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD33}	Steady-state supply voltage	–0.3	3.8	V
V_{DD11}		–0.3	1.4	
V_{IO}	USB 2.0 DP/DM	–0.3	VDD33 + 0.3 ≤ 3.	V
	SuperSpeed USB TXP/M and RXP/M	–0.3	VDD33 + 0.3 ≤ 3.8	
	XI/XO	–0.3	1.98	
	3.3-V Tolerant I/O	–0.3	VDD33 + 0.3 ≤ 3.8	
V_{USB_VBUS}		–0.3	1.2	V
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Section 4.3* is not implied. Expose to absolute-maximum-rated conditions for extended periods may affect device reliability

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD33}	Steady-state supply voltage	3	3.3	3.6	V
V_{DD11}(1)		0.99	1.1	1.26	
V_{IO}	USB 2.0 DP/DM	0		V_{DD33}	V
	SuperSpeed USB TXP/M and RXP/M	0		V_{DD33}	
	XI/XO	0		1.8	
	3.3-V Tolerant I/O	0		V_{DD33}	
V_{USB_VBUS}		0		1.155	V
T_A	Operating free-air temperature range	0	25	70	°C
T_J	Operating junction temperature range	0	25	105	°C

(1) A 1.05-V supply may be used as long as minimum supply conditions are met.

4.4 Thermal Information

THERMAL METRIC		TUSB8040A1 RKM 100 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(1)	25.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(2)	9.5	
θ_{JB}	Junction-to-board thermal resistance(3)	15.2	
ψ_{JT}	Junction-to-top characterization parameter(4)	0.1	
ψ_{JB}	Junction-to-board characterization parameter(5)	7.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(6)	0.4	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

4.5 3.3-V I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage(1)	VDD33		2	VDD33	V
V_{IL}	Low-level input voltage(1)	VDD33		0	0.8	V
			JTAG pins only	0	0.55	
V_I	Input voltage			0	VDD33	V
V_O	Output voltage(2)			0	VDD33	V
t_t	Input transition time (t_{rise} and t_{fall})			0	25	ns
V_{hys}	Input hysteresis(3)				0.13 x VDD33	V
V_{OH}	High-level output voltage	VDD33	I_{OH} = -4 mA	2.4		V
V_{OL}	Low-level output voltage	VDD33	I_{OL} = 4 mA		0.4	V
I_{OZ}	High-impedance, output current(2)	VDD33	V_I = 0 to VDD33		±20	µA
I_{OZP}	High-impedance, output current with internal pullup or pulldown resistor(4)	VDD33	V_I = 0 to VDD33		±225	µA
I_I	Input current(5)	VDD33	V_I = 0 to VDD33		±15	µA

(1) Applies to external inputs and bidirectional buffers.
(2) Applies to external outputs and bidirectional buffers.
(3) Applies to GRSTz.
(4) Applies to pins with internal pullups/pulldowns.
(5) Applies to external input buffers.

4.6 Hub Input Supply Current

Typical values measured at T_A = 25°C

PARAMETER	VDD33	VDD	UNIT
	3.3 V	1.1 V	
LOW POWER MODES			
Power On (after Reset)	4	68	mA
Upstream Disconnect	4	68	mA
Suspend	4	68	mA
ACTIVE MODES (US state / DS State)			
3.0 host / 1 SS Device and Hub in U1	46	260	mA
3.0 host / 1 SS Device and Hub in U0	46	400	mA
3.0 host / 2 SS Devices and Hub in U1	46	330	mA
3.0 host / 2 SS Devices and Hub in U0	46	540	mA
3.0 host / 3 SS Devices and Hub in U1	46	420	mA
3.0 host / 3 SS Devices and Hub in U0	46	650	mA
3.0 host / 4 SS Devices and Hub in U1	46	560	mA
3.0 host / 4 SS Devices and Hub in U0	46	770	mA
3.0 host / 1 SS and 1 HS Devices in U0 and active	90	430	mA
3.0 host / 2 SS and 2 HS Devices in U0 and active	105	570	mA
2.0 host / HS Device active	46	90	mA
2.0 host / 4 HS Device active	90	115	mA

4.7 Timing and Switching Characteristics

4.7.1 Clock Generation

The TUSB8040A1 accepts a crystal input to drive an internal oscillator or an external clock source. If a clock is provided to XI instead of a crystal, XO is left open and VSSOSC should be connected to the PCB ground plane. Otherwise, if a crystal is used, the connection needs to follow the guidelines below. Since XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. It is also recommended to minimize the capacitance between XI and XO. This can be accomplished by connecting the VSSOSC lead to the two external capacitors CL1 and CL2 and shielding them with the clean ground lines. The VSSOSC should not be connected to PCB ground when using a crystal.

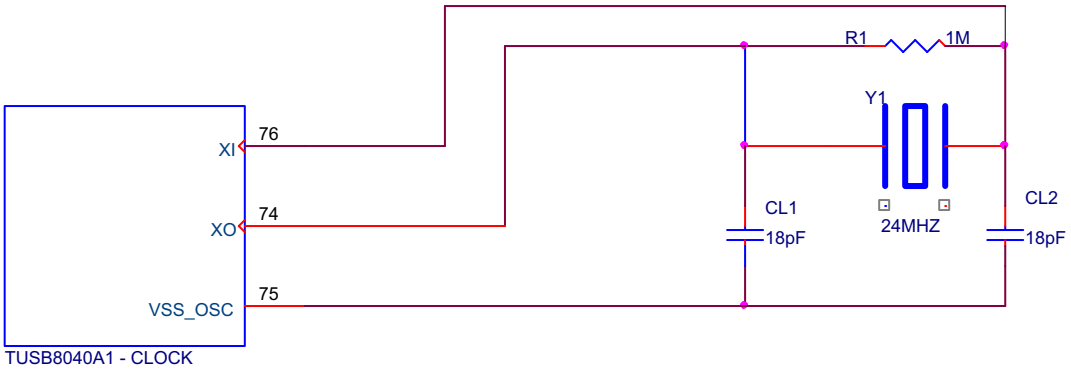


Figure 4-1. TUSB8040A1 Clock

4.7.2 Crystal Requirements

The crystal must be fundamental mode with load capacitance of 12 pF to 24 pF and frequency stability rating of ±100 PPM or better. To ensure proper startup oscillation condition, a maximum crystal equivalent series resistance (ESR) of 50 Ω is recommended. A parallel, 18-pF load capacitor should be used if a crystal source is used. VSSOSC should not be connected to the PCB ground plane.

4.7.3 Input Clock Requirements

When using an external clock source such as an oscillator, the reference clock should have a ±100 PPM or better frequency stability and have less than 50-ps absolute peak to peak jitter or less than 25-ps peak to peak jitter after applying the USB 3.0 jitter transfer function. XI should be tied to the 1.8-V clock source and XO should be left floating. VSSOSC should be connected to the PCB ground plane.

5 Detailed Description

5.1 Overview

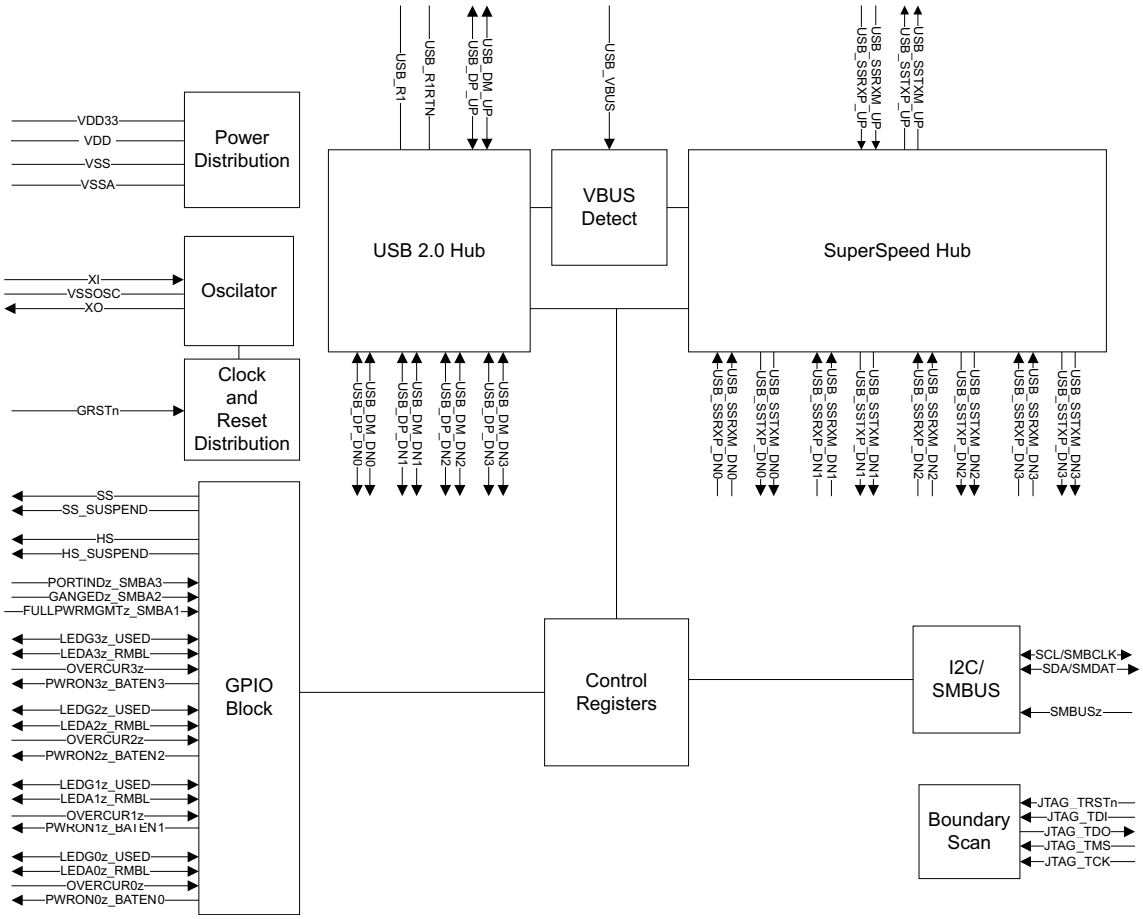
The TUSB8040A1 supports per port or ganged power switching and over-current protection.

An individually port power controlled hub switches power on or off to each downstream port as requested by the USB host. Also when an individually port power controlled hub senses an over-current event, only power to the affected downstream port will be switched off.

A ganged hub switches on power to all its downstream ports when power is required to be on for any port. The power to the downstream ports is not switched off unless all ports are in a state that allows power to be removed. Also when a ganged hub senses an over-current event, power to all downstream ports will be switched off.

The TUSB8040A1 also provides customization using an I^2C EEPROM or configuration via an SMBus host for vendor specific PID, VID, and strings. For the TUSB8040A1 ports can also be marked as disabled or permanently attached using pin selection, I^2C EEPROM or an SMBus host. The Device Status and Command Register at F8h cannot be modified by the contents of the I^2C EEPROM.

5.2 Functional Block Diagram



5.3 Memory

Table 5-1. TUSB8040A1 Register Map

BYTE ADDRESS	CONTENTS
00h	ROM Signature (55h)
01h	Vendor ID LSB
02h	Vendor ID MSB
03h	Product ID LSB
04h	Product ID MSB
05h	Device Configuration Register
06h	Battery Charging Support Register
07h	Device Removable Configuration Register
08h	Port Used Configuration Register
09h-0Fh	Reserved
10h-1Fh	Reserved
20h-21h	LangID Byte [1:0]
22h	Serial Number String Length
23h	Manufacturer String Length
24h	Product String Length
25h-2Fh	Reserved
30h-4Fh	Serial Number String Byte [31:0]
50h-8Fh	Manufacturer String Byte [63:0]
90h-CFh	Product String Byte [63:0]
D0-F7h	Reserved
F8h	Device Status and Command Register
F9-FFh	Reserved

5.4 I^2C EEPROM Operation

The TUSB8040A1 supports a single-master, standard mode (100 kbit/s) connection to a dedicated I^2C EEPROM when the I^2C interface mode is enabled. In I^2C mode, the TUSB8040A1 reads the contents of the EEPROM at bus address 1010000b using 7-bit addressing starting at address 0. If the value of the EEPROM contents at byte 00h equals 55h, the TUSB8040A1 loads the configuration registers according to the EEPROM map. If the first byte is not 55h, the TUSB8040A1 exits the I^2C mode and continues execution with the default values in the configuration registers. The hub will not connect on the upstream port until the configuration is completed.

Note, some bytes located below offset 9h are optional. Please refer to the detailed register descritpions for any requirements on EEPROM configuration of registers.

For details on I^2C operation refer to the UM10204 I^2C-bus Specification and User Manual.

5.5 SMBus Slave Operation

When the SMBus interface mode is enabled, the TUSB8040A1 supports read block and write block protocols as a slave-only SMBus device.

The TUSB8040A1RKM slave address is 1000 pgxy, where:

- p is the state of PORTINDz_SMBA3 at reset,
- g is the state of GANGED_SMBA2 at reset,
- x is the state of FULLPWRMGMTz_SMBA1 at reset, and
- y indicates read (logic 1) or write (logic 0) access.

If the TUSB8040A1 is addressed by a host using an unsupported protocol it will not respond. The TUSB8040A1 will wait indefinitely for configuration by the SMBus host and will not connect on the upstream port until the SMBus host indicates configuration is complete by clearing the CFG_ACTIVE bit.

For details on SMBus requirements refer to the System Management Bus Specification.

5.6 Configuration Registers

The internal configuration registers are accessed on byte boundaries. The configuration register values are loaded with defaults but can be over-written when the TUSB8040A1 is in I^2C or SMBus mode.

5.6.1 ROM Signature Register

Figure 5-1. Register Offset 0h

7	6	5	4	3	2	1	0
romSignature							
RW-0							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-2. Bit Descriptions – ROM Signature Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	romSignature	RW	ROM Signature Register. This register is used by the TUSB8040A1 in I^2C mode to validate the attached EEPROM has been programmed. The first byte of the EEPROM is compared to the mask 55h and if not a match, the TUSB8040A1 aborts the EEPROM load and executes with the register defaults.

5.6.2 Vendor ID LSB Register

Figure 5-2. Register Offset 1h

7	6	5	4	3	2	1	0
vendorIdLsb							
RW-0	RW-1	RW-0	RW-1		RW-0		RW-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-3. Bit Descriptions – Vendor ID LSB Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	vendorIdLsb	RW	Vendor ID LSB. Least significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 51h representing the LSB of the TI Vendor ID 0451h. The value may be over-written to indicate a customer Vendor ID.

5.6.3 Vendor ID MSB Register

Figure 5-3. Register Offset 2h

7	6	5	4	3	2	1	0
vendorIdMsb							
RW-0							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-4. Bit Descriptions – Vendor ID MSB Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	vendorIdMsb	RW	Vendor ID MSB. Most significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 04h representing the MSB of the TI Vendor ID 0451h. The value may be over-written to indicate a customer Vendor ID.

5.6.4 Product ID LSB Register

Figure 5-4. Register Offset 3h

7	6	5	4	3	2	1	0
productIdLsb							
RW-0	RW-1		RW-0			RW-1	RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-5. Bit Descriptions – Product ID LSB Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	productIdLsb	RW	Product ID LSB. Least significant byte of the product ID assigned by Texas Instruments; the default value of this register is 46h representing the LSB of the product ID assigned by Texas Instruments. The value of this register will be reported as configured for the SuperSpeed USB Device descriptor. The USB 2.0 Device descriptor will report the value in this register with bit [1] toggled. This ensures that the USB drivers load properly for both hubs. The value may be over-written to indicate a customer product ID.

5.6.5 Product ID MSB Register

Figure 5-5. Register Offset 4h

7	6	5	4	3	2	1	0
productIdMsb							
RW-1				RW-0			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-6. Bit Descriptions – Product ID MSB Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	productIdMsb	RW	Product ID MSB. Most significant byte of the product ID assigned by Texas Instruments; the default value of this register is 80h representing the MSB of the product ID assigned by Texas Instruments. The value may be over-written to indicate a customer product ID.

5.6.6 Device Configuration Register

Figure 5-6. Register Offset 5h

7	6	5	4	3	2	1	0
customStrings	customSernum	u1u2Disable	portIndz	ganged	fullPwrMgmtz	u1u2TimerOvr	RSVD
RW-0				RW-X			RO-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-7. Bit Descriptions – Device Configuration Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	customStrings	RW	Custom Strings Enable. When this bit is set and the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads the string registers from the contents of the EEPROM. When set and the TUSB8040A1 is in SMBUS mode, the string registers may written by an SMBus host. This bit defaults to 0.
6	customSernum	RW	Custom Serial Number Enable. When this bit is set and the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads the serial number register from the contents of the EEPROM. When set and the TUSB8040A1 is in SMBUS mode, the Serial Number registers may written by an SMBus host. This bit defaults to 0.
5	u1u2Disable	RW	U1 U2 Disable. When this bit is set the TUSB8040A1 will not initiate or accept any U1 or U2 requests on any port, upstream or downstream, unless it receives or sends a Force_LinkPM_Accept LMP. After receiving or sending an FLPMA LMP, it will continue to enable U1 and U2 according to USB 3.0 protocol until it gets a power-on reset or is disconnected on its upstream port. This bit is loaded at the de-assertion of reset with the value of the SDA_SMBDAT terminal. When the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads this bit from the contents of the EEPROM. When the TUSB8040A1 is in SMBUS mode, the value may be over-written by an SMBus host.
4	portIndz	RW	Port Indicator Status. This bit shall be loaded at the de-assertion of reset with the value of PORTINDz_SMBA3 terminal. When the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads this bit from the contents of the EEPROM. When the TUSB8040A1 is in SMBUS mode, the value may be overwritten by an SMBus host.
3	ganged	RW	Ganged. This bit shall be loaded at the de-assertion of reset with the value of GANGEd_SMBA2 terminal. When the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads this bit from the contents of the EEPROM. When the TUSB8040A1 is in SMBUS mode, the value may be overwritten by an SMBus host.
2	fullPwrMgmtz	RW	Full Power Management. This bit is loaded at the de-assertion of reset with the value of the FULLPWRMGMTz_SMBA1 terminal. When this bit is 0, power switching and over-current detection is supported whether bus- or self-powered. When the bit is 1 and the device is bus powered, power switching is supported but over-current detection is not supported. When the bit is 1 and the device is self-powered over-current detection is supported but power switching is not supported. When the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads this bit from the contents of the EEPROM. When the TUSB8040A1 is in SMBUS mode, the value may be over-written by an SMBus host.
1	u1u2TimerOvr	RW	U1 U2 Timer Override. When this bit is set the TUSB8040A1 will override the downstream ports u1/u2 timeout values set by software. If software sets a value in the range of 1-FF, the TUSB8040A1 will use the value FF. If software sets a value of 0, the TUSB8040A1 will use the value 0.This bit is loaded at the de-assertion of reset with the value of the SCL_SMBCLK terminal. When the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads this bit from the contents of the EEPROM. When the TUSB8040A1 is in SMBUS mode, the value may be over-written by an SMBus host.
0	RSVD	RO	Reserved. Read only, returns 0 when read.

5.6.7 Battery Charging Support Register

Figure 5-7. Register Offset 6h

7	6	5	4	3	2	1	0
RSVD				batEn[3:0]			
RO-0				RW-X			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-8. Bit Descriptions – Battery Charging Support Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	RSVD	RO	Reserved. Read only, returns 0 when read.
3:0	batEn[3:0]	RW	Battery Charger Support. The bits in this field indicate whether the downstream port implements the charging port features. A value of 0 indicates the port does not implement the charging port features. A value of 1 indicates the port does support the charging port features. Each bit corresponds directly to a downstream port, i.e. batEn0 corresponds to downstream port 0. When in I^2C/SMBus mode the bits in this field corresponding to the enabled ports per used[3:0] may be over-written by EEPROM contents or by an SMBus host. The default value for these bits are loaded at the de-assertion of reset with the value of the PWRON[3:0]z_BATEN[3:0] as follows: bateEn[3:0] defaults to wxyzb, where w is PWRON3z_BATEN3, x is PWRON2z_BATEN2, y is PWRON1z_BATEN1 and z is PWRON0z_BATEN0.

5.6.8 Device Removable Configuration Register

Figure 5-8. Register Offset 7h

7	6	5	4	3	2	1	0
RSVD				rmbl[3:0]			
RO-0				RW-X			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-9. Bit Descriptions – Device Removable Configuration Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	RSVD	RO	Reserved. Read only, returns 0 when read.
3:0	rmbl[3:0]	RW	Removable. The bits in this field indicate whether a device attached to downstream ports 3 through 0 are removable or permanently attached. A value of 0 indicates the device attached to the port is not removable. A value of 1 indicates the device attached to the port is removable. The default value for these bits are loaded at the de-assertion of reset with the value of LEDA[3:0]z_RMBL[3:0] as follows: rmbl[3:0] defaults to wxyzb, where w is LEDA3z_RMBL3, x is LEDA2z_RMBL2, y is LEDA1z_RMBL1 and z is LEDA0z_RMBL0.

5.6.9 Port Used Configuration Register

Figure 5-9. Register Offset 8h

7	6	5	4	3	2	1	0
RSVD				used[3:0]			
RO-0				RW-X			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-10. Bit Descriptions – Port Used Configuration Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	RSVD	RO	Reserved. Read only, returns 0 when read.
3:0	used[3:0]	RW	Used. The bits in this field indicate whether downstream ports 3 through 0 are enabled or disabled for use. A value of 0 indicates the port is not used. A value of 1 indicates the port is used. The default value for these bits are loaded at the de-assertion of reset with the value of LEDG[3:0]z_USED[3:0] as follows: used[3:0] defaults to wxyzb, where w is LEDG3z_USED3, x is LEDG2z_USED2, y is LEDG1z_USED1 and z is LEDG0z_USED0.

5.6.10 Reserved Register

Figure 5-10. Register Offset 9h

7	6	5	4	3	2	1	0
RSVD							
RW-0				RO-0			RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-11. Bit Descriptions – Reserved Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:6	RSVD	RW	Reserved. When the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads these bits from the contents of the EEPROM. When the TUSB8040A1 is in SMBUS mode, the values may be over-written by an SMBus host. These bits shall be programmed to 0 for normal operation.
5:2	RSVD	RO	Reserved. Read only, returns 0 when read.
1:0	RSVD	RW	Reserved. When the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads these bits from the contents of the EEPROM. When the TUSB8040A1 is in SMBUS mode, the values may be over-written by an SMBus host. These bits shall be programmed to 0 for normal operation.

5.6.11 Reserved Register

Figure 5-11. Register Offset Ah

7	6	5	4	3	2	1	0
RSVD							
RO-0				RW-0		RW-1	RO-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-12. Bit Descriptions – Reserved Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:5	RSVD	RO	Reserved. Read only, returns 0 when read.
4:2	RSVD	RW	Reserved. When the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads these bits from the contents of the EEPROM. When the TUSB8040A1 is in SMBUS mode, the values may be over-written by an SMBus host. These bits shall be programmed to 0 for normal operation.
1	RSVD	RW	Reserved. When the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads these bits from the contents of the EEPROM. When the TUSB8040A1 is in SMBUS mode, the values may be over-written by an SMBus host. This bit shall be programmed to 1 for normal operation.
0	RSVD	RO	Reserved. Read only, returns 0 when read.

5.6.12 Language ID LSB Register

Figure 5-12. Register Offset 20h

7	6	5	4	3	2	1	0
langIdLsb							
RW-0				RW-1		RW-0	RW-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-13. Bit Descriptions – Language ID LSB Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	langIdLsb	RW	Language ID least significant byte. This register contains the value returned in the LSB of the LANGID code in string index 0. The TUSB8040A1 only supports one language ID. The default value of this register is 09h representing the LSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host.

5.6.13 Language ID MSB Register

Figure 5-13. Register Offset 21h

7	6	5	4	3	2	1	0
langIdMsb							
RW-0					RW-1		RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-14. Bit Descriptions – Language ID MSB Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	langIdMsb	RW	Language ID most significant byte. This register contains the value returned in the MSB of the LANGID code in string index 0. The TUSB8040A1 only supports one language ID. The default value of this register is 04h representing the MSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host.

5.6.14 Serial Number String Length Register

Figure 5-14. Register Offset 22h

7	6	5	4	3	2	1	0
RSVD		serNumStringLen					
RO-0		RW-0	RW-1	RW-0	RW-1	RW-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-15. Bit Descriptions – Serial Number String Length Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:6	RSVD	RO	Reserved. Read only, returns 0 when read.
5:0	serNumStringLen	RW	Serial number string length. The string length in bytes for the serial number string. The default value is 14h, indicating that a 20-byte serial number string is supported. The maximum string length is 32 bytes. This field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a serial number string of serNumbStringLen bytes is returned at string index 1 from the data contained in the Serial Number String registers.

5.6.15 Manufacturer String Length Register

Figure 5-15. Register Offset 23h

7	6	5	4	3	2	1	0
RSVD		mfgStringLen					
RO-0		RW-0	RW-1	RW-0	RW-1	RW-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-16. Bit Descriptions – Manufacturer String Length Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	RSVD	RO	Reserved. Read only, returns 0 when read.
6:0	mfgStringLen	RW	Manufacturer string length. The string length in bytes for the manufacturer string. The default value is 0, indicating that a manufacturer string is not provided. The maximum string length is 64 bytes. When the field is non-zero, a manufacturer string of mfgStringLen bytes is returned at string index 3 from the data contained in the Manufacturer String registers.

5.6.16 Product String Length Register

Figure 5-16. Register Offset 24h

7	6	5	4	3	2	1	0
RSVD		prodStringLen					
RO-0		RW-0					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-17. Bit Descriptions – Product String Length Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	RSVD	RO	Reserved. Read only, returns 0 when read.
6:0	prodStringLen	RW	Product string length. The string length in bytes for the product string. The default value is 0, indicating that a product string is not provided. The maximum string length is 64 bytes. When the field is non-zero, a product string of prodStringLen bytes is returned at string index 2 from the data contained in the Product String registers.

5.6.17 Reserved Register

Figure 5-17. Register Offset 2Fh

7	6	5	4	3	2	1	0
RSVD							
RO-0							RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-18. Bit Descriptions – Reserved Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1	RSVD	RO	Reserved. Read only, returns 0 when read.
0	RSVD	RW	Reserved. When the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads this bit from the contents of the EEPROM. When the TUSB8040A1 is in SMBUS mode, the values may be over-written by an SMBus host. This bit shall be programmed to 0 for normal operation.

5.6.18 Serial Number Registers

Figure 5-18. Register Offset 30h-4Fh

7	6	5	4	3	2	1	0
serialNumber[n]							
RW-X							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-19. Bit Descriptions – Serial Number Registers

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	serialNumber[n]	RW	Serial Number byte N. The serial number returned in the Serial Number string descriptor at string index 1. The default value of these registers is calculated from the Die ID fields in the fuseRom. When customSernum is 1, these registers may be over-written by EEPROM contents or by an SMBus host. The serial number will be returned in USB 2.0 descriptor of the TUSB8040A1.

5.6.19 Manufacturer String Registers

Figure 5-19. Register Offset 50h-8Fh

7	6	5	4	3	2	1	0
mfgStringByte[n]							
RW-0							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-20. Bit Descriptions – Manufacturer String Registers

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	mfgStringByte[n]	RW	Manufacturer string byte N. These registers provide the string values returned for string index 3 when mfgStringLen is greater than 0. The number of bytes returned in the string is equal to mfgStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

5.6.20 Product String Registers

Figure 5-20. Register Offset 90h-CFh

7	6	5	4	3	2	1	0
prodStringByte[n]							
RW-0							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-21. Bit Descriptions – Product String Registers

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	prodStringByte[n]	RW	Product string byte N. These registers provide the string values returned for string index 2 when prodStringLen is greater than 0. The number of bytes returned in the string is equal to prodStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

5.6.21 Additional Feature Configuration Register

Figure 5-21. Register Offset F0h

7	6	5	4	3	2	1	0
RSVD							usb3spreadDis
RO-0							RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-22. Bit Descriptions –Additional Feature Configuration Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1	RSVD	RO	Reserved. Read only, returns 0 when read.
0	usb3spreadDis	RW	USB 3.0 Spread Spectrum Clocking Disable. When this bit is set USB 3.0 spread spectrum clocking is disabled. This bit is loaded at the de-assertion of reset with the value of the SS_SUSPEND pin. When the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads this bit from the contents of the EEPROM. When the TUSB8040A1 is in SMBUS mode, the value may be over-written by an SMBus host. This bit shall be programmed to 0 for normal operation.

5.6.22 Reserved Register

Figure 5-22. Register Offset F1h

7	6	5	4	3	2	1	0
RSVD							
RW-0				RO-0			RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-23. Bit Descriptions – Reserved Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:6	RSVD	RW	Reserved. When the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads these bits from the contents of the EEPROM. When the TUSB8040A1 is in SMBUS mode, the values may be over-written by an SMBus host.
5:1	RSVD	RO	Reserved. Read only, returns 0 when read.
0	RSVD	RW	Reserved. When the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads this bit from the contents of the EEPROM. When the TUSB8040A1 is in SMBUS mode, the values may be over-written by an SMBus host. This bit shall be programmed to 0 for normal operation.

5.6.23 Reserved Register

Figure 5-23. Register Offset F2h

7	6	5	4	3	2	1	0
RSVD							
RO-0							RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-24. Bit Descriptions – Reserved Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1	RSVD	RO	Reserved. Read only, returns 0 when read.
0	RSVD	RW	Reserved. When the TUSB8040A1 is in I^2C mode, the TUSB8040A1 loads this bit from the contents of the EEPROM. When the TUSB8040A1 is in SMBUS mode, the values may be over-written by an SMBus host. This bit shall be programmed to 0 for normal operation.

5.6.24 Device Status and Command Register

Figure 5-24. Register Offset F8h

7	6	5	4	3	2	1	0
RSVD						smbusRst	cfgActive
RO-0						RSU-0	RCU-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-25. Bit Descriptions – Device Status and Command Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:2	RSVD	RO	Reserved. Read only, returns 0 when read.
1	smbusRst	RSU	SMBus interface reset. This bit resets the SMBus slave interface to its default state and loads the registers back to their GRSTz values. This bit is set by writing a 1 and is cleared by hardware on completion of the reset. A write of 0 has no effect. (Not used with I^2C)
0	cfgActive	RCU	Configuration active. This bit indicates that configuration of the TUSB8040A1 is currently active. The bit is set by hardware when the device enters the I^2C or SMBus mode. The TUSB8040A1 does not connect on the upstream port while this bit is 1.When in I^2C mode, the bit is cleared by hardware when the TUSB8040A1 exits the I^2C mode. When in the SMBus mode, this bit must be cleared by the SMBus host in order to exit the configuration mode and allow the upstream port to connect. The bit is cleared by a writing 1. A write of 0 has no effect.

6 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The TUSB8040A1 is a four-port USB 3.0 compliant hub that provides simultaneous SuperSpeed USB and highspeed/full-speed connections on the upstream port, and SuperSpeed USB, high-speed, full-speed, or low speed connections on the downstream port. The TUSB8040A1 can be used in any application that needs additional USB compliant ports. For example, a specific notebook may only have two downstream USB ports, thus by using the TUSB8040A1, the notebook can increase the downstream port count to five.

6.2 Typical Application

A common application for the TUSB8040A1 is as a self-powered, standalone USB hub product. The product is powered by an external 5 V DC power adapter. In this application, a USB cable plugs the TUSB8040A1 upstream port into a USB host controller. The downstream ports of the TUSB8040A1 are exposed to users for connecting USB hard drives, cameras, flash drives, or any USB compliant device.

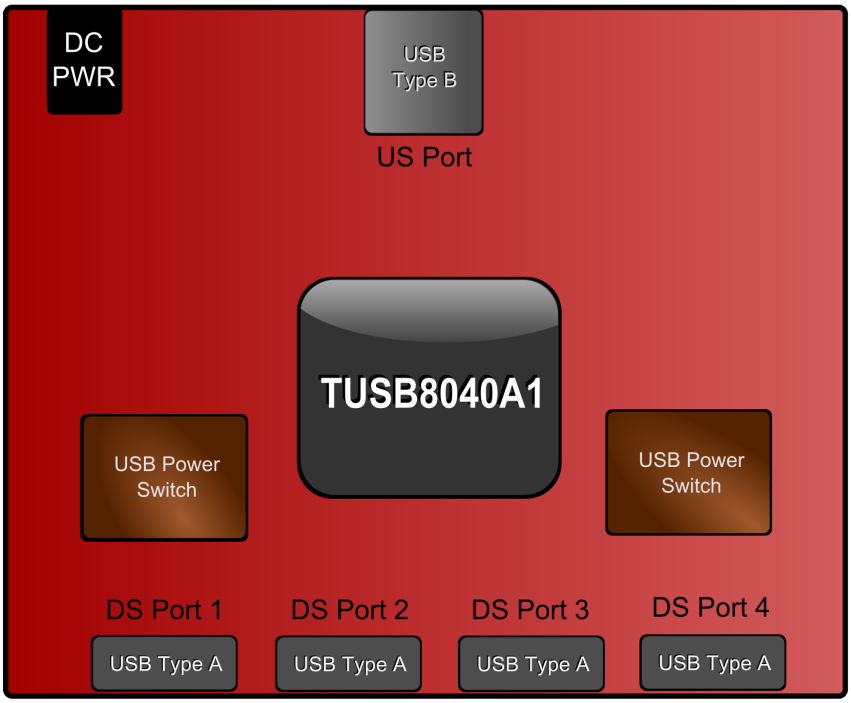


Figure 6-1. Discrete USB Hub Product

6.2.1 Design Requirements

Table 6-1. Design Parameters

Design Parameter	Value
VDD Supply	1.1 V
VDD33 Supply	2.2 V
Upstream Port USB Support (SS, HS, FS)	SS, HS, FS
Downstream Port 0 USB Support (SS, HS, FS, LS)	SS, HS, FS, LS
Downstream Port 1USB Support (SS, HS, FS, LS)	SS, HS, FS, LS
Downstream Port 2 USB Support (SS, HS, FS, LS)	SS, HS, FS, LS
Downstream Port 3 USB Support (SS, HS, FS, LS)	SS, HS, FS, LS
Number of Removable Downstream Ports	4
Number of Non-Removable Downstream Ports	0
Full Power Management of Downstream Ports	Yes (FULLPWRMGMT = 0)
Individual Control of Downstream Port Power Switch	Yes (GANGED = 0)
Power Switch Enable Polarity	Active Low (HS_SUSPEND = 0)
Battery Charge Support for Downstream Port 1	Yes
Battery Charge Support for Downstream Port 2	Yes
Battery Charge Support for Downstream Port 3	Yes
Battery Charge Support for Downstream Port 4	Yes
Downstream Port 1 Is Device Removable	Yes
Downstream Port 2 Is Device Removable	Yes
Downstream Port 3 Is Device Removable	Yes
Downstream Port 4 Is Device Removable	Yes
Downstream Port 1 Used (Enabled)	Yes
Downstream Port 2 Used (Enabled)	Yes
Downstream Port 3 Used (Enabled)	Yes
Downstream Port 4 Used (Enabled)	Yes
I2C EEPROM Support	No
24MHz Clock Source	Crystal

6.2.2 Detailed Design Procedure

6.2.2.1 Upstream Port Implementation

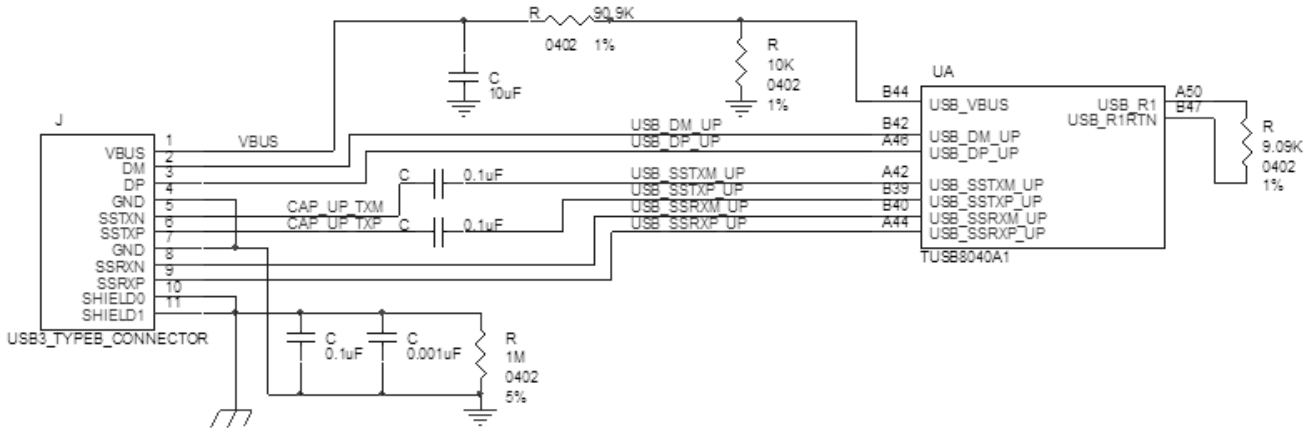


Figure 6-2. Upstream Port Implementation

The upstream port of the TUSB8040A1 is connected to a USB3 Type B connector. The VBUS signal from the USB3 Type B connector is fed through a voltage divider. The purpose of the voltage divider is to ensure the level meets USB_VBUS input requirements. Additionally, a 9.09KΩ+/-1% precision resistor reference return must be connected between terminals USB_R1 and USB_R1RTN.

6.2.2.2 Downstream Port 1 Implementation

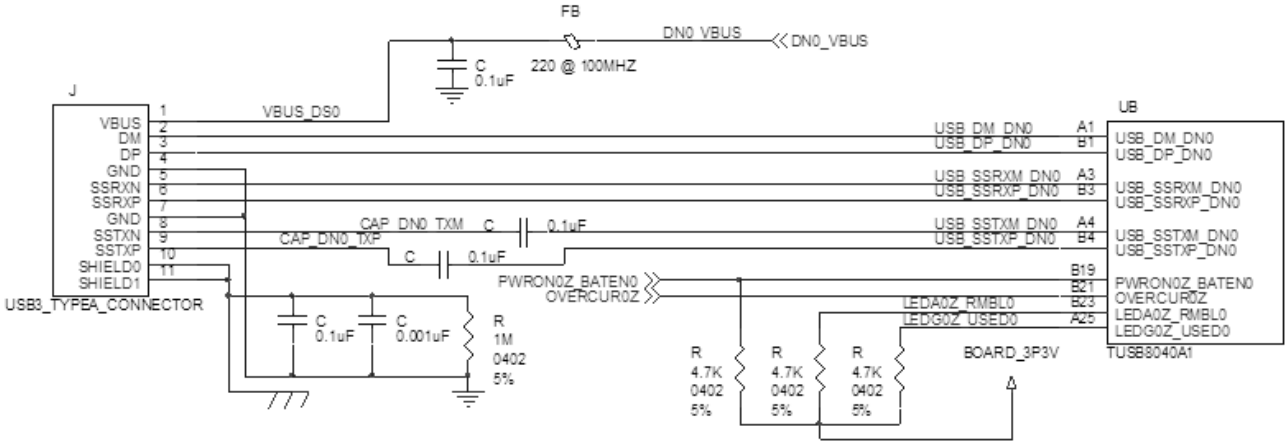


Figure 6-3. Downstream Port 1 Implementation

The downstream port 1 of the TUSB8040A1 is connected to a USB3 Type A connector. With PWRON0z_BATEN0 pin pulled-up, battery charge support is enabled for the port. If battery charge support is not needed, the internal pull-down resistor will disable it by default. Also, the internal pull-up resistors on the LEDG0z_USED0 and LEDA0z_RMBL0 pins mark the port as functional and device removable (for the opposite, external pull-downs are required).

6.2.2.3 Downstream Port 2 Implementation

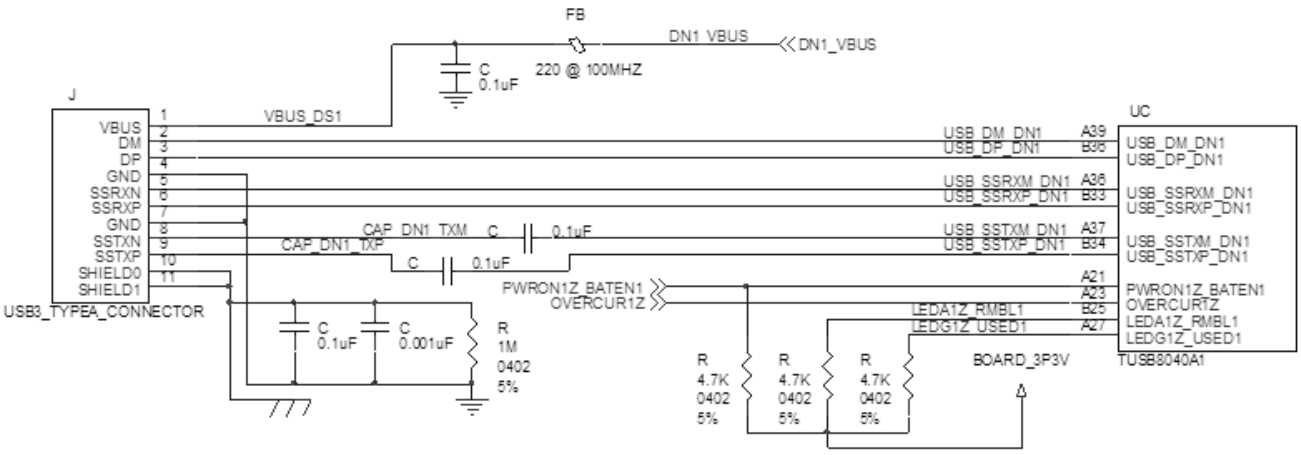


Figure 6-4. Downstream Port 2 Implementation

The downstream port 2 of the TUSB8040A1 is connected to a USB3 Type A connector. With PWRON1z_BATEN1 pin pulled-up, battery charge support is enabled for the port. If battery charge support is not needed, the internal pull-down resistor will disable it by default. Also, the internal pull-up resistors on the LEDG1z_USED1 and LEDA1z_RMBL1 pins mark the port as functional and device removable (for the opposite, external pull-downs are required).

6.2.2.4 Downstream Port 3 Implementation

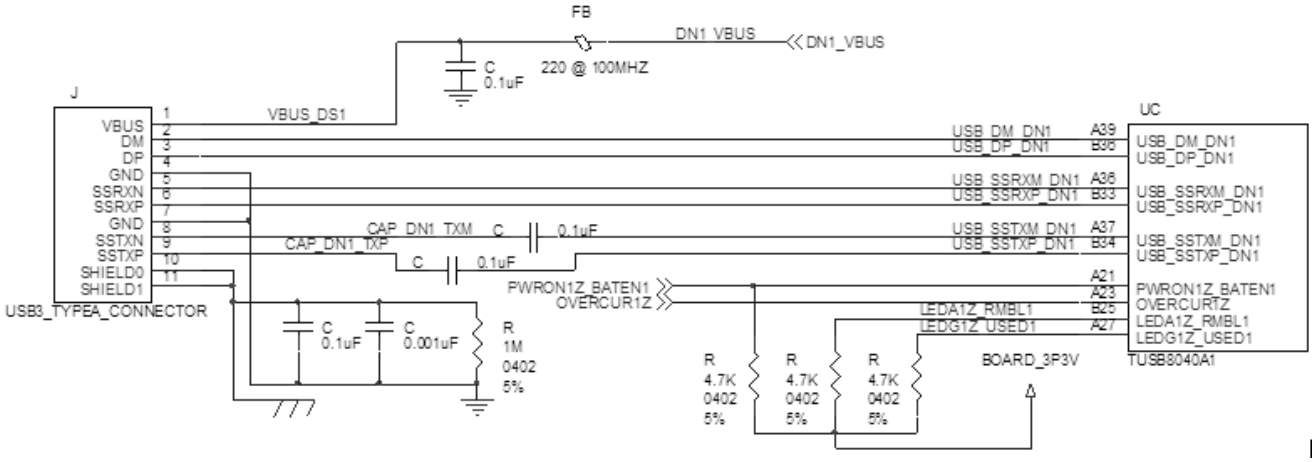


Figure 6-5. Downstream Port 3 Implementation

The downstream port 3 of the TUSB8040A1 is connected to a USB3 Type A connector. With PWRON2z_BATEN2 pin pulled-up, battery charge support is enabled for the port. If battery charge support is not needed, the internal pull-down resistor will disable it by default. Also, the internal pull-up resistors on the LEDG2z_USED2 and LEDA2z_RMBL2 pins mark the port as functional and device removable (for the opposite, external pull-downs are required).

6.2.2.5 Downstream Port 4 Implementation

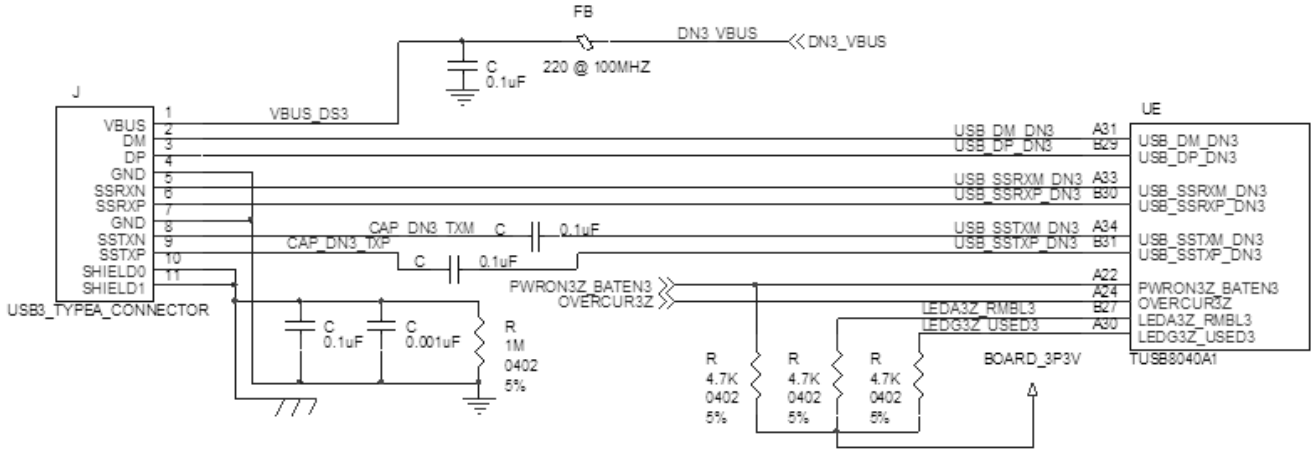


Figure 6-6. Downstream Port 4 Implementation

The downstream port 4 of the TUSB8040A1 is connected to a USB3 Type A connector. With PWRON3z_BATEN3 pin pulled-up, battery charge support is enabled for the port. If battery charge support is not needed, the internal pull-down resistor will disable it by default. Also, the internal pull-up resistors on the LEDG3z_USED3 and LEDA3z_RMBL3 pins mark the port as functional and device removable (for the opposite, external pull-downs are required).

6.2.2.6 VBUS Power Switch Implementation

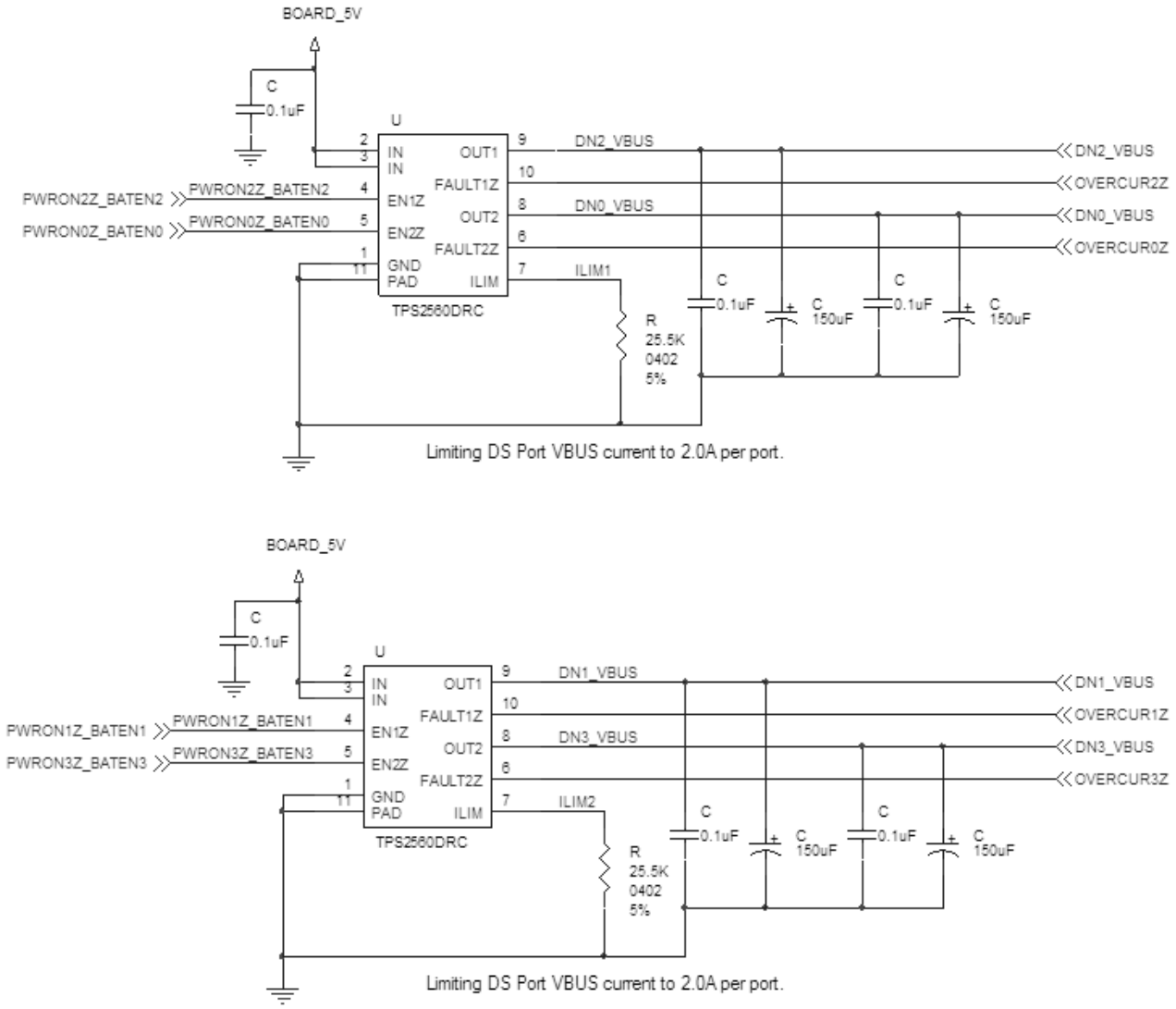


Figure 6-7. VBUS Power Switch Implementation

This implementation uses the Texas Instruments TPS2560 Dual Channel Precision Adjustable Current-Limited power switch. For details on this power switch or other power switches available from Texas Instruments, refer to the Texas Instruments website.

6.2.2.7 Clock, Reset, I²C/SMBUS, and Misc

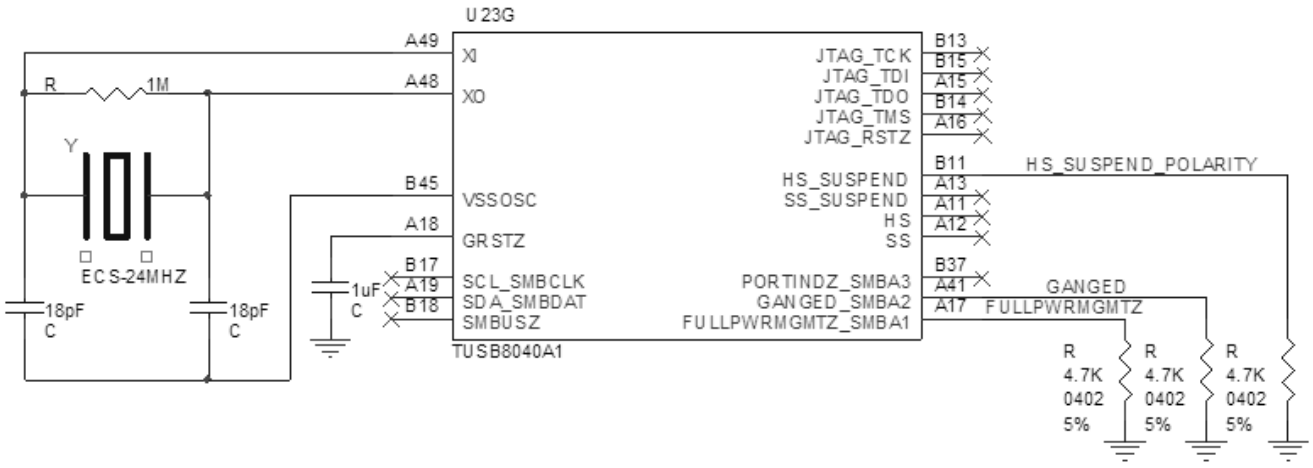


Figure 6-8. Clock, Reset, I²C/SMBUS, and Misc

The HS_SUSPEND is pulled-down, which results in active low power enable (PWRON0z, PWRON1z, PWRON2z, and PWRON3z) for a USB VBUS power switch. The 1 µF capacitor on the GRSTZ pin can only be used if the VDD11 supply is stable before the VDD33 supply. The capacitor may need to be adjusted, depending on the power ramp of the two supplies. Also, the GANGED pin and FULLPWRMGMTZ pin are pulled low, resulting in individual power support for each downstream port. Additionally, this particular implementation has the I²C/SMBUS and JTAG interfaces disabled, thus all terminals related to them are left unconnected.

6.2.2.8 Power Implementation

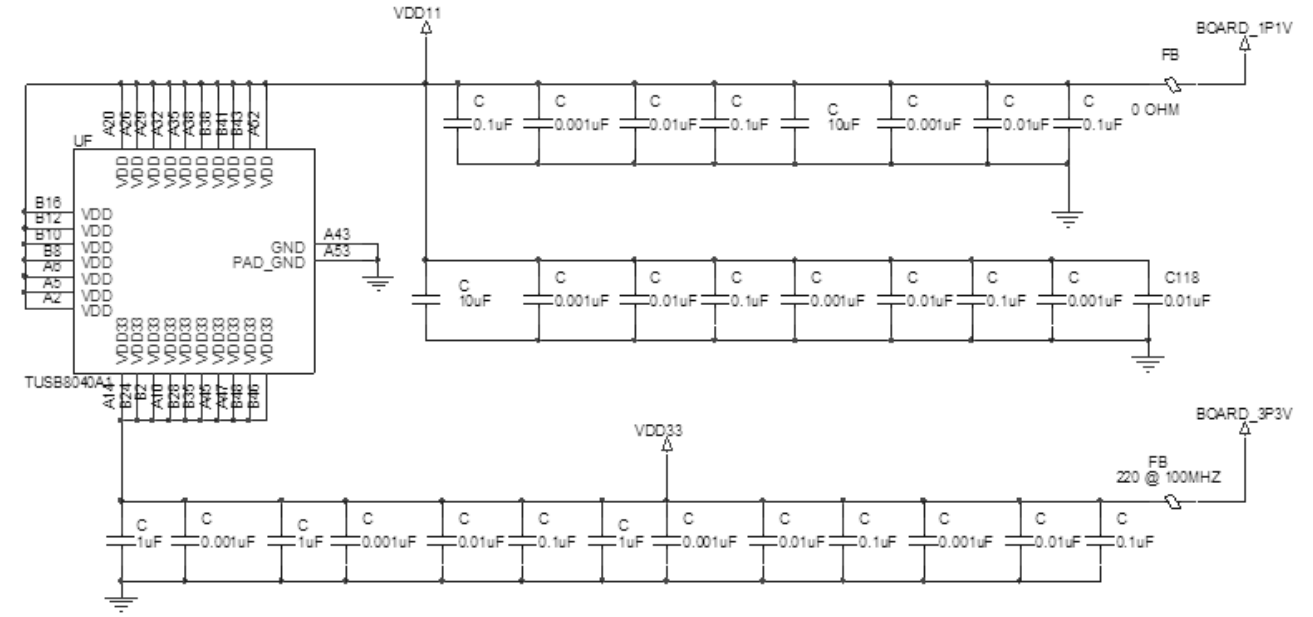


Figure 6-9. Power Implementation

6.2.3 Application Curve

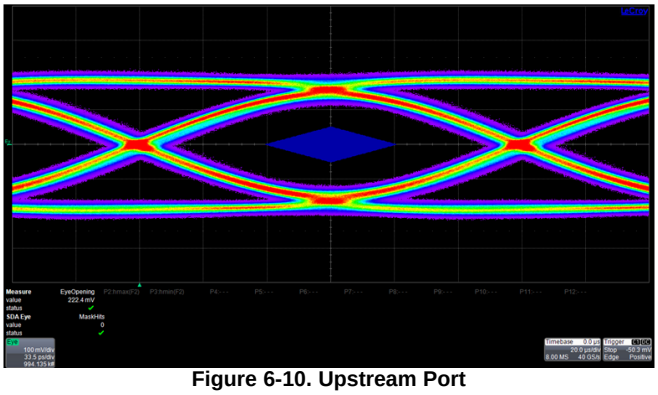


Figure 6-10. Upstream Port

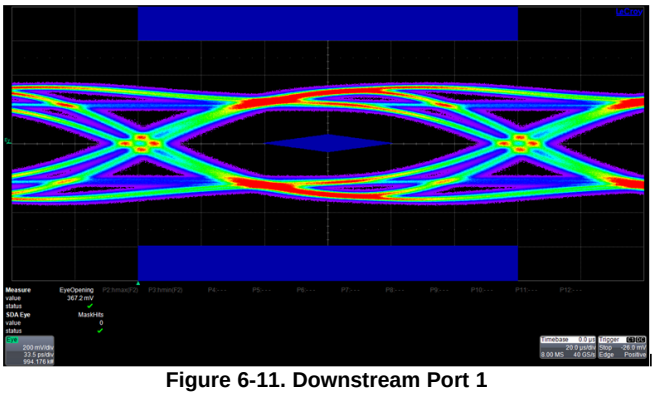


Figure 6-11. Downstream Port 1

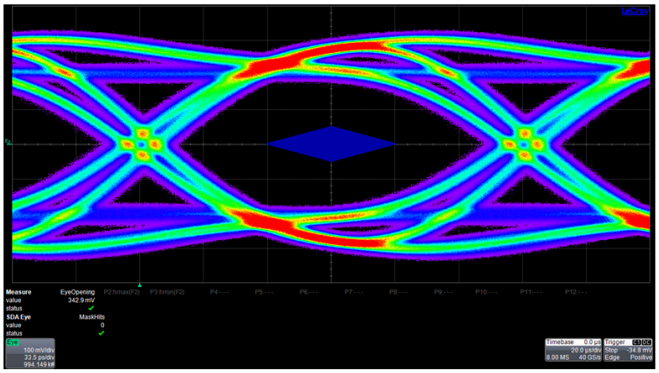


Figure 6-12. Downstream Port 2

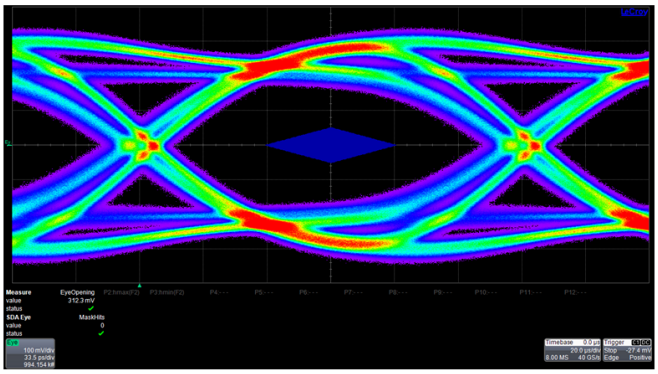


Figure 6-13. Downstream Port 3

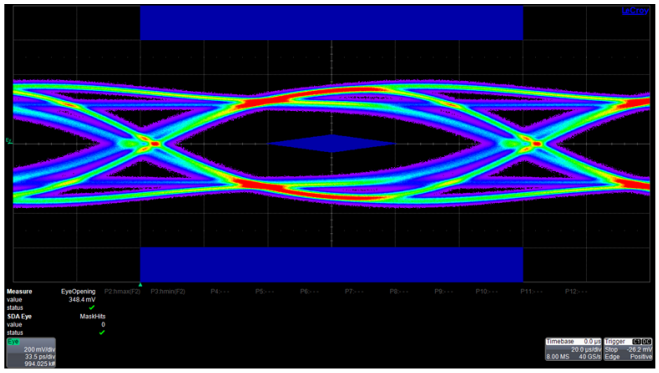


Figure 6-14. Downstream Port 4

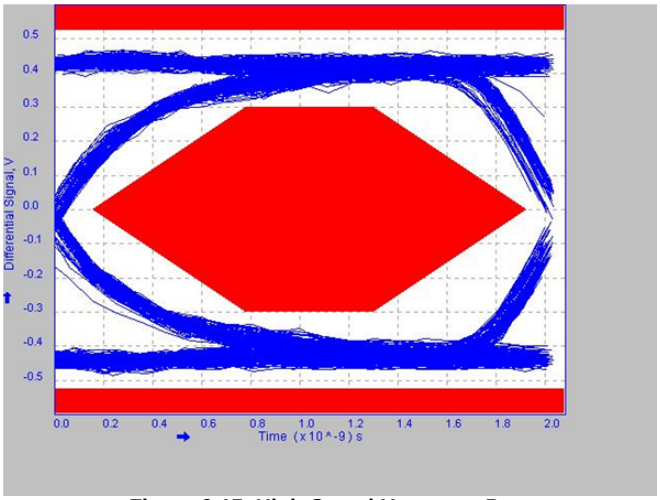


Figure 6-15. High-Speed Upstream Port

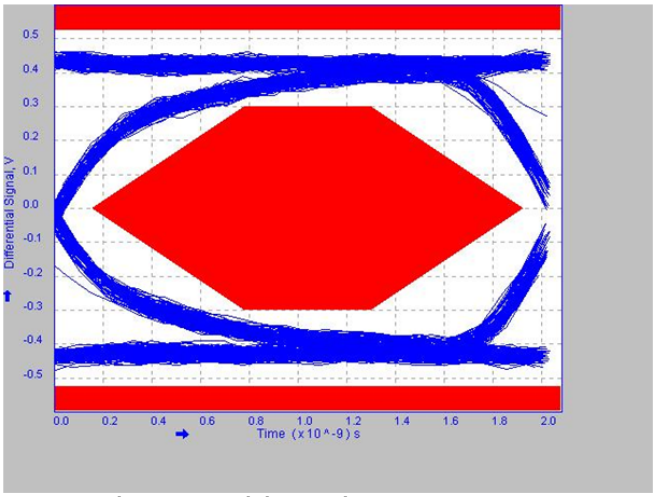


Figure 6-16. High-Speed Downstream Port 1

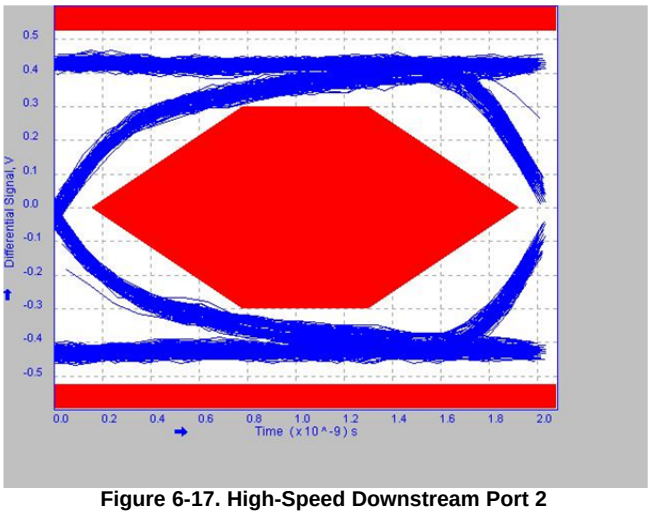


Figure 6-17. High-Speed Downstream Port 2

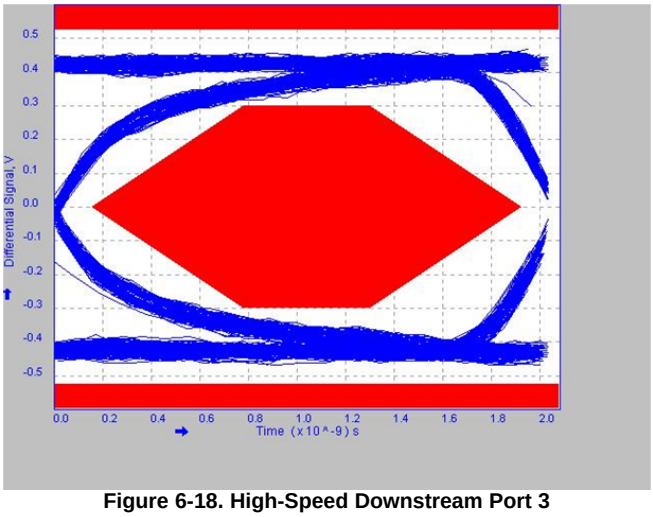


Figure 6-18. High-Speed Downstream Port 3

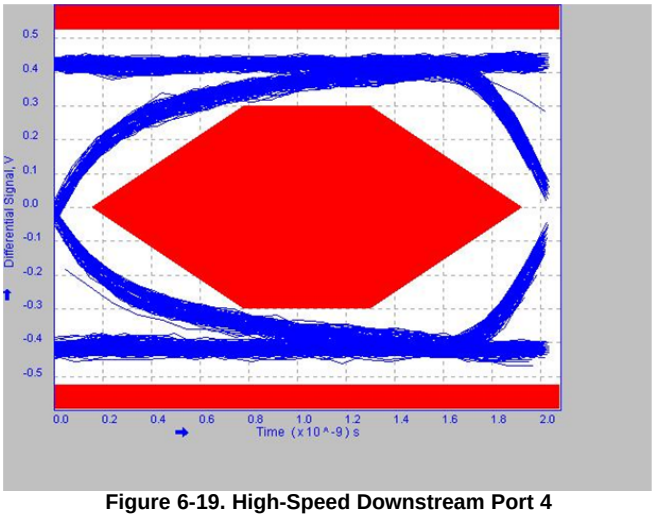


Figure 6-19. High-Speed Downstream Port 4

6.2.4 Layout

6.2.4.1 Layout Guidelines

6.2.4.1.1 Part Placement

- If possible, place all active components on the top layer of the board stack up.
- Place the crystal as close as possible to the TUSB8040A1, and on the top layer of the board stack up to avoid the use of any vias in the clock trace.
- Place the voltage regulators as far away as possible from the TUSB8040A1, the crystal, and the differential pairs.
- Place the TUSB8040A1 apart from the USB connectors (if possible).
- Place the SuperSpeed (SS) transmit differential pair capacitors as close as possible to the USB connector pins. The ESD protection device (if used) should also be placed as close as possible to the USB connectors.
- In general, the bulk capacitors associated with each power rail should be placed as close as possible to the voltage regulators.

6.2.4.1.2 Board Layout Considerations

6.2.4.1.2.1 RKM Package – QFN (Quad Flat No-Lead)

- The RKM package has 0.6-mm (~24 mil) pin pitch. The TUSB8040A1 EVM is routed on 4 layers: signal, power, ground, and signal. This 4 layer board still meets requirements of 0.062 thickness ±0.010.
- The TUSB8040A1 has a thermal pad of 5.5 × 5.5 ±0.1 mm that must be connected to ground through a system of vias.
- All vias under the device should be solder masked to avoid any potential issues with thermal pad layouts.

6.2.4.1.2.2 Impedance

The differential pair traces for each USB port (USB_DP_XX/USB_DM_XX, SB_SSTXP_XX/USB_SSTXM_XX, USB_SSRXP_XX/USB_SSRXM_XX) must be designed with a characteristic impedance of 90 Ω ±10% between the complementary signals (that is, + and –). The width and spacing of the differential pair traces can be modified to achieve the characteristic impedance of 90Ω, and may differ depending on the PCB stack up and materials used. The differential traces on the TUSB8040A1 EVM are 4.1 mils wide with 7.4 mil spacing from a pin pad that is approximately 9.5 mils wide.

The remaining traces should be as close as possible to 50-Ω characteristic impedance. To meet this impedance requirement, the traces on the EVM are 6.0 mils wide. Due to constraints from routing the differential pairs, board stack up, and board thickness requirements, the board fabricator may not be able to get to precisely 50 Ω, in which case maintaining impedances within ±20% of 50 Ω is acceptable.

6.2.4.1.2.3 Critical Signals

- Differential pair signals
- External crystal signals
- Power and ground signals (particularly VBUS and Earth GND)

Important rules for the routing of these critical signals are:

- Run all critical signals on a signal plane adjacent to a solid ground plane layer, if possible.
- Never cross power and ground plane boundaries with critical signals, particularly at a 90° angle.
- Avoid 90° turns in traces, use 45° turns or use bevels instead.
- Keep digital signals away from the differential pairs and the crystal circuitry.
- See the following sections for more information on the routing of critical signals.

6.2.4.1.2.4 Crystal

The XI terminal of the TUSB8040A1 requires a crystal input or an external clock source to the 1.8-V input. Since a 24-MHz crystal is used on the TUSB8040A1 EVM, the other side of the crystal is attached to the XO terminal and the ground connections of the load capacitors are attached to VSS_OSC.

Care should be taken in the layout of the crystal to reduce noise and jitter. The crystal should be located as close as physically possible to the TUSB8040A1 XI and XO terminals. This connection should be short and direct.

6.2.4.1.2.5 USB Interface

The USB ports of the TUSB8040A1 are attached to USB 3.0 connectors. These port connectors allow the hub to communicate to downstream USB 3.0 devices in SS, or downstream USB 2.0 devices in high-speed or full-speed or low-speed. The upstream connection allows simultaneous SS and high-speed connections. The connection speed determination is done automatically by the TUSB8040A1.

6.2.4.1.2.6 Differential Pair Signals

Notes on routing differential pair signals:

- Minimize the trace lengths of the differential pair traces. The maximum recommended trace length for SS differential pair signals and USB 2.0 differential pair signals is eight inches. Longer trace lengths require careful routing to assure proper signal integrity.
- Match the etch lengths of the differential pair traces (that is, DP and DM or SSRXP and SSRXM or SSTXP and SSTXM). There should be less than 5 mils difference between a SS differential pair signal and its complement. The USB 2.0 differential pairs should not exceed 50 mils relative trace length difference.
- Route the differential pair traces parallel to one another and close together as much as possible. The traces should be symmetrical.
- The etch lengths of the differential pair groups do not need to match (that is, the length of the SSRX pair to that of the SSTX pair), but all trace lengths should be minimized.

NOTE

To minimize crosstalk, the spacing between the TX and RX signal pairs for each interface should be five times the width of the trace (5W rule). For instance, on the TUSB8040A1 EVM there are 27.5 mils of space between the TX and RX differential pairs. If this 5W rule cannot be implemented, then the space between the TX and RX differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

- There should be a general keep-out region of at least 20 mils around the differential pairs so that signals, components, or power/ground planes are not routed close to the differential pairs. The exception is at the TUSB8040A1.
- Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, ensure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close to the TUSB8040A1 as possible.
- Do not place power fuses across the differential pair traces.
- It is preferable to route the differential pair signals directly from the port to the via under the TUSB8040A1. On the TUSB8040A1 EVM, the differential pair signals “fly-by” the ESD protection devices so that no stubs are created. Depending on board layout, this may not always be possible.
- The differential pairs should be routed over a solid ground plane. This ground plane should run under the entire trace length from the TUSB8040A1 (or via) to the pins of the USB connectors and extend past the traces by 10 mils. Avoid routing differential pairs at 90° angles over power plane edges.
- To ease routing, the polarity of the SS differential pairs can be swapped. Thus SSTXP can be routed to SSTXM, or SSRXM can be routed to SSRXP.
- To route the differential pairs of the TUSB8040A1 to the USB connectors, it is necessary on the downstream ports to cross the SSTX pair and the SSRX pair. To avoid using multiple sets of vias, these were carefully placed on the TUSB8040A1 EVM so that the crossover was inherent in the board design, and both pairs of signals (along with the USB 2.0 differential pair) were routed on the bottom layer.

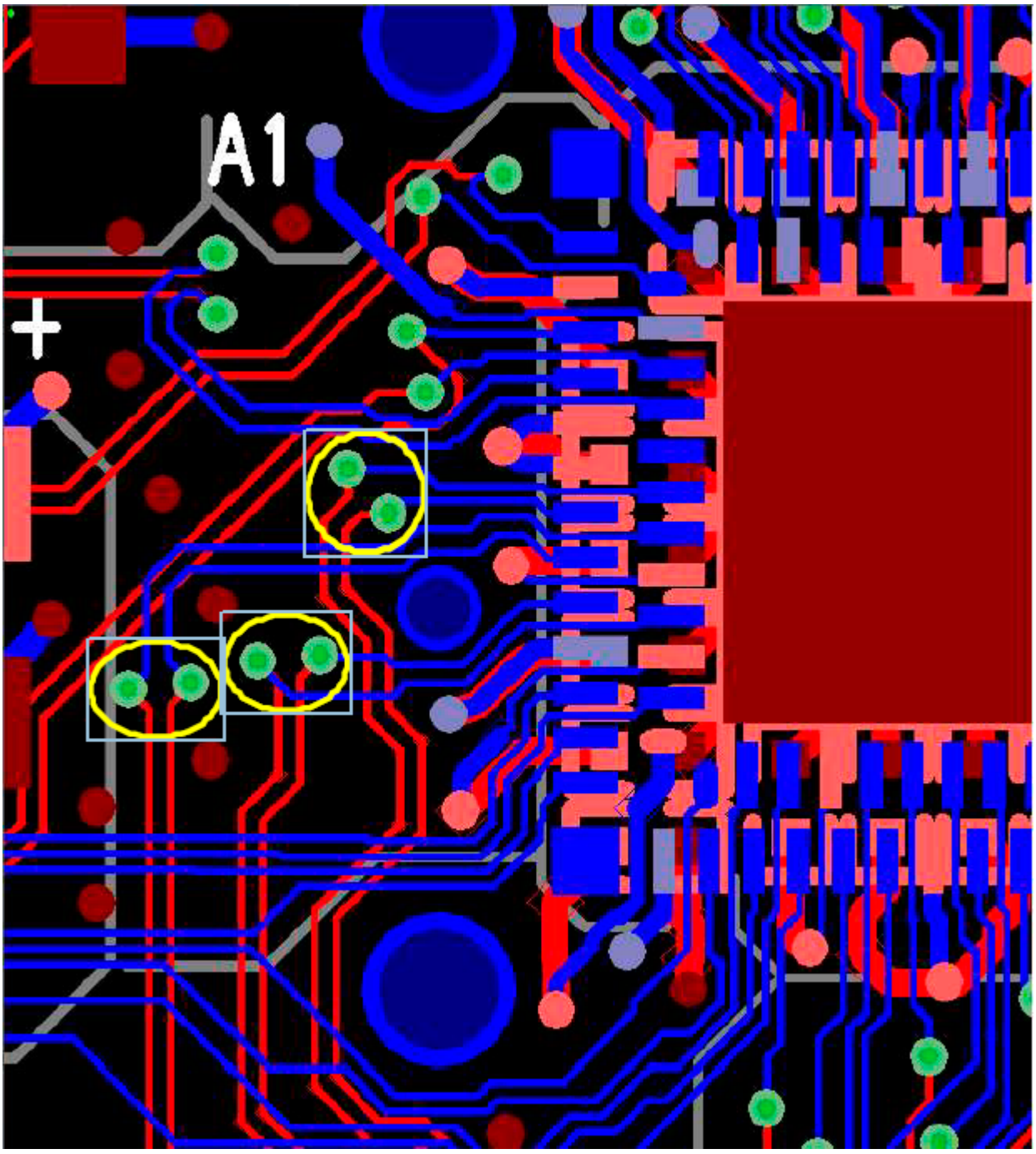


Figure 6-20. Using Via Placement to Cross the SSTX and SSRX Pairs

6.2.4.1.2.6.1 Internal Bond Wire Mismatch

The routing of the SS differential pairs must take into account the internal bond wire mismatch inherent in the dual row RKM package. Internal wire lengths (in mil) are below.

Table 6-2. Internal Bond Wire Mismatch

Signal Name	Pin No.	Bondwire Length (mil)	Difference (mil)
USB_SSTXM_UP USB_SSTXP_UP	A42 B39	125 97	28
USB_SSRXM_UP USB_SSRXP_UP	B40 A44	89 109	20
USB_DM_UP USB_DP_UP	B42 A46	81 103	22
USB_DP_DN0 USB_DM_DN0	B1 A1	102 136	34
USB_SSRXP_DN0 USB_SSRXM_DN0	B3 A3	80 112	32
USB_SSTXP_DN0 USB_SSTXM_DN0	B4 A4	72 102	30
USB_SSRXP_DN2 USB_SSRXM_DN2	B6 A7	59 81	22
USB_SSTXP_DN2 USB_SSTXM_DN2	B7 A8	58 81	23
USB_DP_DN2 USB_DM_DN2	A9 B9	82 62	20
USB_DM_DN3 USB_DP_DN3	A31 B29	87 61	26
USB_SSRXP_DN3 USB_SSRXM_DN3	B30 A33	59 81	22
USB_SSTXP_DN3 USB_SSTXM_DN3	B31 A34	58 81	23
USB_SSRXP_DN1 USB_SSRXM_DN1	B33 A36	66 93	27
USB_SSTXP_DN1 USB_SSTXM_DN1	B34 A37	74 101	27
USB_DM_DN1 USB_DP_DN1	A39 B36	126 92	34

6.2.4.1.2.7 Port Connectors

Most TUSB8040A1 customers will use thru-hole USB 3.0 standard connectors with mounting pegs soldered into the board for more rigid connections. The thru-hole connectors allow differential pairs to be routed on the bottom layer of the EVM without requiring any vias to the top layer at the connector. Routing on the bottom layer of the EVM to the thru-hole connector can reduce the stub length caused by the thru-hole pins.

The outside shield of the connector should be tied to chassis ground to provide a low impedance path to the chassis ground for ESD current. If galvanic isolation is required, the outside shield should be isolated from digital ground with a parallel combination of a 1-MΩ resistor and capacitors of 0.1 µF and 0.001 µF. Pins 4 and 7 of the USB 3.0 connector should be connected to digital ground. Both of these pins should be connected directly to the board ground plane as close to the connector as possible.

6.2.4.1.2.8 Reset Terminals

Asserting the TUSB8040A1 GRSTZ pin low resets the TUSB8040A1. The GRSTZ signal should be held low for a minimum of 3 ms from the time that the power supplies reach the minimum required supply voltage (90% of nominal) and the crystal is active, to ensure a valid reset. An external delay capacitor of 1 µF along with the internal pull-up resistor can be used to generate the power on reset pulse; the voltage ramp of the implementation dictates the necessary capacitor value. An alternative to this passive reset is to actively drive GRSTZ low, using external circuitry for the minimum reset time following power on.

6.2.4.1.2.9 Miscellaneous Terminals

The USB_R1 and USBR1_RTN terminals require a precision resistor. A 9.09-kΩ ±1% resistor should be placed in parallel across these terminals, as close to the device as possible.

While the TUSB8040A1 EVM can utilize external pull up and pull down resistors on these terminals, there are inherent pull-ups and pull-downs implemented within the TUSB8040A1.

NOTE

The internal pull-up and pull-down resistors of the TUSB8040A1 have a nominal value of 22 kΩ (150 µA at 3.3 V). If using an external pull up on a terminal that has an internal pull- down resistor, TI recommends using a value of 7.5 kΩ or smaller. If using an external pull down on a terminal that has an internal pull-up resistor, TI recommends using a value of 7.5 kΩ or smaller.

- **SMBUSz** – The I^2C interface mode is enabled by default via the internal pull-up resistor on this terminal. If a 4.7-kΩ pull-down is placed on this terminal and sampled at power-on reset, SMBUS mode is enabled.
- **SDA_SMBDAT and SCL_SMBCLK** – Serial EEPROM or SMBUS interface. On the EVM, these pins are routed to a serial EEPROM socket with 1-kΩ pull-up resistors installed on both signals. If the TUSB8040A1 is being used in SMBUS mode, then these signals become the data and clock signal, respectively. The TUSB8040A1 has internal pull-downs on these terminals. The SDA_SMBDAT terminal is sampled at the de-assertion of reset to determine if SS low power states U1 and U2 are disabled. If SDA_SMBDAT is high, U1 and U2 low power states are disabled. If SDA_SMBDAT is low, U1 and U2 low power states are enabled. Disabling U1 and U2 allows the TUSB8040A1 to work with USB 3.0 devices that do not implement low power states per the USB 3.0 specification. If the EEPROM or SMBUS is implemented, the value of the u1u2Disable bit in the Device Configuration Register determines if the low power states U1 and U2 are disabled. The SCL_SMBCLK terminal is sampled at the de-assertion of reset to determine if SuperSpeed low power state (U1 and U2) initiation is disabled. If SCL_SMBCLK is high, U1 and U2 low power state initiation is disabled. If SCL_SMBCLK is low, U1 and U2 low power states are completely enabled. Disabling U1 and U2 initiation allows the TUSB8040A1RKM to accept requests to enter low power states from the host or downstream devices, but it will not initiate the transitions. If the EEPROM or SMBUS is implemented, the value of the u1u2TimerOvr bit in the Device Configuration Register determines if the low power state initiation is disabled.
- **HS_SUSPEND_POLARITY** – Downstream port power switch enable polarity is set to active high if a pull-up is placed on this terminal and sampled at power-on reset. The TUSB8040A1 has an internal pull-down on this terminal to set the power enables to active low by default. Since this terminal also acts as an LED output, a pull-up value of 330 Ω is recommended if an LED with series resistance of 1 kΩ is used for the status LED circuit.
- **SS_SUSPEND_SSC** – Spread spectrum clocking is disabled if a pull-up is placed on this terminal and sampled at power-on reset. The TUSB8040A1 has an internal pull down on this terminal to enable SSC by default. Since this terminal also acts as an LED output, a pull-up value of 330 ohm is recommended if a LED with series resistance of 1K is used for the status LED circuit.

6.2.4.1.2.10 Power Control and Battery Charging Terminals

- **FULLPWRMGMTZ_SMBA1** – Full power management is enabled and reported in the USB descriptors when a 4.7-kΩ pull-down is placed on this terminal and sampled at power-on reset. The TUSB8040A1 as an internal pull-up on this terminal, the TUSB8040A1 defaults to a non full power management state, which is a lower cost implementation where no downstream port power control is implemented. This pin also acts as the interface for the SMBA1 signal when a SMBus host is connected to the TUSB8040A1.
- **GANGED_SMBA2** – Individual port power management is enabled and reported in the USB descriptors when a 4.7-kΩ pull-down is placed on this terminal and sampled at power-on reset. The TUSB8040A1 has an internal pull-up on this terminal. The TUSB8040A1 defaults to a ganged power management state, which is a lower cost implementation. This pin also acts as the interface for the SMBA2 signal when a SMBus host is connected to the TUSB8040A1.
- **PWRON0Z_BATEN0** – Battery charging on downstream port 0 is disabled by default via the internal pull-down resistor on this terminal. If a 4.7-kΩ pull-up is placed on this terminal and sampled at power on reset, battery charging on the downstream port 0 is enabled. After reset, this signal acts at the active low power enable/disable for the downstream port power switch for port 0.
- **OVERCUR0Z** – An over-current event on port 0 is reported to the TUSB8040A1 by the downstream port power controller circuitry using this terminal. The TUSB8040A1 has an internal pull-up on this terminal to avoid any unexpected over-current reporting, but an external pull-up resistor is recommended for noisy applications.
- **PWRON1Z_BATEN1** – Battery charging on downstream port 1 is disabled by default via the internal pull-down resistor on this terminal. If a 4.7-kΩ pull-up is placed on this terminal and sampled at power on reset, battery charging on the downstream port 1 is enabled. After reset, this signal acts at the active low power enable/disable for the downstream port power switch for port 1.
- **OVERCUR1Z** – An over-current event on port 1 is reported to the TUSB8040A1 by the downstream port power controller circuitry using this terminal. The TUSB8040A1 has an internal pull-up on this terminal to avoid any unexpected over-current reporting, but an external pull-up resistor is recommended for noisy applications.
- **PWRON2Z_BATEN2** – Battery charging on downstream port 2 is disabled by default via the internal pull-down resistor on this terminal. If a 4.7-kΩ pull-up is placed on this terminal and sampled at power on reset, battery charging on the downstream port 2 is enabled. After reset, this signal acts at the active low power enable/disable for the downstream port power switch for port 2.
- **OVERCUR2Z** – An over-current event on port 2 is reported to the TUSB8040A1 by the downstream port power controller circuitry using this terminal. The TUSB8040A1 has an internal pull-up on this terminal to avoid any unexpected over-current reporting, but an external pull-up resistor is recommended for noisy applications.
- **PWRON3Z_BATEN3** – Battery charging on downstream port 3 is disabled by default via the internal pull-down resistor on this terminal. If a 4.7-kΩ pull-up is placed on this terminal and sampled at power on reset, battery charging on the downstream port 3 is enabled. After reset, this signal acts at the active low power enable/disable for the downstream port power switch for port 3.
- **OVERCUR3Z** – An over-current event on port 3 is reported to the TUSB8040A1 by the downstream port power controller circuitry using this terminal. The TUSB8040A1 has an internal pull-up on this terminal to avoid any unexpected over-current reporting, but an external pull-up resistor is recommended for noisy applications.

6.2.4.1.2.11 USB 2.0 Port Indicator LED Terminals

Table 6-3. Port State to Port Indicator Color Mapping

Power Switching	Downstream Facing Hub Port State			
	Powered-Off	Disconnected, Disabled, Not Configured, Resetting, Testing	Enabled, Transmit, Receive	Suspended, Resuming, Restart
With	Off or amber if over-current	Off	Green	Off
Without	Off	Off or amber if over-current	Green	Off

- **PORTINDZ_SMBA3** – Individual USB 2.0 port indicator LEDs are enabled and reported in the USB descriptors when a 4.7-kΩ pull-down is placed on this terminal and sampled at power-on reset. The TUSB8040A1 has an internal pull-up on this terminal. The TUSB8040A1 defaults to the lower cost implementation without the port LEDs. This pin also acts as the interface for the SMBA3 signal when a SMBus host is connected to the TUSB8040A1.
- **LEDA0Z_RMBL0** – Removable device mode on port 0 is enabled by default via the internal pull-up resistor on this terminal. If a 4.7-kΩ pull-down is placed on this terminal and sampled at power on reset, port 0 is reported in the USB descriptors as a non-removable port with a permanently attached device. After reset, this signal acts as the active low USB 2.0 port indicator status amber LED for port 0.
- **LEDG0Z_USED0** – Port 0 is enabled by default via the internal pull-up resistor on this terminal. If a 4.7-kΩ pull-down is placed on this terminal and sampled at power on reset, port 0 will not be an active port. After reset, this signal acts as the active low USB 2.0 port indicator status green LED for port 0.
- **LEDA1Z_RMBL1** – Removable device mode on port 1 is enabled by default via the internal pull-up resistor on this terminal. If a 4.7-kΩ pull-down is placed on this terminal and sampled at power on reset, port 1 is reported in the USB descriptors as a non-removable port with a permanently attached device. After reset, this signal acts as the active low USB 2.0 port indicator status amber LED for port 1.
- **LEDG1Z_USED1** – Port 1 is enabled by default via the internal pull-up resistor on this terminal. If a 4.7-kΩ pull-down is placed on this terminal and sampled at power on reset, port 1 will not be an active port. After reset, this signal acts as the active low USB 2.0 port indicator status green LED for port 1.
- **LEDA2Z_RMBL2** – Removable device mode on port 2 is enabled by default via the internal pull-up resistor on this terminal. If a 4.7-kΩ pull-down is placed on this terminal and sampled at power on reset, port 2 is reported in the USB descriptors as a non-removable port with a permanently attached device. After reset, this signal acts as the active low USB 2.0 port indicator status amber LED for port 2.
- **LEDG2Z_USED2** – Port 2 is enabled by default via the internal pull-up resistor on this terminal. If a 4.7-kΩ pull-down is placed on this terminal and sampled at power on reset, port 2 will not be an active port. After reset, this signal acts as the active low USB 2.0 port indicator status green LED for port 2.
- **LEDA3Z_RMBL3** – Removable device mode on port 3 is enabled by default via the internal pull-up resistor on this terminal. If a 4.7-kΩ pull-down is placed on this terminal and sampled at power on reset, port 3 is reported in the USB descriptors as a non-removable port with a permanently attached device. After reset, this signal acts as the active low USB 2.0 port indicator status amber LED for port 3.
- **LEDG3Z_USED3** – Port 3 is enabled by default via the internal pull-up resistor on this terminal. If a 4.7-kΩ pull-down is placed on this terminal and sampled at power on reset, port 3 will not be an active port. After reset, this signal acts as the active low USB 2.0 port indicator status green LED for port 3.

6.2.4.1.3 Power

6.2.4.1.3.1 Power

VDD11 and VDDA11 should be implemented as a single power plane, as should VDD33, VDDA33 and VDDA33_OSC.

- The VDD11 terminals supply 1.1-V power to the core of the TUSB8040A1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The DC resistance of the ferrite bead on the 1.1-V power rail can affect the voltage provided to the device, due to the high current draw on the power rail. The output of the 1.1-V voltage regulator may need to be adjusted to account for this, or a ferrite bead with low DC resistance (less than 0.05 Ω) can be selected.
- The VDD33 terminals supply 3.3-V power to the I/O of the TUSB8040A1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- All power rails require a 10-µF capacitor or 1-µF capacitors for stability and noise immunity. These bulk capacitors can be placed anywhere on the power rail. The smaller decoupling capacitors should be placed as close to the TUSB8040A1 power pins as possible, with an optimal grouping of two of differing values per pin.

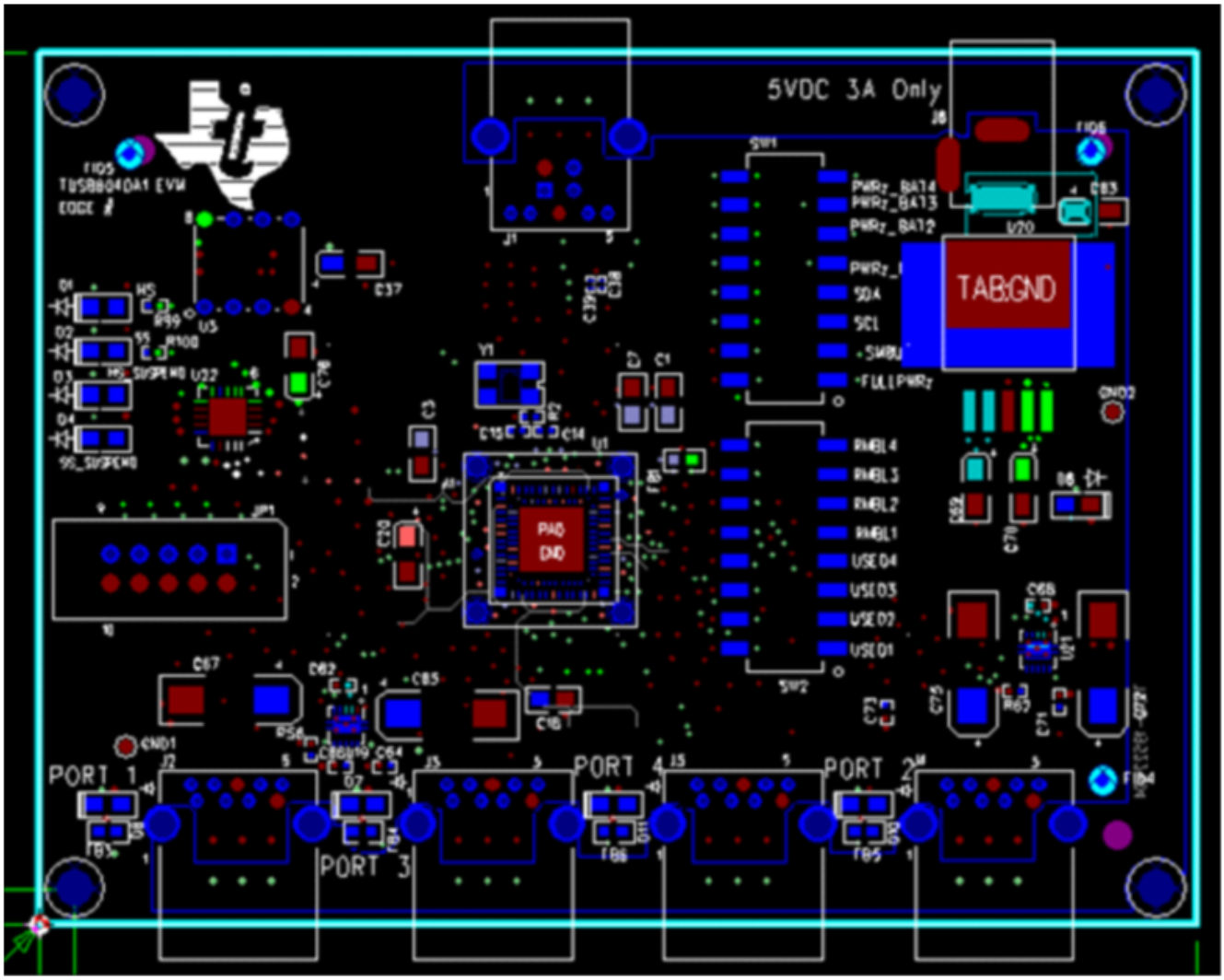
6.2.4.1.3.2 Downstream Port Power

- The downstream port power VBUS must be supplied by a source capable of supplying 5 V and up to 900 mA per port. Downstream port power switches can be controlled by the TUSB8040A1 signals. It is also possible to leave the downstream port power always enabled.
- A large bulk low-ESR capacitor of 22 µF or larger is required on each downstream port's VBUS to limit in-rush current.
- The ferrite beads on the VBUS pins of the downstream USB port connections are recommended for both ESD and EMI reasons. A 0.1-µF capacitor on the USB connector side of the ferrite provides a low impedance path to ground for fast rise time ESD current that might have coupled onto the VBUS trace from the cable.

6.2.4.1.3.3 Ground

Only one board ground plane should be used in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the TUSB8040A1 and any of the voltage regulators should be connected to this plane with vias. An earth or chassis ground is implemented only near the USB port connectors on a different plane for EMI and ESD purposes.

6.2.4.2 Layout Example



Note the EVM dimensions of 3” × 4” accommodates various lab test components; actual production implementations can be much smaller. Also, the TUSB8040A1EVM is laid out to accept either a TUSB8040A1 unit or a socket. This socket functionality would not need to be duplicated on a production implementation.

6.2.5 Power Supply Recommendations

6.2.5.1 Power Up and Reset

The TUSB8040A1 does not have specific power sequencing requirements with respect to the core power (VDD) or I/O and analog power (VDD33). The core power (VDD) or I/O power (VDD33) may be powered up for an indefinite period of time while the other is not powered up if all of these constraints are met:

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered up must be limited to 100 hours over the projected life-time of the device.
- Bus contention while VDD33 is powered down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 3 ms is required. This is defined as the time when the power supplies are in the recommended operating range to the de-assertion of GRSTz. This can be generated using programmable-delay supervisory device or using an RC circuit.

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 3 ms is required. This is defined as the time when the power supplies are in the recommended operating range to the de-assertion of GRSTz. This can be generated using programmable-delay supervisory device or using an RC circuit.

7 Device and Documentation Support

7.1 Trademarks

All trademarks are the property of their respective owners.

7.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB8040A1RKMR	ACTIVE	WQFN-MR	RKM	100	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB8040A1 RKM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

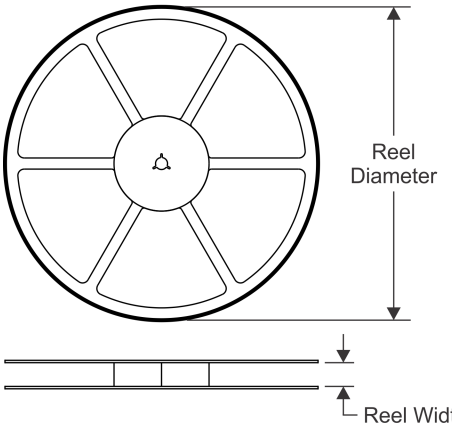
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

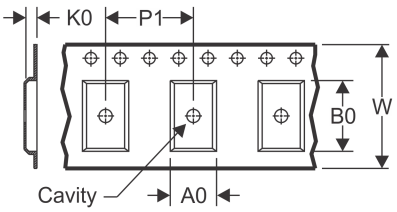
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

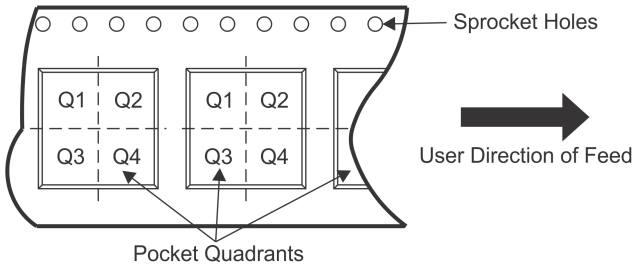


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

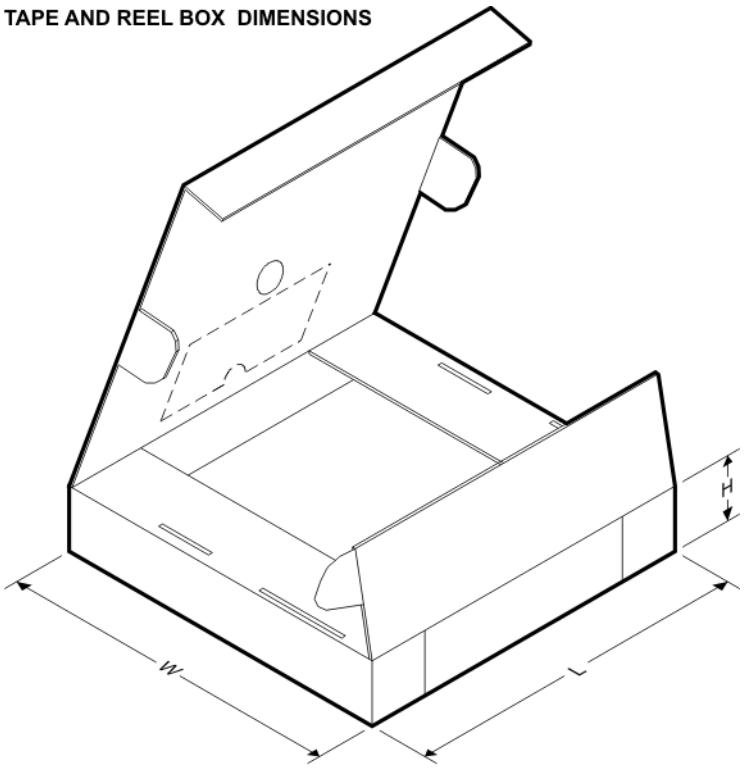
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB8040A1RKMR	WQFN-MR	RKM	100	3000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

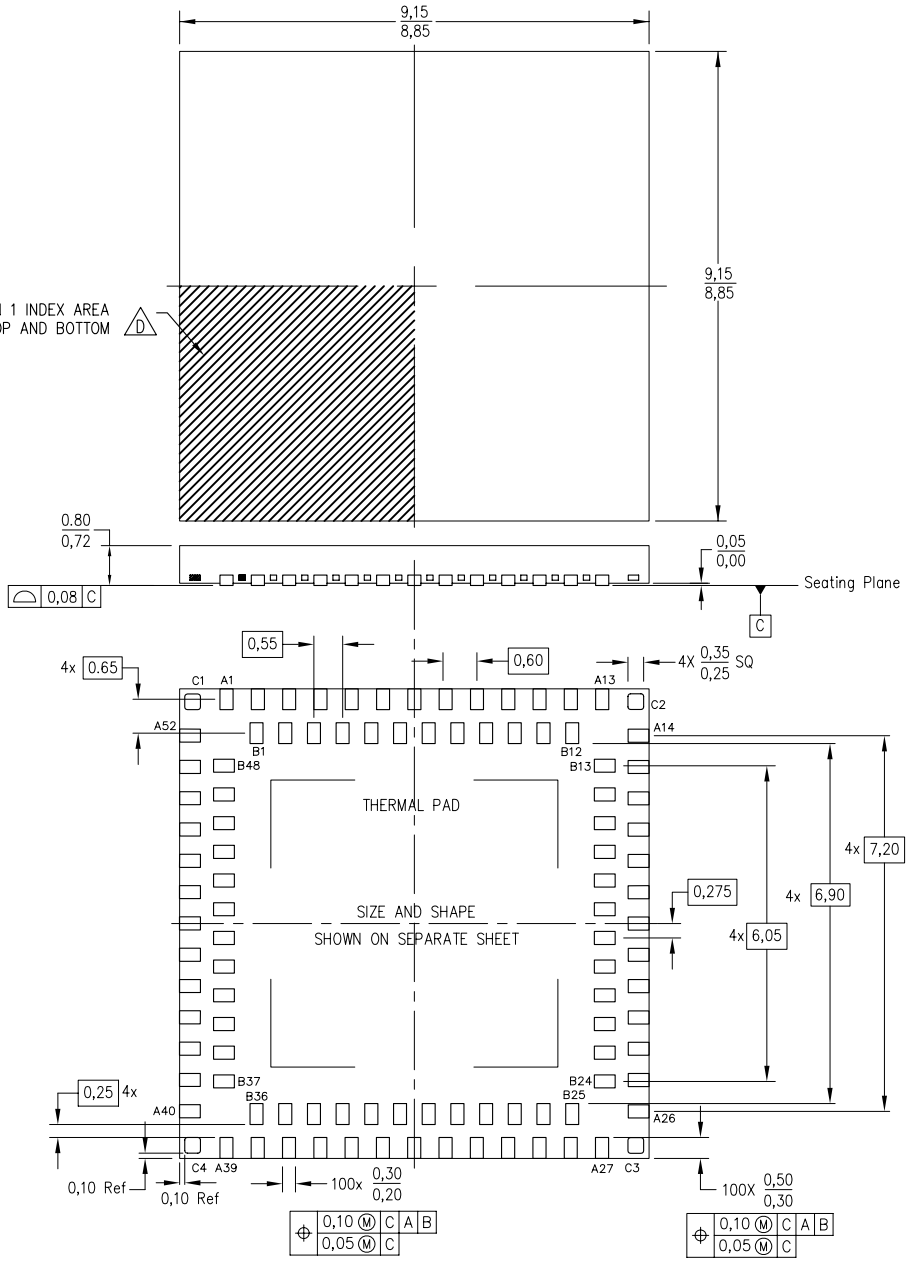
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB8040A1RKMR	WQFN-MR	RKM	100	3000	367.0	367.0	38.0

RKM (S–PWQFN–N100) PLASTIC QUAD FLATPACK NO–LEAD



4211055/C 10/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) staggered multi–row package configuration.
D. Pin A1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin A1 identifiers are either a molded, marked, or metal feature.
E. The package thermal pad must be soldered to the board for thermal and mechanical performance.
F. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

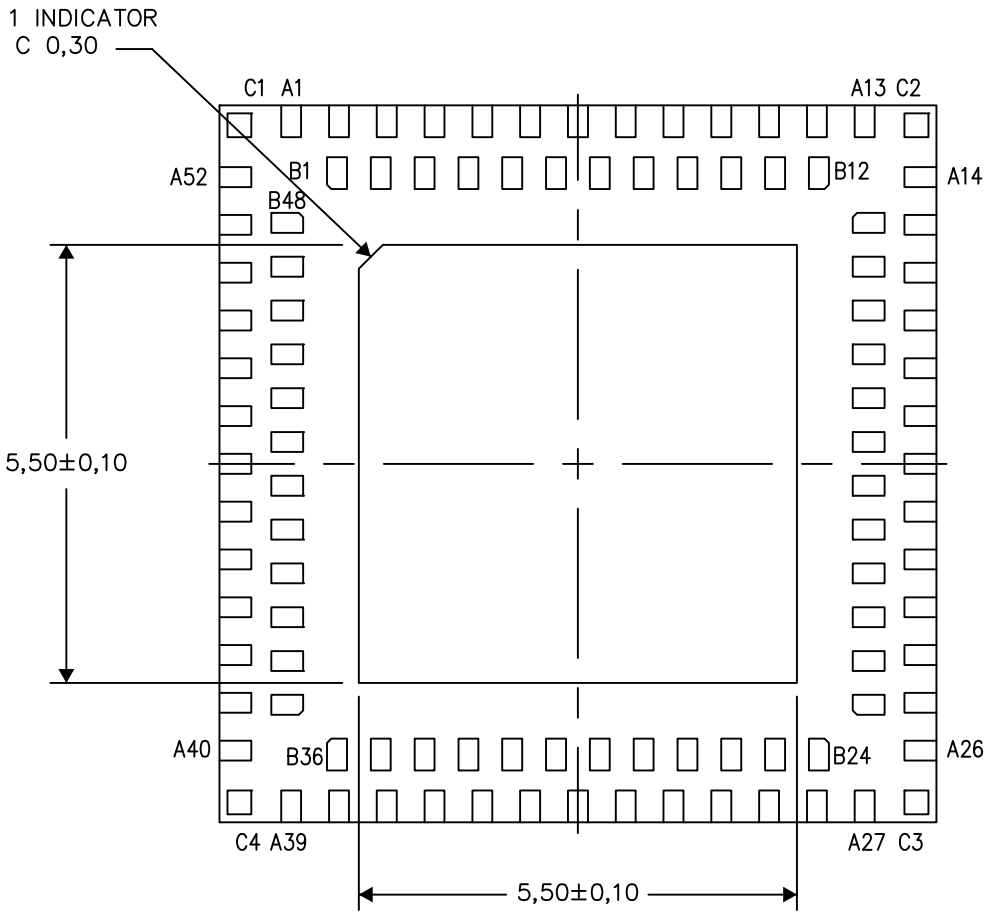
RKM (S–PWQFN–N100) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

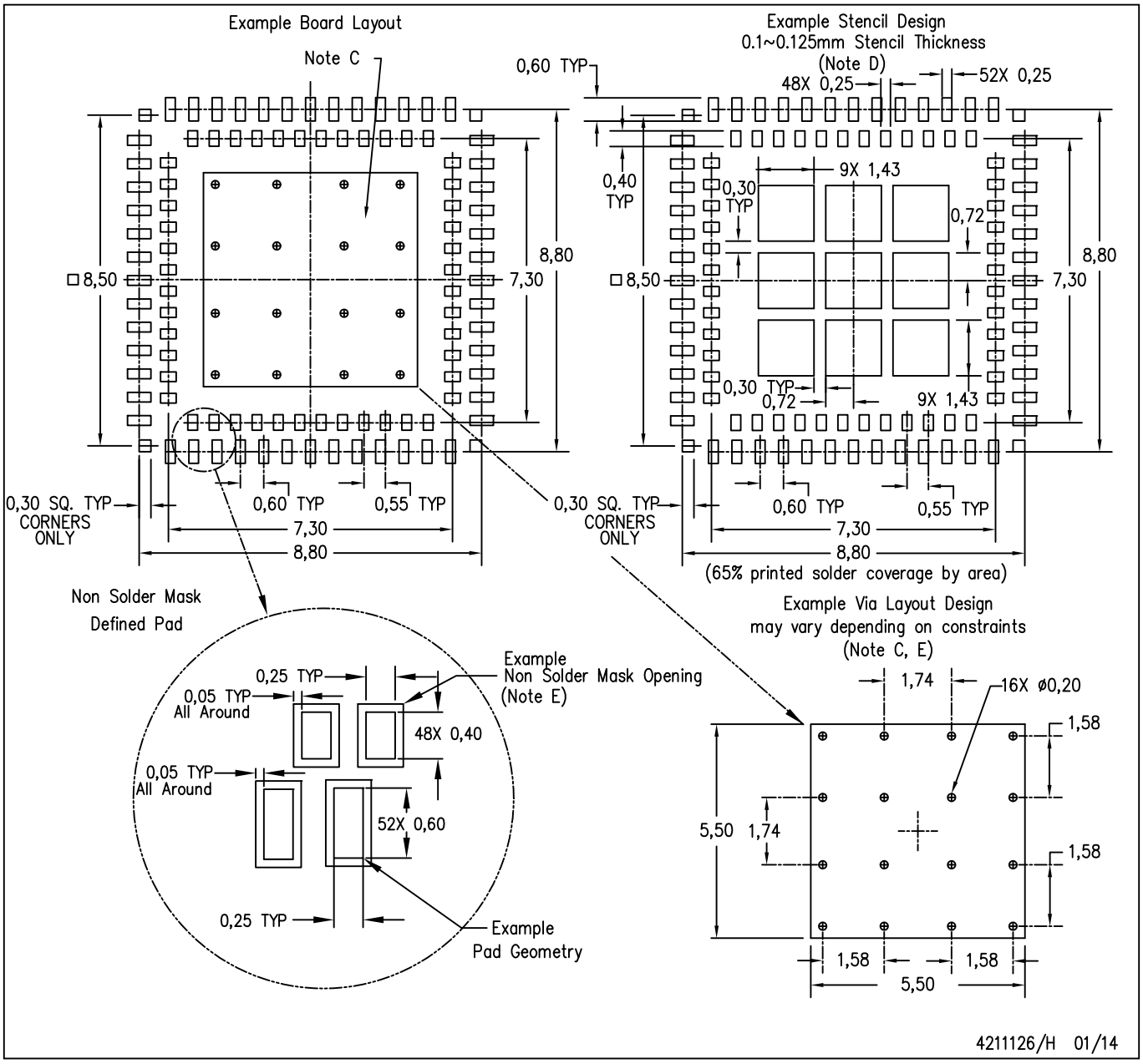


Bottom View

Exposed Thermal Pad Dimensions 4211101/D 01/14

NOTE: All linear dimensions are in millimeters

RKM (S–PWQFN–N100) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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