

# FDPF16N50 / FDPF16N50T

## N-Channel UniFET™ MOSFET

### 500 V, 16 A, 380 mΩ

#### Features

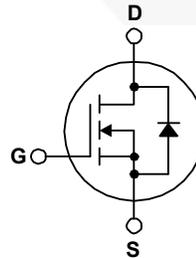
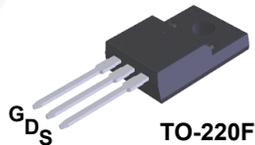
- $R_{DS(on)} = 380 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 8 \text{ A}$
- Low Gate Charge (Typ. 32 nC)
- Low  $C_{rss}$  (Typ. 20 pF)
- 100% Avalanche Tested

#### Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

#### Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



#### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDPF16N50 FDPF16N50T	Unit
$V_{DSS}$	Drain-Source Voltage	500	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	16*
		- Continuous ( $T_C = 100^\circ\text{C}$ )	9.6*
$I_{DM}$	Drain Current - Pulsed (Note 1)	64*	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	780	mJ
$I_{AR}$	Avalanche Current (Note 1)	16	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	20	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	- Derate above $25^\circ\text{C}$	38.5
			0.3
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

\* Drain current limited by maximum junction temperature.

#### Thermal Characteristics

Symbol	Parameter	FDPF16N50 FDPF16N50T	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	3.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDPF16N50	FDPF16N50	TO-220F	Tube	N/A	N/A	50 units
FDPF16N50T	FDPF16N50T	TO-220F	Tube	N/A	N/A	50 units

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted.

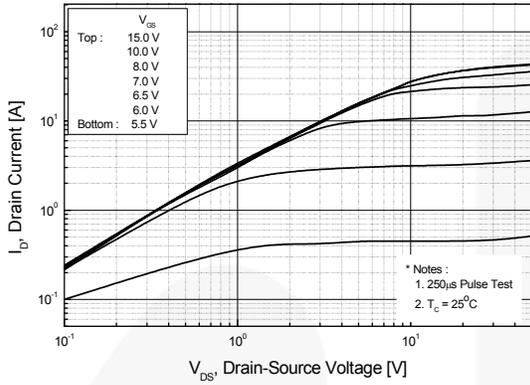
Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	500	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	--	0.5	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500V, V <sub>GS</sub> = 0V V <sub>DS</sub> = 400V, T <sub>C</sub> = 125°C	--	--	1 10	μA μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 8A	--	0.31	0.38	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 8A	--	23	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	1495	1945	pF
C <sub>oss</sub>	Output Capacitance		--	235	310	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	20	30	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250V, I <sub>D</sub> = 16A R <sub>G</sub> = 25Ω	--	40	90	ns
t <sub>r</sub>	Turn-On Rise Time		--	150	310	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	(Note 4)	--	65	140	ns
t <sub>f</sub>	Turn-Off Fall Time		--	80	170	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 400V, I <sub>D</sub> = 16A V <sub>GS</sub> = 10V	--	32	45	nC
Q <sub>gs</sub>	Gate-Source Charge		--	8.5	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		(Note 4)	--	14	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	9.2	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	37	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 16A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 16A di <sub>F</sub> /dt = 100A/μs	--	490	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	5.0	--	μC

### NOTES:

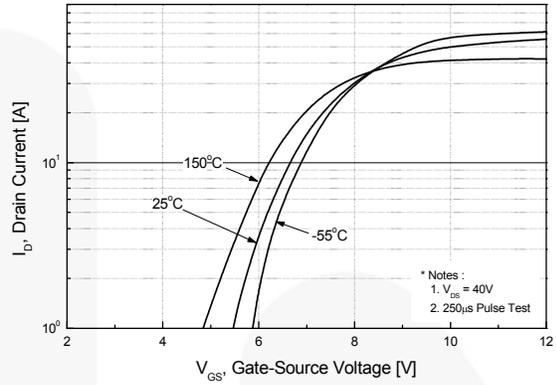
1. Repetitive rating; pulse-width limited by maximum junction temperature.
2. L = 5.5 mH, I<sub>AS</sub> = 16 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 16 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

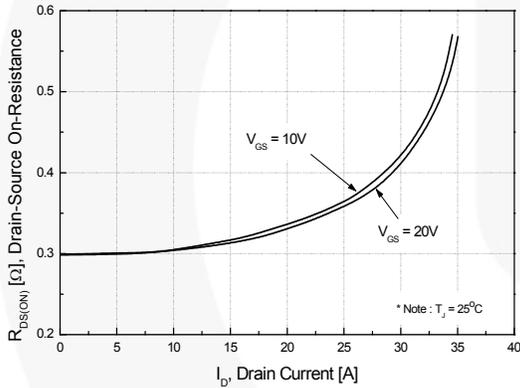
**Figure 1. On-Region Characteristics**



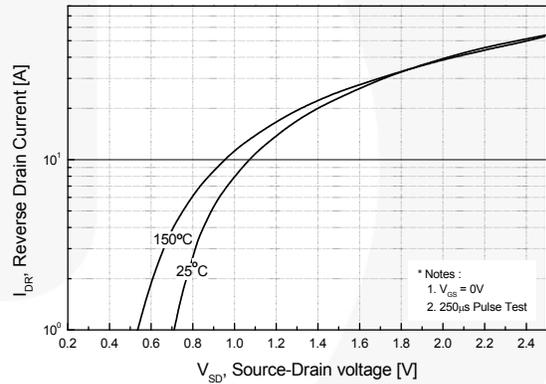
**Figure 2. Transfer Characteristics**



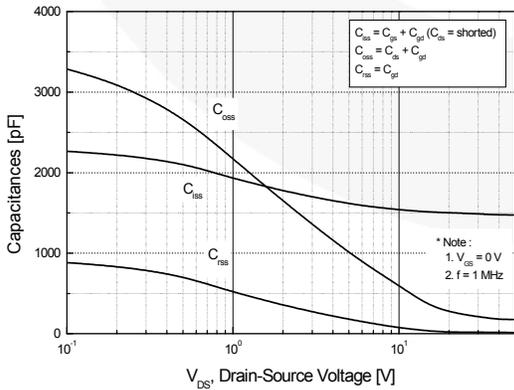
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



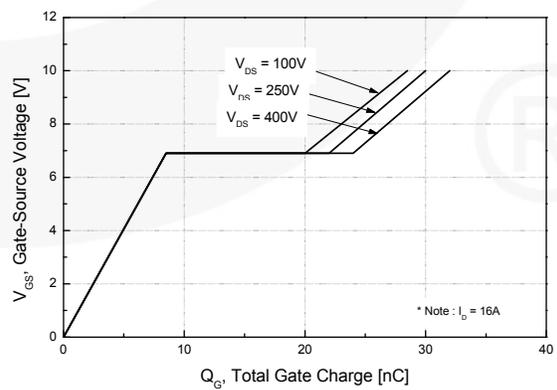
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

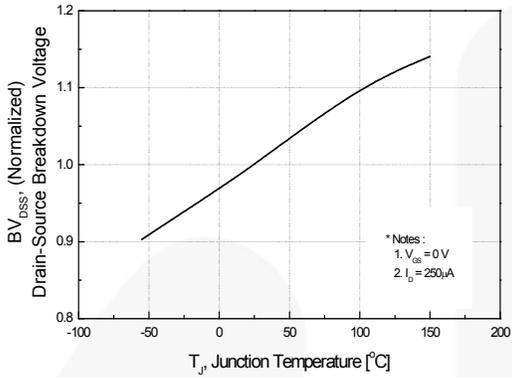


**Figure 6. Gate Charge Characteristics**

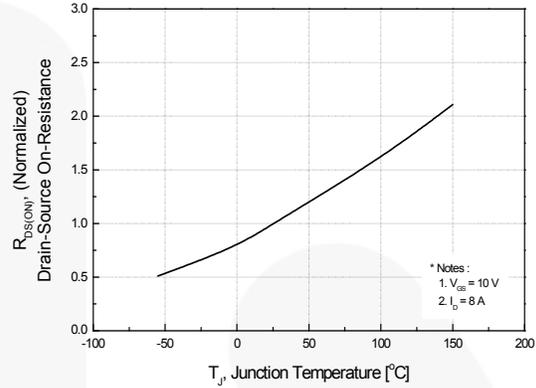


**Typical Performance Characteristics** (Continued)

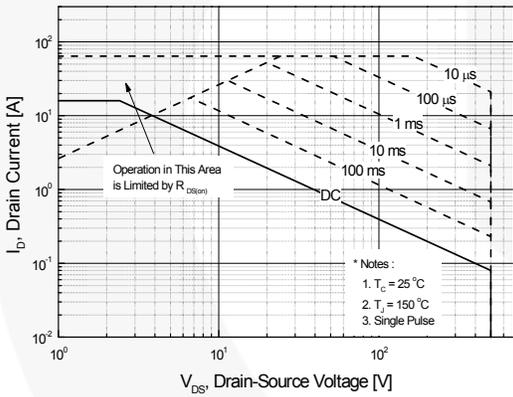
**Figure 7. Breakdown Voltage Variation vs. Temperature**



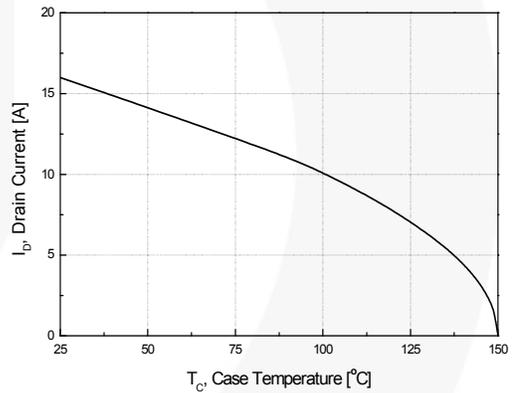
**Figure 8. On-Resistance Variation vs. Temperature**



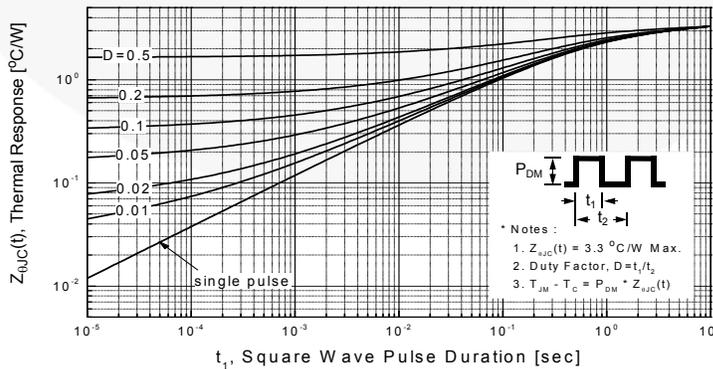
**Figure 9. Maximum Safe Operating Area**

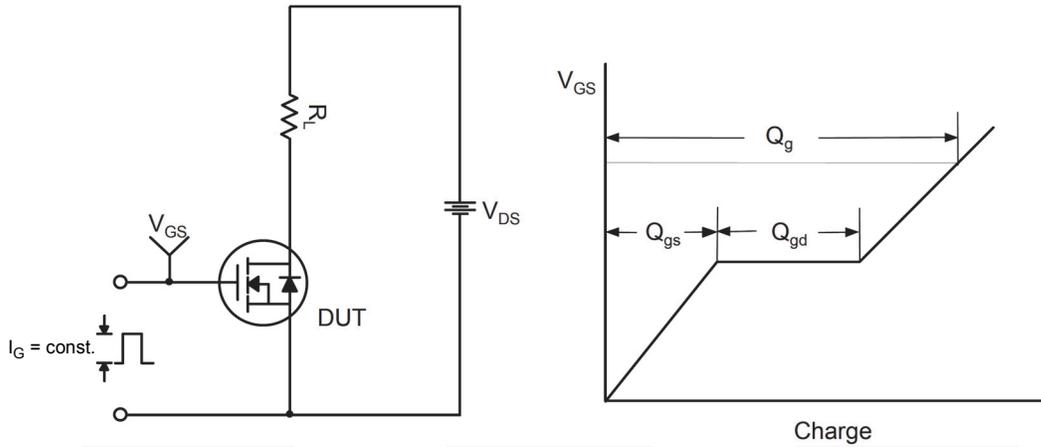


**Figure 10. Maximum Drain Current vs. Case Temperature**

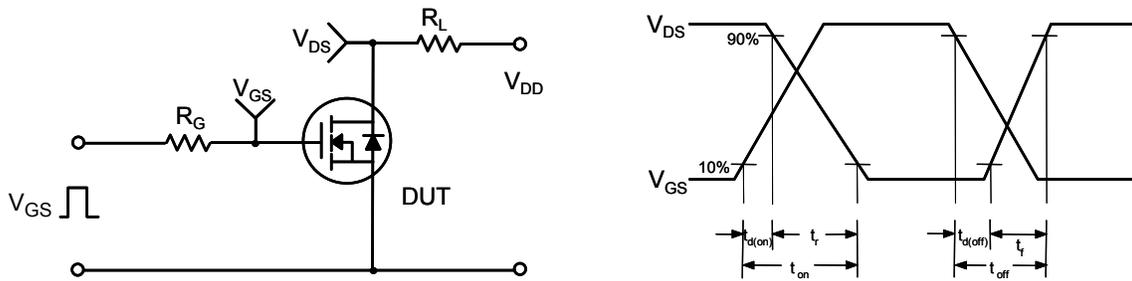


**Figure 11. Transient Thermal Response Curve**

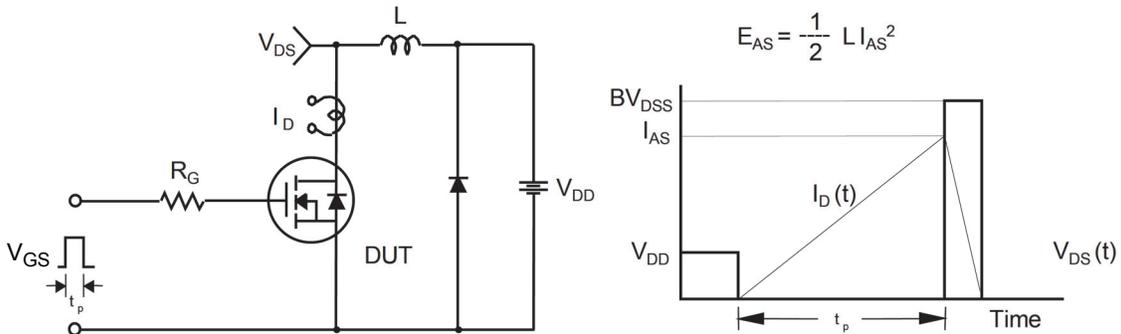




**Figure 12. Gate Charge Test Circuit & Waveform**



**Figure 13. Resistive Switching Test Circuit & Waveforms**



**Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms**

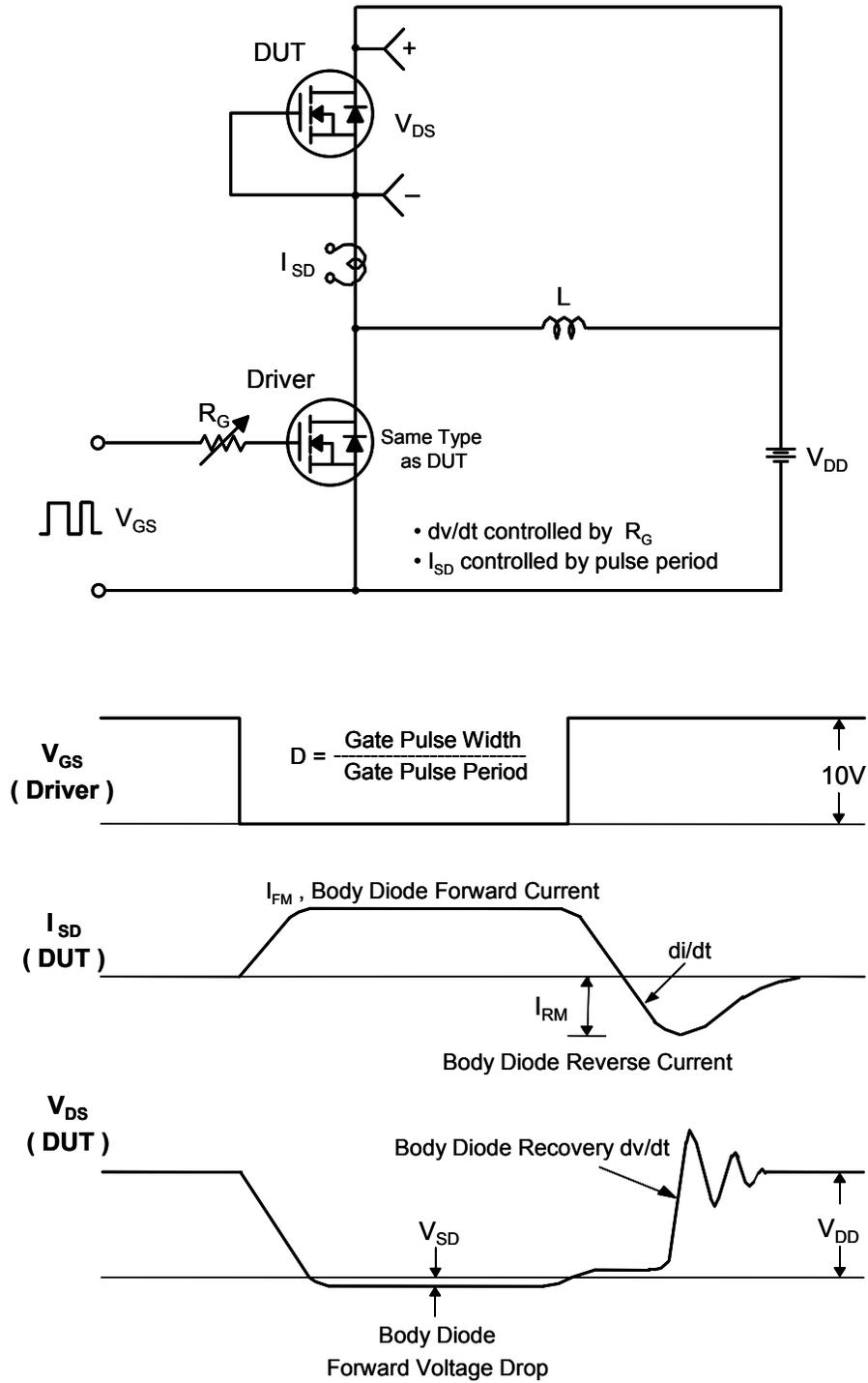
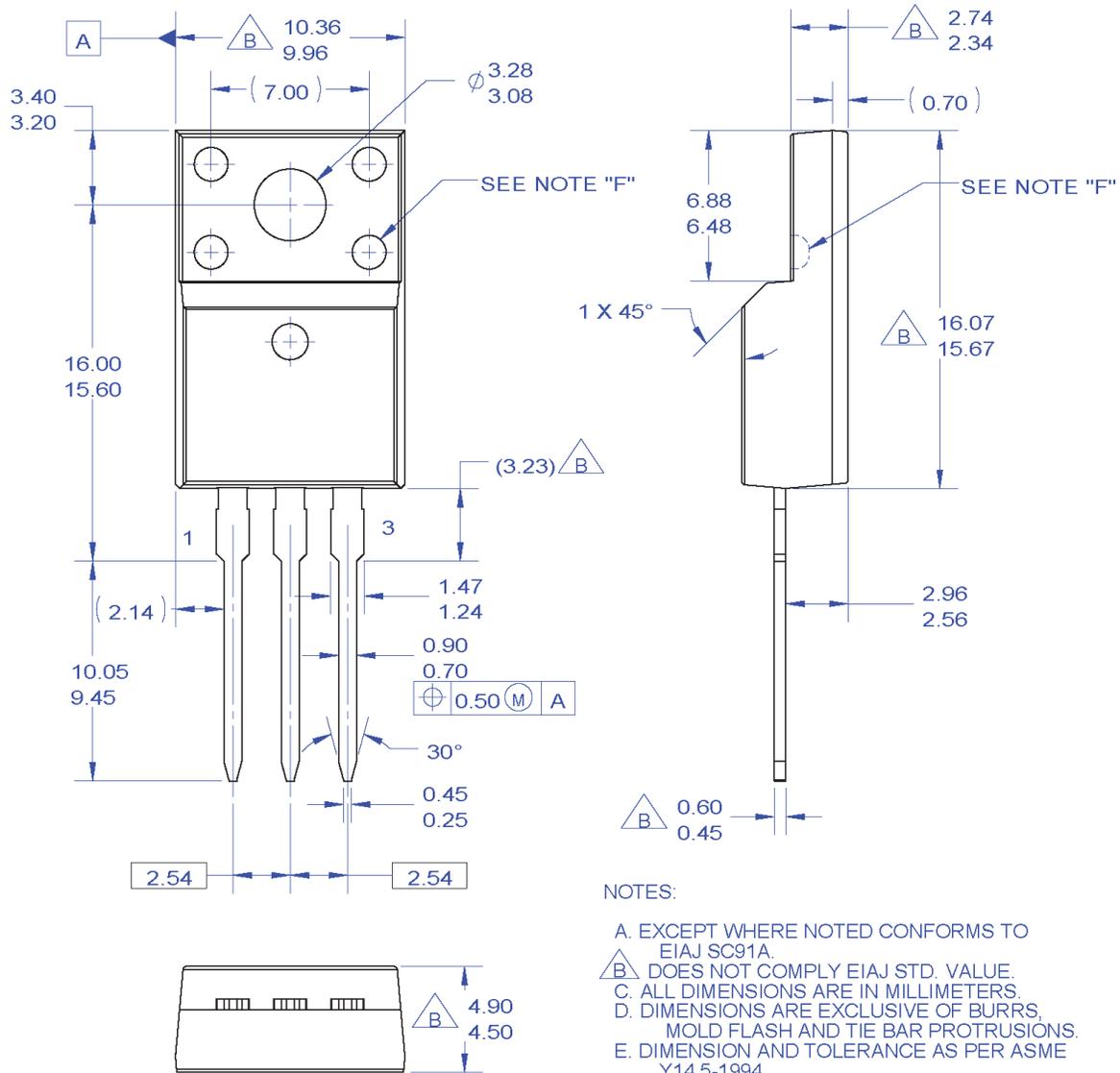


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



### NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.  
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3

**Figure 17. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead**

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| BitSiC™                  | Global Power ResourceSM | Programmable Active Droop™                      | TinyBoost®       |
| Build it Now™            | GreenBridge™            | QFET®   | TinyBuck®        |
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| EfficientMax™            | MicroPak2™              | MotionMax™                                      | TRUECURRENT®*    |
| ESBC™                    | mWSaver®                | OPTOLOGIC®                                      | µSerDes™         |
| <b>F</b> ®               | OPTOPLANAR®             | STEALTH™  | UHC®             |
| Fairchild®               | SPM®                    | SuperFET®                                       | Ultra FRFET™     |
| Fairchild Semiconductor® | SPM®                    | SuperSOT™-3                                     | UniFET™          |
| FACT Quiet Series™       | SPM®                    | SuperSOT™-6                                     | VCX™             |
| FACT®                    | SPM®                    | SuperSOT™-8                                     | VisualMax™       |
| FAST®                    | SPM®                    | SupreMOS®                                       | VoltagePlus™     |
| FastvCore™               | SPM®                    | SyncFET™  | XS™              |
| FETBench™                | SPM®                    |   |                  |
| FPS™                     | SPM®                    |   |                  |

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