3.3 V FULL-DUPLEX RS-485 DRIVERS AND RECEIVERS

Check for Samples: SN65HVD30 – SN65HVD35

FEATURES

- **1/8 Unit-Load Option Available (Up to 256 Nodes on the Bus)**
- **Bus-Pin ESD Protection Exceeds 15 kV HBM**
- **Optional Driver Output Transition Times for Signaling Rates(1) of 1 Mbps, 5 Mbps and 26 Mbps**
- **Low-Current Standby Mode: < 1 μA**
- **Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications**
- **5-V Tolerant Inputs**
- **Bus Idle, Open, and Short Circuit Failsafe**
- **Driver Current Limiting and Thermal Shutdown**
- **Designed for RS-422 and RS-485 Networks**
- **5-V Devices available, SN65HVD50-55**

(1) Line Signaling Rate is the number of voltage transitions made per second expressed in units of bps (bits per second).

APPLICATIONS

- **Utility Meters**
- **DTE/DCE Interfaces**
- **Industrial, Process, and Building Automation**
- **Point-of-Sale (POS) Terminals and Networks**

DESCRIPTION

The SN65HVD3X devices are 3-state differential line drivers and differential-input line receivers that operate with 3.3-V power supply.

Each driver and receiver has separate input and output pins for full-duplex bus communication designs. They are designed for RS-422 and RS-485 data transmission over cable lengths of up to 1500 meters.

The SN65HVD30, SN65HVD31, and SN65HVD32 are fully enabled with no external enabling pins.

The SN65HVD33, SN65HVD34, and SN65HVD35 have active-high driver enables and active-low receiver enables. A low, less than 1μA, standby current can be achieved by disabling both the driver and receiver.

All devices are characterized for ambient temperatures from –40°C to 85°C. Low power dissipation allows operation at temperatures up to 105°C or 125°C, depending on package option.

IMPROVED REPLACEMENT FOR:

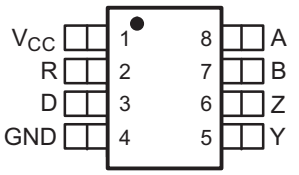
Part Number	Replace with	
xxx3491 xxx3490	SN65HVD33: SN65HVD30:	Better ESD protection (15kV vs 2kV or not specified) Higher Signaling Rate (26Mbps vs 20Mbps) Fractional Unit Load (64 Nodes vs 32)
MAX3491E MAX3490E	SN65HVD33: SN65HVD30:	Higher Signaling Rate (26Mbps vs 12Mbps) Fractional Unit Load (64 Nodes vs 32)
MAX3076E MAX3077E	SN65HVD33: SN65HVD30:	Higher Signaling Rate (26Mbps vs 16Mbps) Lower Standby Current (1 μA vs 10 μA)
MAX3073E MAX3074E	SN65HVD34: SN65HVD31:	Higher Signaling Rate (5Mbps vs 500kbps) Lower Standby Current (1 μA vs 10 μA)
MAX3070E MAX3071E	SN65HVD35: SN65HVD32:	Higher Signaling Rate (1Mbps vs 250kbps) Lower Standby Current (1 μA vs 10 μA)

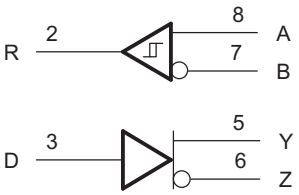
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SN65HVD30, SN65HVD31, SN65HVD32

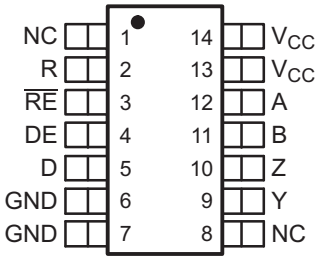
D PACKAGE (TOP VIEW)



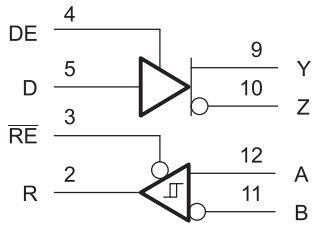


SN65HVD33, SN65HVD34, SN65HVD35

D PACKAGE (TOP VIEW)

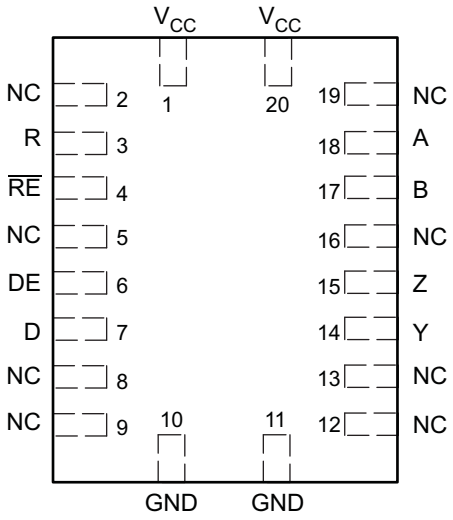


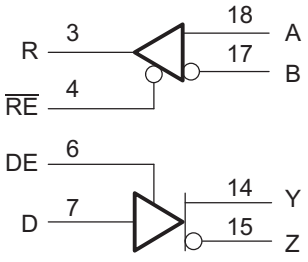
NC - No internal connection
Pins 6 and 7 are connected together internally
Pins 13 and 14 are connected together internally



SN65HVD33

RHL PACKAGE (TOP VIEW)





NC - No internal connection
Pins 10 and 11 are connected together internally
Pins 1 and 20 are connected together internally

AVAILABLE OPTIONS

SIGNALING RATE	UNIT LOADS	ENABLES	BASE PART NUMBER	SOIC MARKING
26 Mbps	1/2	No	SN65HVD30	VP30
5 Mbps	1/8	No	SN65HVD31	VP31
1 Mbps	1/8	No	SN65HVD32	VP32
26 Mbps	1/2	Yes	SN65HVD33	65HVD33
5 Mbps	1/8	Yes	SN65HVD34	65HVD34
1 Mbps	1/8	Yes	SN65HVD35	65HVD35

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1) (2)

		UNIT
V_{CC}	Supply voltage range	–0.3 V to 6 V
$V_{(A)}$, $V_{(B)}$, $V_{(Y)}$, $V_{(Z)}$	Voltage range at any bus terminal (A, B, Y, Z)	–9 V to 14 V
$V_{(TRANS)}$	Voltage input, transient pulse through 100 Ω. See Figure 12 (A, B, Y, Z)(3)	–50 to 50 V
V_I	Input voltage range (D, DE, $\overline{RE}$)	-0.5 V to 7 V
I_O	Output current (receiver output only, R)	11 mA

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) This tests survivability only and the output state of the receiver is not specified.

DISSIPATION RATINGS

PACKAGE	JEDEC THERMAL MODEL	T_A < 25°C RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C RATING	T_A = 105°C RATING	T_A = 125°C RATING
SOIC (D) 8 pin	Low k	625 mW	5 mW/°C	325 mW		
	High k	1000 mW	8 mW/°C	520 mW	360 mW	
SOIC (D) 14 pin	Low k	765 mW	6.1 mW/°C	400 mW	275 mW	
	High k	1350 mW	10.8 mW/°C	705 mW	485 mW	270 mW
QFN (RHL) 20 pin	High k	1710 mW	13.7 mW/°C	890 mW	6150 mW	340 mW

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		3.6	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–7 (1)		12	V
$1/t_{UI}$	Signaling rate	SN65HVD30, SN65HVD33			26	Mbps
		SN65HVD31, SN65HVD34			5	Mbps
		SN65HVD32, SN65HVD35			1	Mbps
R_L	Differential load resistance		54	60		Ω
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_{OH}	High-level output current	Driver	–60			mA
		Receiver	–8			mA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	mA
T_J	Junction temperature		–40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ELECTROSTATIC DISCHARGE PROTECTION

PARAMETER	TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
Human body model	Bus terminals and GND		±16		kV
Human body model (2)	All pins		±4		kV
Charged-device-model (3)	All pins		±1		kV

(1) All typical values at 25°C with 3.3-V supply.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(3) Tested in accordance with JEDEC Standard 22, Test Method C101.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$V_{I(K)}$	Input clamp voltage		I_I = –18 mA		–1.5			V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage		I_O = 0		2.5		V_{CC}	V
			R_L = 54 Ω, See Figure 1 (RS-485)		1.5	2		
			R_L = 100 Ω, See Figure 1 ,(2) (RS-422)		2	2.3		
			V_{test} = –7 V to 12 V, See Figure 2		1.5			
$\Delta\|V_{OD(SS)}\|$	Change in magnitude of steady-state differential output voltage between states		R_L = 54 Ω, See Figure 1 and Figure 2		–0.2		0.2	V
$V_{OD(RING)}$	Differential Output Voltage overshoot and undershoot		R_L = 54 Ω, C_L = 50 pF, See Figure 5 and Figure 3				10%(3)	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	HVD30, HVD33	See Figure 4			0.5		V
		HVD31, HVD34, HVD32, HVD35				0.25		
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 4		1.6		2.3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				–0.05		0.05	
$I_{Z(Z)}$ or $I_{Y(Z)}$	High-impedance state output current	HVD30, HVD31, HVD32	V_{CC} = 0 V, V_Z or V_Y = 12 V, Other input at 0 V				90	µA
			V_{CC} = 0 V, V_Z or V_Y = –7 V, Other input at 0 V		–10			
		HVD33, HVD34, HVD35	V_{CC} = 3 V or 0 V, DE = 0 V V_Z or V_Y = 12 V	Other input at 0 V			90	
			V_{CC} = 3 V or 0 V, DE = 0 V V_Z or V_Y = –7 V		–10			
$I_{Z(S)}$ or $I_{Y(S)}$	Short Circuit output current(4)		V_Z or V_Y = –7 V	Other input at 0 V	–250		250	mA
			V_Z or V_Y = 12 V		–250		250	
I_I	Input current	D, DE			0		100	µA
$C_{(OD)}$	Differential output capacitance		V_{OD} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			16		pF

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) V_{CC} is 3.3 Vdc ± 5%
(3) 10% of the peak-to-peak differential output voltage swing, per TIA/EIA-485
(4) Under some conditions of short-circuit to negative voltages, output currents exceeding the ANSI TIA/EIA-485-A maximum current of 250 mA may occur. Continuous exposure may affect device reliability. This applies to the HVD30,HVD31,HVD33, and HVD34.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD30, HVD33	R_L = 54 Ω, C_L = 50 pF, See Figure 5	4	10	18	ns
		HVD31, HVD34		25	38	65	
		HVD32, HVD35		120	175	305	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD30, HVD33		4	9	18	ns
		HVD31, HVD34		25	38	65	
		HVD32, HVD35		120	175	305	
t_r	Differential output signal rise time	HVD30, HVD33		2.5	5	12	ns
		HVD31, HVD34		20	37	60	
		HVD32, HVD35		120	185	300	
t_f	Differential output signal fall time	HVD30, HVD33		2.5	5	12	ns
		HVD31, HVD34		20	35	60	
		HVD32, HVD35		120	180	300	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	HVD30, HVD33			0.6		ns
		HVD31, HVD34			2.0		
		HVD32, HVD35			5.1		
t_{PZH1}	Propagation delay time, high-impedance-to-high-level output	HVD33	R_L = 110 Ω, $\overline{RE}$ at 0 V, D = 3 V and S1 = Y, or D = 0 V and S1 = Z See Figure 6			45	ns
		HVD34				235	
		HVD35				490	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD33				25	ns
		HVD34				65	
		HVD35				165	
t_{PZL1}	Propagation delay time, high-impedance-to-low-level output	HVD33	R_L = 110 Ω, $\overline{RE}$ at 0 V, D = 3 V and S1 = Z, or D = 0 V and S1 = Y See Figure 7			35	ns
		HVD34				190	
		HVD35				490	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD33				30	ns
		HVD34				120	
		HVD35				290	
t_{PZH1}, t_{PZL1}	Driver enable delay with bus voltage offset		V_O= 2 V (Typ)		500	900	ns
t_{PZH2}	Propagation delay time, standby-to-high-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, D = 3 V and S1 = Y, or D = 0 V and S1 = Z See Figure 6			4000	ns
t_{PZL2}	Propagation delay time, standby-to-low-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, D = 3 V and S1 = Z, or D = 0 V and S1 = Y See Figure 7			4000	ns

(1) All typical values are at 25°C and with a 3.3-V supply.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage		I_O = –8 mA				–0.02	V
V_{IT-}	Negative-going differential input threshold voltage		I_O = 8 mA		–0.20			V
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})					50		mV
V_{IK}	Enable-input clamp voltage		I_I = –18 mA		–1.5			V
V_O	Output voltage		V_{ID} = 200 mV, I_O = –8 mA, See Figure 8		2.4			V
			V_{ID} = –200 mV, I_O = 8 mA, See Figure 8				0.4	
$I_{O(Z)}$	High-impedance-state output current		V_O = 0 or V_{CC}, $\overline{RE}$ at V_{CC}		–1		1	µA
I_A or I_B	Bus input current	HVD31, HVD32, HVD34, HVD35	V_A or V_B = 12 V	Other input at 0V		0.05	0.1	mA
			V_A or V_B = 12 V, V_{CC} = 0 V			0.06	0.1	
			V_A or V_B = -7 V		–0.10	–0.04		
			V_A or V_B = -7 V, V_{CC} = 0 V		–0.10	–0.03		
		HVD30, HVD33	V_A or V_B = 12 V	Other input at 0V		0.20	0.35	mA
			V_A or V_B = 12 V, V_{CC} = 0 V			0.24	0.4	
			V_A or V_B = -7 V		–0.35	–0.18		
			V_A or V_B = -7 V, V_{CC} = 0 V		–0.25	–0.13		
I_{IH}	Input current, $\overline{RE}$		V_{IH} = 0.8 V or 2 V		–60			µA
C_{ID}	Differential input capacitance		V_{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			15		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

SUPPLY CURRENT CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	HVD30	D at 0 V or V_{CC} and No Load			2.1	mA
		HVD31, HVD32			3.8	6.4	
		HVD33	$\overline{RE}$ at 0 V, D at 0 V or V_{CC}, DE at 0 V, No load (Receiver enabled and driver disabled)			1.8	mA
		HVD34, HVD35				2.2	
		HVD33, HVD34, HVD35	$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, No load (Receiver disabled and driver disabled)		0.022	1	µA
		HVD33	$\overline{RE}$ at 0 V, D at 0 V or V_{CC}, DE at V_{CC}, No load (Receiver enabled and driver enabled)			2.1	mA
		HVD34, HVD35				6.5	
		HVD33	$\overline{RE}$ at V_{CC}, D at 0 V or V_{CC}, DE at V_{CC} No load (Receiver disabled and driver enabled)			1.8	mA
		HVD34, HVD35				6.2	

(1) All typical values are at 25°C and with a 3.3-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD30, HVD33	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, See Figure 9			26	45	ns
		HVD31, HVD32, HVD34, HVD35				47	70	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD30, HVD33				29	45	
		HVD31, HVD32, HVD34, HVD35				49	70	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	HVD30, HVD33					7	
		HVD31, HVD34, HVD32, HVD35					10	
t_r	Output signal rise time						5	
t_f	Output signal fall time						6	
t_{PHZ}	Output disable time from high level		DE at 3 V	C_L = 15 pF, See Figure 10			20	
t_{PZH1}	Output enable time to high level						20	
t_{PZH2}	Propagation delay time, standby-to-high-level output		DE at 0 V				4000	
t_{PLZ}	Output disable time from low level		DE at 3 V	C_L = 15 pF, See Figure 11			20	
t_{PZL1}	Output enable time to low level						20	
t_{PZL2}	Propagation delay time, standby-to-low-level output		DE at 0 V				4000	

(1) All typical values are at 25°C and with a 3.3-V supply

DEVICE POWER DISSIPATION – P_D

PARAMETER				TEST CONDITIONS	VALUE	UNITS
θ_{JA}	Junction-to-Ambient Thermal Resistance		SOIC-8	JEDEC Low-K model	231	°C/W
				JEDEC High-K model	135	
			SOIC-14	JEDEC Low-K model	163	
				JEDEC High-K model	92	
			QFN-20		73	
θ_{JB}	Junction-to- Board Thermal Resistance		SOIC-8		44	°C/W
			SOIC-14		61	
			QFN-20			
θ_{JC}	Junction-to-Case Thermal Resistance		SOIC-8		43	°C/W
			SOIC-14		59	
			QFN-20		14	
P_D	Power Dissipation Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: HVD30,33 at 25 Mbps, HVD31,34 at 5 Mbps, HVD32,35 at 1 Mbps	Typical	HVD30,33	V_{CC} = 3.3V, T_J = 25°C, R_L = 60 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver)		mW
			HVD31,34			
			HVD32,35			
		Worst-case	HVD30,33	V_{CC} = 3.6V, T_J = 140°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver)	197	mW
			HVD31,34		213	
			HVD32,35		248	
T_{SD}	Thermal Shut-down Junction Temperature				170	°C

PARAMETER MEASUREMENT INFORMATION

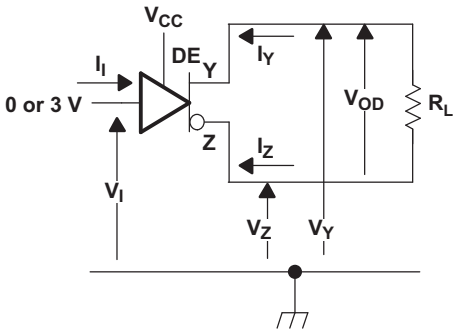


Figure 1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

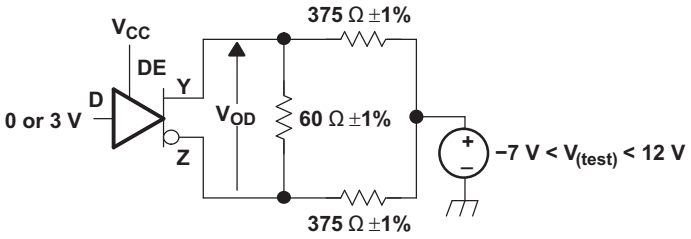


Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit

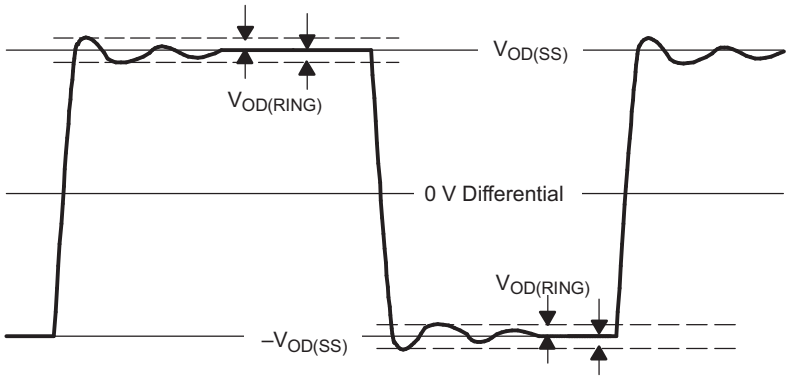
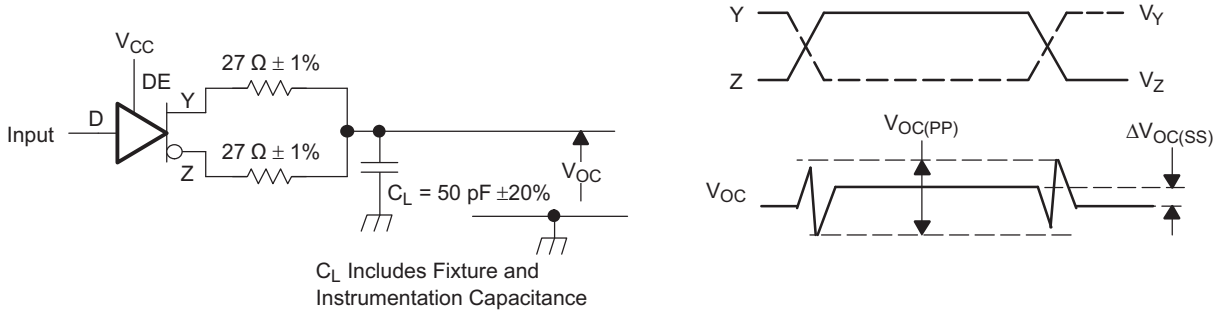


Figure 3. $V_{OD(RING)}$ Waveform and Definitions

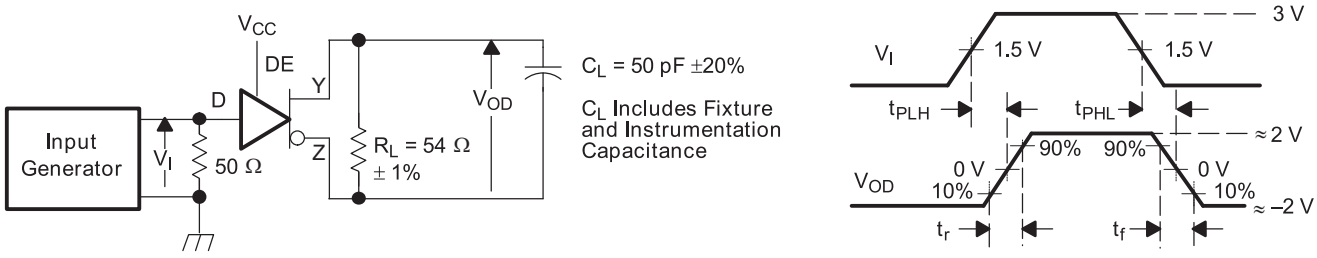
$V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

PARAMETER MEASUREMENT INFORMATION (continued)



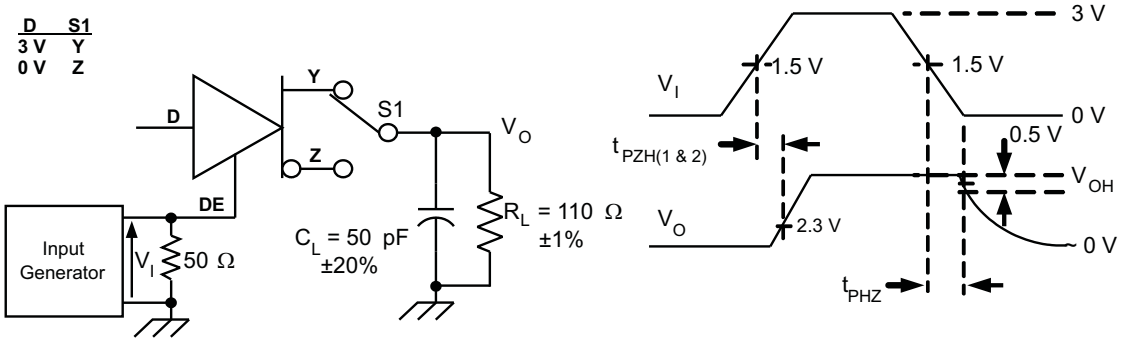
Input: PRR = 500 kHz, 50% Duty Cycle,t_r<6ns, t_f<6ns, Z_O = 50 Ω

Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

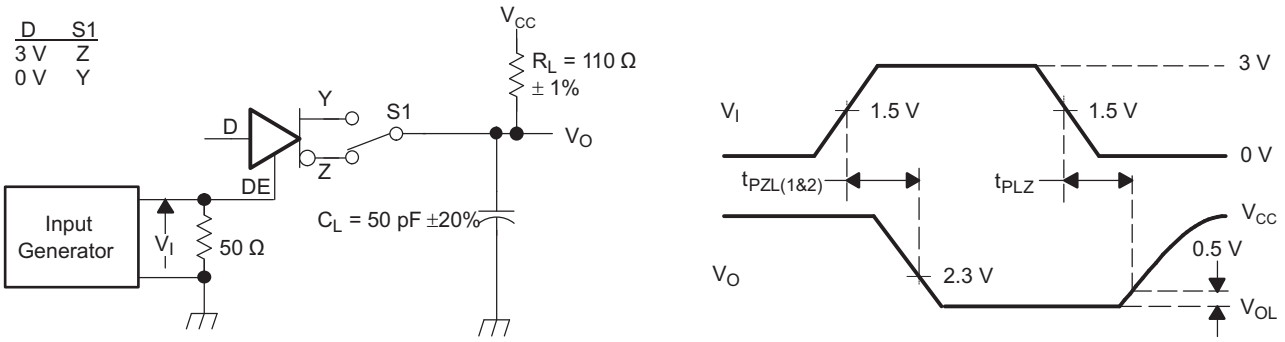
Figure 5. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 50 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_0 = 50 Ω
C_L Includes Fixture and Instrumentation Capacitance

Figure 6. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



Generator: PRR = 50 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_0 = 50 Ω

C_L Includes Fixture and Instrumentation Capacitance

Figure 7. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

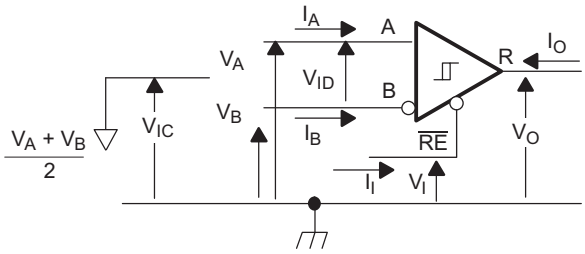
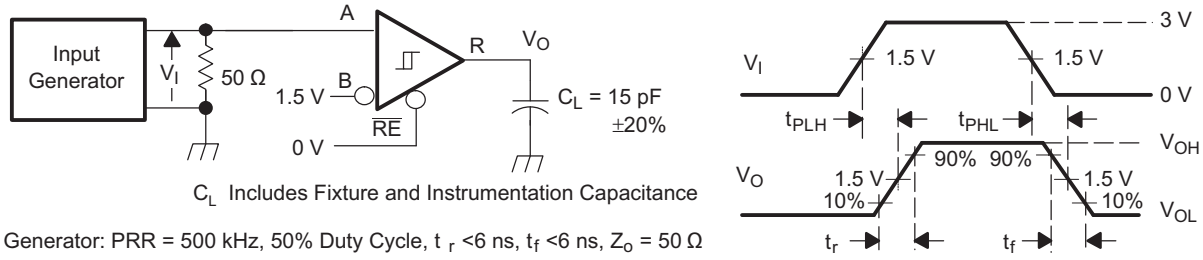


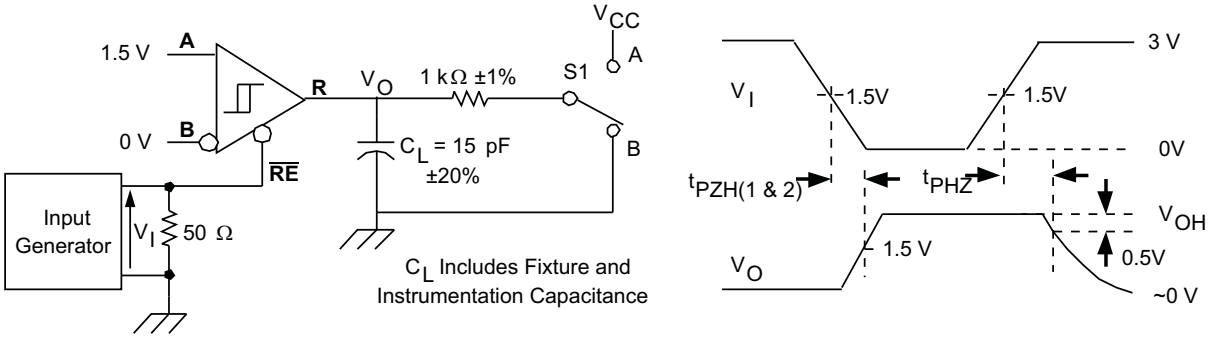
Figure 8. Receiver Voltage and Current Definitions



C_L Includes Fixture and Instrumentation Capacitance

Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

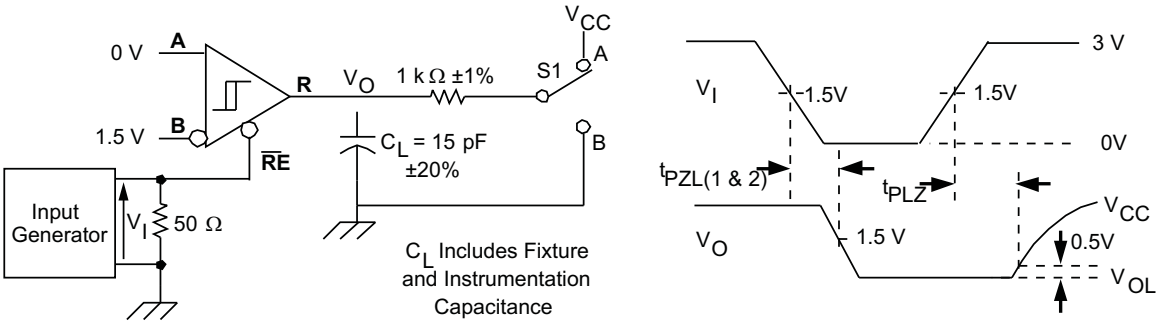
Figure 9. Receiver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 50 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_0 = 50 Ω

Figure 10. Receiver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



Generator: PRR = 50 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_0 = 50 Ω

Figure 11. Receiver Enable Time From Standby (Driver Disabled)

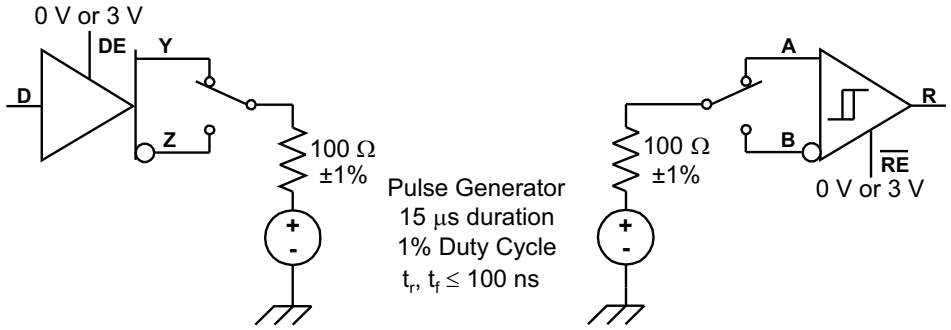


Figure 12. Test Circuit, Transient Over Voltage Test

DEVICE INFORMATION

LOW-POWER STANDBY MODE

When both the driver and receiver are disabled (DE low and $\overline{RE}$ high) the device is in standby mode. If the enable inputs are in this state for less than 60 ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

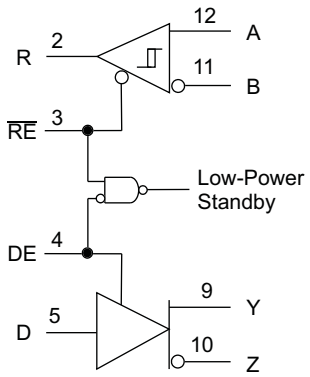


Figure 13. Low-Power Standby Logic Diagram

If only the driver is re-enabled (DE transitions to high) the driver outputs are driven according to the D input after the enable times given by t_{PZH2} and t_{PZL2} in the driver switching characteristics. If the D input is open when the driver is enabled, the driver outputs defaults to A high and B low, in accordance with the driver failsafe feature.

If only the receiver is re-enabled ($\overline{RE}$ transitions to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by t_{PZH2} and t_{PZL2} in the receiver switching characteristics. If there is no valid state on the bus the receiver responds as described in the failsafe operation section.

If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input. Note that the state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

DRIVER OUTPUT CURRENT LIMITING

The RS-485 standard (ANSI/TIA/EIA-485-A or equivalently ISO 8482) specifies a 250 mA driver output current limit to prevent damage caused by data contention on the bus. That applies in the event that two or more transceivers drive the bus to opposing states at the same time. The HVD3x family of devices includes current limiting circuitry that prevents damage under these conditions. Note that this current limit prevents damage during the bus contention, but the logic state of the bus may be indeterminate as specified by the standard, so communication errors may occur.

In a specific combination of circumstances, a condition may occur in which current through the bus pin exceeds the 250 mA limit. This combination of conditions is not normally included in RS-485 applications:

- *loading capacitance on the pin is less than 500 pF*
- *the bus pin is directly connected to a voltage more negative than –1V*
- *the device is supplied with Vcc equal or greater than 3.3V*
- *the driver is enabled*
- the bus pin is driving to the logic high state.

In these specific conditions, the normal current limit circuitry and thermal shutdown circuitry will not limit or shutdown the current flow. If the current is allowed to continue, the device will heat up in a localized area near the driver outputs, and the device may be damaged.

Typical RS-485 twisted-pair cable has capacitance of approximately 50 pF/meter. Therefore it is expected that 10 meters of cable would provide sufficient capacitance to prevent this latch-up condition.

The –7 to +12V common mode range specified by RS-485 is intended to allow communication between transceivers separated by significant distances, when ground offsets may occur due to temporary current surges, electrical noise, etc. In those circumstances, the inherent cable needed to connect separated transceivers will ensure that the conditions above do not occur. For transceiver separated by only a short cable length, or backplane applications, it would be unusual for there to be a steady-state negative common-mode voltage. It is possible for a negative power supply to be shorted to the bus lines due to mis-wiring or cable damage, however, this is a different root cause fault, and robust devices such as the HVD178x family should be used for surviving power supply or mis-wiring faults.

The 250 mA current limit in the RS-485 standard is intended to prevent damage caused by data contention on the bus; that is, in the event that two or more transceivers drive the bus to different states at the same time. These devices will not be damaged under these conditions, because all RS-485 drivers have output impedance sufficient to prevent the direct connection condition stated above. Typical RS-485 driver output impedance is on the order of 10 to 30 Ω.

HOT-PLUGGING

These devices are designed to operate in *hot swap* or *hot pluggable* applications. Key features for hot-pluggable applications are power-up, power-down glitch-free operation, default disabled input/output pins, and receiver failsafe. As shown in Figure 24, an internal Power-On Reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious bits are transmitted on the bus pin outputs as the power supply turns on or turns off.

As shown in the device FUNCTION TABLES, the enable inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

RECEIVER FAILSAFE

The differential receiver is *failsafe* to invalid bus states caused by open bus conditions such as, a disconnected connector, shorted bus conditions caused by damaged cabling, or idle bus conditions that occur when no driver is actively driving a valid RD-485 bus state on the network. In any of these cases, the differential receiver will output a failsafe HIGH state, so that small noise signals do not cause spurious transitions at the receiver output.

SAFE OPERATION WITH BUS CONTENTION

These devices incorporate a driver current limit of 250 mA across the RS-485 common-mode range of –7 V to +12 V. As stated in the *"Application Guidelines for TIA/EIA-485-A"* (1) this sets a practical limitation to prevent damage during bus contention events. Contention can occur during system initialization, during system faults, or whenever two or more drivers are active at the same time.

Figure 14 shows a 2-node system to demonstrate bus contention by forcing both drivers to be active in opposing states.

(1) TIA/EIA Telecommunications System Bulletin TSB89, "Application Guidelines for TIA/EIA-485-A"

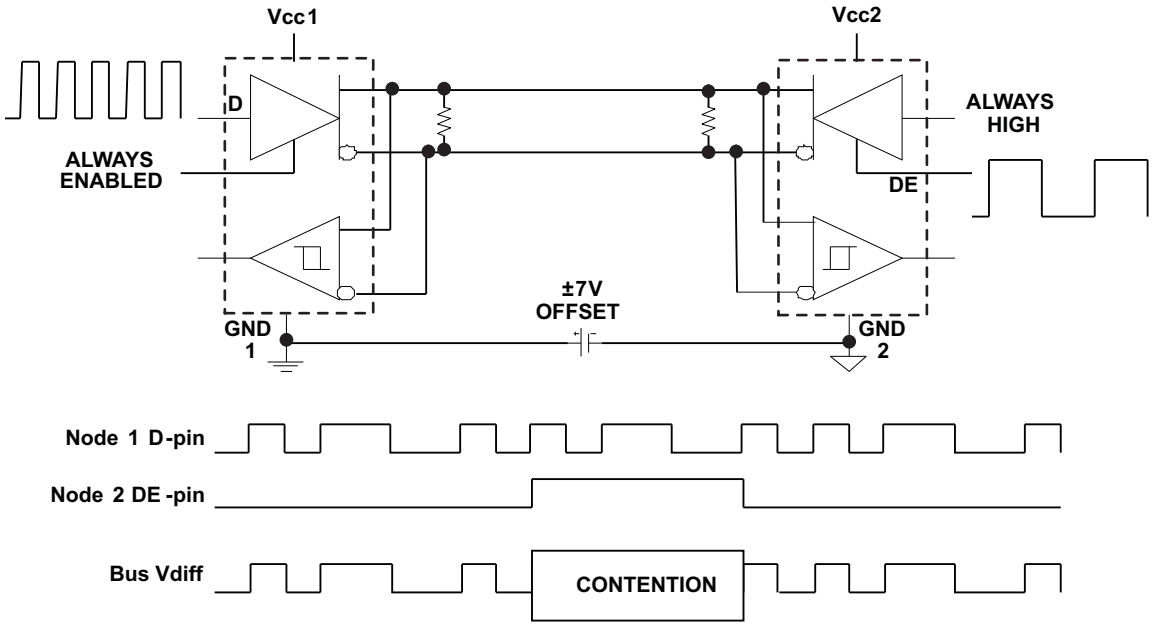


Figure 14. Bus Contention Example

Figure 15 shows typical operation in a bus contention event. The bottom trace illustrates how the SN65HVD33 at Node 1 continues normal operation after a contention event between the two drivers, with a –7 V ground offset on Node 2. This illustrates how the HVD3x family of devices operates robustly in spite of bus contention faults, even with large common-mode offsets.

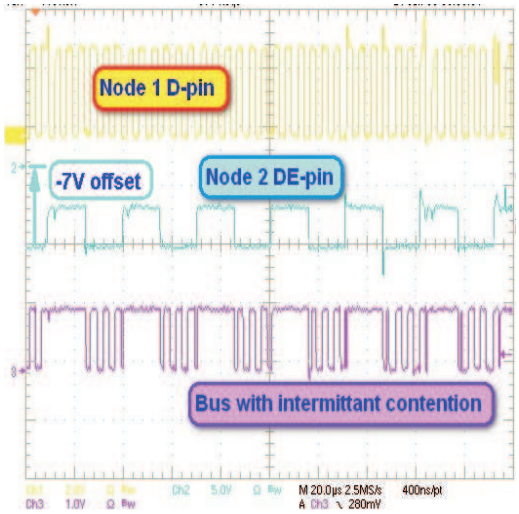


Figure 15. HVD3x Drivers Operate Correctly After Bus Contention Faults

FUNCTION TABLES

Table 1. SN65HVD33, SN65HVD34, SN65HVD35 DRIVER

INPUTS		OUTPUTS	
D	**DE**	**Y**	**Z**
H	H	H	L
L	H	L	H
X	L or open	Z	Z
Open	H	L	H

Table 2. SN65HVD33, SN65HVD34, SN65HVD35 RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \leq -0.2$ V	L	L
-0.2 V $< V_{ID} < -0.02$ V	L	?
-0.02 V $\leq V_{ID}$	L	H
X	H or open	Z
Open Circuit	L	H
Idle circuit	L	H
Short Circuit, $V_{(A)} = V_{(B)}$	L	H

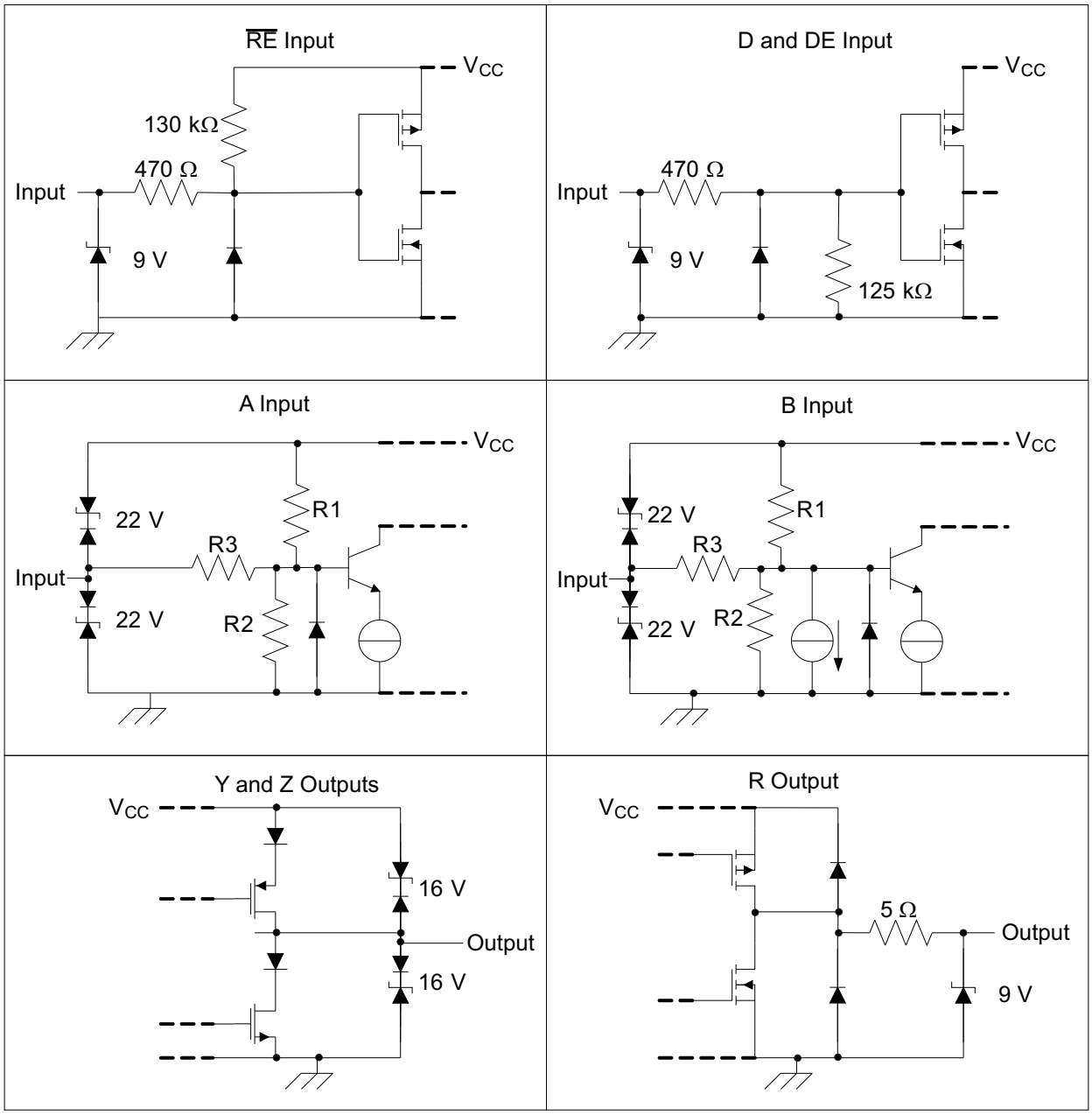
Table 3. SN65HVD30, SN65HVD31, SN65HVD32 DRIVER

	OUTPUTS	
INPUT D	**Y**	**Z**
H	H	L
L	L	H
Open	L	H

Table 4. SN65HVD30, SN65HVD31, SN65HVD32 RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	OUTPUT R
$V_{ID} \leq -0.2$ V	L
-0.2 V $< V_{ID} < -0.02$ V	?
-0.02 V $\leq V_{ID}$	H
Open Circuit	H
Idle circuit	H
Short Circuit, $V_{(A)} = V_{(B)}$	H

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
SN65HVD30, SN65HVD33	9 kΩ	45 kΩ
SN65HVD31, SN65HVD32, SN65HVD34, SN65HVD35	36 kΩ	180 kΩ

TYPICAL CHARACTERISTICS

HVD30, HVD33
RMS SUPPLY CURRENT
vs
SIGNALING RATE

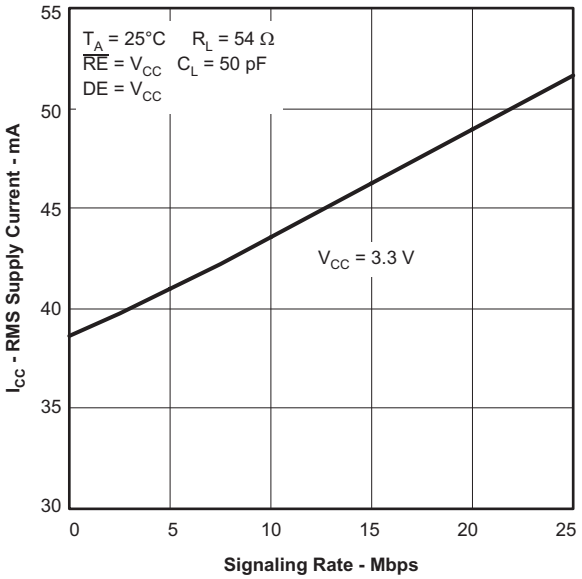


Figure 16.

HVD31, HVD34
RMS SUPPLY CURRENT
vs
SIGNALING RATE

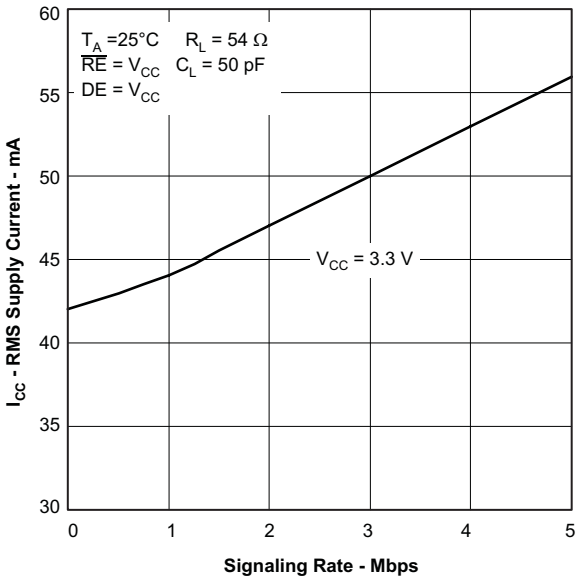


Figure 17.

HVD32, HVD35
RMS SUPPLY CURRENT
vs
SIGNALING RATE

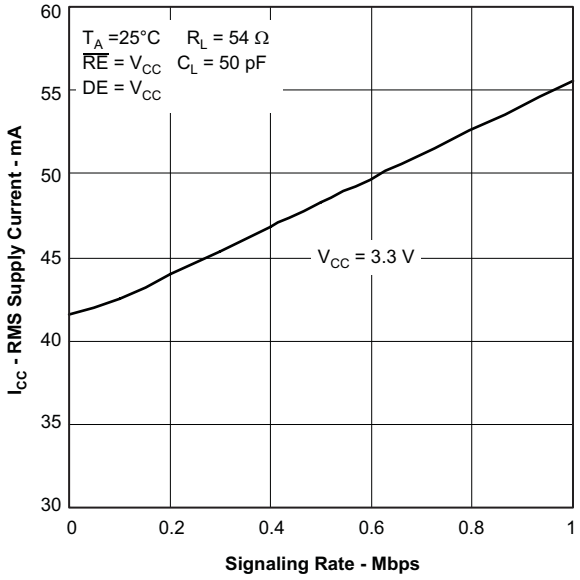


Figure 18.

TYPICAL CHARACTERISTICS (continued)

HVD30, HVD33
BUS INPUT CURRENT
vs
INPUT VOLTAGE

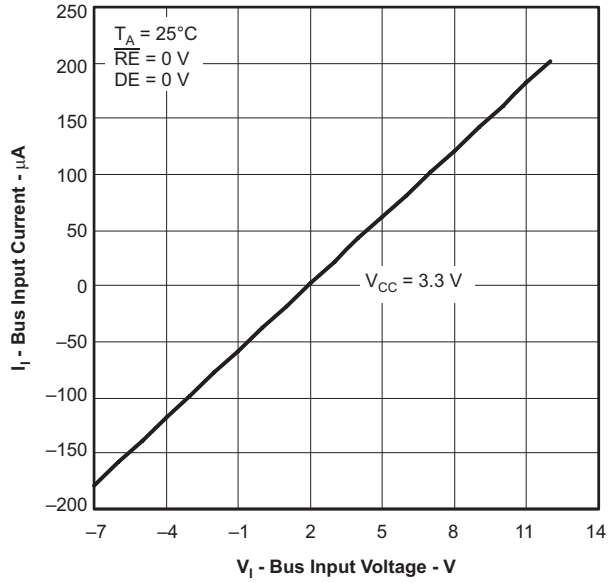


Figure 19.

HVD31, HVD32, HVD34, HVD35
BUS INPUT CURRENT
vs
INPUT VOLTAGE

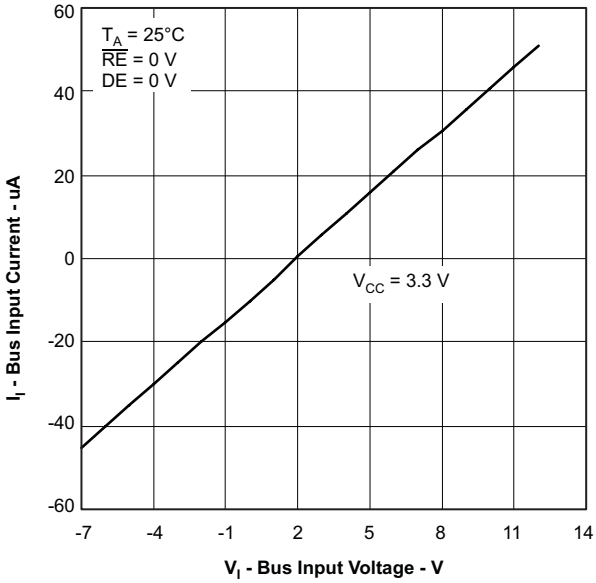


Figure 20.

DRIVER OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

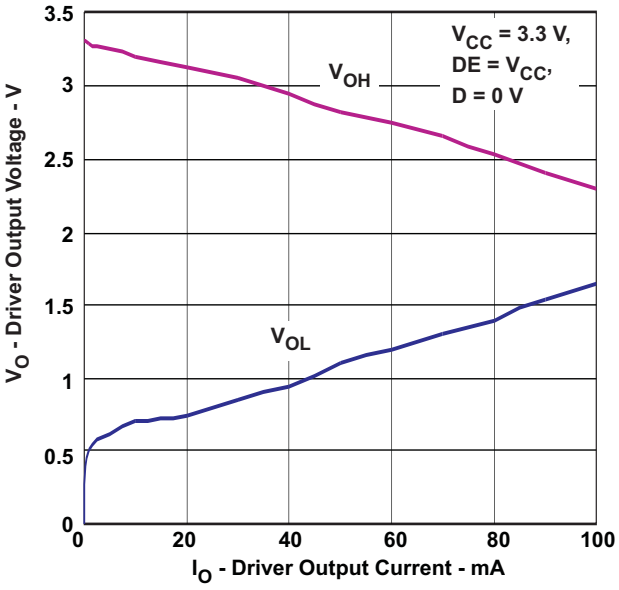


Figure 21.

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

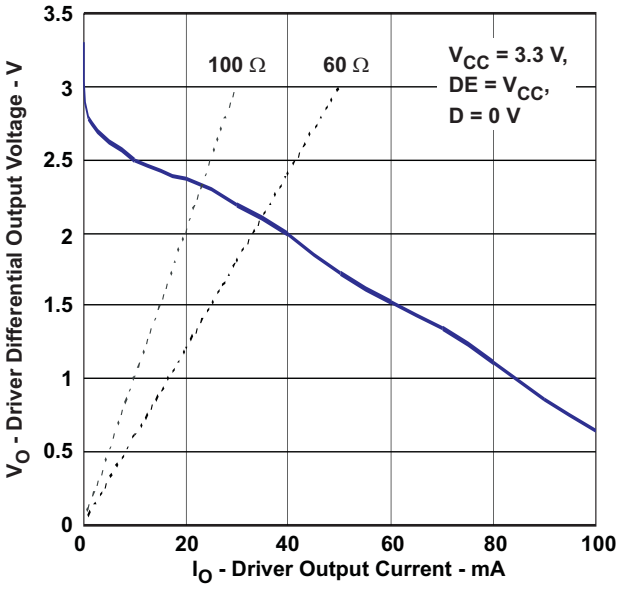


Figure 22.

TYPICAL CHARACTERISTICS (continued)

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

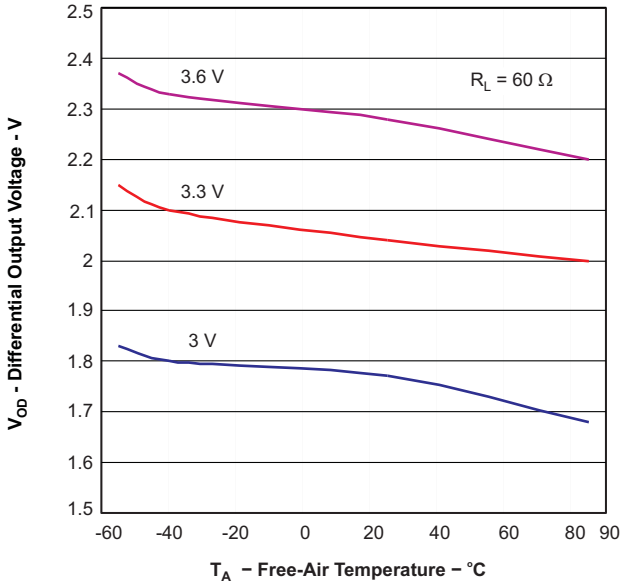


Figure 23.

DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE

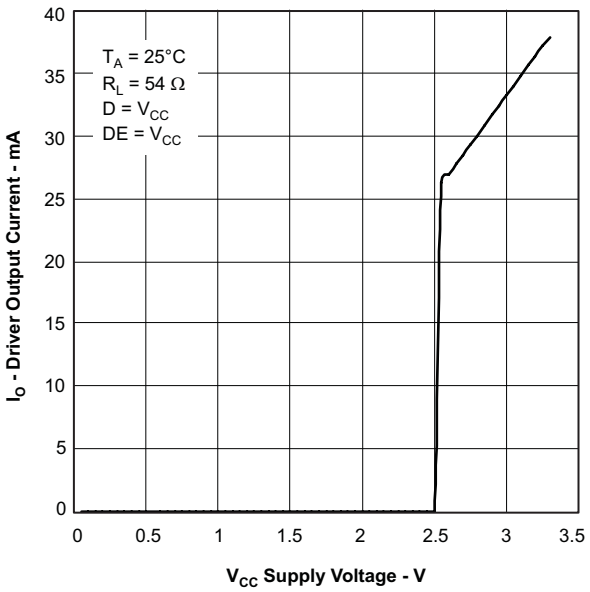


Figure 24.

HVD30, HVD33 DRIVER PROPAGATION DELAY vs FREE-AIR TEMPERATURE

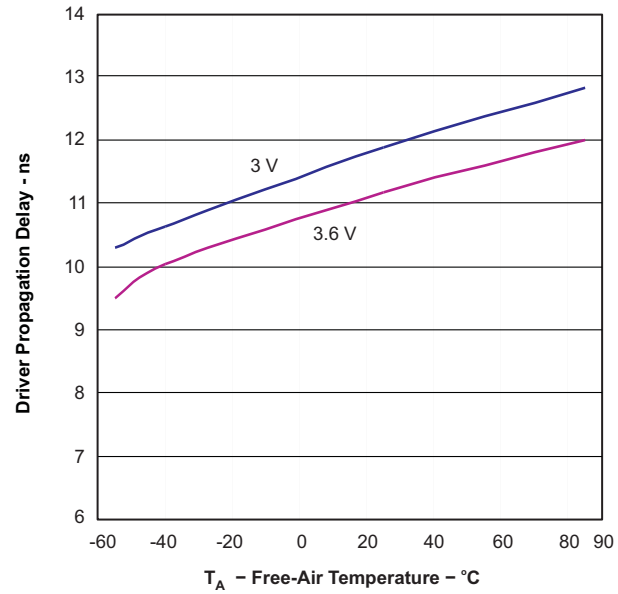


Figure 25.

HVD30, HVD33 DRIVER RISE/FALL TIME vs FREE-AIR TEMPERATURE

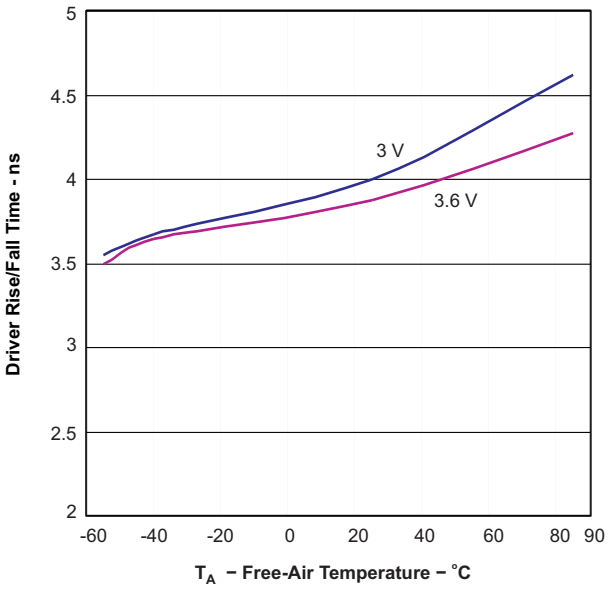


Figure 26.

TYPICAL CHARACTERISTICS (continued)

RECEIVER THRESHOLD vs AMBIENT TEMPERATURE

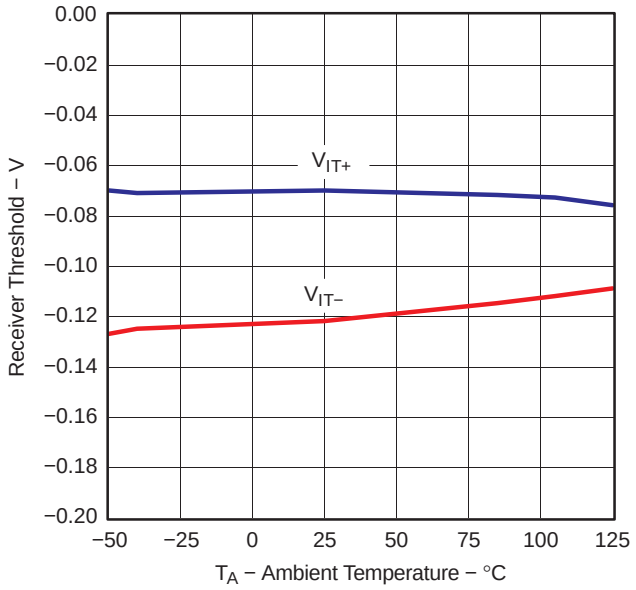


Figure 27.

RECEIVER THRESHOLD vs COMMON-MODE VOLTAGE

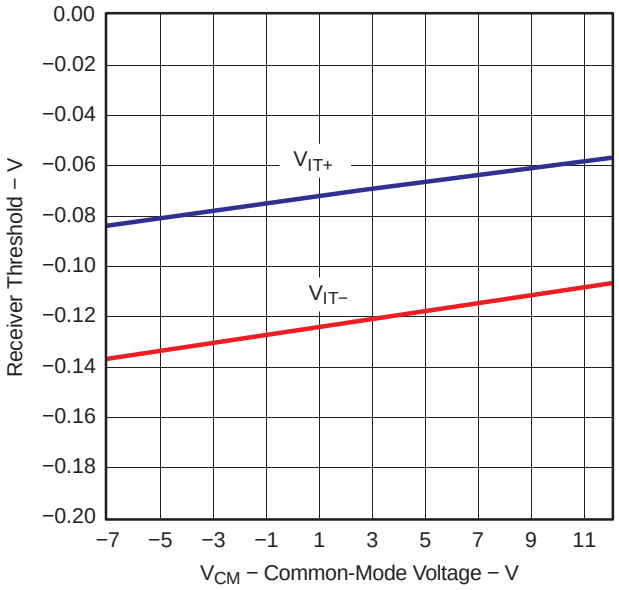


Figure 28.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

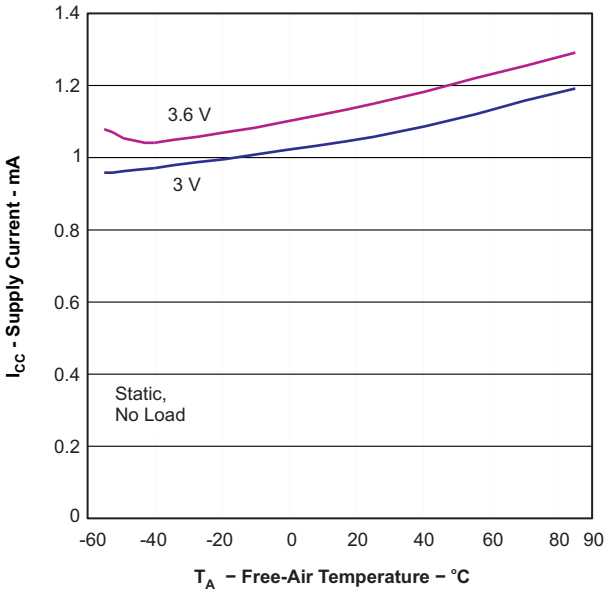


Figure 29.

ENABLE TIME vs COMMON-MODE VOLTAGE (SEE Figure 31)

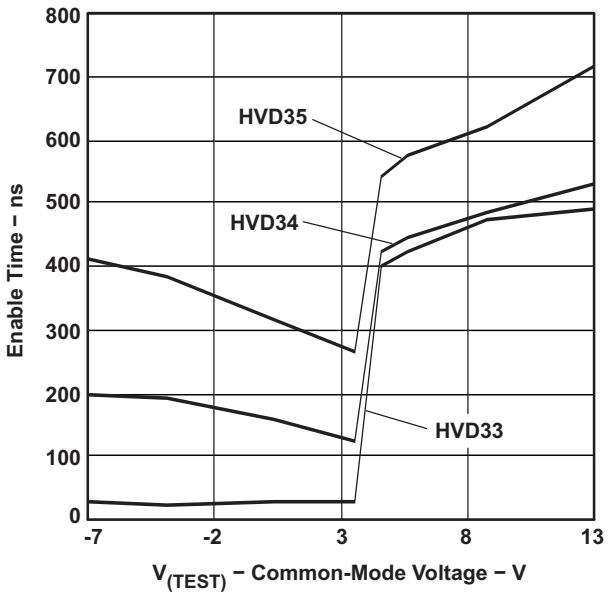


Figure 30.

TYPICAL CHARACTERISTICS (continued)

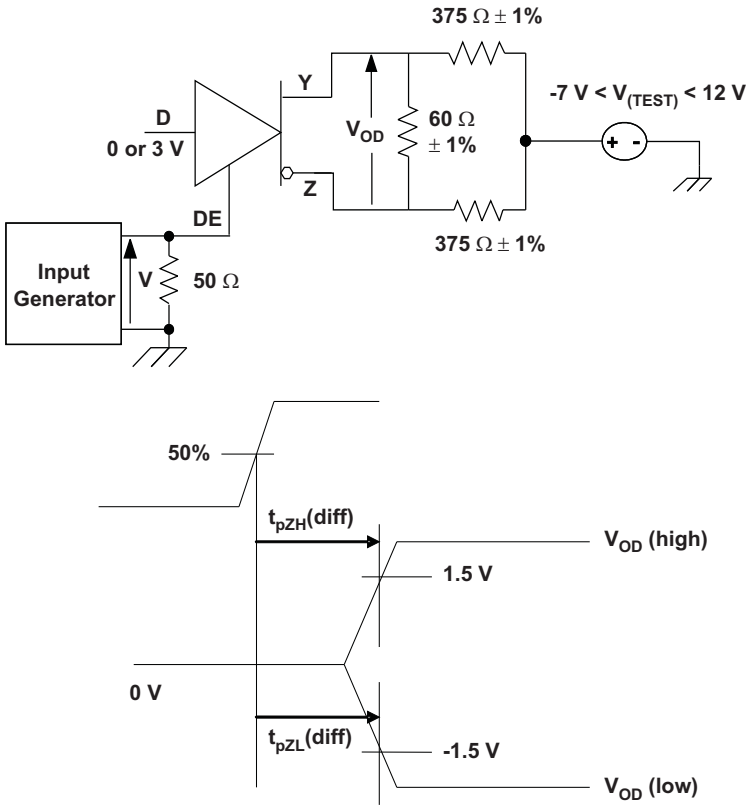


Figure 31. Driver Enable Time From DE to V_{OD}

The time $t_{pZL}(x)$ is the measure from DE to $V_{OD}(x)$. V_{OD} is valid when it is greater than 1.5 V.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65HVD30D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP30	Samples
SN65HVD30DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP30	Samples
SN65HVD30DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP30	Samples
SN65HVD30DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP30	Samples
SN65HVD31D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		VP31	Samples
SN65HVD31DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		VP31	Samples
SN65HVD31DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		VP31	Samples
SN65HVD31DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		VP31	Samples
SN65HVD32D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		VP32	Samples
SN65HVD32DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		VP32	Samples
SN65HVD32DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		VP32	Samples
SN65HVD32DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		VP32	Samples
SN65HVD33D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD33	Samples
SN65HVD33DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD33	Samples
SN65HVD33DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD33	Samples
SN65HVD33DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD33	Samples
SN65HVD33RHLR	ACTIVE	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65HVD33	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65HVD33RHLT	ACTIVE	QFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65HVD33	Samples
SN65HVD34D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD34	Samples
SN65HVD34DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD34	Samples
SN65HVD34DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD34	Samples
SN65HVD34DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD34	Samples
SN65HVD35D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD35	Samples
SN65HVD35DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD35	Samples
SN65HVD35DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD35	Samples
SN65HVD35DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65HVD35	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

OTHER QUALIFIED VERSIONS OF SN65HVD30, SN65HVD33 :

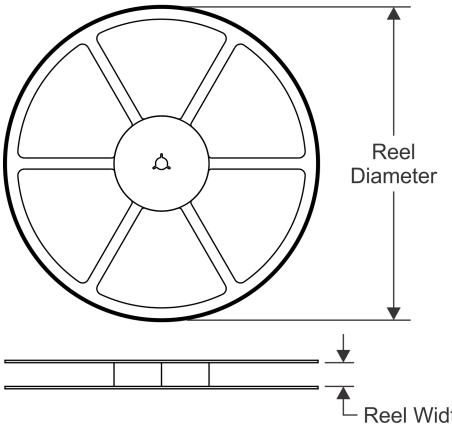
- Enhanced Product: SN65HVD30-EP, SN65HVD33-EP

NOTE: Qualified Version Definitions:

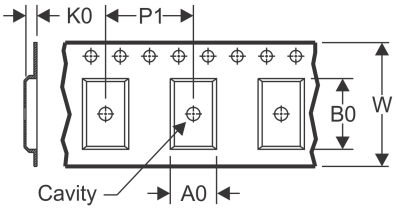
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

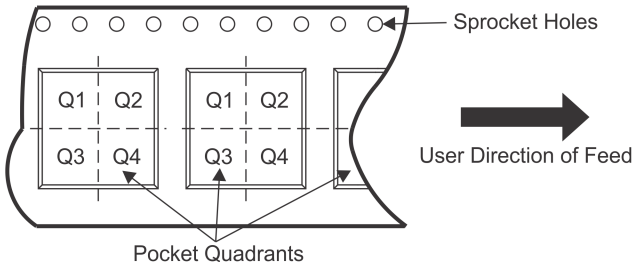


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

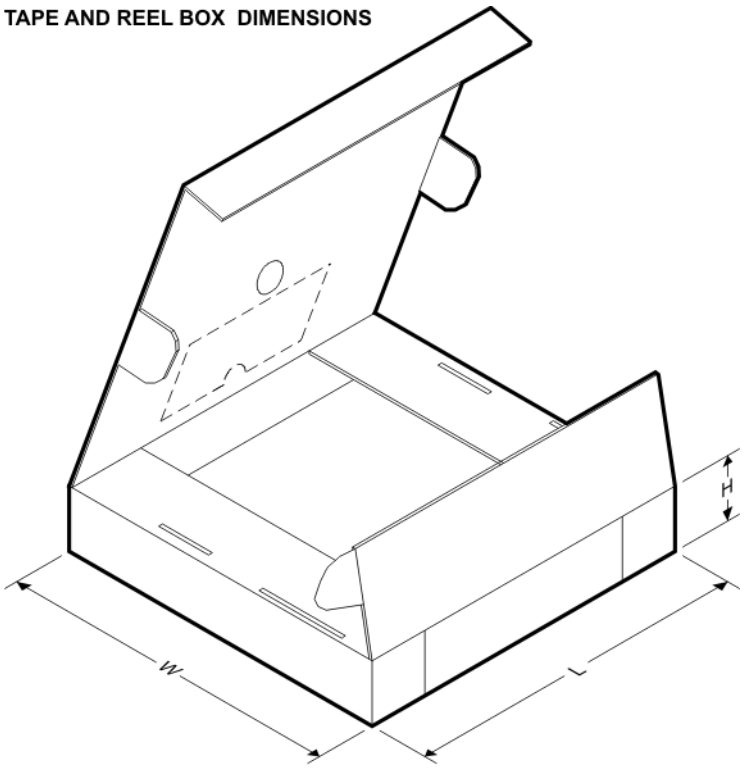
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD30DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD31DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD32DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD33RHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN65HVD33RHLT	QFN	RHL	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN65HVD34DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD35DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

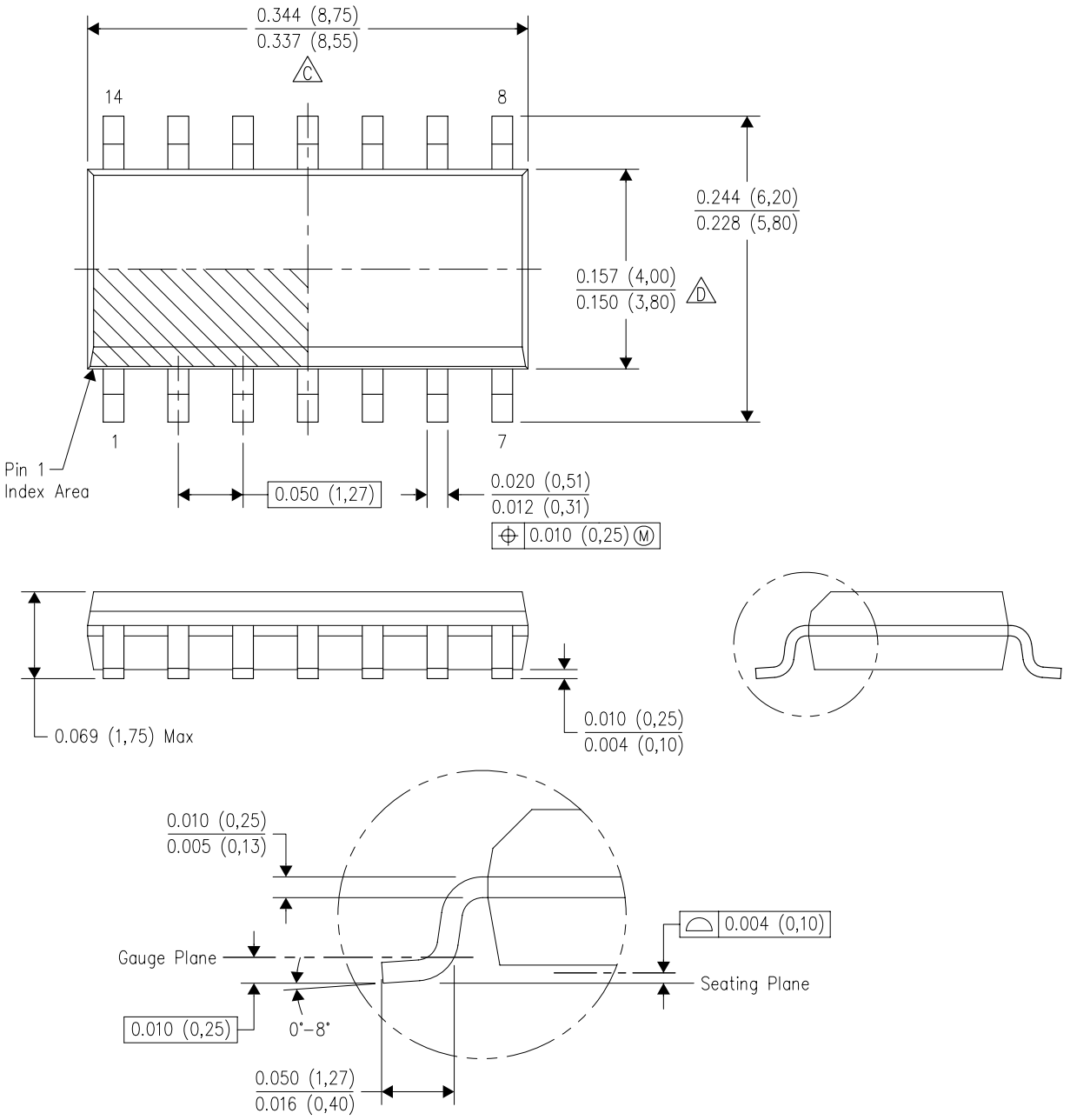
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD30DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD31DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD32DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD33RHLR	QFN	RHL	20	3000	367.0	367.0	35.0
SN65HVD33RHLT	QFN	RHL	20	250	210.0	185.0	35.0
SN65HVD34DR	SOIC	D	14	2500	367.0	367.0	38.0
SN65HVD35DR	SOIC	D	14	2500	367.0	367.0	38.0

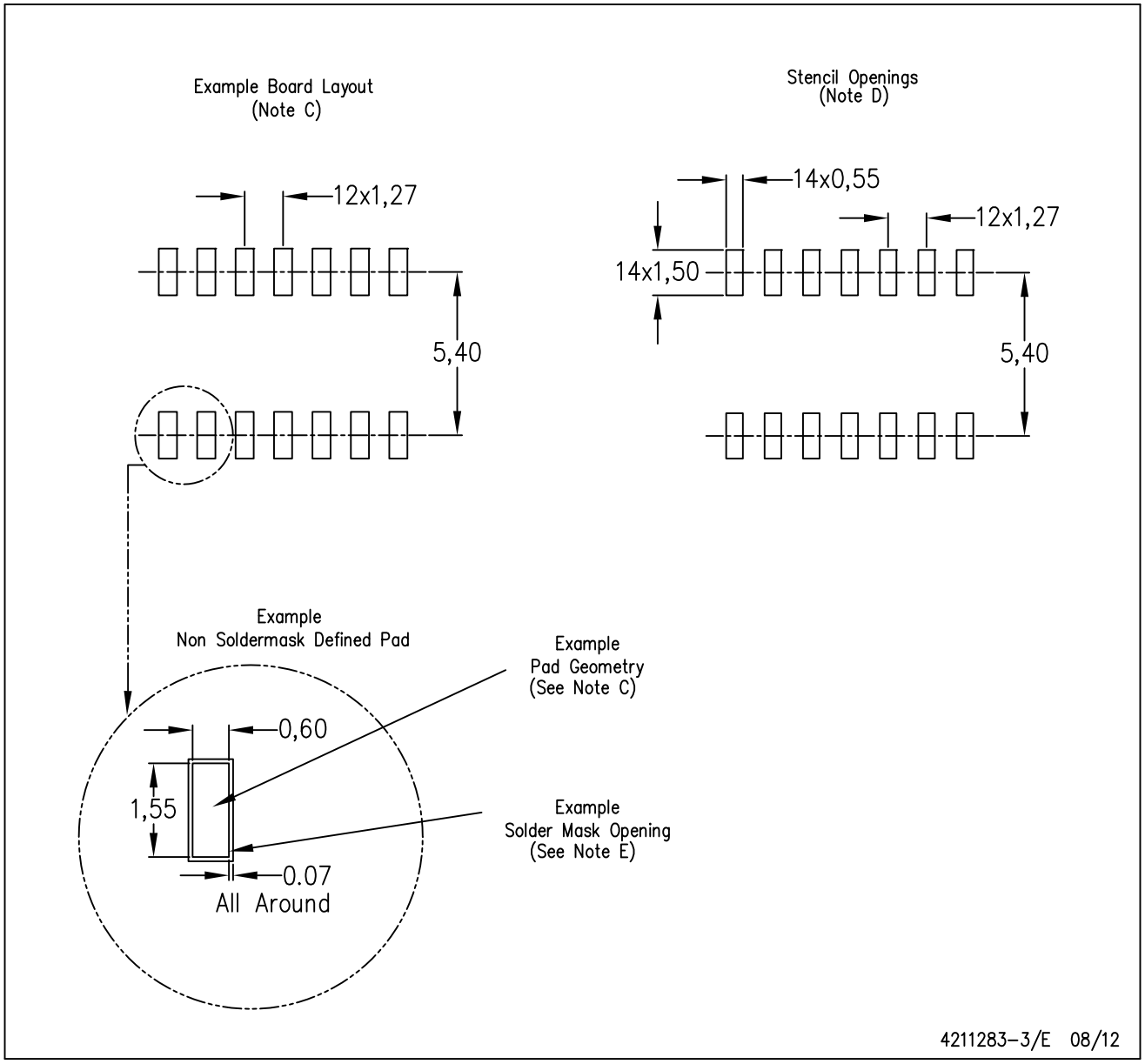
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

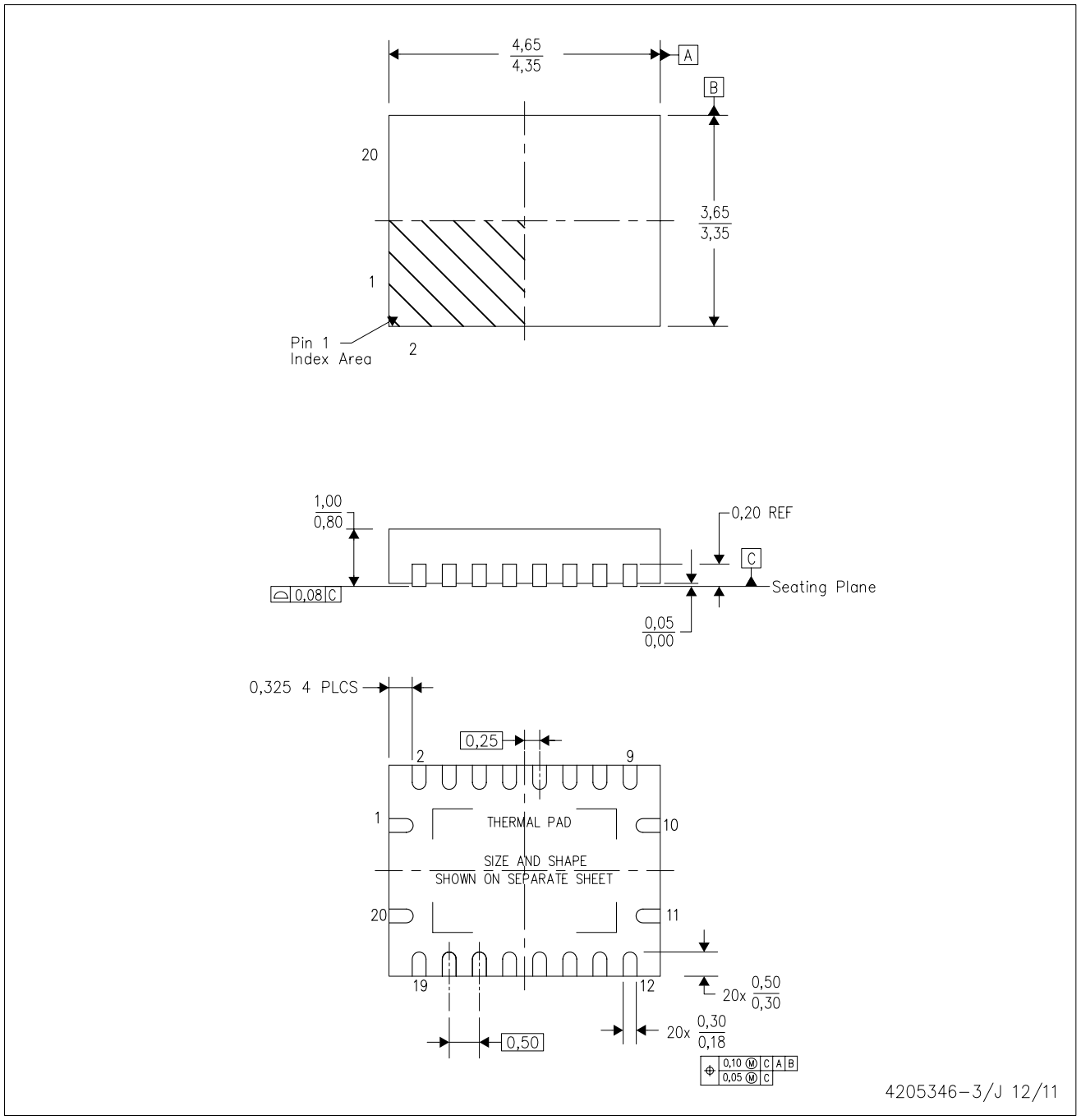
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHL (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

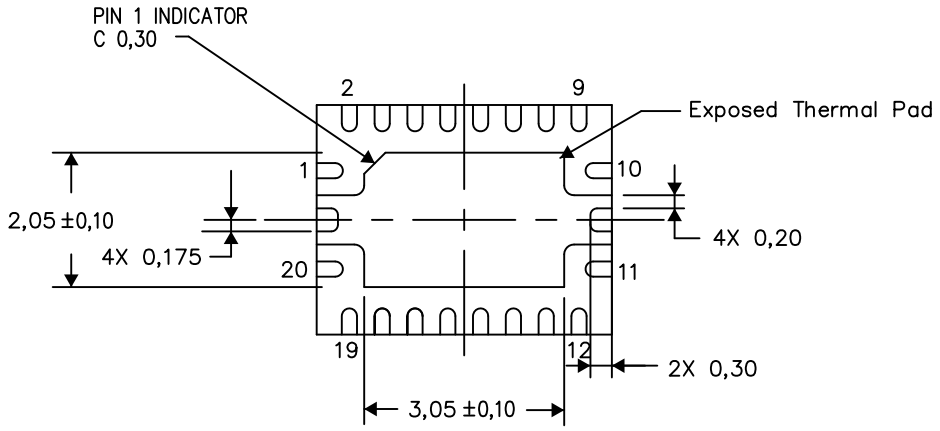
RHL (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



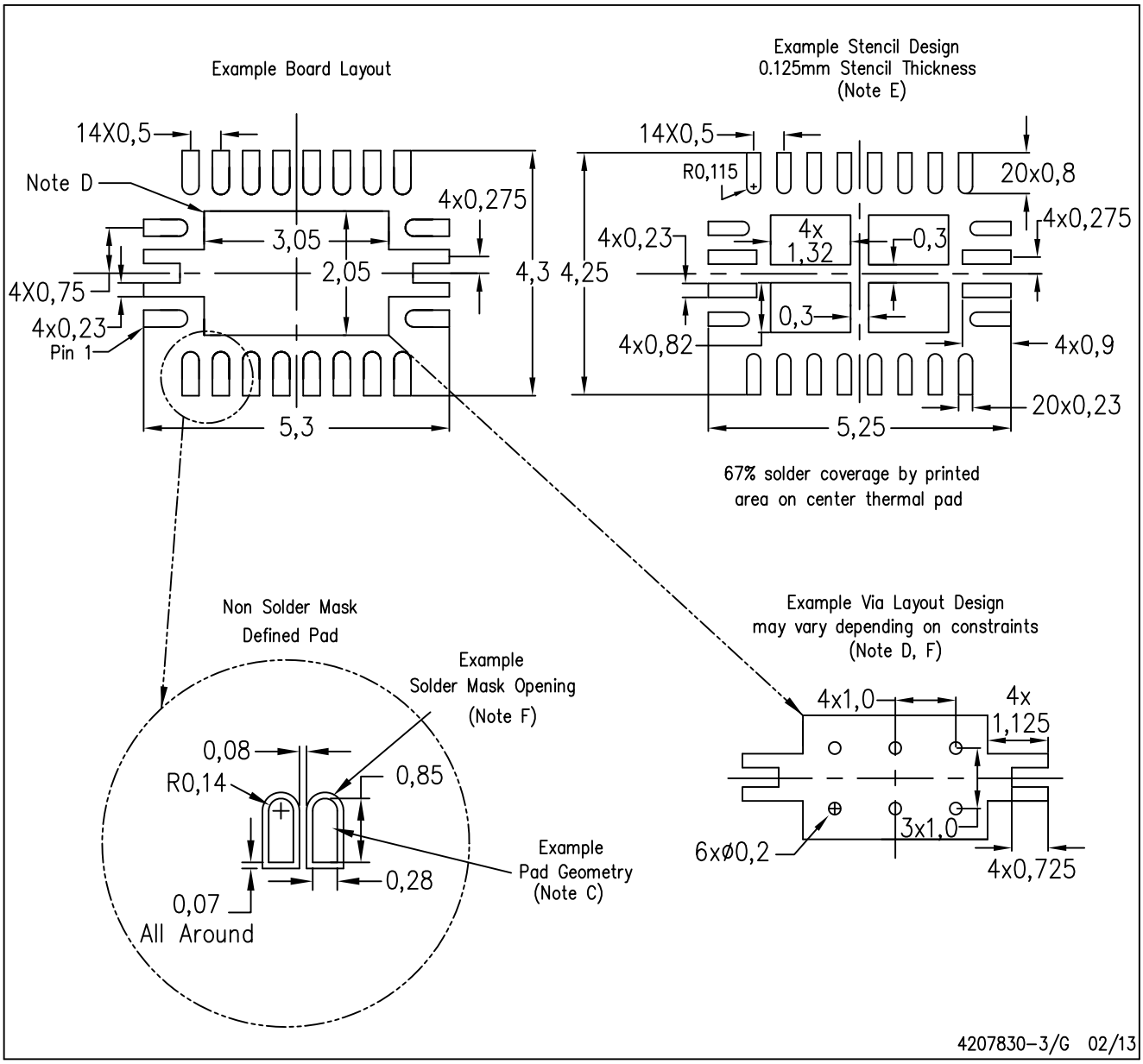
Bottom View

Exposed Thermal Pad Dimensions

4206363–3/M 08/12

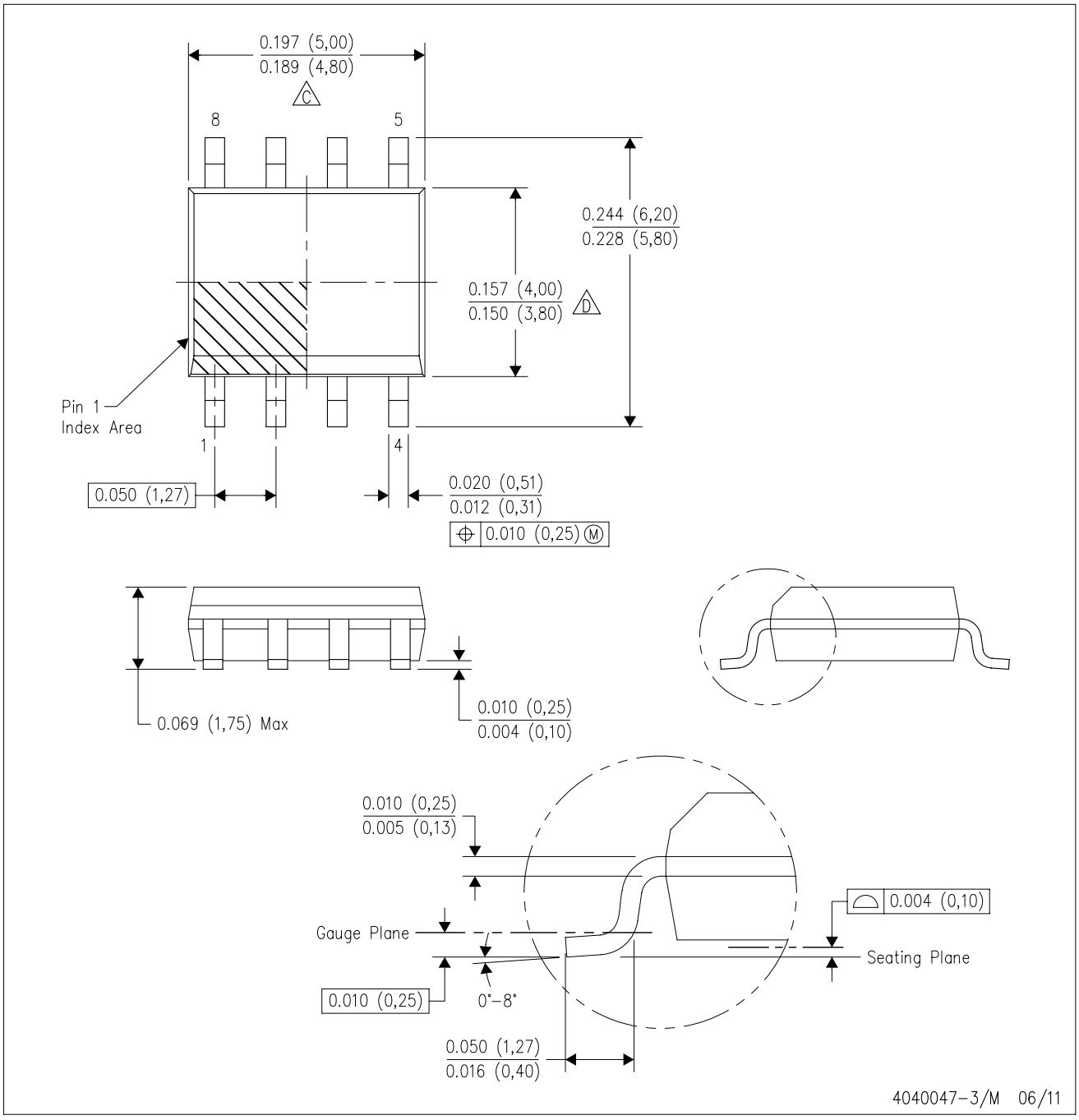
NOTE: All linear dimensions are in millimeters

RHL (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



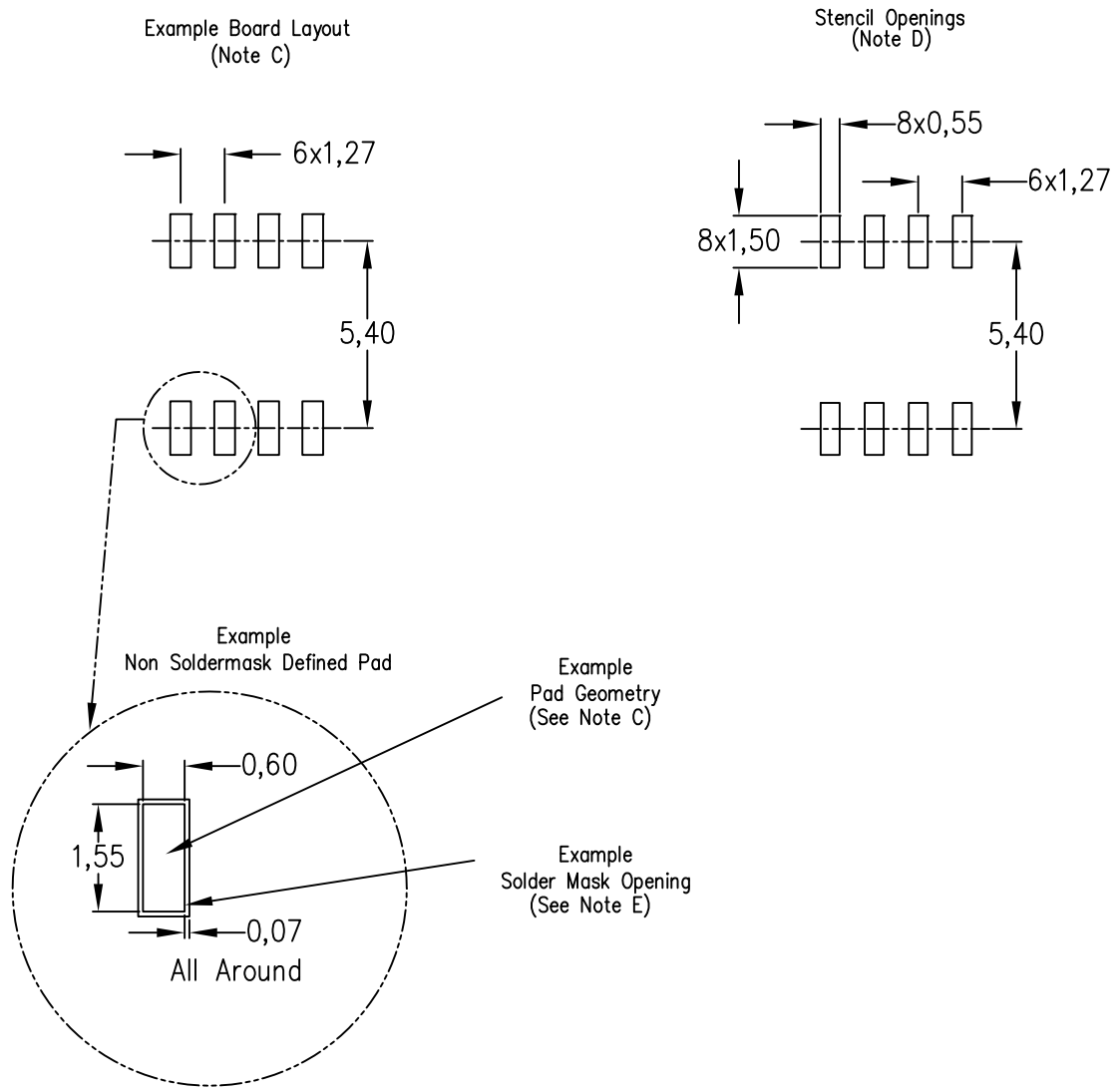
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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