

ADS8342EVM

User's Guide

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Texas Instruments
Post Office Box 655303
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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the ADS8342 Modular EVM. A complete circuit description as well as schematic diagram is included.

How to Use This Manual

This document contains the following chapters:

- Section 1 – EVM Overview
- Section 2 – Analog Interface
- Section 3 – Digital Interface
- Section 4 – Power Supply Options
- Section 5 – EVM Operation
- Section 6 – ADS8342 Modular EVM BOM and Schematic

Related Documentation From Texas Instruments

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Data Sheets:	Literature Number:
ADS8342	SBAS277
Application Notes/ Additional Literature from Texas Instruments:	Literature Number:
Op Amps for Everyone	SL0D006
5-6K Interface Board	SLAU104
Single and Bipolar Supply Signal Conditioning Boards	SLAU105
Controlling the ADS8342 with TMS320 Series DSP's	SLAU176
Third Party Tools:	Vendor Website:
HPA449 Development Board (MSP430 Tools)	www.softbaugh.com

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EVM Overview



This chapter contains the features and introduction.

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1.1 Features

- Four true bipolar inputs
- High speed parallel interface
- Direct operation with a variety of DSK platforms from Texas Instruments

1.2 Introduction

The ADS8342 modular EVM is a platform for evaluation of all operating modes of the ADS8342. It provides a buffered parallel data output and an on-board analog front end (AFE) circuit as an example of a typical input configuration. Jumpers located on the EVM provide static control over the CLKDIV and BYTE pins.

The new modular EVM form factor allows for direct evaluation of the ADC's performance and operating characteristics with a variety of host processors. This EVM is compatible with the 5-6K interface board (SLAU104) from Texas Instruments, as well as the HPA449 development board from SoftBaugh, Inc. (www.softbaugh.com).

Analog Interface

The ADS8342 modular EVM easily interfaces to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual row header/socket combination at J1. Connector J1 and jumpers W1 through W4 provide access to the ADS8342 analog input pins. Analog signals applied to J1 are fed directly to the data converter when shunts are placed on pins 1-2 of W1–W4.

When using the onboard AFE, a single analog input can be applied to any of the four input channels by moving the shunt on W1–W4 to cover pins 2-3. The SMA connector labeled INPUT applies the signal to be converted to the AFE.

The AFE consists of a single channel OPA726 op amp at U2. Gain and filter configurations can be modified as necessary by using the pin sockets installed at resistor and capacitor locations R9–R12, C21 and C27.



Digital Interface

The following section describes the ADS8342 EVM digital interface. Topics include the jumper configuration for byte and conversion-clock division ratio, the parallel data interface and the parallel control signals A0, A1, \overline{RD} , \overline{CS} , and CONVST.

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3.1 Conversion Clock and BYTE Control

Jumpers W5–W7 control the clock divide and parallel data format of the ADS8342. W6 and W7 connect to CLKDIV0 and CLKDIV1 respectively and perform the following actions:

Jumper		Action
W6	W7	
open	open	External conversion clock (20MHz MAX) divided by 8
open	closed	External conversion clock (20MHz MAX) divided by 4
closed	open	External conversion clock (10MHz MAX) divided by 2
closed	closed	External conversion clock (5MHz MAX) divided by 1

Jumper W5 controls the BYTE pin of the ADS8342. When closed, the ADS8342 operates in 16 bit output or *word* mode. When open, the ADS8342 operates in *BYTE* mode and data is accessed by reading D0-D7 twice.

3.2 Parallel Control

The ADS8342 modular EVM interfaces to multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a 10-pin dual-row header/socket combination at J4. This header/socket combination provides access to the \overline{RD} , \overline{CONVST} , and clock pins of the ADS8342.

Signal	Description
J4.1 DC_CSa	Daughter card chip select—active low signal used to access the EVM
J4.3 \overline{WR}	Processor write strobe—active low signal used to initiate a conversion
J4.5 \overline{RD}	Processor read strobe—active low signal used to access parallel data
J4.7 EVM_A0	EVM address line 0—used in conjunction with EVM_A1 to chip select the ADS8342
J4.9 EVM_A1	EVM address line 1—used in conjunction with EVM_A0 to chip select the ADS8342
J4.11 EVM_A2	EVM address line 2—connects to the ADS8342 A1 pin, controls channel read
J4.13 EVM_A3	EVM address line 3—connects to the ADS8342 A1 pin, controls channel read
J4.15 EVM_A4	EVM address line 4—not used
J4.17 TOUT	Processor timer output—optional conversion clock source
J4.19 INT	Processor interrupt input—connects to the ADS8342 BUSY pin

3.3 Parallel Data

The ADS8342 modular EVM uses Samtec part numbers SSW-116-22-F-D-VS-K and TSM-116-01-T-DV-P to provide a 16-pin dual-row header/socket combination at J3. This header/socket combination provides access to the parallel data pins of the ADS8342. Data line D0 is connected to J3 pin 1. Data lines 1-15 are located on odd-numbered pins 3-31 respectively. Even-numbered pins 2-32 are connected to digital ground.

Power Supply Options

The ADS8342 modular EVM board requires ± 5 VDC for the ADS8342 circuit. Positive 3.3 VDC is required for the digital circuitry found on the EVM. Power to the EVM is applied to the 10-pin dual-row header/socket combination of J2. When used in combination with one of the DAP Interface boards, the socket portion of J2 (bottom side of the PWB) provides connection to the common power bus described in document SLAU104. The pin portion may be used to allow stacking of future DAC boards, or as a convenient point to apply external power supplies in stand-alone operation. The following table shows the pin out of J2.

Signal	Pin Number		Signal
Unused	1	2	Unused
+5VA	3	4	Unused
DGND	5	6	AGND
Unused	7	8	Unused
+3.3VD	9	10	+5VD

Note: While filters are provided for all power supply inputs, optimal performance of the EVM requires a clean, well-regulated power source.



EVM Operation

The analog input source for channels AIN0–AIN3 is applied directly to connector J1, pins 2, 4, 6, or 8 (top or bottom side) or through the onboard AFE via the SMA connector labeled INPUT. When using the AFE circuit, resistors R9, R10, R11 and R12 as well as capacitors C21 and C27 provide customizable filtering of the input signal. J1 or AFE inputs are selected through jumpers W1–W4. For J1 use, shunts must be installed at pins 1-2.

The digital control signals are applied directly to J4 (top or bottom side). The ADS8342 modular EVM can also be connected directly to a DSP, microcontroller, or FPGA interface board. If an external conversion clock is required, the clock is applied to the SMA connector labeled EXT CLK in accordance with the clock division factor (see table in Section 3.1).

The ADS8342 EVM is designed for use with the 5-6K interface board. Conversions are initiated by writing to the external DSP data bus at an address determined by jumper settings on the EVM and interface board.

With a proper conversion clock applied the EVM, the ADC responds to a /CONVST signal (via the processor /WR strobe) and provides the host with an interrupt via J4 pin 19. The host must then access data from channel A0 through A3 by reading from the appropriate address (see SLAU104 and SLAA176 for details). When operating in BYTE mode, two successive reads from the selected analog input channel are required to obtain a full 16 bit data transfer.

The following table shows the default jumper locations of the ADS8364 EVM:

Jumper	Default Position	Function
W1 W2 W3 W4	1-2	1-2: AINx samples analog signal applied at J1 2-3: AINx samples signal from analog front end (U2)
W5	Closed	Closed: BYTE pin of ADS8342 pulled low Open: BYTE pin of ADS8342 pulled high
W6	Closed	Closed: CLKDIV0 pin of ADS8342 pulled low (See Section 3.1) Open: CLKDIV0 pin of ADS8342 pulled high
W7	Closed	Closed: CLKDIV1 pin of ADS8342 pulled low (See Section 3.1) Open: CLKDIV1 pin of ADS8342 pulled high
W8	2-3	1-2: CLK is driven by an external clock EXT CLK buffered by U6 2-3: CLK is driven by TOUT signal from J4
W9	1-2	1-2: Digital output buffer U3 is enabled by DC_CSa signal applied at J4 2-3: Digital output buffer U3 is enabled by RD and the decoded address from U7 (See W11)
W10	1-2	1-2: U2 - input driven by signal applied to analog INPUT SMA_J connector 2-3: U2 - input connected to ground
W11	5-6	Address decode select 1-2: 3 3-4: 2 5-6: 1 7-8: 0
W12	2-3	1-2: U2 + input driven by signal applied to analog INPUT SMA_J connector 2-3: U2 + input connected to ground

ADS8342 Modular EVM BOM and Schematic

This chapter contains the ADS8342 modular EVM bill of materials and the schematic.

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6.1 Bill of Materials

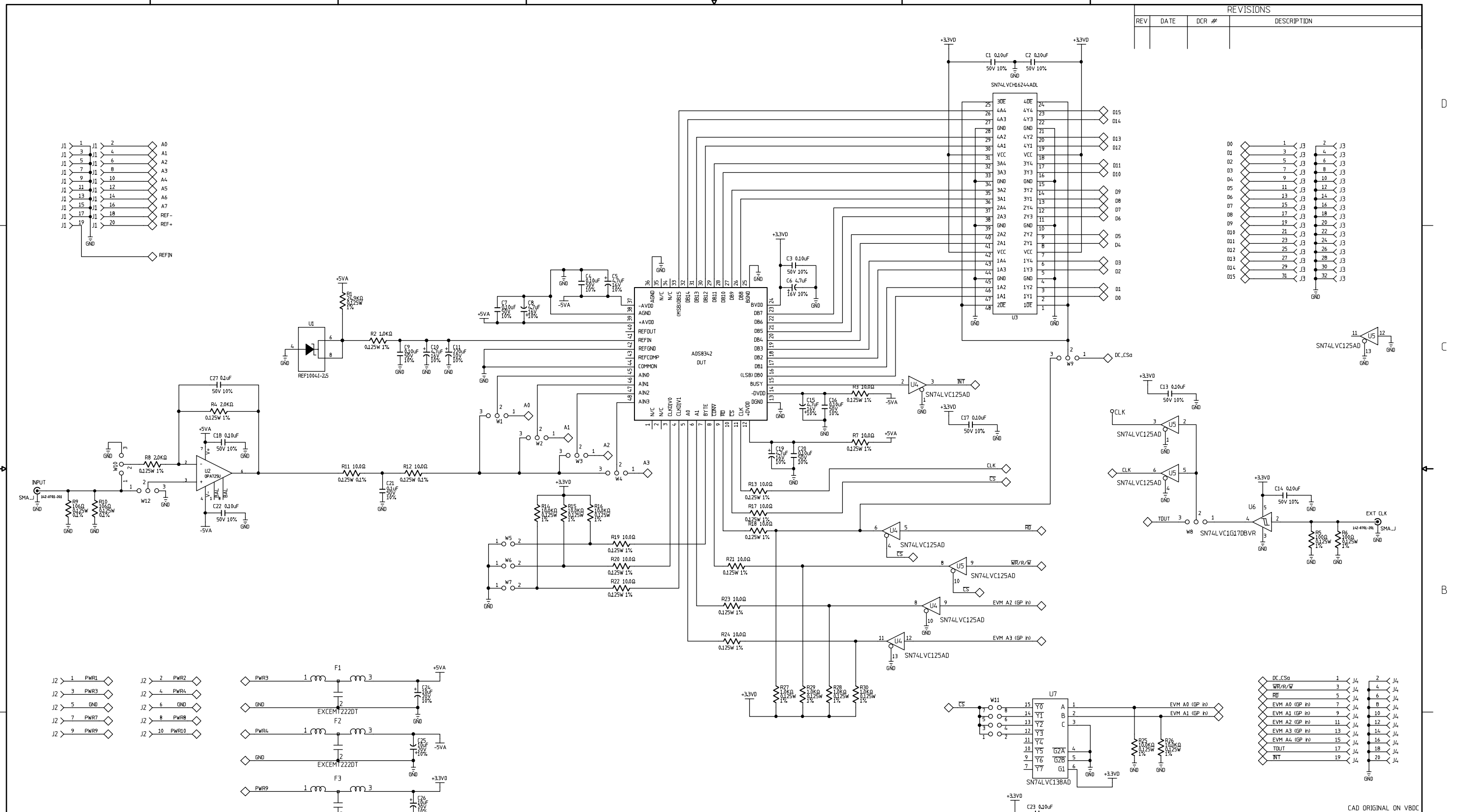
The following table contains a complete bill of materials for the ADS8342 modular EVM board. The schematic diagram is also provided for reference.

Designators	Description	Manufacturer	Mfg. Part Number
C1-C4 C7 C9 C13 C14 C16-C18 C20 C22 C23	0.1 μ F, 1206, ceramic, X7R, 50 V, 10%	AVX Corp.	12065C104KAT2A
C5 C6 C8 C10 C15 C19	4.7 μ F, A case, tantalum, 16 V, 10%	Panasonic	T491A475K016AS
C11	220 μ F, 10 V tantalum, 10%	AVX Corp.	TAP227K010CCS
C24-C26	10 μ F, C case, tantalum, 20 V, 20%	Panasonic	ECS-T1DC106R
F1-F3	EMI filters	Panasonic	EXC-EMT222DT
J1 J4 (top side)	10 Pin, dual row, SMT header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
J1 J4 (bottom side)	10 Pin, dual row, SMT socket (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
J3 (top side)	16 Pin, dual row, SMT header (32 Pos.)	Samtec	TSM-116-01-T-DV-P
J3 (bottom side)	16 Pin, dual row, SMT socket (32 Pos.)	Samtec	SSW-116-22-F-D-VS-K
INPUT EXT CLK	SMA connector	Lighthouse Tech	LTI-SASF54GT
J2 (top side)	5 Pin, dual row, SMT header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
J2 (bottom side)	5 Pin, dual row, SMT socket (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
R1	24.9 k Ω , 1206, 1%	Yageo America	9C12063A2492FKHFT
R5 R6	100 Ω , 1206, 5%	Yageo America	9C12063A1000JLHFT
R8	20 k Ω , 1206, 1%	Yageo America	9C12063A2002FKHFT
R14-R16 R25 R26	10 k Ω , 1206, 5%	Yageo America	9C12063A1002JLHFT
R2 R27-R30	1 k Ω , 1206, 5%	Yageo America	9C12063A1001JLHFT
R3 R7 R13 R17-R24	10 Ω , 1206, 5%	Yageo America	9C12063A10R0JLHFT
CLK	Red test point loop	Keystone	5000K
U1	REF1004 - 25	Texas Instruments	REF1004C-2.5
U2	OPA726	Texas Instruments	OPA726AID
U3	SN74LVCH16244	Texas Instruments	SN74LVCH16244ADL
U4 U5	SN74LVC125A	Texas Instruments	SN74LVC125AD
U6	SN74LVC1G17	Texas Instruments	SN74LVC1G17DBVR
DUT	ADS8342	Texas Instruments	ADS8342IBPFBT
U7	SN74LVC138A	Texas Instruments	SN74LVC138AD
W5-W7	2 Pin , 0.1" Header	Samtec	TSW-102-07-L-S
W11	4 Pin, dual row, TH header (8 Pos.)	Samtec	TSW-104-07-L-D
W1-W4 W8-W10 W12	3 Pin , 0.1" header	Samtec	TSW-103-07-L-S
User selectable components			
R9 R10	100 Ω , Axial, 0.25 W, 1%	Yageo America	MFR-25FRF-100K
R11 R12	10 Ω , Axial, 0.25 W, 1%	Yageo America	MFR-25FRF-10R0
C21 C27	0.1 μ F, Axial, X7R	Kemet	C320C104K5R5CA

6.2 Schematic

The ADS8342 modular EVM schematic is on the following page.

REVISIONS			
REV	DATE	DCR #	DESCRIPTION



USED ON		TEXAS INSTRUMENTS TUCSON CORP. P.O. BOX 11400-TUCSON, ARIZONA 85734	
CONTRACT NO.		ADS8342 Evaluation Board	
APPROVALS	DATE		
DRAWN Michael Snedeker			
CHECKED			
ISSUED			
SIZE D	CAGE CODE 13919	DWG. NO.	REV A
SCALE:		SHEET	

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➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com