INPUT POWER MONITOR WITH DIGITAL INTERFACE

FEATURES

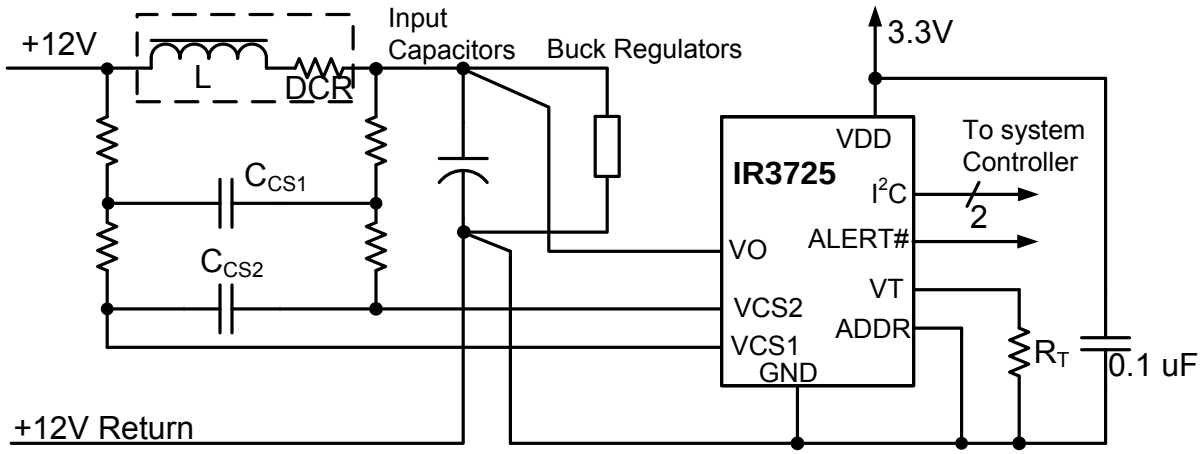
- Accurate power, current, or voltage reporting
  - 1.5 % maximum power error
  - 1.0 % maximum current error
- Serial digital interface
  - SMBus and I^2C compatible
- Programmable averaging interval
- Flexible current sensing
  - Resistive or Inductor DCR
- Applications
  - Synchronous rectified buck converters
  - Multiphase converters
- 12pin 3x4 DFN lead free
- RoHS Compliant

DESCRIPTION

The IR3725 is a highly configurable power monitor IC that uses proprietary digital technology to measure a 12V rail current, its voltage, or its average power over a user specified time interval. Configuration and result reporting are managed through a serial digital interface. The current is measured as a voltage across a shunt resistance, an input inductor, or a copper trace resistance.

The real time voltage and current signals are multiplied, digitized, and averaged over a user selectable averaging interval providing TruePower™ measurement of highly dynamic loads.

TYPICAL APPLICATION CIRCUIT



ORDERING INFORMATION

Device	Package	Order Quantity
IR3725MTRPBF	12 lead DFN (4x3 mm body)	3000 piece reel
IR3725MPBF	12 lead DFN (4x3 mm body)	Sample Quantity

ABSOLUTE MAXIMUM RATINGS

All voltages referenced to GND
VDD: 3.9V
ALERT#:.....3.9V
ALERT#..... < VDD + 0.3V
VCS1, VCS2, VO 25.0V
All other Analog and Digital pins.....3.9V

Operating Junction Temperature .... -10°C to 150°C
Storage Temperature Range ..... -65°C to 150°C
Thermal Impedance (θ_{JC}).....1.6 °C/W
Thermal Impedance (θ_{JA}).....30 °C/W
ESD Rating ..... HBM Class 1C JEDEC Standard
MSL Rating .....Level 2
Reflow Temperature ..... 260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS

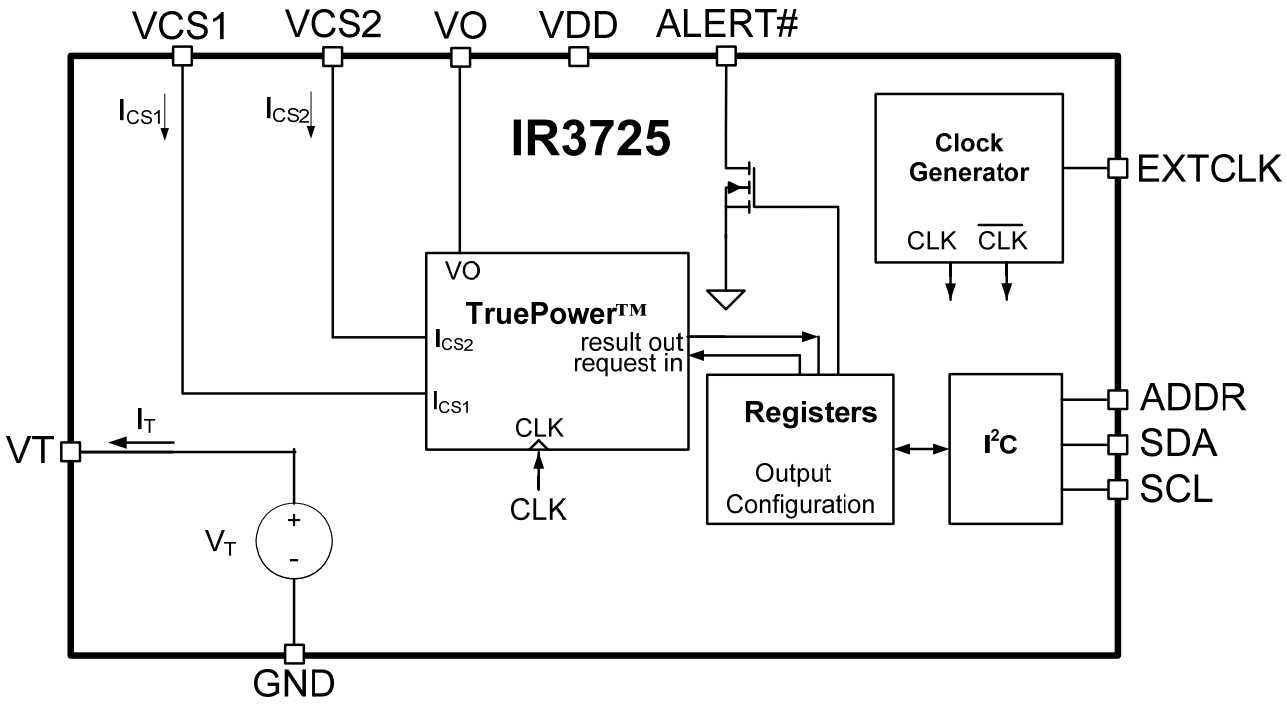
Unless otherwise specified, these specifications apply: VDD = 3.3V ± 5%, 0°C ≤ T_J ≤ 125°C, 8V ≤ VO ≤ 23.5V, and operation in the typical application circuit. See notes following table.

PARAMETER	TEST CONDITION	NOTE	MIN	TYP	MAX	UNIT
BIAS SUPPLY						
VDD Turn-on Threshold, VDD_{UP}					3.1	V
VDD Turn-off Threshold, VDD_{DN}			2.4			V
VDD UVLO Hysteresis			75			mV
VDD Operating Current	R_T = 25.5 kΩ			700	1000	µA
VDD Shutdown Current	Config Reg enable bit d4=1			18	100	µA
VOLTAGE REFERENCE						
V_T Voltage	R_T = 25.5 kΩ		1.40	1.50	1.60	V
Reference load, R_T		1	20	25.5	45.3	kΩ
VOLTAGE SENSOR						
Voltage, full scale, V_{FS}				23.5		V
CURRENT SENSOR						
Voltage, Current Gain, V_{IG}	R_T = 25.5 kΩ			1.48		V
DIGITIZER						
Internal Sampling frequency	Driven from internal clock			512		kHz
External Sampling frequency	Driven from external clock		922	1024	1126	kHz
POWER INFORMATION						
Minimum Averaging Interval	Config Reg [d3..d0] = b‘0000	1	0.85	1	1.15	ms
Maximum Averaging Interval	Config Reg [d3..d0] = b‘1000	1	217	256	295	ms

PARAMETER	TEST CONDITION	NOTE	MIN	TYP	MAX	UNIT
ACCURACY						
Power measurement error	VO=12V, DCR voltage = 75 mV, R_T=25.5kΩ, RCS1=RCS2=1.5kΩ	1, 2			2	%
	T_j = 0 - 85 °C				1.5	
Voltage measurement error	VO=12 V, DCR voltage = 75mV, RT=25.5kΩ, RCS1=RCS2=1.5kΩ	1, 2			1.5	%
	Tj = 0 – 85 °C				1.3	
Current measurement error	VO=12V, DCR voltage = 75 mV, R_T=25.5kΩ, RCS1=RCS2=1.5kΩ Tj = 0 – 85 °C	1, 2			1.6	%

NOTES:
1. Guaranteed by design, not tested in production
2. Assumes no error contributed by external components

BLOCK DIAGRAM



PIN DESCRIPTION

NAME	NUMBER	I/O LEVEL	DESCRIPTION
VCS1	1	Analog 12V	Current sensing input 1
VCS2	2	Analog 12V	Current sensing input 2
VO	3	Analog 12V	Voltage sensing input
VT	4	Analog	Thermistor sensing input
GND	5	0V	IC bias supply and signal ground
VDD	6	3.3V	3.3V bias supply
EXTCLK	7	3.3V Digital	Input for optional external clock
ADDR	8	3.3V Digital	Bus Address selection input
SCL	9	3.3V Digital	Bus Clock; Input only
SDA	10	3.3V Digital	Bus Data; Input / Open drain output
ALERT#	11	3.3V Digital	Programmable output function; Open drain output clamped to VDD
NC	12		Do not connect

IC PIN FUNCTIONS

VDD PIN

This pin provides operational bias current to circuits internal to the IR3725. Bypass it with a high quality ceramic capacitor to the GND pin.

GND PIN

This pin returns operational bias current to its source. It is also the reference to which the voltage VO is measured, and it sinks the reference current established by the external resistor R_T.

VO PIN

This pin is to be electrically connected to the location in the circuit where voltage for the power calculation is desired to be monitored. Power accuracy may be degraded if the voltage at this pin is below VO_{min}.

VCS1 AND VCS2 PINS

The average current into these pins is used to calculate power. Current sources internal to the IR3725 will null the average voltage between this pin pair.

VT FUNCTION

A voltage internal to the IR3725 drives the VT pin while the pin current is monitored and used to set the amplitude of the switched current source IT. This pin should be connected to GND through a precision resistor network RT. This network may include provision for canceling the positive temperature coefficient of the inductor's DC resistance (DCR).

ALERT# FUNCTION

The ALERT# pin is a multi-use pin. During normal use it can be configured via the serial bus as an open drain ALERT# pin that will be driven logic low when new data is available in the output register. After the output register has been read via the serial bus the ALERT# will be released to its high resistance state. This pin can also be programmed to pull low when the output exceeds the programmable level.

ADDR PIN

The ADDR pin is an input that establishes the serial bus address. Valid addresses are selected by grounding, floating, or wiring to VDD the ADDR pin. Table 1, “User Selectable Addresses”, provides a mapping of possible selections. Bypass this pin to GND with a high quality ceramic capacitor when floated.

Table 1 User selectable addresses

ADDR pin configuration	Bus Address
Low	b’1110 000
Open	b’1110 010
High	b’1110 110

EXTCLK

This pin is a Schmitt trigger input for an optional externally provided square wave clock. The duty ratio of this externally provided clock, if used, shall be between 40% and 60%. If no external clock is connected, the internal clock will be used. Connect this pin to GND if no external clock is used.

SCL

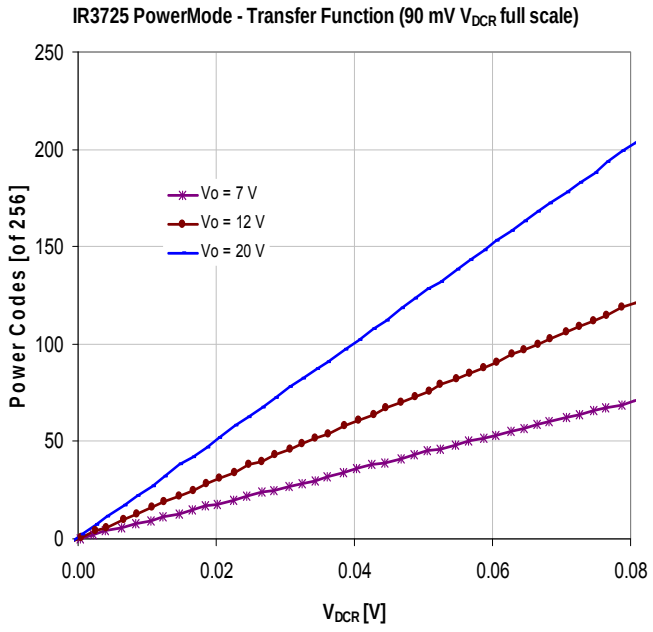
SCL is the serial bus clock and is capable of functioning with a rate as low as 10 kHz. It will continue to function as the rate is increased to 400 kHz. This device is considered a slave, and therefore uses the SCL as an input only.

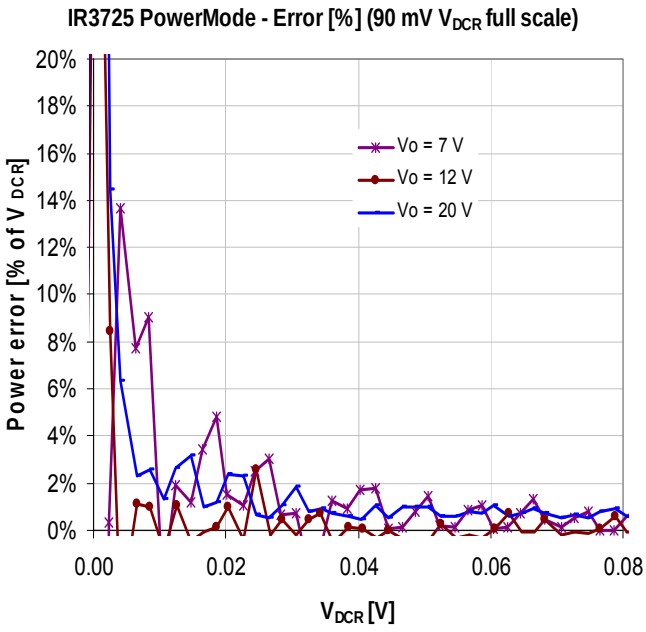
SDA

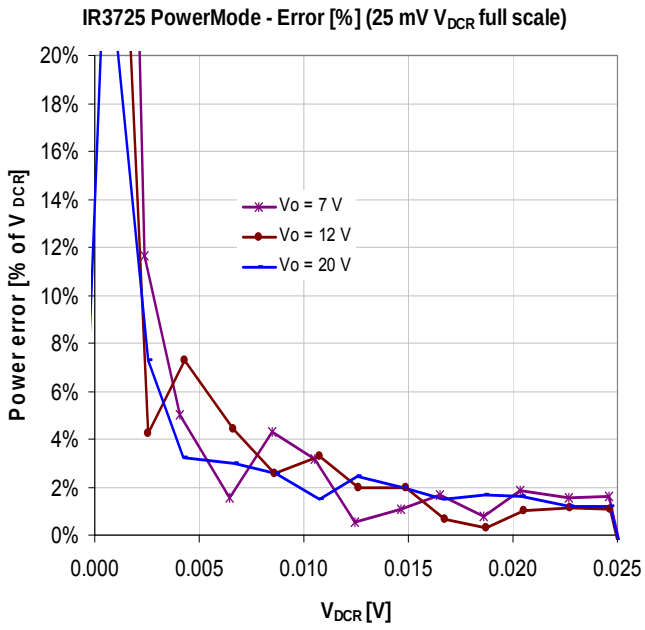
SDA is monitored as data input during master to slave transactions, and is driven as data output during slave to master transactions as indicated in the Packet Protocol section to follow.

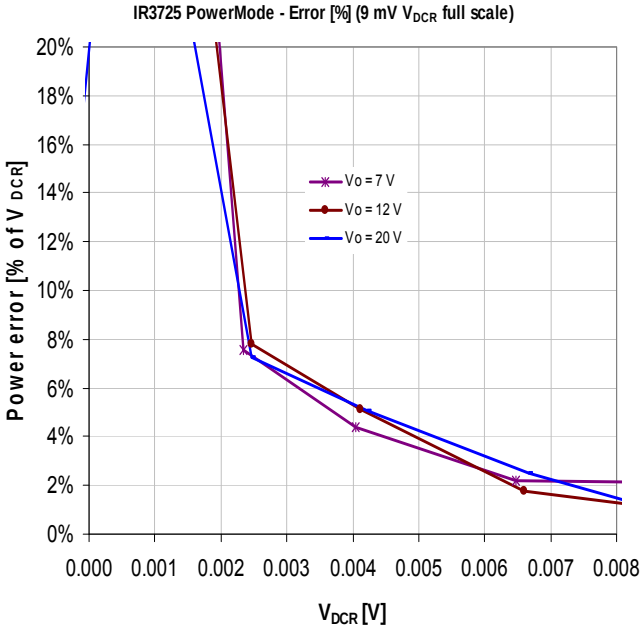
TYPICAL PERFORMANCE CHARACTERISTICS

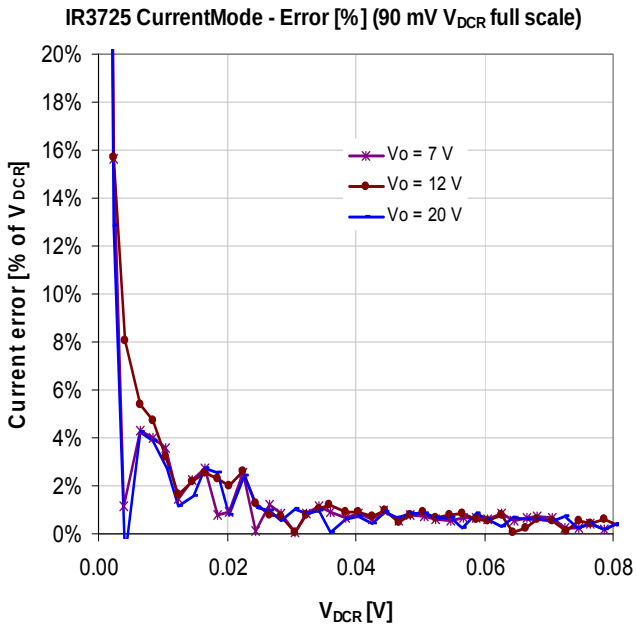
(One device tested using "Resistor Sensing Circuit", VDD = 3.3 V, C_{CS2} = 10 u F, R_T = 25.5 k Ω, 90 mV full scale uses R_{CS1} = R_{CS2} = 1.5 k Ω, 25 mV full scale uses R_{CS1} = R_{CS2} = 432 Ω, 9 mV full scale uses R_{CS1} = R_{CS2} = 150 Ω. Each data point is average of eight samples.)

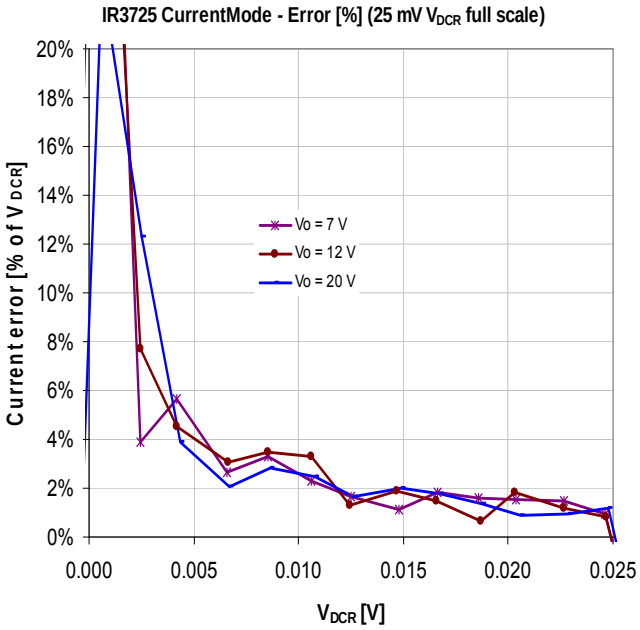


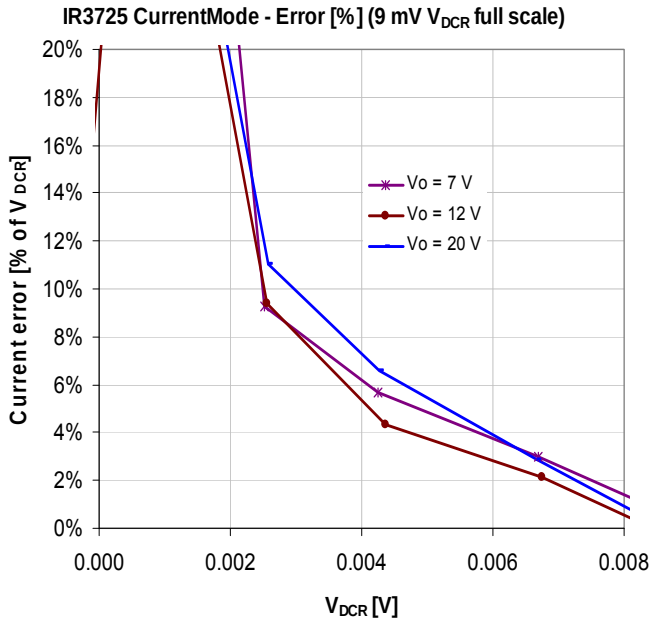


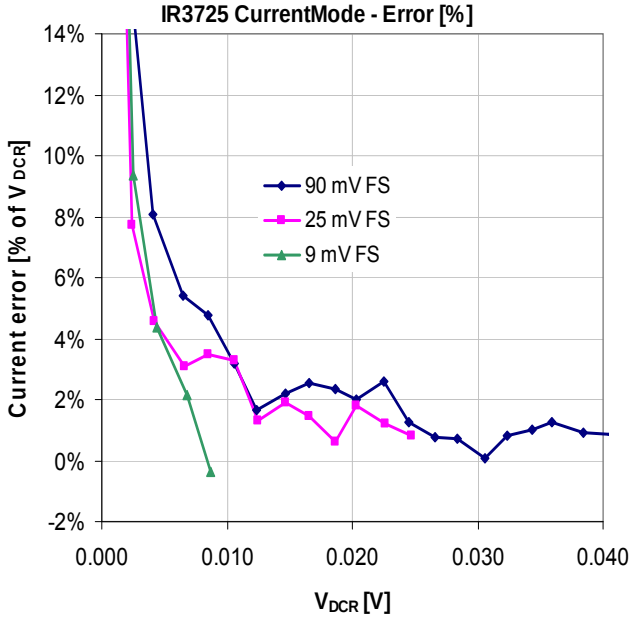





IR3725 CurrentMode - Error [%] (90 mV VDCR full scale)
Current error [% of VDCR]
VDCR [V]
Vo = 7 V
Vo = 12 V
Vo = 20 V
20%
18%
16%
14%
12%
10%
8%
6%
4%
2%
0%
0.00
0.02
0.04
0.06
0.08


IR3725 CurrentMode - Error [%] (25 mV VDCR full scale)
Current error [% of VDCR]
VDCR [V]
Vo = 7 V
Vo = 12 V
Vo = 20 V
20%
18%
16%
14%
12%
10%
8%
6%
4%
2%
0%
0.000
0.005
0.010
0.015
0.020
0.025


IR3725 CurrentMode - Error [%] (9 mV VDCR full scale)
Current error [% of VDCR]
VDCR [V]
Vo = 7 V
Vo = 12 V
Vo = 20 V
20%
18%
16%
14%
12%
10%
8%
6%
4%
2%
0%
0.000
0.002
0.004
0.006
0.008


IR3725 CurrentMode - Error [%]
Current error [% of VDCR]
VDCR [V]
90 mV FS
25 mV FS
9 mV FS
14%
12%
10%
8%
6%
4%
2%
0%
-2%
0.000
0.010
0.020
0.030
0.040

FUNCTIONAL DESCRIPTION

Please refer to the Functional Description Diagram below. Power flow through the inductor is the product of output voltage VO times the inductor current I_L. An average voltage V_{DCR} will be developed across the inductor as a result of current flow I_L. This voltage will result in a net current flow imbalance into the VCS pins that is equal to V_{DCR} / (Rcs1 + Rcs2). A voltage nulling circuit inside the IC sinks enough current to equalize the voltages of Vcs1 and Vcs2. The current required to balance the voltages of these two nodes is reported as a fraction of the current V_{IG} / R_T using 256 as the denominator. Current will be reported as an integer number of counts in two's compliment binary format with a range of -256 to 256. Positive values will be reported when current flow is in the direction of the current flow arrow in the diagram below.

The voltage is reported as a positive integer number of counts equal to (voltage * 256) / V_{FS}. V_{FS} is defined in the ELECTRICAL SPECIFICATIONS.

Power is reported as an integer number of counts in two's compliment binary format with a range of -256 to 256. Positive values will be reported when current flow is in the direction of the current flow arrow in the diagram below. Power expressed in counts will be (power * 256) / (I_{FS} * V_{FS}) where I_{FS} equals V_{IG}*(Rcs1 + Rcs2) / (R_T*DCR). The full scale power P_{FS} is the product of full-scale voltage and full scale current.

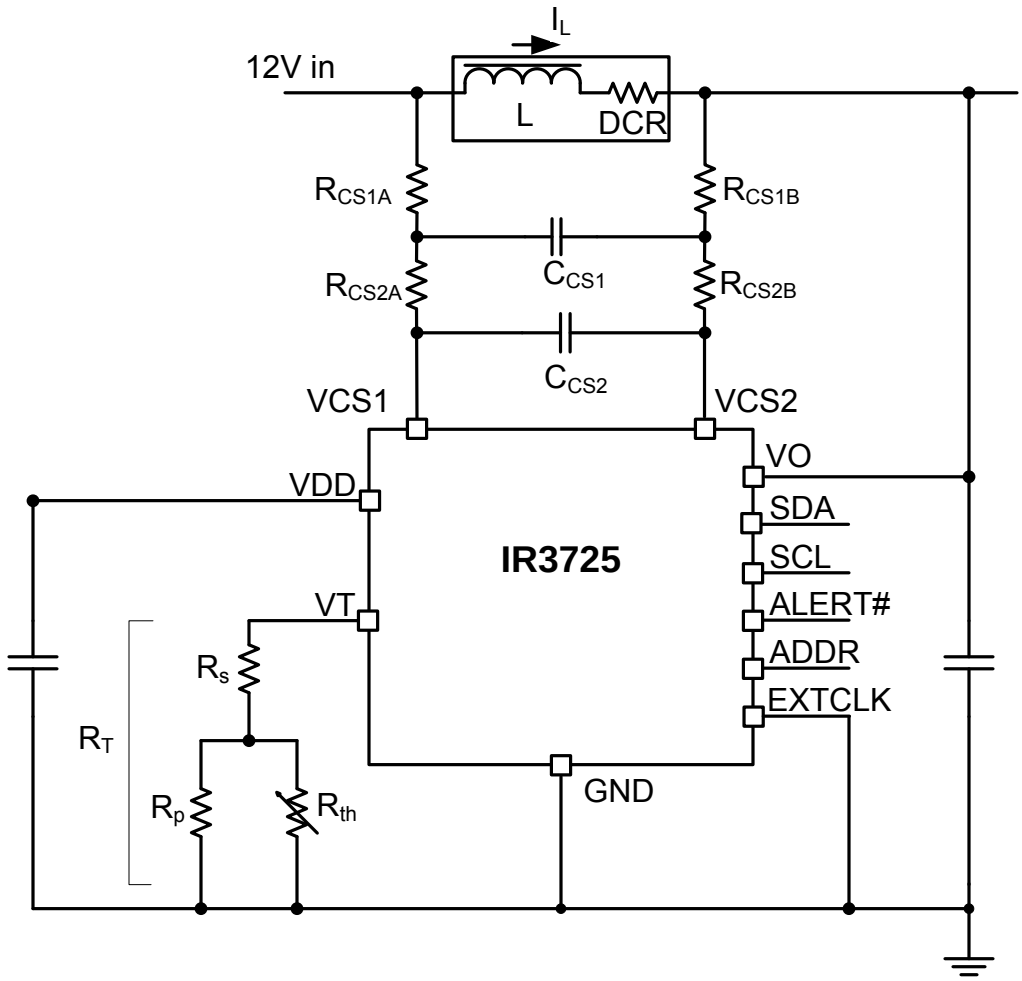


Figure 1 Functional Description Diagram

RESISTOR CURRENT SENSING APPLICATION

The voltage on the shunt resistor of the circuit below is directly proportional to the current from the source. Shunts developing 5 mV to 75 mV at I_{FS} have been used. Accuracy is enhanced at the higher voltage. Select R_T to be a 25.5 kΩ 1% or better initial tolerance resistor. Sinking current capability of VCS1 or VCS2 is V_{IG} / R_T.

Chose R_{CS1} and R_{CS2} such that this current through either of them develops the same voltage that is developed by the shunt at full scale current.

$$I_{FS} * R_{SHUNT} = (V_{IG} / R_T) * R_{CS}$$

C_{CS2} is the integrator capacitor and should have a ceramic dielectric with a value between 0.1 µF and 10 µF.

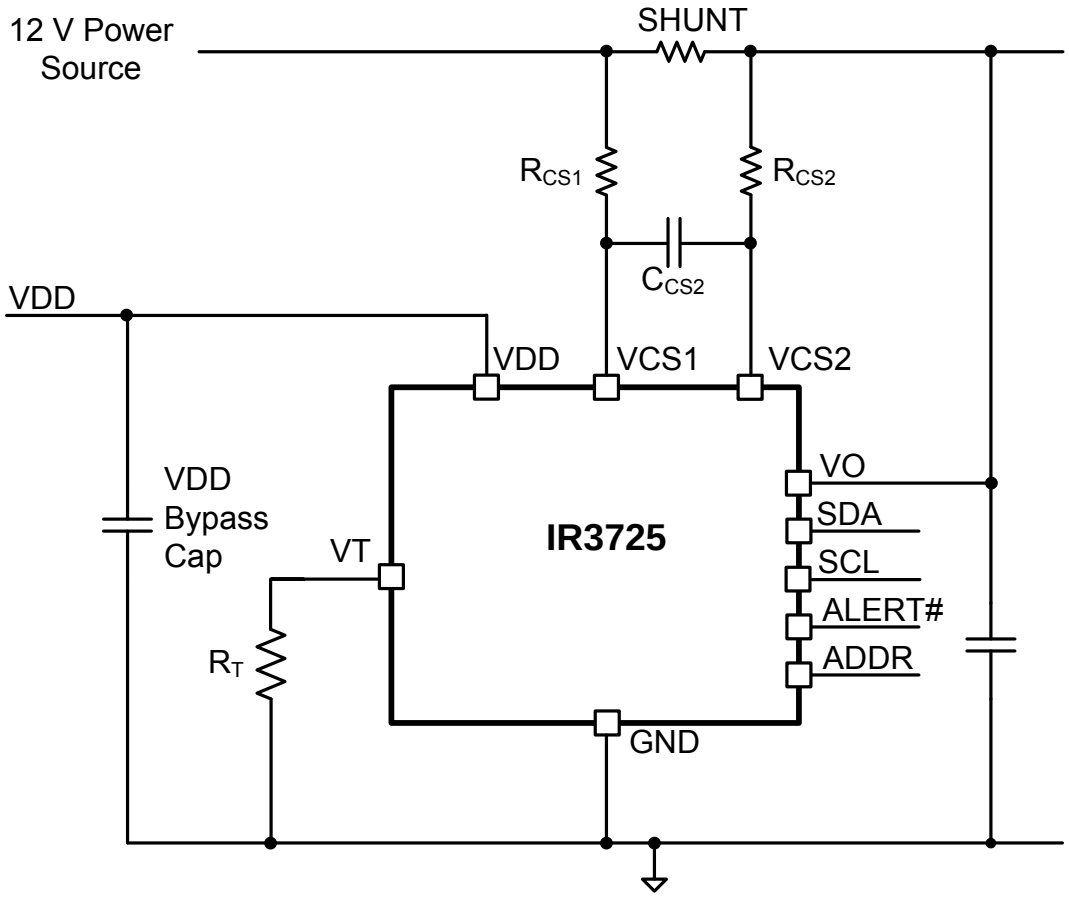


Figure 2 Resistor Sensing Circuit

INDUCTOR DCR CURRENT SENSING APPLICATION

Referring to the Functional Description Diagram, it can be seen that the shunt function can be accomplished by the DC resistance of the inductor that is already present. Omitting the resistive shunt reduces BOM cost and increases efficiency. In exchange for these two significant advantages two easily compensated design complications are introduced, a time constant and a temperature coefficient.
The inductor voltage sensed between the Rcs1 resistors is not simply proportional to the inductor current, but rather is expressed in the Laplace equation below.

$$V_L = I_L \cdot DCR\left(1 + s\frac{L}{DCR}\right)$$

This inductor time constant is canceled when

$$\frac{L}{DCR} = 2 \cdot \frac{R_{CS1} \cdot R_{CS2}}{R_{CS1} + R_{CS2}} \cdot C_{CS1} \cdot$$

Let $\frac{R_{CS1} \cdot R_{CS2}}{R_{CS1} + R_{CS2}} = R_{eq} \cdot$

A second equation is used to set the full-scale inductor current.

$I_{FS} = \frac{V_{IG}}{R_T} \cdot \frac{(R_{CS1} + R_{CS2})}{DCR}$. Let

$R_{CS1} + R_{CS2} = R_{sum}$ and solve for Rsum.

Select a standard value C_{CS1} that is larger than $\frac{4 \cdot L}{DCR \cdot R_{sum}}$. Solve for R_{eq}.

We now know Req and Rsum, but we do not know the individual resistor values R_{CS1} or R_{CS2}. The next step is to solve for them simultaneously. By substituting R_{sum} into the R_{eq} equation the following can be written:

$R_{eq} = \frac{R_{CS1} \cdot R_{CS2}}{R_{sum}}$, which can then be rearranged to

$$R_{CS1}^2 - R_{CS1} \cdot R_{sum} + R_{eq} \cdot R_{sum} = 0 \ .$$

Note that this equation is of the form $ax^2 + bx + c = 0$ where a=1, b=-Rsum, and c=Req•Rsum. The roots of this quadratic equation will be R_{CS1} and R_{CS2}. Use the higher value resistor as R_{CS1} in order to minimize ripple current in C_{CS1}.

$$R_{CS1} = R_{SUM} \cdot \frac{1 + \sqrt{1 - 4 \cdot \frac{R_{eq}}{R_{SUM}}}}{2}$$

$$R_{CS2} = R_{SUM} \cdot \frac{1 - \sqrt{1 - 4 \cdot \frac{R_{eq}}{R_{SUM}}}}{2}$$

THERMAL COMPENSATION FOR INDUCTOR DCR CURRENT SENSING

The positive temperature coefficient of the inductor DCR can be compensated if R_T varies inversely proportional to the DCR. DCR of a copper coil, as a function of temperature, is approximated by

$$DCR(T) = DCR(T_R) \cdot (1 + (T - T_R) \cdot TCR_{Cu}) \quad . \qquad (1)$$

T_R is some reference temperature, usually 25 °C, and TCR_{Cu} is the resistive temperature coefficient of copper, usually assumed to be 0.39 %/°C near room temperature. Note that equation 1 is linearly increasing with temperature and has an offset of $DCR(T_R)$ at the reference temperature.
If R_T incorporates a negative temperature coefficient thermistor then temperature effects of DCR can be minimized. Consider a circuit of two resistors and a thermistor as shown in the R_T network below.

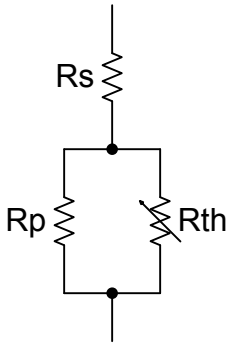


Figure 3 R_T Network

If Rth is an NTC thermistor then the resistance of the network will decrease as temperature increases. Unfortunately, most thermistors exhibit far more variation with temperature than copper wire. One equation used to model thermistors is

$$R_{th}(T) = R_{th}(T_0) \cdot e^{\left(\beta\left(\frac{1}{T} - \frac{1}{T_0}\right)\right)} \qquad (2)$$

where $R_{th}(T)$ is the thermistor resistance at some temperature T, $R_{th}(T_0)$ is the thermistor resistance at the reference temperature T_0, and β is the material constant provided by the thermistor manufacturer. Kelvin degrees are used in the exponential term of equation 2. If R_S is large and R_P is small, the curvature of the equivalent network resistance can be reduced from the curvature of the thermistor alone. Although the exponential equation 2 can never compensate linear equation 1 at all temperatures, a spreadsheet can be constructed to minimize error over the temperature interval of interest. The resistance R_T of the network shown as a function of temperature is

$$R_T(T) = R_s + \frac{1}{\frac{1}{R_p} + \frac{1}{R_{th}(T)}} \qquad (3)$$

using $R_{th}(T)$ from equation 2.
Equation 4 may be written as a function of temperature using equations 1 and 3 as follows:

$$I_{FS}(T) = \frac{V_{IG}}{R_T(T)} \cdot \frac{(R_{CS1} + R_{CS2})}{DCR(T)} . \qquad (4)$$

With Rs and Rp as additional free variables, use a spreadsheet to solve equation 4 for the desired full scale current while minimizing the $I_{FS}(T)$ variation over temperature.

ERROR MANAGEMENT

Component value errors external to the IR3725 contribute to power and current measurement error. The power reported by the IR3725 is a function not only of actual power or current, but also of products and quotients of R_T, R_{CS1}, R_{CS2}, DCR (or R_{SHUNT}), as well as parameters internal to the IR3725. The tolerance of these components increases the total power or current error. Small signal resistors are typically available in 1% tolerance, but 0.1% parts are available. Shunts are also available at 1% or 0.1% tolerance. The DCR tolerance of inductors can be 5%, but 3% are available. Fortunately, it is not typical that worst-case errors would systematically stack in one direction. It is statistically likely that a high going value would be paired with a low going value to somewhat cancel the error. Because of this, tolerances can be added in quadrature (RSS). As an example, a 3% DCR used with a 1% R_T, a 1% R_{CS}, and 1.5% IR3725 contributes

$$\sqrt{(0.03)^2 + (0.01)^2 + (0.01)^2 + (0.015)^2} \approx 3.6\%$$

error to a typical system.

Quantization error occurs in digital systems because the full scale is partitioned into a finite number of intervals and the number of the interval containing the measured value is reported. It is not likely that the measured value would correspond exactly to the center of the interval. The error could be as large as half the width of the interval. With a binary word size of eight, full scale is partitioned into 255 intervals. Consider a measurement made near full scale. Any signal in this interval is less than ± .2% (one-half of 100% / 256) away from the interval's center, and would therefore never have more error than that due to quantization. On the other hand, consider a measurement at one-tenth full scale. One-half of an interval size at this level corresponds to 2% of the reported value! Relative quantization error increases as the measured value becomes small compared to the full-scale value.
Quantization error can be reduced by averaging a sequence of returned values.

LAYOUT GUIDELINES

The following guidelines will minimize noise and error. Refer to the Functional Description Diagram.

1. Bypass VDD to GND with a high quality ceramic capacitor.
2. Place Ccs2 close to IC pins Vcs1 and Vcs2. Route Vcs1 and Vcs2 to the current sensing element as a differential pair.
3. Sense the current sensing element at its terminals, Kelvin style. Current and power will be over reported if printed wire board resistance is included between the sense points.
4. If inductor DCR current sensing is used, place the compensating thermistor near the inductor. Route the thermistor leads back to the vicinity of the IC with differential routing. Void any vias going to ground along the path back until near the IC. Locate the thermistor network (not the thermistor) near the IC.
5. VO should sense the voltage at the point of interest. Bypass VO to GND with a high quality ceramic capacitor near the IC.
6. Use an isolated dedicated ground plane connected only to grounded components associated with the IC in the figure. Connect this dedicated ground plane at one location to the ground of the monitored voltage.
7. Do not connect pin 12 to any electrically active node.

CONFIGURATION REGISTER

A configuration register is maintained via the serial bus MFR_SPECIFIC_00 command, code # D0h. The low order nibble (d3, d2, d1, d0) contains a binary number N from zero to eight. The averaging interval is 2^N milliseconds. N defaults to zero on start up.

The next bit (d4) is to be used as a function shutdown bit. b'1 commands an energy saving shutdown mode, and power on default b'0 commands fully functioning mode.

d5 high enables the EXTCLK pin to receive the external clock signal, and default d5 low enables the internal clock.

The next two bits (d7, d6) program the output parameter. B'00 causes power to be measured and is the power on default state. B'01 causes voltage to be measured. B'10 causes current to be measured. B'11 is not defined and should not be used.

The next bit (d8) is used to configure the ALERT# pin. b'0 is the power on default, and commands ALERT# to be pulled low when new data is available. b'1 programs the ALERT# to pull low when the programmable threshold level is exceeded, whether it is power, voltage, or current.

Register bits (d15...d9) are the ALERT# threshold register. If the output register is larger than this register, and if (d8) is b'1, then the ALERT# pin will pull low. The two least significant bits of the output register are not represented in the ALERT# threshold register. d15…d9 defaults to zero on start up.

The results of a configuration register change will be reflected in the OUTPUT REGISTER after previously requested operations have completed. Initialize the configuration register after start up.

BIT #	CONFIGURATION REGISTER
d0	Averaging interval (LSB)
d1	Averaging interval
d2	Averaging interval
d3	Averaging interval (MSB)
d4	Shutdown
d5	External clock
d6	OUTPUT config (LSB)
d7	OUTPUT config (MSB)
d8	ALERT# configuration
d9	ALERT# threshold (LSB + 2)
d10	ALERT# threshold
d11	ALERT# threshold
d12	ALERT# threshold
d13	ALERT# threshold
d14	ALERT# threshold
d15	ALERT# threshold (MSB)

OUTPUT REGISTER

The output register is loaded with a two's compliment factor of voltage, current, or power, depending on the last request loaded into the configuration register. Serial bus "Direct Data Format" is used. The value of the output register is to be multiplied by a scale factor that is derived below to yield power, voltage, or current in engineering units of watts, volts, or amps. Maximum power is the product of maximum voltage and maximum current.
The range of valid output register values is indicated in Table 2 below.

Table 2 Output Register Range of Returned Values

Parameter	Returned value (twos compliment binary)	Returned value (decimal)
FS voltage	0100 0000 0000 0000	256
Zero voltage	0000 0000 0000 0000	0
+FS current	0100 0000 0000 0000	256
-FS current	1100 0000 0000 0000	-256
+FS power	0100 0000 0000 0000	256
-FS power	1100 0000 0000 0000	-256

A binary point is implicitly located to the left of the first six least significant figures, as in the example below.

SYYY YYYY YY.00 0000

The "S" above is the twos compliment sign bit, and the "Y's" are the twos compliment integers. Six zeros pad out the two byte response. These padding zeros could be considered a factor of the slope, which is allowed by the Direct Data Format. The output register multiplied by its scale factor K_x yields the requested quantity in engineering units, volts, amps, or watts.

The equations below convert digital counts to engineering units:

Voltage = counts * V_{FS} / 256

Current = counts * V_{IG} * (R_{CS1}+R_{CS2}) / (R_T * DCR * 256)

Power = counts * V_{FS}*V_{IG}*(Rcs1 + Rcs2) / (R_T*DCR*256)

There is but one output register, and it holds the measurement type (voltage, current, or power) last requested by the configuration register. It is incumbent upon the user to establish correct configuration before requesting a read. READ_VOUT, READ_IOUT, and READ_POUT are equivalent in that each returns the contents of the same output register.

BIT#	OUTPUT REGISTER
d15:d0	Output variable, D0 is LSB

RESERVED COMMAND CODES

Command codes D2h through D5h, D7h, and D8h are reserved for manufacturing use only and could lead to undesirable device behavior.

PACKET PROTOCOL

S = Start Condition
W = Bus write (0)
R = Bus read (1)
A = Acknowledge, = 0 for ACK, =1 for NACK
P = Stop Condition

	=	master to slave
	=	slave to master

Bus Write CONFIGURATION Register

S	Slave Address	W	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P
S	see Table 1	0	A	1 1 0 1 0 0 0 0	A	d7 d6 d5 d4 d3 d2 d1 d0	A	d15 d14 d13 d12 d11 d10 d9 d8	A	P

Bus Read CONFIGURATION Register

S	Slave Address	W	A	Command Code	A	S	Slave Address	R	A	Data Byte Low	A	Data Byte High	A	P
S	see Table 1	0	A	1 1 0 1 0 0 0 0	A	S	See Table 1	1	A	d7 d6 d5 d4 d3 d2 d1 d0	A	d15 d14 d13 d12 d11 d10 d9 d8	1	P

Bus READ_VOUT (Output Register for Configuration register Data Byte Low = 01XXXXXX)

S	Slave Address	W	A	Command Code	A	S	Slave Address	R	A	Data Byte Low	A	Data Byte High	A	P
S	see Table 1	0	A	1 0 0 0 1 0 1 1	A	S	See Table 1	1	A	d7 d6 d5 d4 d3 d2 d1 d0	A	d15 d14 d13 d12 d11 d10 d9 d8	1	P

Bus READ_IOUT (Output Register for Configuration register Data Byte Low = 10XXXXXX)

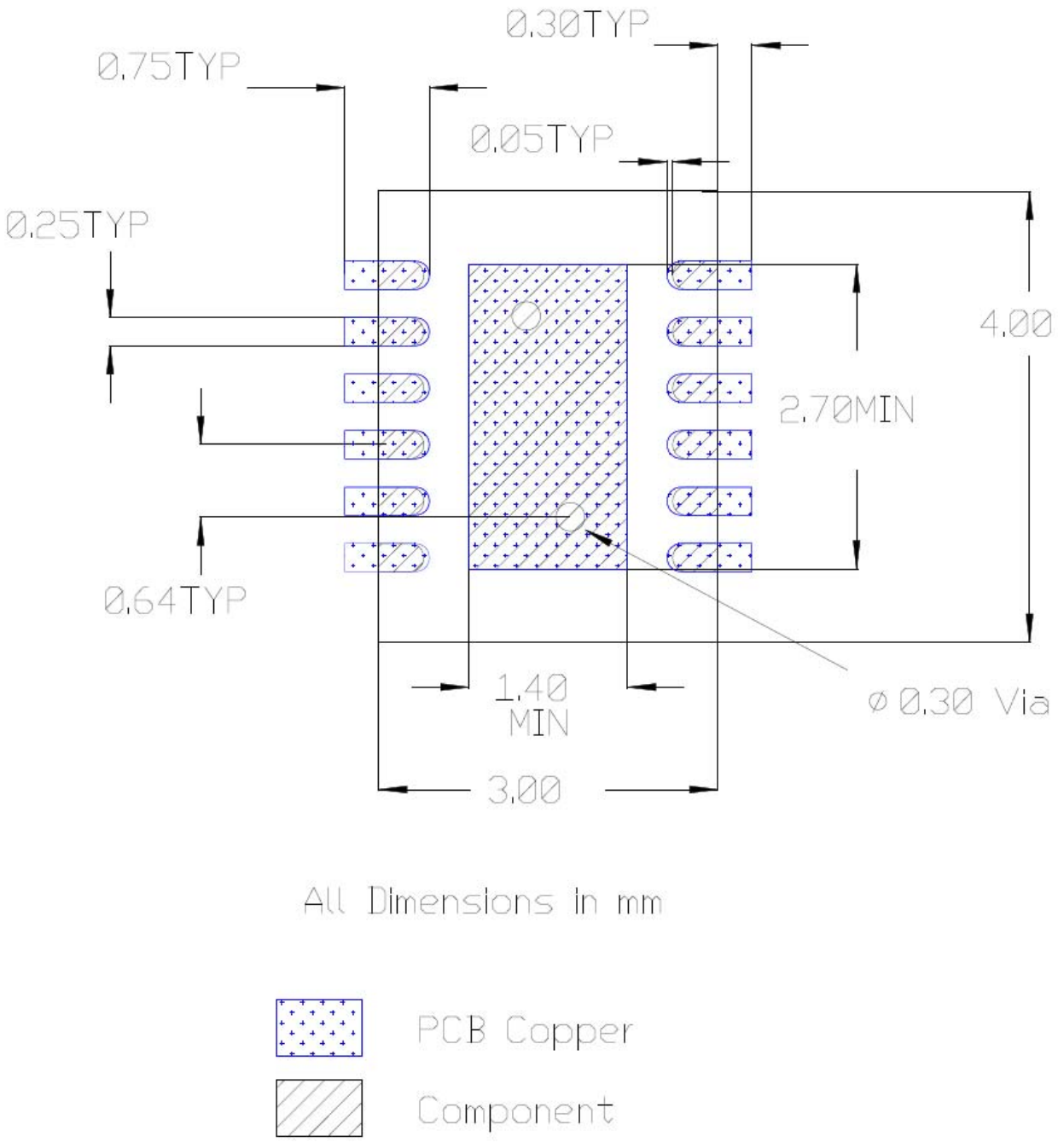
S	Slave Address	W	A	Command Code	A	S	Slave Address	R	A	Data Byte Low	A	Data Byte High	A	P
S	see Table 1	0	A	1 0 0 0 1 1 0 0	A	S	See Table 1	1	A	d7 d6 d5 d4 d3 d2 d1 d0	A	d15 d14 d13 d12 d11 d10 d9 d8	1	P

Bus READ_POUT (Output Register for Configuration register Data Byte Low = 00XXXXXX)

S	Slave Address	W	A	Command Code	A	S	Slave Address	R	A	Data Byte Low	A	Data Byte High	A	P
S	see Table 1	0	A	1 0 0 1 0 1 1 0	A	S	See Table 1	1	A	d7 d6 d5 d4 d3 d2 d1 d0	A	d15 d14 d13 d12 d11 d10 d9 d8	1	P

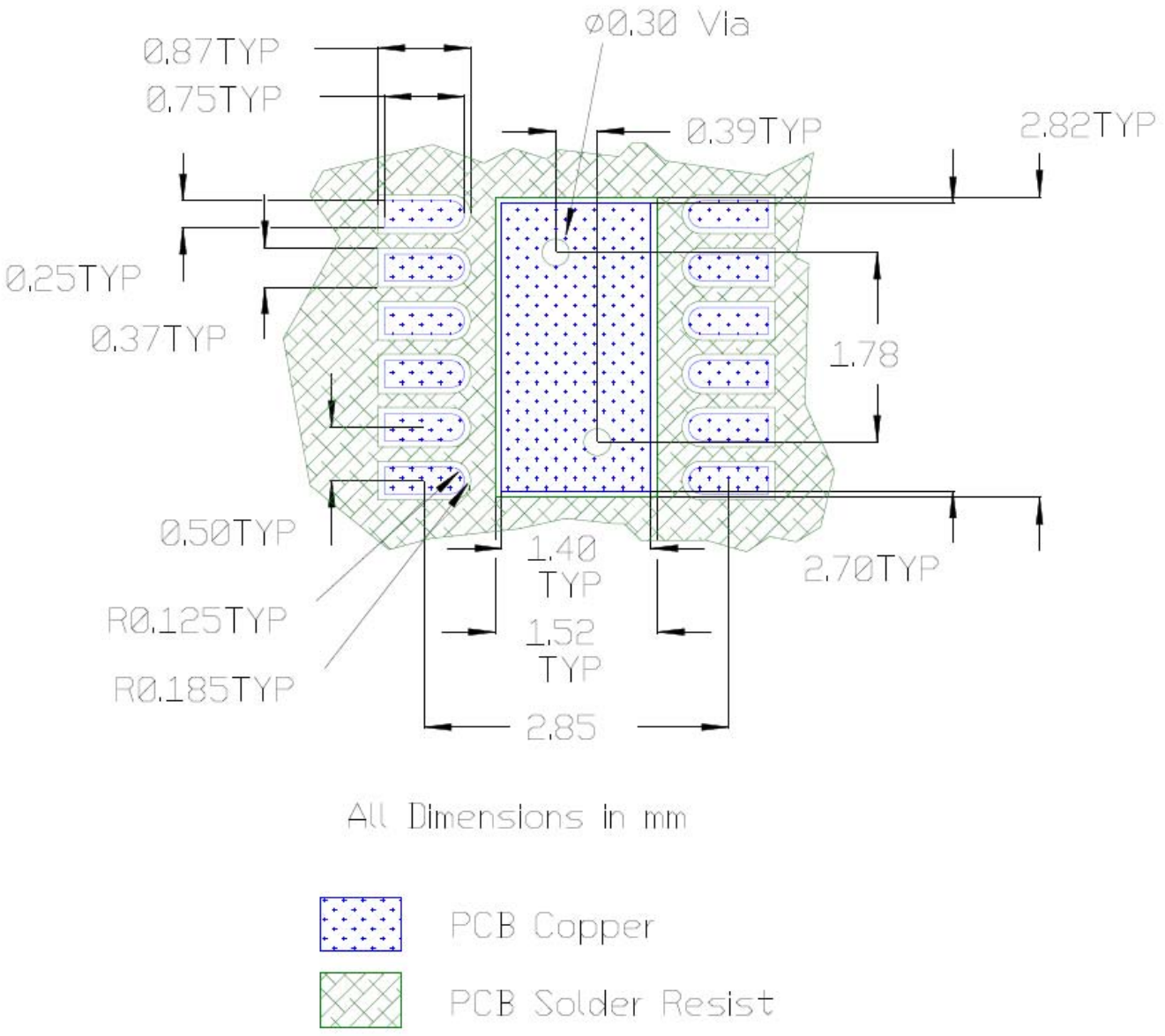
PCB PAD AND COMPONENT PLACEMENT

The figure below shows a suggested pad and component placement.



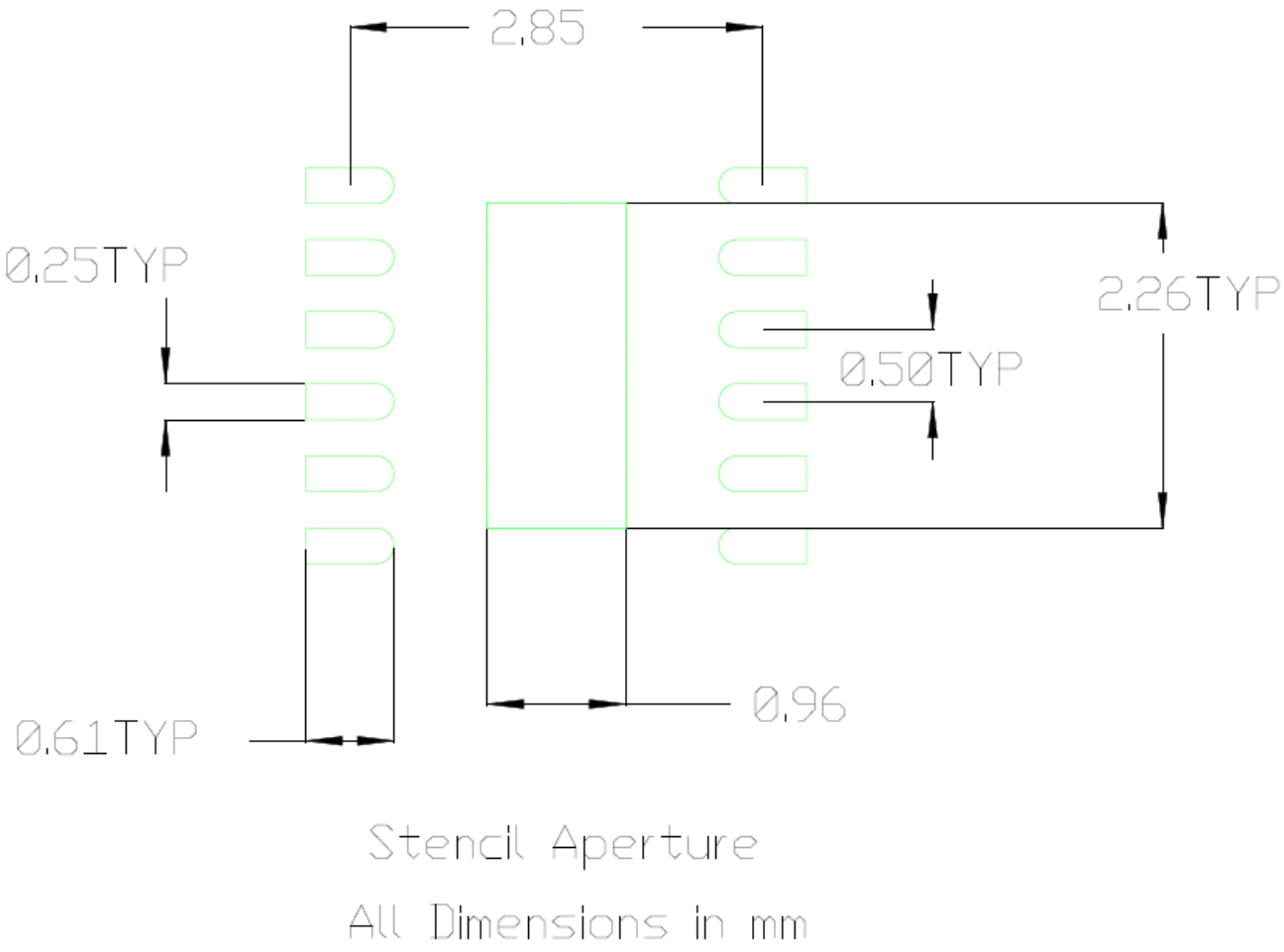
SOLDER RESIST

The figure below shows a suggested solder resist placement.



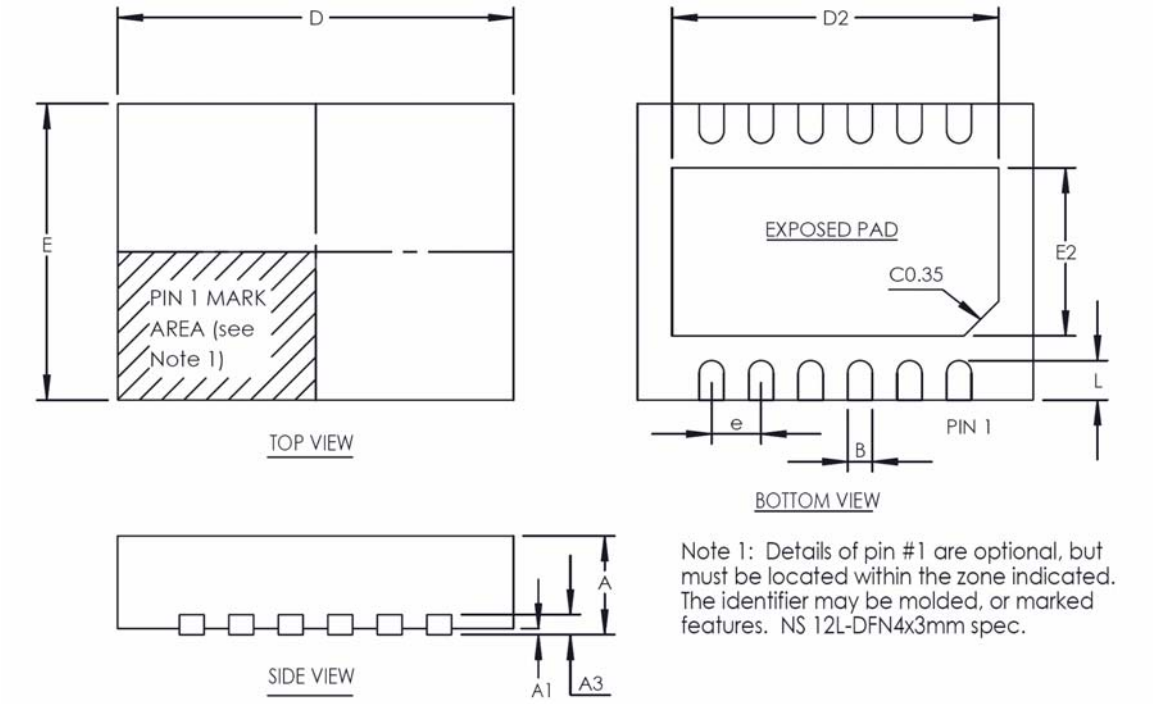
STENCIL DESIGN

The figure below shows a suggested solder stencil design.



PACKAGE INFORMATION

4 X 3 MM 12L DFN LEAD FREE



Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features. NS 12L-DFN4x3mm spec.

SYMBOL	12-PIN 4x3 (unit: MM)		
DESIGN	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0.00	0.025	0.05
A3		0.20 REF	
B	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	3.20	3.30	3.40
E	2.90	3.00	3.10
E2	1.60	1.70	1.80
e		0.5 TYP	
L	0.30	0.40	0.50

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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