

# PSMN1R4-40YLD

N-channel 40 V 1.4 m $\Omega$  logic level MOSFET in LFPAK56 using NextPower-S3 technology

26 August 2014

**Product data sheet** 

## 1. General description

Logic level gate drive N-channel enhancement mode MOSFET in 175 °C LFPAK56 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

#### 2. Features and benefits

- NextPower-S3 technology delivers 'superfast switching with soft recovery'
- Low Q<sub>RR</sub>, Q<sub>G</sub> and Q<sub>GD</sub> for high system efficiency and low EMI designs
- Schottky-Plus body-diode, gives soft switching without the associated high I<sub>DSS</sub> leakage
- Optimised for 4.5 V gate drive utilising NextPower-S3 Superjunction technology
- High reliability LFPAK (Power-SO8) package, copper-clip, solder die attach and qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

## 3. Applications

- Synchronous rectification
- DC-to-DC converters
- High performance & high efficiency server power supply
- Motor control
- Power OR-ing

#### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	-	40	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; <u>Fig. 2</u>	[1]	-	-	100	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	-	238	W
Tj	junction temperature			-55	-	175	°C
Static characte	eristics						,
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ Fig. 10		-	1.12	1.4	mΩ





Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		$V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10	-	1.38	1.85	mΩ
Dynamic cha	racteristics					
$Q_{GD}$	gate-drain charge	$V_{GS}$ = 4.5 V; $I_D$ = 25 A; $V_{DS}$ = 20 V; Fig. 12; Fig. 13	-	13	-	nC
Q <sub>G(tot)</sub>	total gate charge	$V_{GS}$ = 4.5 V; $I_D$ = 25 A; $V_{DS}$ = 20 V; Fig. 12; Fig. 13	-	45	-	nC

<sup>[1]</sup> Continuous current is limited by package.

## 5. Pinning information

**Table 2. Pinning information** 

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D I
2	S	source	<u> </u>	
3	S	source	q j	G_U: 4
4	G	gate	טַטַטַט	mbb076 S
mb	D	mounting base; connected to drain	1 2 3 4 LFPAK56; Power- SO8 (SOT669)	

# 6. Ordering information

Table 3. Ordering information

Type number	Package	kage				
	Name	Description	Version			
PSMN1R4-40YLD	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669			

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R4-40YLD	1D440L

**Product data sheet** 

# **Limiting values**

Table 5. **Limiting values** 

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	40	V
$V_{DSM}$	peak drain-source voltage	$t_p \le 20 \text{ ns; } f \le 500 \text{ kHz;}$ $E_{DS(AL)} \le 200 \text{ nJ; pulsed}$		-	45	V
$V_{DGR}$	drain-gate voltage	25 °C ≤ $T_j$ ≤ 175 °C; $R_{GS}$ = 20 kΩ		-	40	V
V <sub>GS</sub>	gate-source voltage			-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	238	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	[1]	-	100	Α
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <u>Fig. 2</u>	[1]	-	100	Α
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 °C$ ; Fig. 3		-	1201	Α
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature			-	260	°C
V <sub>ESD</sub>	electrostatic discharge voltage	НВМ		2	-	kV
Source-drain	diode			'		
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	-	100	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	1201	Α
Avalanche ru	ggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$T_{j(init)}$ = 25 °C; $I_D$ = 74 A; $R_{GS}$ = 50 Ω; unclamped; $t_p$ = 0.23 ms; $V_{GS}$ = 10 V; $V_{sup} \le$ 40 V	[2]	-	446	mJ
		$V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 25 A; $V_{sup}$ ≤ 40 V; $R_{GS}$ = 50 Ω; unclamped; $t_D$ = 2.52 ms	[2]	-	1641	mJ

Continuous current is limited by package. Protected by 100% test

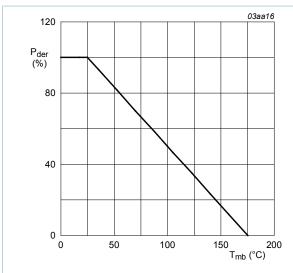
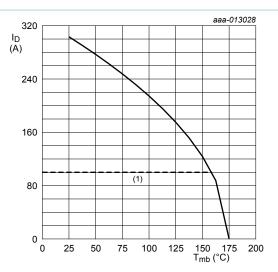


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$



(1) Capped at 100A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \ge 5V$$

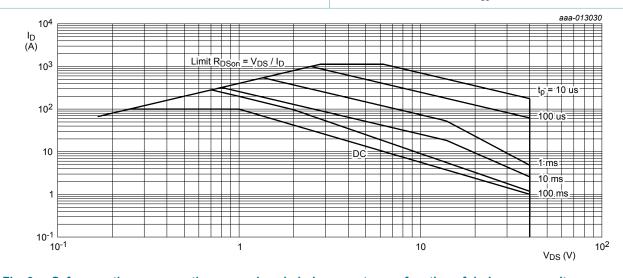


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb} = 25$ °C;  $I_{DM}$  is a single pulse

#### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 4	-	0.56	0.63	K/W

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance	<u>Fig. 5</u>	-	50	-	K/W
	from junction to ambient	Fig. 6	-	125	-	K/W

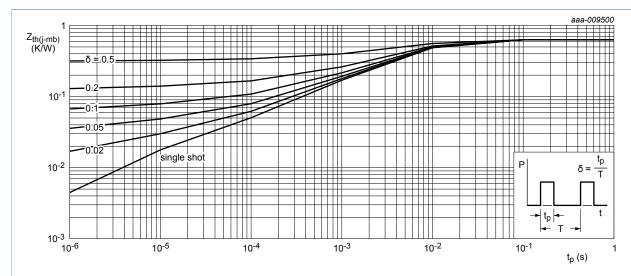


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

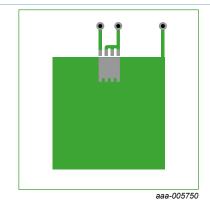


Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

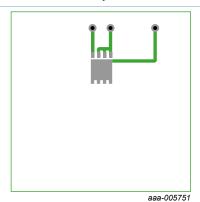


Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

#### 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Static characteristics							
V <sub>(BR)DSS</sub>		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$		40	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$		36	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$		1.05	1.7	2.2	V

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T <sub>j</sub> ≤ 150 °C	-	-4.8	-	mV/K
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 32 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	-	1	μA
		V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 125 °C	-	12	-	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	100	nA
		V <sub>GS</sub> = -16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <u>Fig. 10</u>	-	1.12	1.4	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; Fig. 11; Fig. 10	-	-	2.65	mΩ
		$V_{GS}$ = 4.5 V; $I_{D}$ = 25 A; $T_{j}$ = 25 °C; Fig. 10	-	1.38	1.85	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; Fig. 11; Fig. 10	-	-	3.4	mΩ
$R_G$	gate resistance	f = 1 MHz	-	1.1	-	Ω
Dynamic ch	aracteristics			'		
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 10 V; Fig. 12; Fig. 13	-	96	-	nC
		I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 4.5 V; Fig. 12; Fig. 13	-	45	-	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V	-	85	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 4.5 V;	-	15	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate- source charge	Fig. 12; Fig. 13	-	9	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate- source charge		-	6	-	nC
$Q_{GD}$	gate-drain charge		-	13	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; <u>Fig. 12</u> ; <u>Fig. 13</u>	-	2.7	-	V
C <sub>iss</sub>	input capacitance	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	6661	-	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 14</u>	-	1543	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	299	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS}$ = 20 V; $R_L$ = 0.8 $\Omega$ ; $V_{GS}$ = 4.5 V;	-	39	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5 \Omega$	-	49	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	47	-	ns
t <sub>f</sub>	fall time	1	-	30	-	ns

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Q <sub>oss</sub>	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}$		-	50	-	nC
Source-drain	diode						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 15$		-	0.78	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$		-	47	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 20 V; <u>Fig. 16</u>	[1]	-	61	-	nC
t <sub>a</sub>	reverse recovery rise time	$I_S$ = 25 A; $dI_S/dt$ = -100 A/ $\mu$ s; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; Fig. 16		-	25.4	-	ns
t <sub>b</sub>	reverse recovery fall time			-	21.7	-	ns

#### [1] includes capacitive recovery

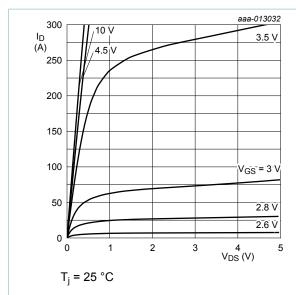


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

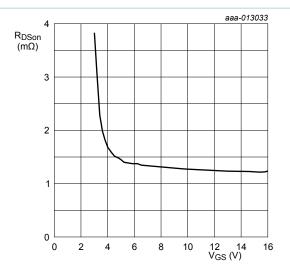


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^{\circ}C; \ I_D = 25A$$

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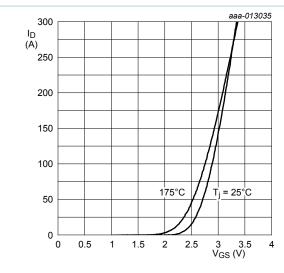


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

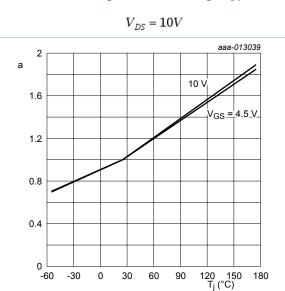


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

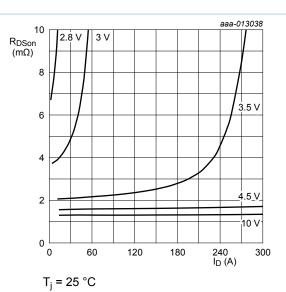


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

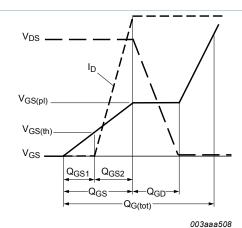


Fig. 12. Gate charge waveform definitions

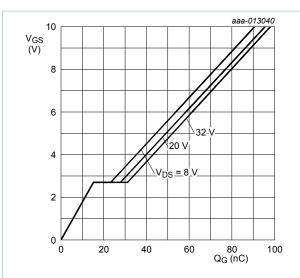


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}C; \ I_D = 25A$$

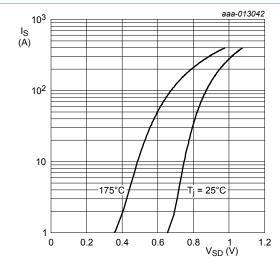


Fig. 15. Source current as a function of source-drain voltage; typical values

$$V_{GS} = 0V$$

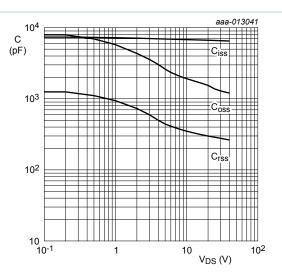


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

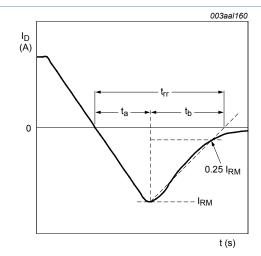
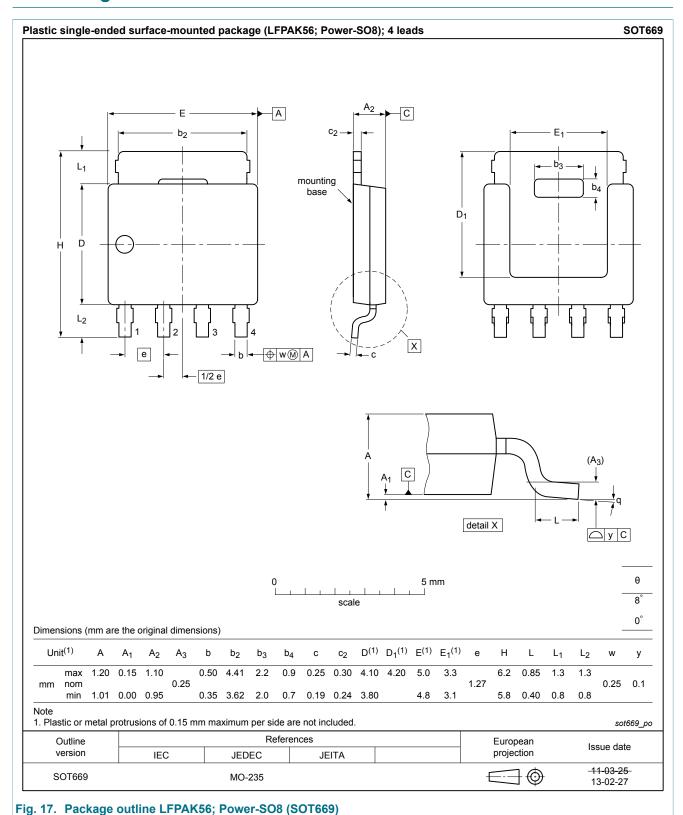


Fig. 16. Reverse recovery timing definition

## 11. Package outline



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