



DS21349 3.3V T1/J1 Line Interface Unit

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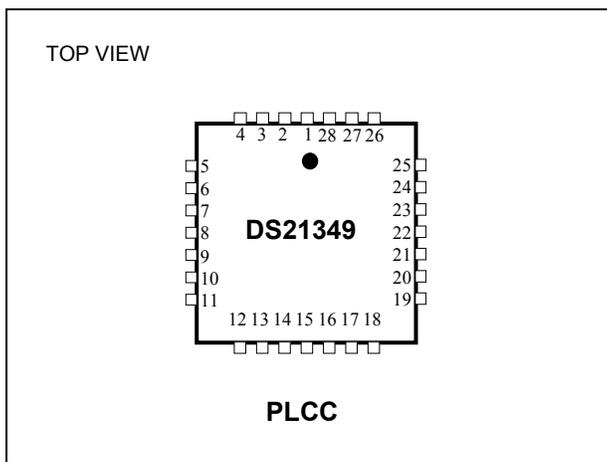
GENERAL DESCRIPTION

The DS21349 is a fully integrated LIU for long-haul or short-haul T1 applications over twisted-pair installations. It interfaces to two twisted-pair lines—one pair for transmit and one pair for receive through an appropriate network interface. The device can be configured for control through software or hardware mode. Software control is accomplished over a serial port in hardware mode; individual pin settings allow stand-alone operation. The device provides a precise, crystal-less jitter attenuator that can be placed in either the transmit or receive path.

APPLICATIONS

Routers
Data Service Units (DSUs)
Channel Service Units (CSUs)
Muxes
Switches
Channel Banks
T1/E1 Test Equipment

PIN CONFIGURATION



FEATURES

- Fully Integrated Line Interface Unit (LIU)
- Pin Compatible with LevelOne LXT362
- Supports Both Long Haul and Short Haul
- Crystal-Less Jitter Attenuator
- Jitter Attenuator Programmable for Transmit or Receive Path
- Meets ANSI T1.102, T1.403, T1.408, and AT&T 62411
- Usable Receive Sensitivity of 0dB to -36dB That Allows the Device to Operate on 0.63mm (22AWG) Cables Up to 6k Feet in Length
- Five Line Build-Out Settings for Short-Haul Applications
- Four CSU Filters from 0dB to -22.5dB
- Transmit/Receive Performance Monitors with Driver-Fail, Monitor-Open, and Loss-of-Signal Outputs
- Bipolar or NRZ Interface
- Programmable B8ZS Encoder/Decoder
- QRSS Generator/Detector
- Local, Remote, and Analog Loopbacks
- Generates and Detects In-Band Loop-Up and Loop-Down Codes
- Serial Interface Provides Access to Control Registers

ORDERING INFORMATION

| PART | TEMP RANGE | PIN-PACKAGE |
|------------|----------------|-------------|
| DS21349Q | 0°C to +70°C | 28 PLCC |
| DS21349Q+ | 0°C to +70°C | 28 PLCC |
| DS21349QN | -40°C to +85°C | 28 PLCC |
| DS21349QN+ | -40°C to +85°C | 28 PLCC |

+Denotes lead-free/RoHS-compliant package.

Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.

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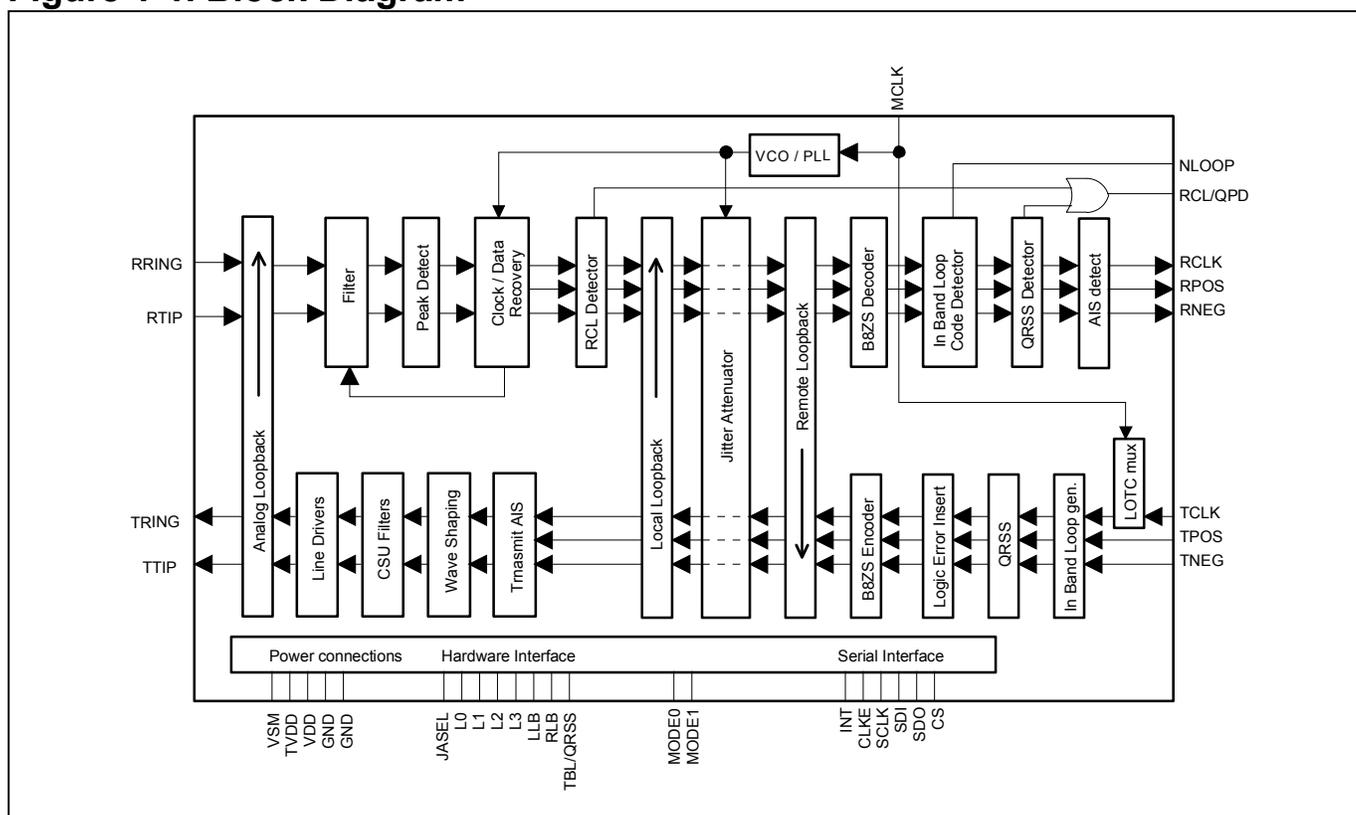
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1. DETAILED DESCRIPTION

The DS21349 is a complete T1 line interface unit (LIU) for short-haul and long-haul applications. Receive sensitivity adjusts automatically to the incoming signal and can be limited to -18dB, -26dB, or -36dB. The device can generate the necessary DSX-1 line build-outs or CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB. The on-board crystal-less jitter attenuator requires a 1.544MHz reference clock. The jitter attenuator FIFO is selectable to either 32 bits or 128 bits in depth and can be placed in either the transmit or receive data paths. The DS21349 has diagnostic capabilities such as loopbacks and QRSS pattern generation and detection. The device can also generate and detect the in-band loop-up and loop-down codes specified in AT&T 62411. The device can be configured for control using a serial interface, or for hardware mode. The device fully meets all of the latest T1 specifications including ANSI T1.102-1999, ANSI T1.403-1999, ANSI T1.408, and AT&T 62411.

Figure 1-1. Block Diagram



2. OPERATING MODES

The DS21349 has several pins with multiple functions and names according to the selected operating mode. These operating modes are summarized in the tables below.

Table 2-A. Operating Modes

| PIN | QRSS DISABLED | | QRSS ENABLED | |
|-----|---------------|--------|--------------|-------|
| | BIPOLAR | NRZ | BIPOLAR | NRZ |
| 1 | MCLK | | | |
| 2 | TCLK | | | |
| 3 | TPOS | TDATA | INSLER | |
| 4 | TNEG | INSBPV | INSBPV | |
| 6 | RNEG | BPV | RNEG | BPV |
| 7 | RPOS | RDATA | RPOS | RDATA |
| 8 | RCLK | | | |
| 13 | TTIP | | | |
| 16 | TRING | | | |
| 19 | RTIP | | | |
| 20 | RRING | | | |

Control pins are affected by serial port and hardware modes.

Table 2-B. Control Pins for Hardware and Software Modes

| PIN | HARDWARE MODE | | SERIAL PORT MODE | |
|-----|---------------|---------|------------------|---------|
| | NRZ | QRSS | NRZ | QRSS |
| 5 | MODE1 | | MODE1 | |
| 9 | MODE0 | | MODE0 | |
| 11 | JASEL | | N.C. | |
| 12 | RCL | RCL/QPD | RCL | RCL/QPD |
| 23 | L0 | | INT | |
| 24 | L1 | | SDI | |
| 25 | L2 | | SDO | |
| 17 | L3 | | N.C. | |
| 18 | NLOOP | | NLOOP | |
| 26 | RLB | NLB | CS | |
| 27 | LLB | ALB | SCLK | |
| 28 | TAIS | QRSS | CLKE | |

Figure 2-1. Hardware Mode Pinout

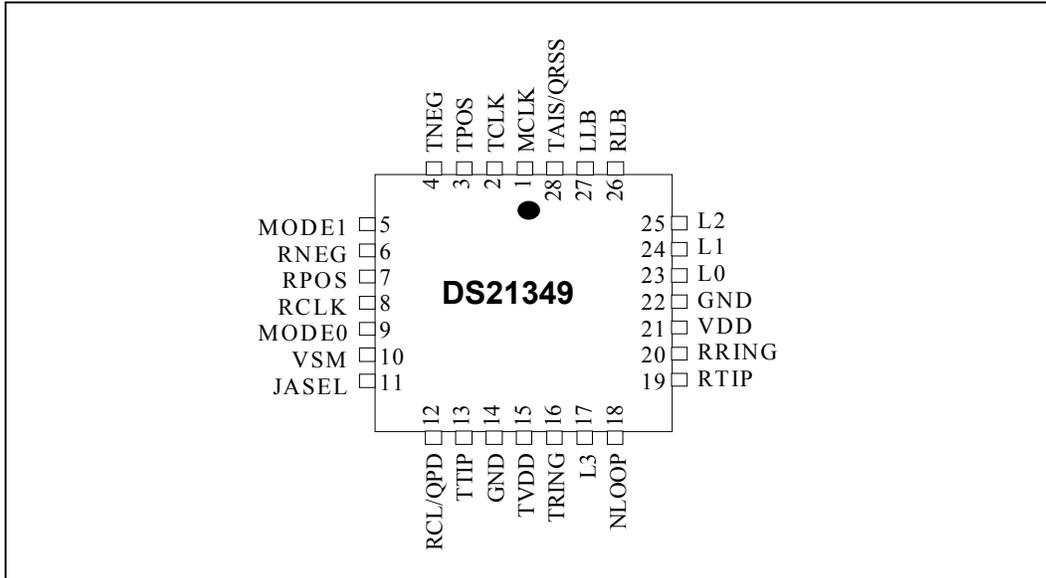


Figure 2-2. Serial Port Mode Pinout

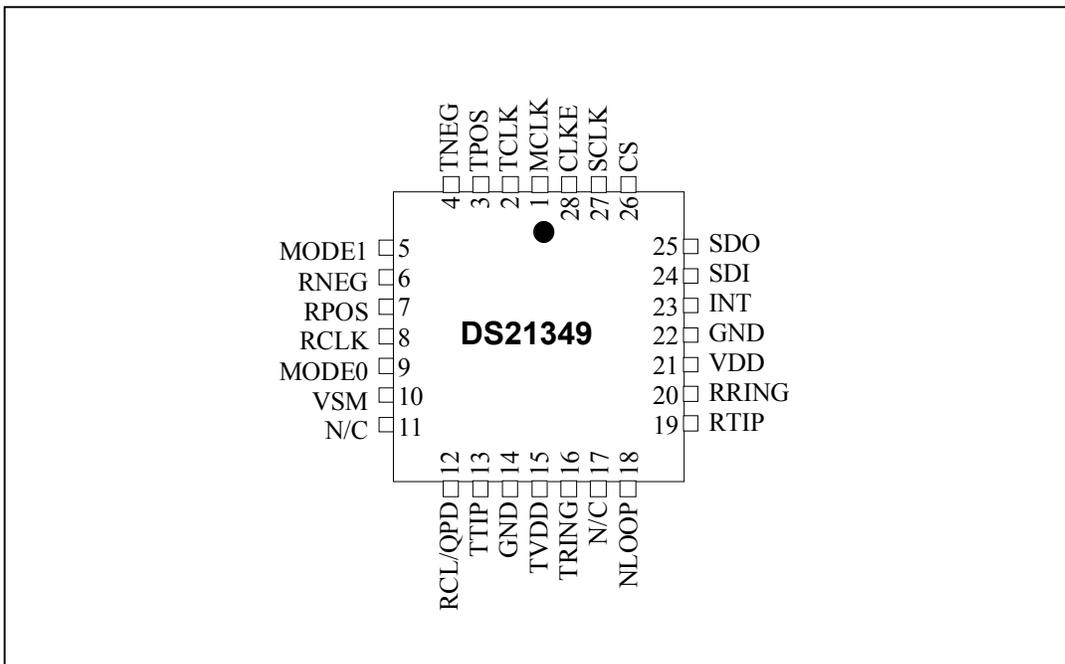


Table 2-C. Signal Descriptions

| PIN | NAME | I/O | FUNCTION |
|-----------|-------------------------|----------------|---|
| 1 | MCLK | I | Master Clock. A 1.544MHz clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. ¹ |
| 2 | TCLK | I | Transmit Clock. A 1.544MHz primary clock. Used to clock data through the transmit side formatter. Can be sourced internally by MCLK or RCLK. |
| 3 | TPOS | I | Transmit Positive Data. Sampled on the falling edge of TCLK for data to be transmitted out onto the line. |
| | TDATA | | Transmit NRZ Data. Sampled on the falling edge of TCLK for data to be transmitted onto the line. |
| | INSLER | | Transmit Insert Logic Error. Rising edge on INSLER inserts a logic error into the outbound QRSS pattern. Sampled on falling edge of TCLK. |
| 4 | TNEG | I | Transmit Negative Data. Sampled on the falling edge of TCLK for data to be transmitted out onto the line. |
| | INSBPV | | Transmit Insert Bipolar Violation. INSBPV is sampled on the falling edge of TCLK. Rising edge inserts one BPV. |
| 5 | MODE1 | I ² | Mode Select 1. Connect low to select hardware mode. Connect high to select serial port mode. See also MODE0. |
| 6 | RNEG | O | Receive Negative Data. Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with the bipolar data out of the line interface. Always valid on rising edge of RCLK in hardware mode. |
| | BPV | | Receive Bipolar Violation. Transitions high for one clock cycle marking an inbound bipolar violation. Valid on rising edge of RCLK. |
| 7 | RPOS | O | Receive Positive Data. Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with bipolar data out of the line interface. Always valid on rising edge of RCLK in hardware mode. |
| | RDATA | | Receive Data. RDATA is the NRZ output from the line interface. Set NRZE (CCR1.6) to a 1 for NRZ applications. In NRZ mode, data is output on RPOS while a received error causes a positive-going pulse synchronous with RCLK at RNEG (Section 6). |
| 8 | RCLK | O | Receive Clock. Buffered recovered clock from the line. Synchronous to MCLK in absence of signal at RTIP and RRING. |
| 9 | MODE0 | I ² | Mode Select 0. Set high to disable all output pins (including the serial control port). Set low for normal operation. Useful in board level testing. See also MODE1. |
| 10 | VSM | I | Voltage Supply Mode. Connect high for 3.3V operation. Has 10kΩ pullup. |
| 11 | JASEL | I ² | Jitter Attenuator Select 0 = Place the jitter attenuator on the transmit side 1 = Place the jitter attenuator on the receive side Float = Disable jitter attenuator Not used in software mode |
| 12 | RCL | O | Receive Carrier Loss. An output that toggles high during a receive carrier loss. |
| | $\overline{\text{QPD}}$ | | $\overline{\text{QPD}}$. Output high when QRSS detector is searching for QRSS data pattern. Output high for one-half clock cycle on bit error. Connect to external counter to count bit errors. |
| 13/ 16 | TTIP/ TRING | O | Transmit Tip and Ring. Analog line driver outputs. These pins connect through a step-up transformer to the line (Section 5). |
| 14 | VSS | — | Ground for Transmitter Block |
| 15 | TVDD | — | Positive Supply. 3.3V ±5% for the transmitter block. See also VSM pin 10. |

| PIN | NAME | I/O | FUNCTION |
|-----------|-------------------------|-------|---|
| 17 | L3 | I | LBO3. LBO0 through LBO3 are used to select transmitter output pulse, and receiver gain. |
| 18 | NLOOP | O | Network Loopback Active. Output high when RLB is activated by in-band loop-up command present for 5 seconds. Output is reset when RLP is deactivated by in-band loop-down command present for 5 seconds. Activation of remote loopback through hardware pin 26 or control bit RLB releases the NLOOP output. |
| 19/ 20 | RTIP/ RRING | I | Receive Tip and Ring. Analog inputs for clock recovery circuitry. These pins connect through a 1:1 transformer to the line (Section 6). |
| 21 | VDD | — | Positive Supply. 3.3V \pm 5%. See also VSM pin 10. |
| 22 | VSS | — | Signal Ground |
| 23 | L0 | I/O | LBO0. LBO0 through LBO3 are used to select transmitter output pulse, and receiver gain. |
| | $\overline{\text{INT}}$ | | $\overline{\text{INT}}$. Used to alert the host when one or more bits are set in the status register. |
| 24 | L1 | I | LBO1. LBO0 through LBO3 are used to select transmitter output pulse, and receiver gain. |
| | SDI | | Serial Data Input. Input for serial address and data stream. Sampled on rising of SCLK. |
| 25 | L2 | O | LBO2. LBO0 through LBO3 are used to select transmitter output pulse, and receiver gain. |
| | SDO | | Serial Data Output. Updated on falling edge of SCLK if CLKE is connected high. Updated on rising edge of SCLK if CLKE is connected low. SDO is high-Z during write cycle or when CS is high. |
| 26 | RLB | I^2 | Remote Loopback. Used to invoke remote loopback. When held high, the transmitter inputs are ignored and inbound data received at RTIP and RRING is routed to the transmitter outputs, TTIP and TRING and transmitted at the inbound recovered clock rate. |
| | NLB | | Network Loopback. Enables network loopback detection when RLB floats. |
| | $\overline{\text{CS}}$ | | Chip Select. Must be low to read or write to the device. $\overline{\text{CS}}$ is an active-low signal. |
| 27 | LLB | I^2 | Local Loopback. Used to invoke local loopback. When held high, digital inputs TPOS and TNEG are looped back to RPOS and RNEG, through the jitter attenuator if enabled. Floating this input invokes analog loopback. The analog output signal at TTIP and TRING is routed to the receive inputs RTIP and RRING. |
| | SCLK | | Serial Clock Input. Input clock to operate serial port. Max clock rate, 2.048MHz. |
| 28 | TAIS | I^2 | Transmit AIS. Input high forces transmitter to output unframed all ones. Unavailable in remote loopback. |
| | QRSS | | QRSS. Floating this pin enables QRSS pattern generator and detector. Input low enables normal transmission of data. |
| | CLKE | | Clock Edge Select 0 = Update RNEG/RPOS on falling edge of RCLK, SDO updated on rising edge of SCLK. 1 = Update RNEG/RPOS on rising edge of RCLK, SDO updated on falling edge of SCLK. |

Note 1: G.703 requires an accuracy of ± 50 ppm for T1. TR62411 and ANSI specifications require an accuracy of ± 32 ppm for T1 interfaces.

Note 2: Input pins have three operating modes.

3. INITIALIZATION AND RESET

During power-up, all control registers are cleared, disabling the transmitter outputs. The device requires a master clock supplied to the MCLK input pin to operate the PLL. This master clock must be independent, free-running, and jitter free.

A reset initializes the status and state machines for the RCL, AIS, NLOOP, and QRSS blocks. Under software control, setting the RESET bit (CR2.7) clears all registers. Allow up to 100ms for the receiver to recover from initialization.

4. REGISTER DEFINITIONS

The DS21349 contains eight registers for configuring the device and reading status. These are accessible using the serial port. [Table 4-A](#) lists the register names and addresses.

Reading or writing to the internal registers requires writing one address/command byte prior to transferring register data. The first bit written (LSb) of the address/command byte specifies whether the access is a read (1) or a write (0). The next 6 bits identify the register address.

The last bit (MSb) of the address/command byte is the burst mode bit. When the burst bit is enabled (set to 1) and a READ operation is performed, addresses 10h through 17h are read sequentially, starting at address 10h. And when the burst bit is enabled and a WRITE operation is performed, addresses 10h through 17h are written sequentially, starting at address 10h. Burst operation is stopped once address 17h is read. All data transfers are initiated by driving the \overline{CS} input low. All data transfers are terminated if the \overline{CS} input transitions high. Port control logic is disabled and SDO is tri-stated when \overline{CS} is high.

Table 4-A. Register Map

| REGISTER | SYMBOL | ADDRESS |
|----------------------------|--------|---------|
| Control Register 1 | CR1 | B010000 |
| Control Register 2 | CR2 | B010001 |
| Control Register 3 | CR3 | B010010 |
| Interrupt Mask Register | IMR | B010011 |
| Transition Status Register | TSR | B010100 |
| Status Register | SR | B010101 |
| Information Register | IR | B010110 |
| Control Register 4 | CR4 | B010111 |

Table 4-B. Register Bit Positions

| SYMBOL | 7 (MSb) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSb) |
|--------|---------|--------|--------|----------|----------|---------|-------|---------|
| CR1 | JASEL1 | JASEL0 | ENCENB | UNIENB | L3 | L2 | L1 | L0 |
| CR2 | RESET | PAT1 | PAT0 | TAIS | ENLOOP | ALB | LLB | RLB |
| CR3 | JA6HZ | TPD | — | EQZMON20 | EQZMON26 | JA128 | LIRST | TAOZ |
| IMR | Z16D | JALT | DFMO | B8ZSD | QRSS | AIS | NLOOP | RCL |
| TSR | Z16D | JALT | DFMO | B8ZSD | QRSS | AIS | NLOOP | RCL |
| SR | — | — | DFMO | — | QRSS | AIS | NLOOP | RCL |
| IR | RL3 | RL2 | RL1 | RL0 | LUP | LDN | TSCD | LOTG |
| CR4 | — | — | — | — | — | RCL2048 | XFMR2 | XFMR1 |

Note: Set unused bits to 0 for normal operation.

CR1 (B010000): Control Register 1

| MSb | | | | LSb | | | |
|--------|--------|--------|--------|-----|----|----|----|
| JASEL1 | JASEL0 | ENCENB | UNIENB | L3 | L2 | L1 | L0 |

| SYMBOL | POSITION | FUNCTION |
|--------|----------|--|
| JASEL1 | CR1.7 | Jitter attenuator select (Table 4-C) |
| JASEL0 | CR1.6 | Jitter attenuator select (Table 4-C) |
| ENCENB | CR1.5 | B8ZS and NRZ control (Table 4-D) |
| UNIENB | CR1.4 | BPV and NRZ control (Table 4-D) |
| L3 | CR1.3 | Line build-out control (Table 4-E) |
| L2 | CR1.2 | Line build-out control (Table 4-E) |
| L1 | CR1.1 | Line build-out control (Table 4-E) |
| L0 | CR1.0 | Line build-out control (Table 4-E) |

Table 4-C. Jitter Attenuator Selection

| JASEL1 | JASEL0 | JITTER ATTENUATOR FUNCTION |
|--------|--------|----------------------------|
| 0 | 1 | Transmit path |
| 1 | 1 | Receive path |
| X | 0 | Disabled |

Table 4-D. Line Code and Interface Selection

| UNIENB | ENCENB | LINE CODE | INTERFACE |
|--------|--------|-----------|-----------|
| 0 | 0 | AMI | Bipolar |
| 1 | 0 | AMI | NRZ |
| X | 1 | B8ZS | NRZ |

Table 4-E. Line Build-Out Selection

| L3 | L2 | L1 | L0 | APPLICATION | OUTPUT SIGNAL | Rx GAIN (dB) |
|----|----|----|----|---------------|------------------------|--------------|
| 0 | 0 | 0 | 0 | T1 Long Haul | 0dB | 36 |
| 0 | 0 | 1 | 0 | T1 Long Haul | -7.5dB | 36 |
| 0 | 1 | 0 | 0 | T1 Long Haul | -15dB | 36 |
| 0 | 1 | 1 | 0 | T1 Long Haul | -22.5dB | 36 |
| 0 | 0 | 0 | 1 | T1 Long Haul | 0dB | 26 |
| 0 | 0 | 1 | 1 | T1 Long Haul | -7.5dB | 26 |
| 0 | 1 | 0 | 1 | T1 Long Haul | -15dB | 26 |
| 0 | 1 | 1 | 1 | T1 Long Haul | -22.5dB | 26 |
| 1 | 0 | 0 | 1 | D4 Short Haul | 6V | 18 |
| 1 | 0 | 1 | 1 | T1 Short Haul | DSX-1 (0ft to 133ft) | 18 |
| 1 | 1 | 0 | 0 | T1 Short Haul | DSX-1 (133ft to 266ft) | 18 |
| 1 | 1 | 0 | 1 | T1 Short Haul | DSX-1 (266ft to 399ft) | 18 |
| 1 | 1 | 1 | 0 | T1 Short Haul | DSX-1 (399ft to 533ft) | 18 |
| 1 | 1 | 1 | 1 | T1 Short Haul | DSX-1 (533ft to 655ft) | 18 |

CR2 (B010001): Control Register 2

| MSb | | | | | | LSb | |
|-------|------|------|------|--------|-----|-----|-----|
| RESET | PAT1 | PAT0 | TAIS | ENLOOP | ALB | LLB | RLB |

| SYMBOL | POSITION | FUNCTION |
|--------|----------|---|
| RESET | CR2.7 | Resets device states and clears all registers. |
| PAT1 | CR2.6 | Selects output data pattern (Table 4-F). |
| PAT0 | CR2.5 | Selects output data pattern (Table 4-F). |
| TAIS | CR2.4 | 0 = Transmit data normally 1 = Transmit unframed all ones |
| ENLOOP | CR2.3 | 0 = Disable in-band loop-code detection 1 = Enable in-band loop-code detection |
| ALB | CR2.2 | 0 = Disable analog loopback 1 = Enable analog loopback |
| LLB | CR2.1 | 0 = Disable local loopback 1 = Enable local loopback |
| RLB | CR2.0 | 0 = Disable remote loopback 1 = Enable remote loopback |

Table 4-F. Data Pattern Selection

| PAT0 | PAT1 | DATA SOURCE |
|------|------|-----------------------|
| 0 | 0 | TPOS/TNEG |
| 0 | 1 | Transmit QRSS |
| 1 | 0 | In-band loop-up 00001 |
| 1 | 1 | In-band loop-down 001 |

CR3 (B010010): Control Register 3

| MSb | | | | | | LSb | |
|-------|-----|---|----------|----------|-------|-------|------|
| JA6HZ | TPD | — | EQZMON20 | EQZMON26 | JA128 | LIRST | TAOZ |

| SYMBOL | POSITION | FUNCTION |
|----------|----------|--|
| JA6HZ | CR3.7 | 0 = Set bandwidth of jitter attenuator to 3Hz 1 = Set bandwidth of jitter attenuator to 6Hz; not available if JA128 = 1 |
| TPD | CR3.6 | 0 = Enable transmitter outputs 1 = Disable transmitter outputs |
| — | CR3.5 | — |
| EQZMON20 | CR3.4 | 0 = Normal receiver operation 1 = Add 20dB of resistive gain to inbound signal |
| EQZMON26 | CR3.3 | 0 = Normal receiver operation 1 = Add 26dB of resistive gain to inbound signal |
| JA128 | CR3.2 | 0 = Jitter attenuator buffer depth = 32 bits 1 = Jitter attenuator buffer depth = 128 bits |
| LIRST | CR3.1 | 0 = Normal operation 1 = Reset the receive LIU state machine |
| TAOZ | CR3.0 | 0 = Disable transmit alternate 1s and 0s 1 = Enable transmit alternate 1s and 0s |

IMR (B010011): Interrupt Mask Register

MSb

LSb

| | | | | | | | |
|------|------|------|-------|------|-----|-------|-----|
| Z16D | JALT | DFMO | B8ZSD | QRSS | AIS | NLOOP | RCL |
|------|------|------|-------|------|-----|-------|-----|

| SYMBOL | POSITION | FUNCTION |
|--------|----------|---|
| Z16D | IMR.7 | 0 = Enable 16-zero detect interrupt 1 = Disable 16-zero detect interrupt |
| JALT | IMR.6 | 0 = Enable jitter-attenuator limit-trip interrupt 1 = Disable jitter-attenuator limit-trip interrupt |
| DFMO | IMR.5 | 0 = Enable driver-open interrupt 1 = Disable driver-open interrupt |
| B8ZSD | IMR.4 | 0 = Enable B8ZS-detect interrupt 1 = Disable B8ZS-detect interrupt |
| QRSS | IMR.3 | 0 = Enable QRSS interrupt 1 = Disable QRSS interrupt |
| AIS | IMR.2 | 0 = Enable AIS interrupt 1 = Disable AIS interrupt |
| NLOOP | IMR.1 | 0 = Enable network-loopback interrupt 1 = Disable network-loopback interrupt |
| RCL | IMR.0 | 0 = Enable receive carrier-loss interrupt 1 = Disable receive carrier-loss interrupt |

TSR (B010100): Transition Status Register

MSb

LSb

| | | | | | | | |
|------|------|------|-------|------|-----|-------|-----|
| Z16D | JALT | DFMO | B8ZSD | QRSS | AIS | NLOOP | RCL |
|------|------|------|-------|------|-----|-------|-----|

| SYMBOL | POSITION | FUNCTION |
|--------|----------|---|
| Z16D | TSR.7 | Set when the receiver detects 16 consecutive 0s; cleared when IMR.7 is cleared. |
| JALT | TSR.6 | Set when the jitter attenuator FIFO reaches to within 4 bits of its limit; cleared when IMR.6 is cleared. |
| DFMO | TSR.5 | Set when SR.5 changes state; cleared when IMR.5 is cleared. |
| B8ZSD | TSR.4 | Set when the receiver detects B8ZS codewords; cleared when IMR.4 is cleared. |
| QRSS | TSR.3 | Set when SR.3 changes state; cleared when IMR.3 is cleared. |
| AIS | TSR.2 | Set when SR.2 changes state; cleared when IMR.2 is cleared. |
| NLOOP | TSR.1 | Set when SR.1 changes state; cleared when IMR.1 is cleared. |
| RCL | TSR.0 | Set when SR.0 changes state; cleared when IMR.0 is cleared. |

SR (B010101): Status Register

| MSb | | | | LSb | | | |
|-----|---|------|---|------|-----|-------|-----|
| — | — | DFMO | — | QRSS | AIS | NLOOP | RCL |

| SYMBOL | POSITION | FUNCTION |
|--------|----------|---|
| — | SR.7 | — |
| — | SR.6 | — |
| DFMO | SR.5 | Set when transmitter detects open circuit. |
| — | SR.4 | — |
| QRSS | SR.3 | Set when the QRSS pattern is present at the receiver. |
| AIS | SR.2 | Set when the AIS pattern is present at the receiver. |
| NLOOP | SR.1 | Set when the in-band loop-up code is present at the receiver. |
| RCL | SR.0 | Set when receiver has detected consecutive s set forth by CR4.2. Cleared when the receiver detects 14 1s in a window of 112 clock cycles. |

IR (B010110): Information Register

| MSb | | | | LSb | | | |
|-----|-----|-----|-----|-----|-----|------|------|
| RL3 | RL2 | RL1 | RL0 | LUP | LDN | TSCD | LOTC |

| SYMBOL | POSITION | FUNCTION |
|--------|----------|---|
| RL3 | IR.7 | — |
| RL2 | IR.6 | — |
| RL1 | IR.5 | — |
| RL0 | IR.4 | — |
| LUP | IR.3 | Set when in-band loop-up code is being received. |
| LDN | IR.2 | Set when in-band loop-down code is being received. |
| TSCD | IR.1 | Set when transmitter detects a short circuit. |
| LOTC | IR.0 | Set when TCLK has not transitioned for approximately 5 μ s. |

Receive Level Indication: RL0 is the LSB and RL3 is the MSB of a 4-bit nibble that is used to indicate the inbound signal strength. Convert the binary to decimal and multiply by -2.5dB. The result indicates the approximate attenuation seen at the receiver inputs.

CR4 (B010111): Control Register 4

| MSb | | | | | LSb | | |
|-----|---|---|---|---|---------|-------|-------|
| — | — | — | — | — | RCL2048 | XFMR2 | XFMR1 |

| SYMBOL | POSITION | FUNCTION |
|---------|----------|---|
| — | CR4.7 | — |
| — | CR4.6 | — |
| — | CR4.5 | — |
| — | CR4.4 | — |
| — | CR4.3 | — |
| RCL2048 | CR4.2 | 0 = RCL threshold: 192 consecutive 0s 1 = RCL threshold: 2048 consecutive 0s |
| XFMR2 | CR4.1 | Set to 0 for use with standard transformers. Set to 1 for use with alternate transformers (Table 11-C) |
| XFMR1 | CR4.0 | Set to 0 for use with standard transformers. Set to 1 for use with alternate transformers (Table 11-C) |

5. TRANSMITTER

5.1 Transmit Digital Data Interface

Data is clocked into the device at the TCLK rate. In bipolar mode, TPOS and TNEG are the data inputs; in NRZ mode, TDATA is the data input. Input data can pass through either the jitter attenuator or the B8ZS encoder or both. In software mode, setting ENCENB enables B8ZS encoding. In hardware mode, floating the MODE1 pin enables B8ZS encoding. With B8ZS encoding enabled, the L0 through L3 inputs determine the coding and is listed in [Table 4-E](#). TCLK supplies input synchronization. See Section [12](#) for the TCLK and MCLK timing requirements.

5.2 Transmit Monitoring

In software mode, the DFMO bit in the status register is set when an open circuit in the transmitter path is detected. A transition on this bit can provide an interrupt, and a transition sets the DFMO bit in the transition status register. Setting CDFMO in the interrupt mask register, leaving a 1 in that bit location masks the interrupt.

5.3 Transmit Idle Mode

Transmit idle mode allows multiple transceivers to be connected to a single line for redundant applications. When TCLK is not present, transmit idle mode becomes active, and TTIP and TRING change to high-impedance state. Remote loopback, dual loopback, TAIS, or detection of network loop-up code in the receive direction temporarily disable the high-impedance state.

5.4 Transmit Pulse Shape

As shown in [Table 4-E](#), line build-out control inputs (L0 through L3) determine the transmit pulse shape. In software mode, these control inputs are located in control register 1; in hardware mode, these control inputs are the L0 through L3 pins.

Shaped pulses meeting the various T1, DS1, and DSX-1 specifications are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The transceiver produces DSX-1 pulses for short-haul T1 applications (settings from 0dB to 6dB of cable) and DS1 pulses for long-haul T1 applications (settings from 0dB to -22.5dB). Refer to [Table 4-E](#) for pulse mask specifications.

6. RECEIVER

A 1:1 transformer provides the interface between the twisted pair and receiver inputs RTIP and RRING. Recovered data is output at RPOS and RNEG (or RDATA in NRZ mode), and the recovered clock is output at RCLK. See Section [12](#) for receiver timing specifications.

6.1 Receive Equalizer

The receiver can apply up to 36dB of gain. Control of the equalizer is accomplished by the L0 through L3 control inputs. These control signals are detailed in [Table 4-E](#) and determine the maximum gain that is applied. In software mode, these control signals are in Control Register 1; in hardware mode, these control inputs are the L0 through L3 pins. With L0 low, up to 36dB of gain can be applied; when L0 is high, 26dB can be applied in the gain limit to provide better noise immunity in shorter loop operations.

6.2 Receive Data Recovery

The clock and data recovery engine provides input jitter tolerance that exceeds the requirements of AT&T 62411. Inbound signal is filtered, equalized, and over-sampled 16 times. Then it is applied to the B8ZS decoder if enabled.

6.3 Receive Digital-Data Interface

Recovered data is routed to the RCL monitor. In software mode, data also goes through the alarm indication signal (AIS) monitor. The jitter attenuator can be enabled or disabled in the receive path or transmit path. Received data can be routed to the B8ZS decoder or bypassed. Finally, the device can send the digital data to the framer as either bipolar or NRZ data.

6.4 Receive Monitor Mode

The receive equalizer can be used in monitor-mode applications. Monitor-mode applications require 20dB of resistive attenuation of the signal, plus an allowance for cable attenuation (less than 20dB). In software mode, setting CR3.4 (EQZMON20) enables the device to operate in monitor-mode applications that require 20dB of resistive attenuation of the signal. Setting CR3.3 (EQZMON26) enables the device to operate in monitor-mode applications that require 26dB of resistive attenuation. Setting both CR3.3 and CR3.4 enables the device to operate in monitor-mode applications that require 32dB of resistive attenuation. The monitor mode feature is not available in hardware mode.

7. JITTER ATTENUATION

The jitter attenuator only requires a jitter-free clock at 1.544MHz applied to the MCLK input. In hardware mode, the jitter attenuator is a 32-bit FIFO buffer. Pulling the JASEL pin high places the jitter attenuator in the receive path. Pulling the JASEL pin low places the jitter attenuator in the transmit path, floating the JASEL pin disables the jitter attenuator. In software mode, clearing CR1.6 (JASEL0) disables the jitter attenuator, setting CR1.6 enables the jitter attenuator. If enabled, clearing CR1.7 (JASEL1) places the jitter attenuator in the transmit path, setting CR1.7 places the jitter attenuator in the receive path. The jitter attenuator FIFO is 32 bits in length if CR3.2 (JA128) is cleared, 128 bits if set. The device clocks data in the jitter attenuator using TCLK if placed in the transmit path, and RCLK if placed in the receive path. Data is clocked out of the jitter attenuator using the dejittered clock produced by the internal PLL. When the jitter attenuator is within two bits of overflowing or underflowing, the jitter attenuator will adjust the output clock by one-eighth of a clock cycle. The jitter attenuator adds an average delay of 16 bits if the buffer depth is 32 bits in length, 64 bits if the buffer depth is 128 bits in length. In the event of an RCL condition, if the jitter attenuator is in the receive path then RCLK is derived from MCLK. Transition Status register bit TSR.6 (JALT) indicates that the jitter attenuator has adjusted the output clock. This bit is latched, when set it remains set until the software reads the bit. The JALT can also produce a hardware interrupt.

8. HARDWARE MODE

The DS21349 operates in hardware mode when the MODE1 pin is pulled low or floated. In hardware mode, configuration of the device is under control of various input pins. RPOS, RNEG, and RDATA are valid on the rising edge of RCLK only. Some functions such as INT, clock edge select, and some diagnostic modes are not available.

9. SOFTWARE MODE

The DS21349 operates in software mode when the MODE1 pin is pulled high. In software mode, a microprocessor controls the device and reads its status through the serial port, which provides access to the internal registers. The host processor can completely configure the device as well as get diagnostics and status reports through the serial port. In NRZ mode, bipolar violation insertions and logic error insertions are controlled by the BPV and INSLER pins. Similarly, the recovered clock, data, and BPV detection are available only at output pins. All other mode settings and diagnostic information are available through the serial port. [Figure 9-1](#) and [Figure 9-2](#) show the serial port data structure. The registers are accessible through a 16-bit word composed of an 8-bit command and address byte and a subsequent 8-bit data byte. Software mode allows control of the output timing. The CLKE pin determines when SDO is valid relative to SCLK and when receive data is valid relative to RCLK.

9.1 Interrupt Handling

In software mode, the DS21349 provides a latched interrupt output pin. When enabled, a change in any of the status register bits generates an interrupt. When an interrupt occurs, the INT output pin is driven low. The INT output pin structure is an open-drain only. Each device that shares the INT line requires an external pullup resistor. The interrupt is cleared when the interrupt condition no longer exists, and a 1 is written to the appropriate bit in the interrupt mask register. Leaving a 1 in any of the bits in the interrupt mask register masks that interrupt. Clearing that bit re-enables the interrupt.

Table 9-A. CLKE Pin Selection

| CLKE PIN | OUTPUT | OUTPUT UPDATED ON |
|----------|--------|-------------------|
| LOW | RPOS | Falling RCLK |
| | RNEG | |
| | RDATA | |
| | SDO | Rising SCLK |
| HIGH | RPOS | Rising RCLK |
| | RNEG | |
| | RDATA | |
| | SDO | Falling SCLK |

Figure 9-1. Serial Data Port Operation for Read Access

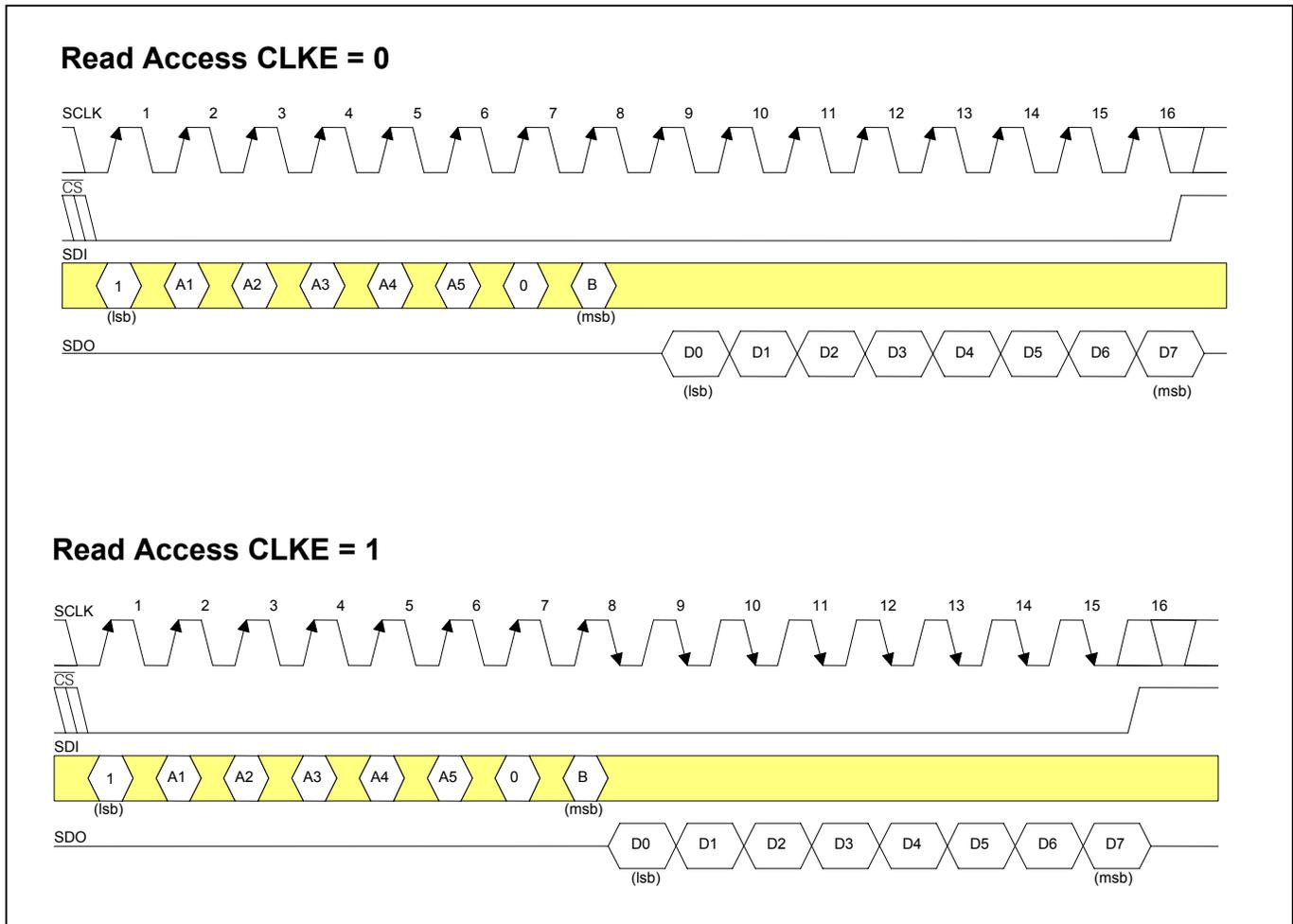


Figure 9-2. Serial Data Port Operation for Write Access

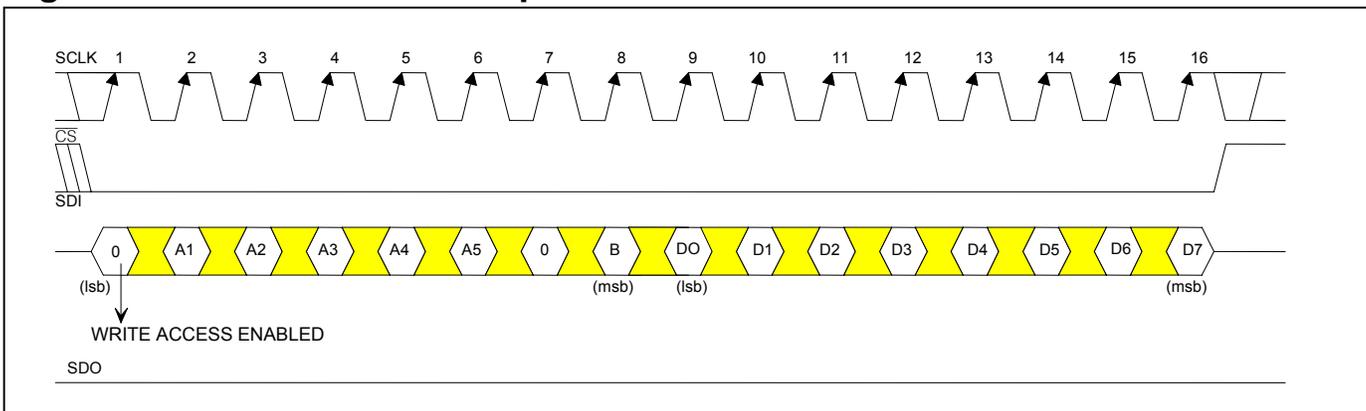


Table 9-B. Control and Operation Mode Selection

| MODE1 | MODE0 | HARDWARE | SOFTWARE | NRZ | BIPOLAR | AMI | B8ZS | OUTPUTS DISABLED |
|--------------|--------------|-----------------|-----------------|------------|----------------|------------|-------------|-----------------------------|
| Low | Low | On | Off | Off | On | Off | Off | No |
| Low | High | On | Off | Off | On | Off | Off | Yes |
| Low | Open | On | Off | On | Off | On | Off | No |
| High | Low | Off | On | X | X | X | X | No |
| High | High | Off | On | X | X | X | X | Yes |
| High | Open | Off | On | X | X | X | X | No |
| Open | Low | On | Off | On | Off | Off | On | No |
| Open | High | On | Off | On | Off | Off | On | Yes |
| Open | Open | On | Off | On | Off | Off | On | No |

10. DIAGNOSTIC MODE OPERATION

The DS21349 offers several diagnostic modes as listed in [Table 10-A](#). Various diagnostic modes are only available in software mode. In hardware mode, the diagnostic modes are selected by a combination of pin settings. In software mode, the diagnostic modes are selected by setting appropriate bits in the diagnostic control register.

Table 10-A. Diagnostic Modes

| DIAGNOSTIC MODE | AVAILABILITY | | SOFTWARE MODE |
|---|--------------|----------|---------------|
| | HARDWARE | SOFTWARE | MASKABLE |
| Local Loopback (LLB) | Yes | Yes | No |
| Analog Loopback (ALB) | Yes | Yes | No |
| Remote Loopback (RLB) | Yes | Yes | No |
| In-Band Network Loopback (NLB) | Yes | Yes | Yes |
| Dual Loopback (DLOOP) | Yes | Yes | No |
| Internal Data Pattern Generation and Detection | | | |
| Transmit AIS (TAIS) | Yes | Yes | No |
| Quasirandom Signal Source (QRSS) | Yes | Yes | Yes |
| In-Band Loop-Up/Down Code Generator | No | Yes | No |
| Error Insertion and Detection | | | |
| Bipolar Violation Insertion (INSBPV) | Yes | Yes | No |
| Logic Error Insertion (INSLER) | Yes | Yes | No |
| Bipolar Violation Detection (BPV) | Yes | Yes | No |
| Logic Error Detection, QRSS (QPD) | Yes | Yes | No |
| Alarm Condition Monitoring | | | |
| Receive Carrier Loss (RCL) Monitoring | Yes | Yes | Yes |
| Receive Alarm Indication Signal (AIS) Monitoring | No | Yes | Yes |
| Transmit Driver Failure Monitoring (DFMO) | No | Yes | Yes |
| Jitter Attenuator Limit Trip (JALT) | No | Yes | Yes |
| Other Diagnostic Reports | | | |
| Receive Line Attenuation Indicator (LATN) | No | Yes | No |

10.1 Loopback Modes

10.1.1 Local Loopback (LLB)

When local loopback is enabled (set LLB in CR2, or pull the LLB pin high), inbound data at the receiver inputs are ignored. TCLK and TPOS/TNEG pass through the jitter attenuator if enabled and are output at RCLK and RPOS/RNEG. The transmit path is unaffected by LLB, and will continue to transmit data normally (or AIS if TAIS is enabled).

10.1.2 Analog Loopback (ALB)

When analog loopback (ALB) is enabled (set ALB in CR2, or float the LLB pin), the receiver input pins are disconnected from the clock and data recovery circuit and replaced by TTIP and TRING. This tests the entire device including the jitter attenuator, transmitter, and receiver circuits.

10.1.3 Remote Loopback (RLB)

When remote loopback (RLB) is enabled (set RLB in CR2, or pull RLB pin high), inbound data at the receiver inputs is looped back to the transmitter path. Data passes through the jitter attenuator if enabled. The B8ZS encoder and decoder are not included in the loopback path. The receive path continues to operate normally.

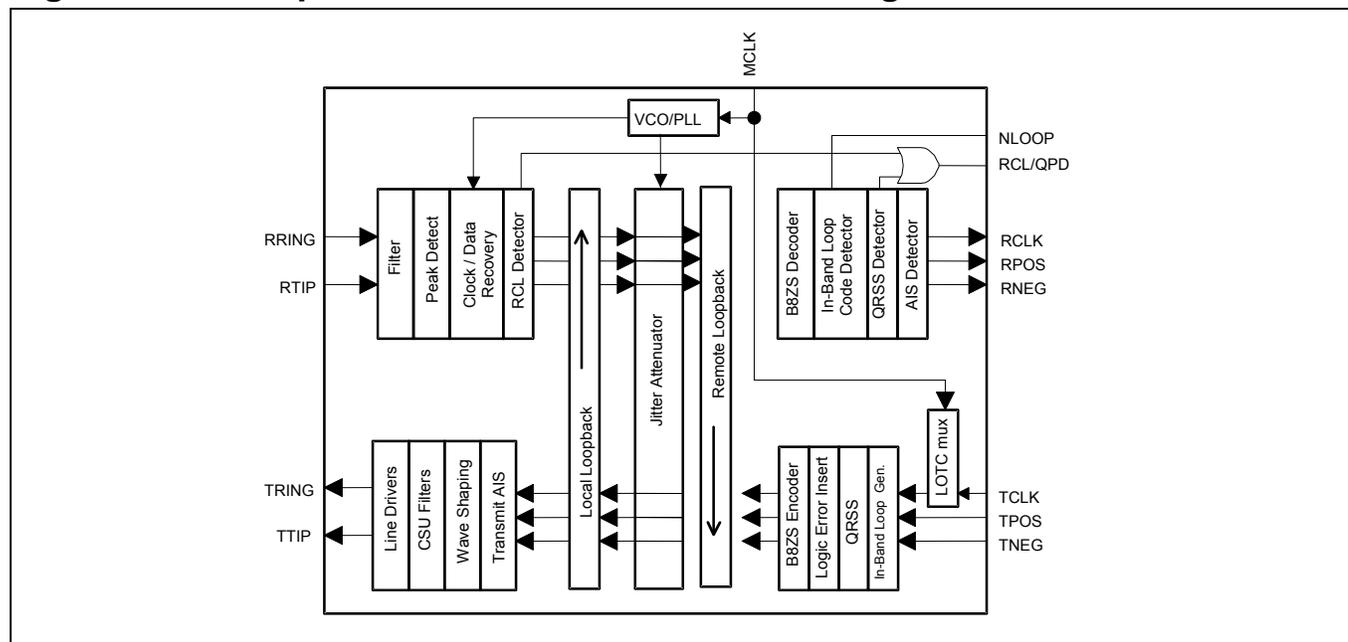
10.1.4 Network Loopback

When ENLOOP is enabled (set ENLOOP in CR2, or float the ENLOOP pin), the in-band loop code detector is enabled. The receiver detects the in-band loop code patterns (00001 = loop up and 001 = loop down) present in the inbound data. The detectors detect both framed and unframed loop codes. When the loop-up pattern is detected and present for 5 seconds, the device invokes remote loopback. ENLOOP is dropped when:

- 1) The in-band loop-down pattern is present for 5 seconds.
- 2) RLB is activated.
- 3) ALB is activated.

10.1.5 Dual Loopback

Dual loopback is the simultaneous enabling of RLB and LLB. If the jitter attenuator is enabled and, when both loopback paths are enabled, the jitter attenuator is placed in the local loopback path.

Figure 10-1. Loopbacks in the DS21349 Block Diagram


10.2 Internal Pattern Generation and Detection

10.2.1 Transmit Alarm-Indication Signal (TAIS)

When TAIS is enabled (set TAIS in CR2, or pulling the TAIS pin high), the transmitter inputs TPOS/TNEG and TDATA are ignored and the device transmits unframed all ones at the transmitter outputs at the TCLK frequency. If TCLK is not present, then the device uses MCLK to transmit. Both TAIS and LLB can be enabled at the same time. The transmitter input data is looped back to the receiver outputs through the jitter attenuator if enabled and the unframed all ones pattern is transmitted at TTIP and TRING.

10.2.2 Quasirandom Signal Source (QRSS)

The QRSS data pattern is described in AT&T 62411. The pattern is represented by the polynomial $2^{20} - 1$ with the additional requirement that no more than 14 consecutive 0s be present in the pattern. When QRSS is enabled (PAT0 = 0 and PAT1 = 1 in CR2 or float the QRSS pin), the data at the transmitter inputs TPOS/TNEG or TDATA is ignored and replaced by the output of the QRSS pattern generator. In addition, logic errors can be inserted into the data pattern with a rising edge on the INSLER input pin. If no logic errors are to be inserted, then the INSLER pin must remain low. If the logic error occurs on the same clock cycle as a 1 that has been inserted to suppress 15 0s, then the logic error is delayed until the next clock cycle. The logic error insertion is available in both NRZ and bipolar data modes. Enabling the QRSS pattern also enables the QRSS detector in the receiver. Pattern synchronization occurs when there are no errors in 64 bits. When synchronized, the QPD output pin goes low. Once synchronized, an error in the pattern causes the QPD output to go high for one-half RCLK cycle. In software mode, the level on the CLKE pin determines the relationship between QPD and RCLK. When CLKE is low, QPD is high when RCLK is high. When CLKE is high, QPD is high when RCLK is low. The QPD output can be used to trigger an external bit error counter. When RCL is active or the receiver is not synchronized to the QRSS pattern, then QPD maintains an output high.

In software mode, the device can generate an interrupt to indicate that the QRSS pattern synchronization has been declared or lost. Clearing the QRSS bit in the interrupt mask register enables the interrupt. Use the QPD output to increment an external bit error counter and use the interrupt to reset the counter. The QRSS bit in the status register is set when the QRSS pattern is detected and cleared when pattern is lost (more than 6 bit errors in a window of 64 bits). The QRSS bit in the transition status register indicates that the QRSS status has changed since the last QRSS interrupt clear command.

10.2.3 In-Band Network Loop-Up or Loop-Down Code Generator

In-band network loop-up or loop-down transmission is available in software mode only. The loop-up code is transmitted when $PAT0 = 1$ and $PAT1 = 0$ in CR2. Logic errors and bipolar violations can still be inserted when loop codes are being transmitted.

10.3 Error Insertion and Detection

10.3.1 Bipolar Violation Insertion (INSBPV)

INSBPV is available in NRZ mode. Sampling occurs on the falling edge of TCLK. A rising edge on the NSBPV pin inserts a BPV on the next available mark, except in the following conditions:

- 1) If the BPV would violate a B8ZS codeword.
- 2) When LLB and TAIS are both active. In this case, the BPV is looped back to the BPV pin and the line driver transmits all ones with no violation.
- 3) When RLB is active.
- 4) When NLOOP is active.

BPVs can be inserted in both NRZ and bipolar data modes when the DS21349 is configured to transmit internally generated data patterns (QRSS or in-band loop codes).

10.3.2 Logic Error Insertion (INSLE)

When transmitting QRSS or in-band loop codes, a logic error is inserted into the outbound data pattern on a rising edge of the INSLER pin. Remember, when transmitting the QRSS pattern, logic error insertion is inhibited if the error would replace a 1 with a 0 and result in a string of 15 or more consecutive 0s.

10.3.3 Logic Error Detection (QPD)

After QRSS pattern synchronization, logic errors are reported at the QPD output pin. If a logic error occurs, the QPD pin goes high for one-half RCLK cycle. In software mode, the CLKE pin determines the phase relationship between QPD and RCLK. When CLKE is low, QPD is high when RCLK is high. When CLKE is high, QPD is high when RCLK is low. To count logic errors, use the QPD output to increment an external error counter. A continuous output high indicates loss of synchronization to the QRSS pattern or receive-carrier loss.

10.3.4 Bipolar Violation Detection (BPV)

When the B8ZS encoders and decoders are disabled or when configured for NRZ mode, bipolar violations are reported at the BPV output pin. BPV goes high for a full clock cycle to indicate a bipolar violation. When the B8ZS encoders and decoders are enabled, BPVs that are not part of codewords are not reported.

10.4 Alarm Monitoring

10.4.1 Receive-Carrier Loss (RCL)

The receiver counts inbound 0s and declares RCL when the counter reaches 192. This applies to hardware mode and software mode if the RCL2048 bit is cleared in CR4. In software mode, setting the RCL2048 bit changes the RCL counter to declare receive-carrier loss after 2048 consecutive 0s. Once set, the RCL bit will remain set until the receiver detects a 12.5% density of 1s in a sliding window of 112 bits, provided that there are no more than 98 consecutive 0s in that 112-bit window. When RCL is active, RCLK is replaced by MCLK. RCL is indicated by an output high on the RCL pin and with a 1 in SR.0.

10.4.2 Alarm-Indication-Signal Detection (AIS)

AIS detection is only available in software mode. The receiver declares receipt of AIS when fewer than six 0s are detected in 4632 bits (3ms). AIS is cleared when three or more 0s are received in 4632 bits. The AIS bit in the status register (SR.2) indicates the presence of AIS. When the AIS status bit changes, the AIS bit in the transition status register (TSR.2) is set. A change in the AIS status will generate an interrupt if the AIS interrupt mask bit (IMR.2) bit is cleared.

10.4.3 Driver-Fail Monitor-Open (DFMO)

The DFMO bit is set in the status register when the transmitter outputs detect an open circuit. DFMO can generate an interrupt if the DFMO interrupt mask bit (IMR.5) is cleared. This is not supported in hardware mode.

10.4.4 Jitter Attenuator Limit Trip (JALT)

If the incoming jitter exceeds either 120 UIp-p (buffer depth is 128 bits) or 28 UIp-p (buffer depth is 32 bits), then the DS21349 will divide the internal nominal 24.704MHz (T1) clock by either 15 or 17 instead of the normal 16 to keep the buffer from overflowing. When the device divides by either 15 or 17, it also sets the jitter attenuator limit trip (JALT) bit in information register 1 (IR1).

10.5 Other Diagnostic Reports

10.5.1 Receive Line-Attenuation Indication

The device reports the approximate inbound signal strength in the status register (IR). The four most significant bits indicate the signal strength in approximately 2.5dB increments.

11. NETWORK INTERFACE

Transformer specifications are listed in [Table 11-A](#) and [Table 11-B](#). [Table 11-C](#) illustrates the series resistance necessary for the basic interface and is associated with different transformer turns ratios. Smaller turns ratios result in lower power-supply requirements. However, series resistance provides added protection from potentially damaging voltages that can occur during lightning strikes. A basic network interface is illustrated in [Figure 11-1](#). For a complete discussion of network interface design, refer to *Application Note 324: T1/E1 Network Interface Design*.

Table 11-A. Specifications for Receive Transformer

| SPECIFICATION | RECOMMENDED VALUE |
|-----------------------------------|---------------------|
| Turns Ratio (all applications) | 1:1 $\pm 2\%$ |
| Primary Inductance | 600 μ H minimum |
| Leakage Inductance | 1.0 μ H maximum |
| Interwinding Capacitance | 40pF maximum |
| Receive Transformer DC Resistance | |
| Primary (Device Side) | 2 Ω maximum |
| Secondary | 2 Ω maximum |

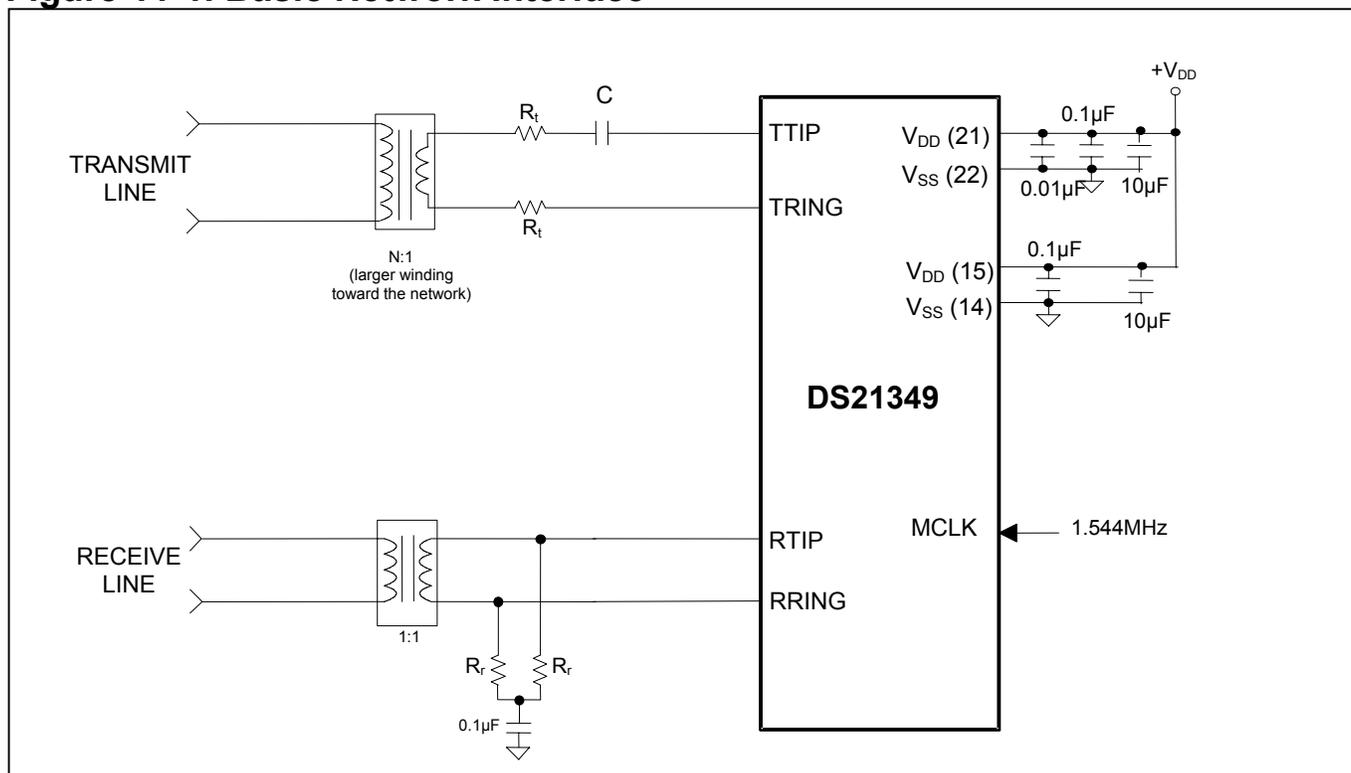
Table 11-B. Specifications for Transmit Transformer

| SPECIFICATION | RECOMMENDED VALUE |
|------------------------------------|----------------------|
| Turns Ratio, 3.3V | 1:3 $\pm 2\%$ |
| Primary Inductance | 600 μ H minimum |
| Leakage Inductance | 1.0 μ H maximum |
| Interwinding Capacitance | 40pF maximum |
| Transmit Transformer DC Resistance | |
| Primary (Device Side) | 1.0 Ω maximum |
| Secondary | 2.0 Ω maximum |

Table 11-C. Transformer Turns Ratio vs. Series Resistance

| XFMR1 (CR4.0) | XFMR2 (CR4.1) | OPERATING VOLTAGE (V) | APPLICATION | N | Rt (Ω) |
|---------------|---------------|-----------------------|-------------|-------|-----------------|
| 0 | 0 | 3.3 | Long/Short | 1:3 | 0 |
| | | | D4 | | |
| 0 | 1 | 3.3 | Long/Short | 1:2 | 0 |
| | | | | 1:3 | 3 |
| 1 | 0 | 3.3 | Long/Short | 1:2.5 | 0 |
| | | | | 1:3 | 1 |
| 1 | 1 | 3.3 | Long/Short | 1:2 | 0 |
| | | | | 1:3 | 3 |

Figure 11-1. Basic Network Interface



Note 1: All resistor values are $\pm 1\%$.

Note 2: The R_r resistors should be 50 Ω each for T1 lines.

Note 3: $C = 1 \mu\text{F}$ if using a 1:2 transformer; $C = 2 \mu\text{F}$ if using a 1:3 transformer.

Figure 11-2. T1 Transmit Pulse Template

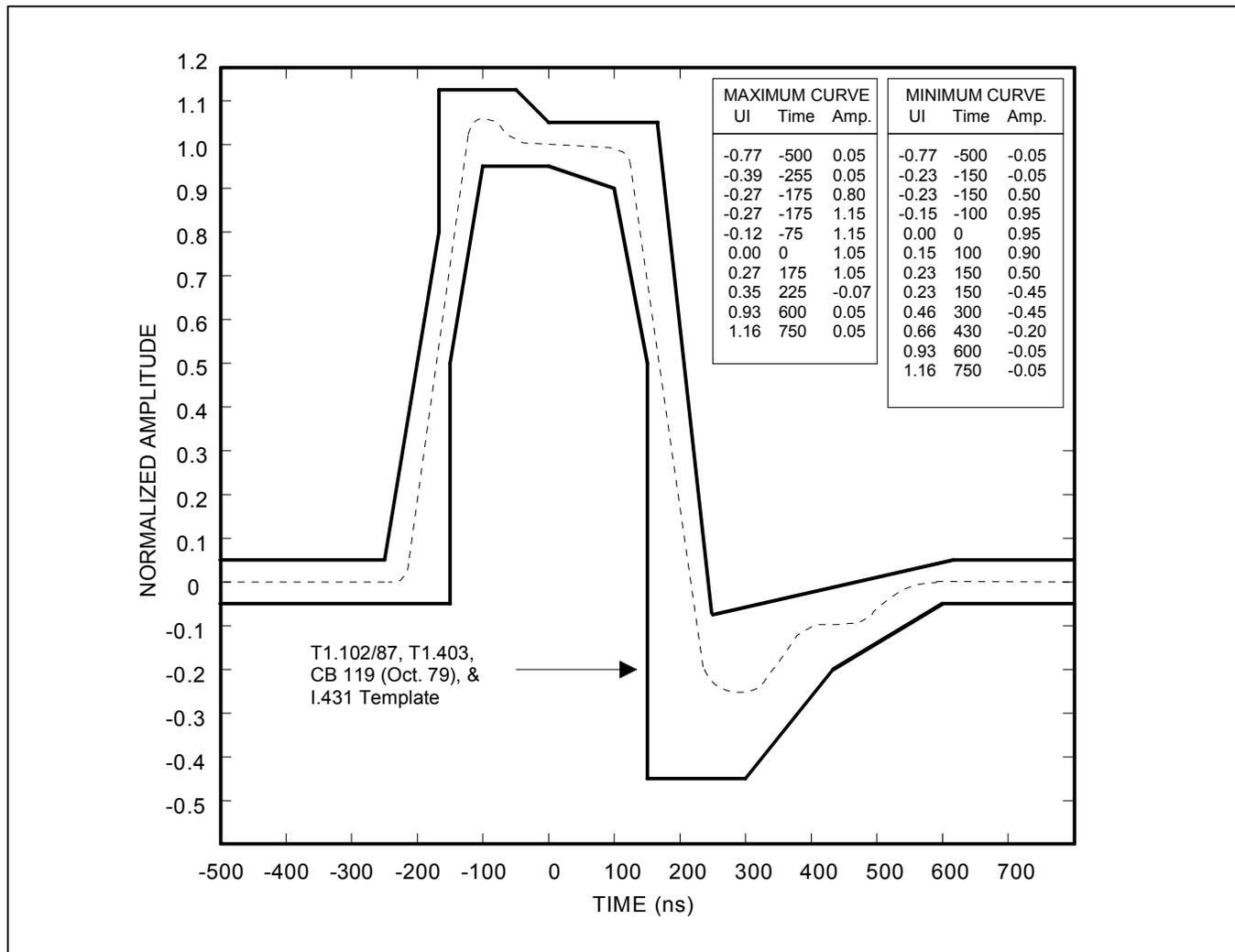
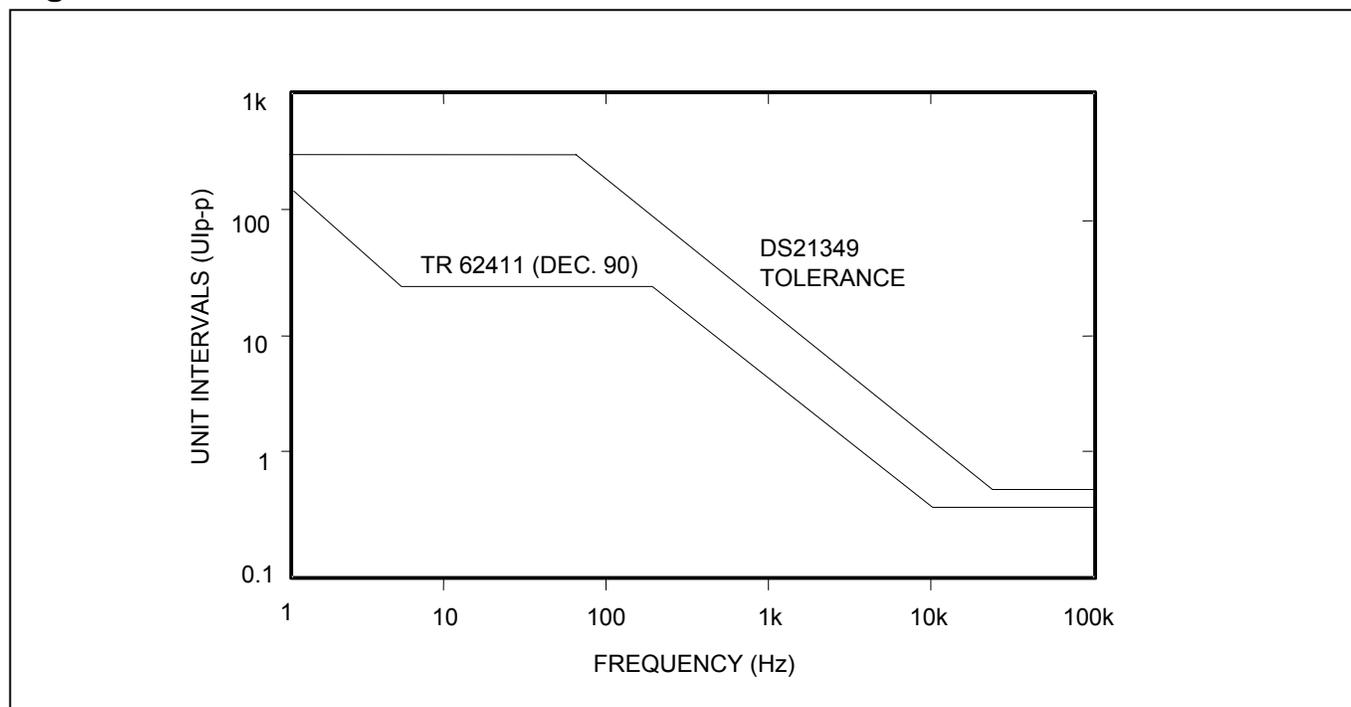
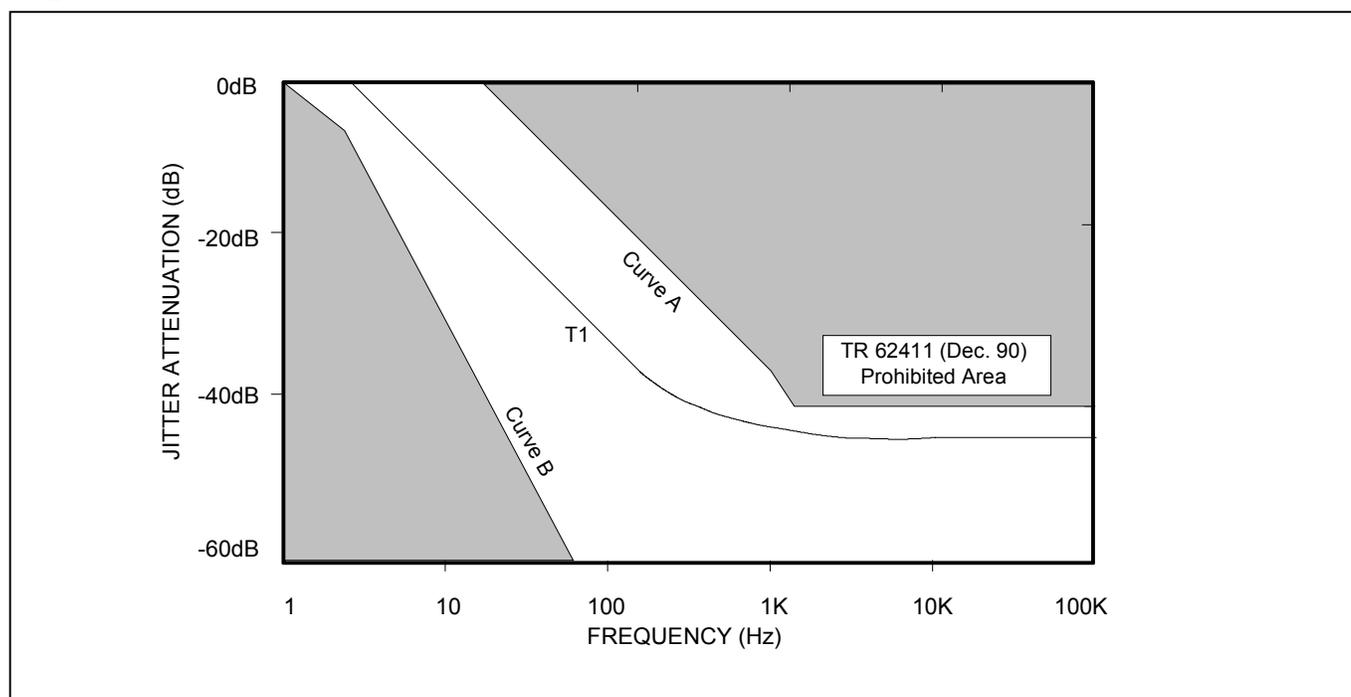


Figure 11-3. Jitter Tolerance**Figure 11-4. Jitter Attenuation**

12. DC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

| | |
|---|---------------------------------------|
| Voltage Range on Any Pin Relative to Ground | -1.0V to +6.0V |
| Operating Temperature Range for DS21349QN | -40°C to +85°C |
| Storage Temperature Range | -55°C to +125°C |
| Soldering Temperature | See IPC/JEDEC J-STD-020 Specification |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|------------------------------------|----------|-------|-----|-------|-------|
| Logic 1 | V_{IH} | 2.0 | | 5.5 | V |
| Logic 0 | V_{IL} | -0.3 | | +0.8 | V |
| Supply for 3.3V Operation (Note 1) | V_{DD} | 3.135 | 3.3 | 3.465 | V |

CAPACITANCE

($T_A = +25^\circ\text{C}$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|--------------------|-----------|-----|-----|-----|-------|
| Input Capacitance | C_{IN} | | 5 | | pF |
| Output Capacitance | C_{OUT} | | 7 | | pF |

DC CHARACTERISTICS

($V_{DD} = 3.3\text{V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|--|----------|------|-----|------|---------------|
| Input Leakage (Note 2) | I_{IL} | -1.0 | | +1.0 | μA |
| Output Leakage (Note 3) | I_{LO} | | | 1.0 | μA |
| Output Current (2.4V) | I_{OH} | -1.0 | | | mA |
| Output Current (0.4V) | I_{OL} | +4.0 | | | mA |
| Power Dissipation at 3.3V (Notes 4, 5) | P_{DD} | | 300 | | mW |

Note 1: Applies to V_{DD} .

Note 2: $0\text{V} < V_{IN} < V_{DD}$.

Note 3: Applied to $\overline{\text{INT}}$ when tri-stated

Note 4: $\text{TCLK} = \text{MCLK} = 1.544\text{MHz}$.

Note 5: Power dissipation for an all-ones data density.

AC CHARACTERISTICS: SERIAL PORT (MODE1 = 1)

($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$.) (Figure 12-1 and Figure 12-2)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|-----------|-----|-----|-----|-------|
| Setup Time \overline{CS} to SCLK | t_{CSS} | 50 | | | ns |
| Setup Time SDI to SCLK | t_{SSS} | 50 | | | ns |
| Hold Time SCLK to SDI | t_{SSH} | 50 | | | ns |
| SCLK High/Low Time | t_{SLH} | 200 | | | ns |
| SCLK Rise/Fall Time | t_{SRF} | | | 50 | ns |
| SCLK to \overline{CS} Inactive | t_{LSC} | 50 | | | ns |
| \overline{CS} Inactive Time | t_{CM} | 250 | | | ns |
| SCLK to SDO Valid | t_{SSV} | | | 75 | ns |
| SCLK to SDO Tri-State | t_{SSH} | | 100 | | ns |
| \overline{CS} Inactive or SCLK to SDO Tri-State | t_{CSH} | | 100 | | ns |

Figure 12-1. Serial Bus Read Timing (MODE1 = 1)

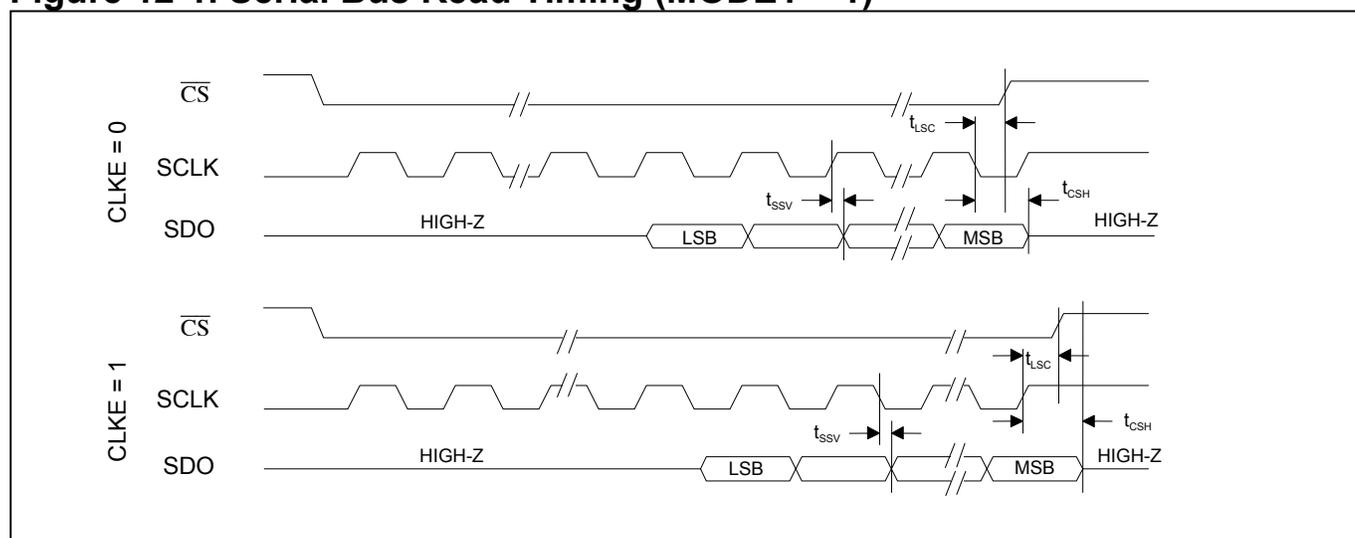
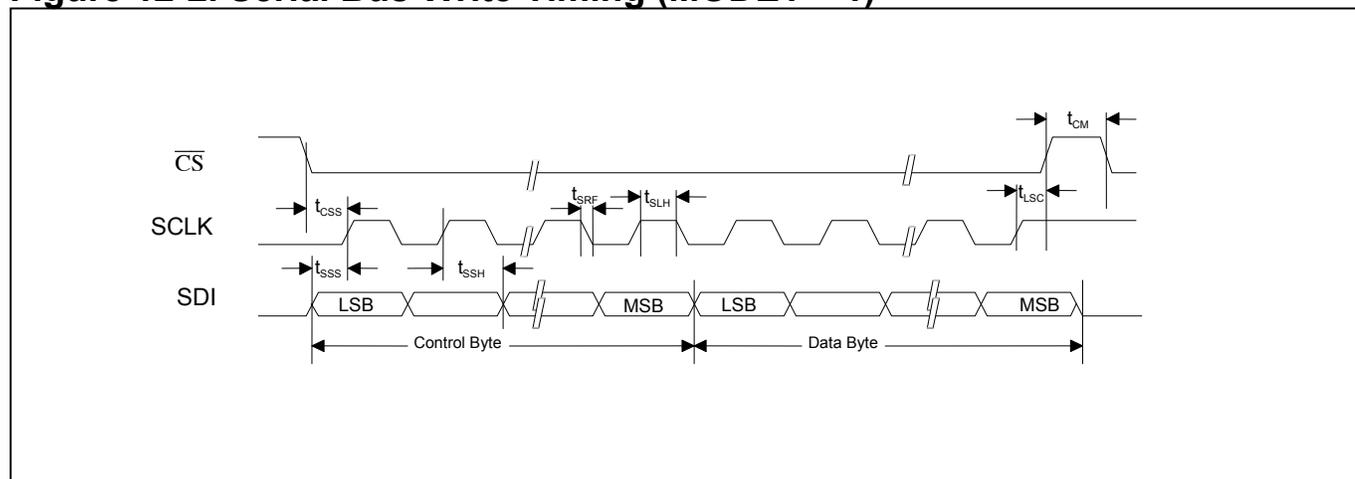


Figure 12-2. Serial Bus Write Timing (MODE1 = 1)



AC CHARACTERISTICS: RECEIVE SIDE

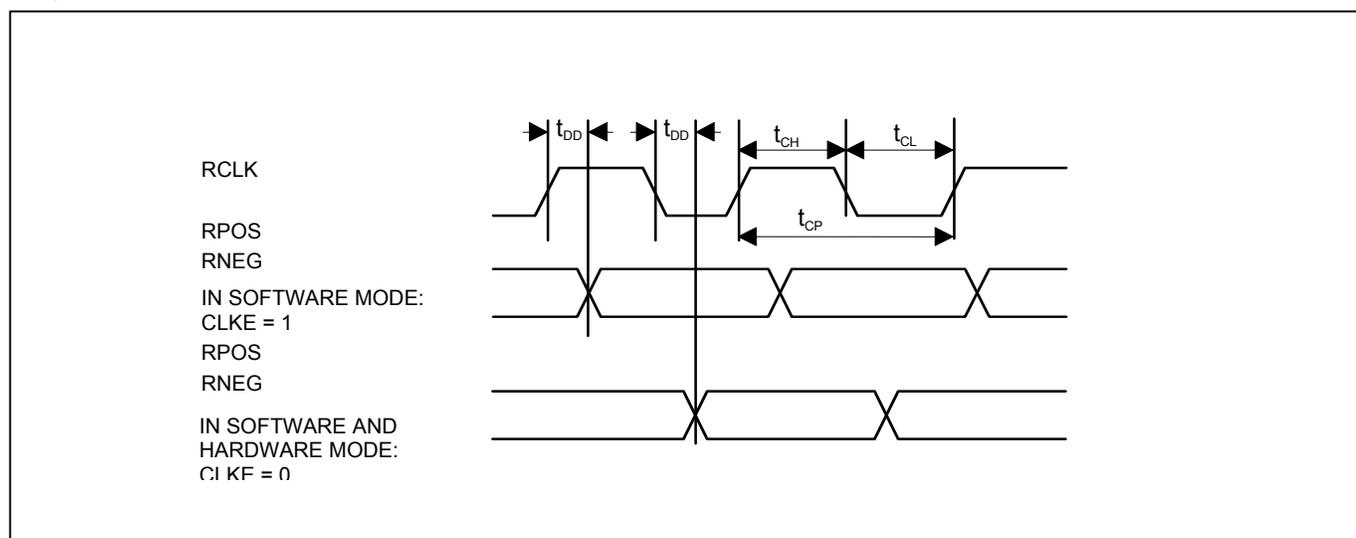
($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.) (Figure 12-3)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|--------------------------------|----------|-----|-----|-----|-------|
| RCLK Period | t_{CP} | | 648 | | ns |
| RCLK Pulse Width (Note 6) | t_{CH} | 200 | | | ns |
| | t_{CL} | | | | |
| RCLK Pulse Width (Note 7) | t_{CH} | 150 | | | ns |
| | t_{CL} | | | | |
| Delay RCLK to RPOS, RNEG Valid | t_{DD} | | | 50 | ns |

Note 6: Jitter attenuator enabled in the receive path.

Note 7: Jitter attenuator disabled or enabled in the transmit path.

Figure 12-3. AC Characteristics for Receive Side

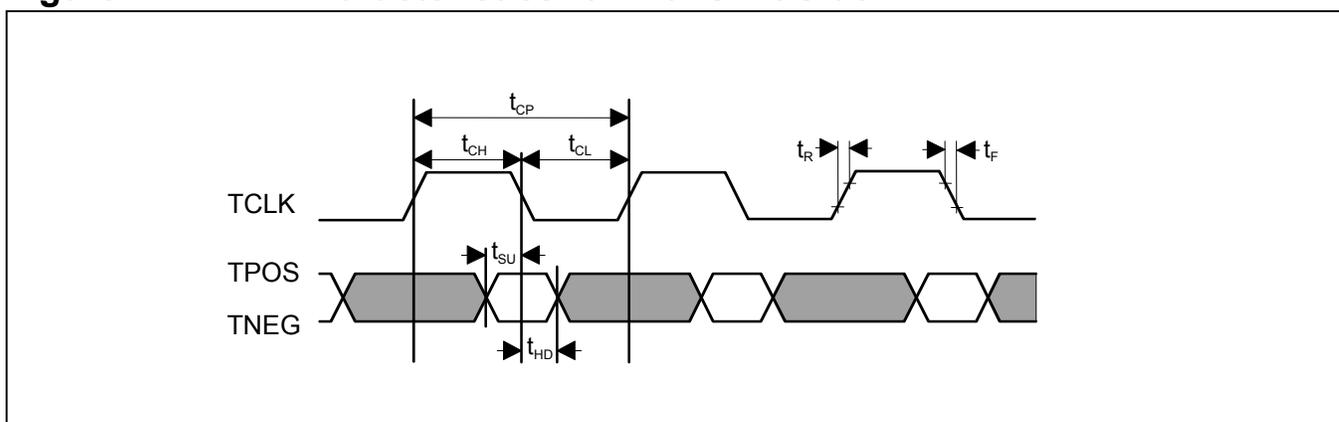


AC CHARACTERISTICS: TRANSMIT SIDE

($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.) (Figure 12-4)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|--|----------------------|-----|-----|-----|-------|
| TCLK Period | t_{CP} | | 648 | | ns |
| TCLK Pulse Width | t_{CH} t_{CL} | 75 | | | ns |
| TPOS/TNEG Setup to TCLK Falling or Rising | t_{SU} | 20 | | | ns |
| TPOS/TNEG Hold from TCLK Falling or Rising | t_{HD} | 20 | | | ns |
| TCLK Rise and Fall Times | t_R , t_F | | | 25 | ns |

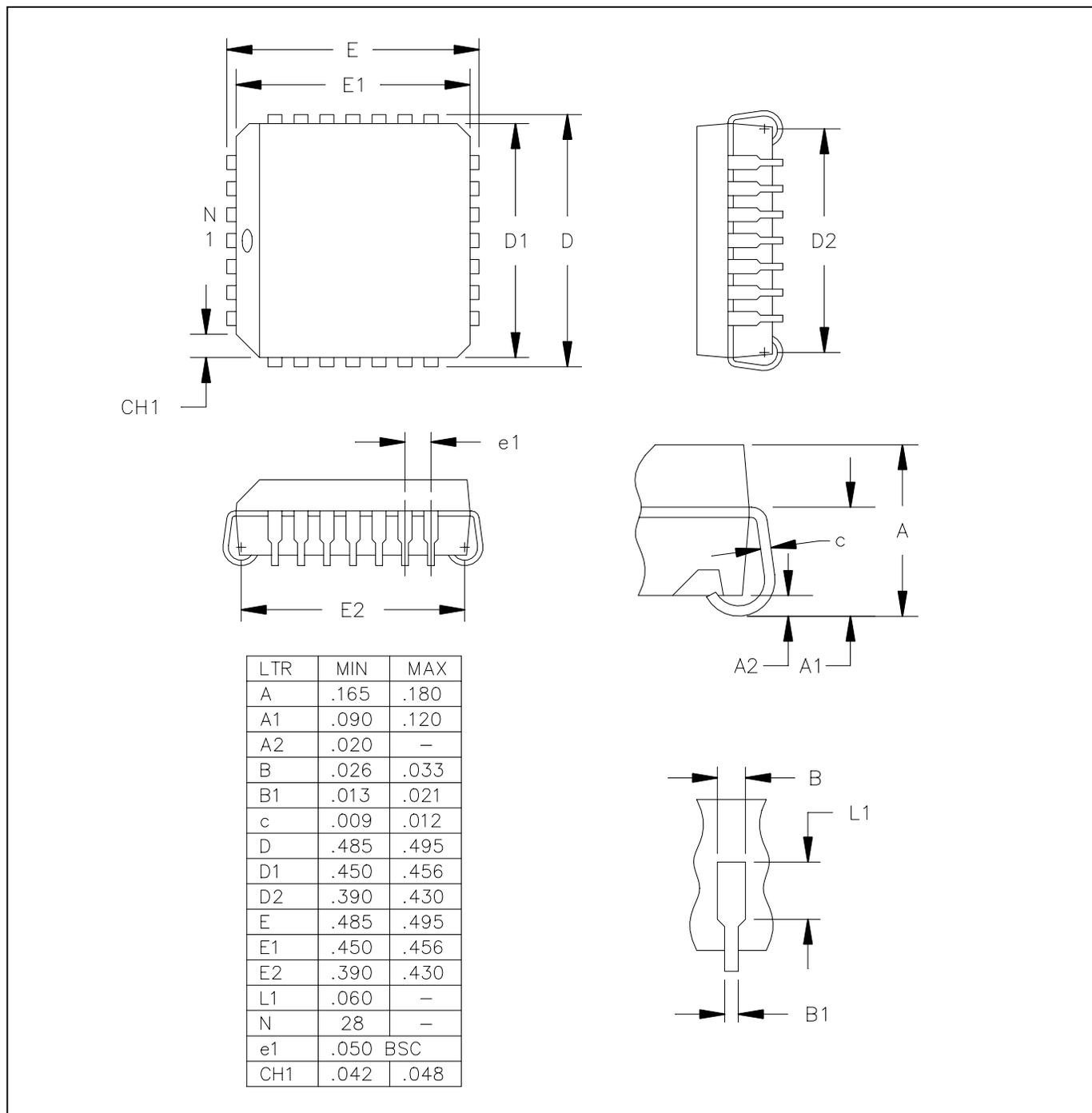
Figure 12-4. AC Characteristics for Transmit Side



13. PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. The package number provided for each package is a link to the latest package outline information.)

13.1 28-Pin PLCC ([56-G4001-001](#))



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