TPDxF003 Four-, Six-, and Eight-Channel EMI Filters With Integrated ESD Protection

1 Features

- Four-, Six-, and Eight-Channel EMI Filtering for Data Ports
- –3 dB Bandwidth of 200 MHz
- Greater than 25 dB attenuation at 1 GHz
- IEC 61000-4-2 Level 4 ESD Protection
  - ±12-kV Contact Discharge
  - ±20-kV Air Gap Discharge
- Pi-Style (C-R-C) Filter Configuration (R = 100 Ω, C_{TOTAL} = 17 pF)
- Low 10-nA Leakage Current
- Easy Flow-Through Routing

2 Applications

- Display Interfaces
- Cell Phones
- Tablets
- SVGA Video Connections
- Memory Interfaces

3 Description

The TPDxF003 family is a series of highly integrated devices designed to provide Electromagnetic Interference (EMI) filtering in all systems subjected to electromagnetic interference. These filters also provide a Transient Voltage Suppressor (TVS) diode circuit for Electrostatic Discharge (ESD) protection which prevents damage to the application when subjected to ESD stress far exceeding IEC 61000-4-2 (Level 4).

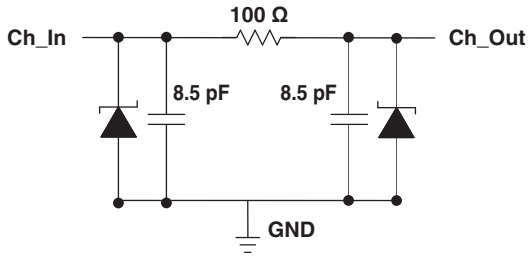
The TPDxF003 family is specified for –40°C to 85°C operation. These filters are also packaged in space-saving 0.4-mm pitch DQD packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4F003	WSON (8)	1.70 mm x 1.35 mm
TPD6F003	WSON (12)	2.50 mm x 1.35 mm
TPD8F003	WSON (16)	3.30 mm x 1.35 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Equivalent Schematic



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4 Revision History

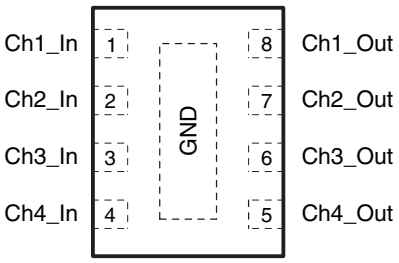
Changes from Revision D (January 2010) to Revision E **Page**

- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

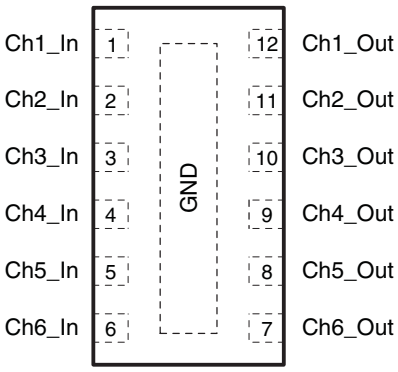
DQD PACKAGE
(TOP VIEW)

TPD4F003



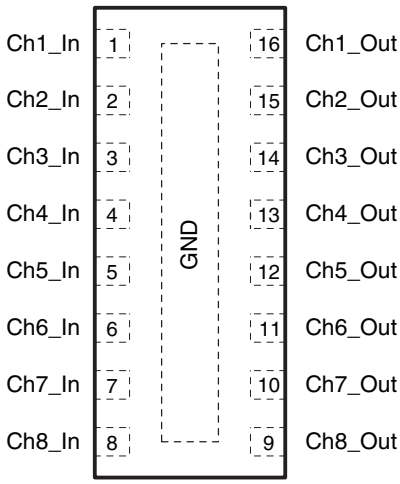
1.7 mm x 1.35 mm x 0.75 mm
(0.4-mm pitch)

TPD6F003



2.5 mm x 1.35 mm x 0.75 mm
(0.4-mm pitch)

TPD8F003



3.3 mm x 1.35 mm x 0.75 mm
(0.4-mm pitch)

Pin Functions - TPD4F003

PIN		I/O	DESCRIPTION
NAME	No.		
ChX_In	1, 2, 3, 4	IO	ESD-protected channel, connected to corresponding ChX_Out
ChX_Out	5, 6, 7, 8	IO	ESD-protected channel, connected to corresponding ChX_In
GND	GND	G	Ground

Pin Functions - TPD6F003

PIN		I/O	Description
Name	No.		
ChX_In	1, 2, 3, 4, 5, 6	IO	ESD-protected channel, connected to corresponding ChX_Out
ChX_Out	7, 8, 9, 10, 11, 12	IO	ESD-protected channel, connected to corresponding ChX_In
GND	GND	G	Ground

Pin Functions - TPD8F003

PIN		I/O	Description
Name	No.		
ChX_In	1, 2, 3, 4, 5, 6, 7, 8	IO	ESD-protected channel, connected to corresponding ChX_Out
ChX_Out	9, 10, 11, 12, 13, 14, 15, 16	IO	ESD-protected channel, connected to corresponding ChX_In
GND	GND	G	Ground

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	IO to GND		6	V
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		±15	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		±1500	V
		IEC 61000-4-2 ESD Rating - Contact		±12	kV
		IEC 61000-4-2 ESD Rating - Air		±20	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{IO}	0	5.5	V
T_A	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPD4F003	TPD6F003	TPD8F003	UNIT
		DQD			
		8 PINS	12 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.6	89.2	80.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	108.5	100.1	88.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	66.4	50.5	45.8	
ψ_{JT}	Junction-to-top characterization parameter	6.8	9.4	9.2	
ψ_{JB}	Junction-to-board characterization parameter	65.9	50.0	45.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	33.2	31.0	31.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{BR}	DC breakdown voltage	I_{IO} = 10 µA	6			V
R	Resistance		85	100	115	Ω
C	Capacitance (C1 or C2)	V_{IO} = 2.5 V		8.5		pF
I_{IO}	Channel leakage current	V_{IO} = 3.3 V		10		nA
f_C	Cut-off frequency	Z_{SOURCE} = 50 Ω, Z_{LOAD} = 50 Ω		200		MHz

(1) Typical values are at T_A = 25°C.

6.6 Typical Characteristics

6.6.1 IEC Clamping Waveforms (clamp voltage measured both at Ch_Out and Ch_In)

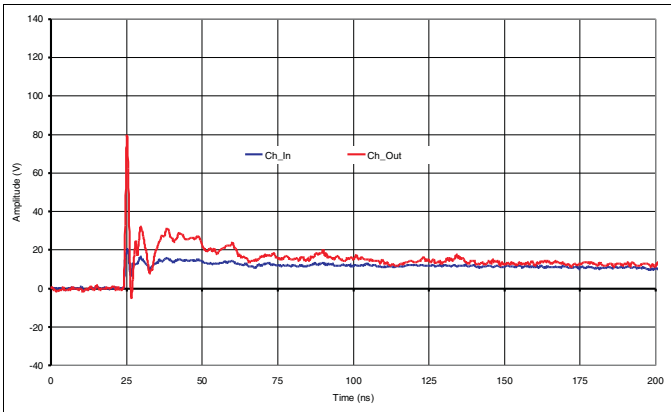


Figure 1. With 8 kV Contact ESD Stress at Ch_Out

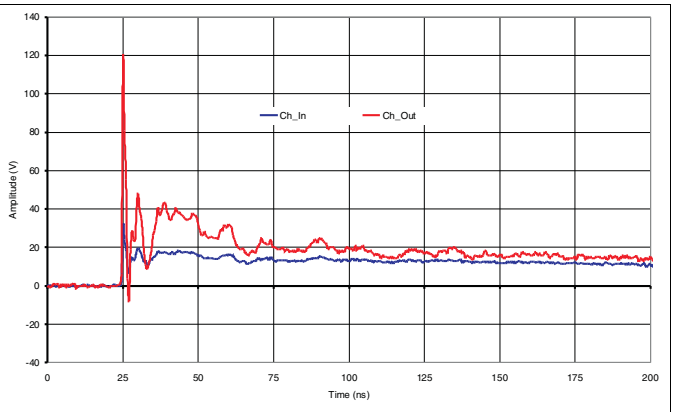


Figure 2. With 12 kV Contact ESD Stress at Ch_Out

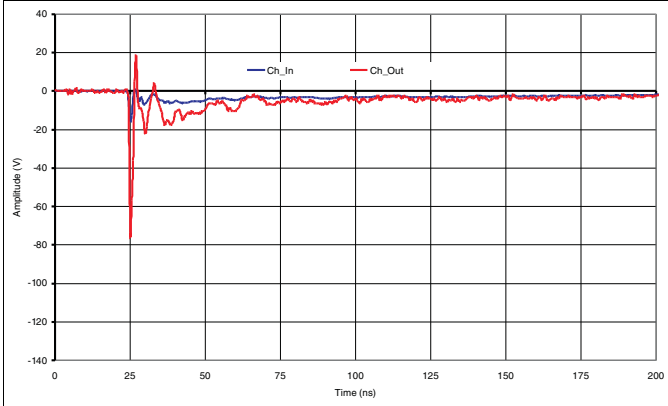


Figure 3. With -8 kV Contact ESD Stress at Ch_Out

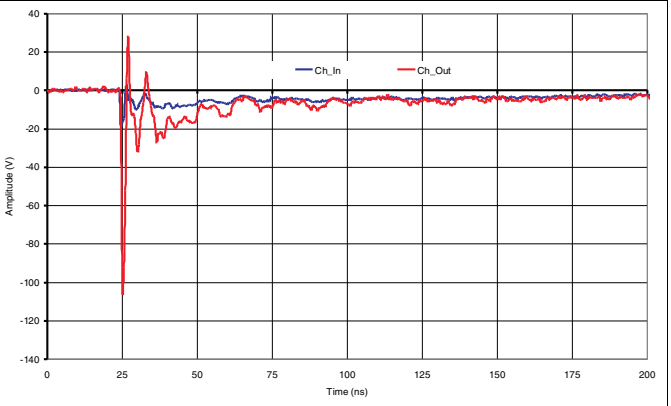


Figure 4. With -12 kV Contact ESD Stress at Ch_Out

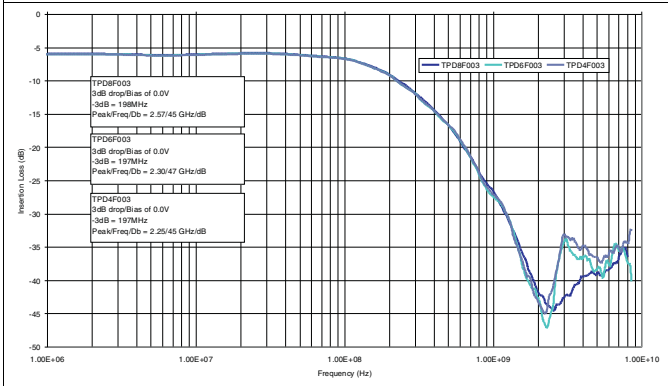


Figure 5. Frequency Response

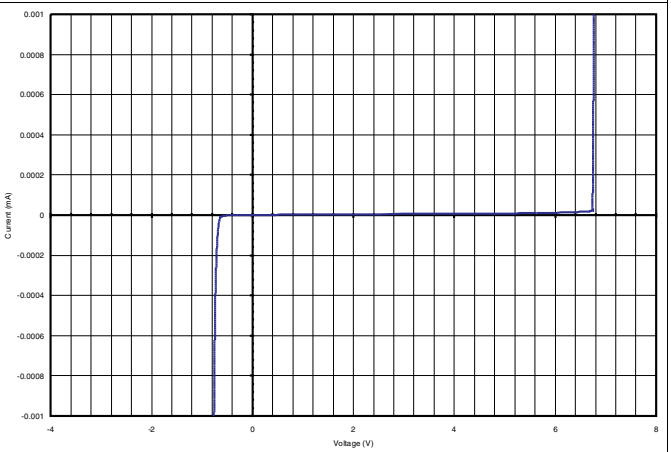


Figure 6. DC Voltage-Current Sweep Across Input/Output Pins

6.6.2 Channel-to-Channel Crosstalk

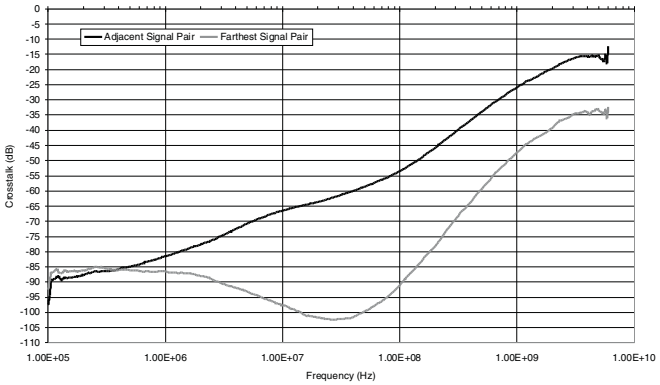


Figure 7. TPD4F003

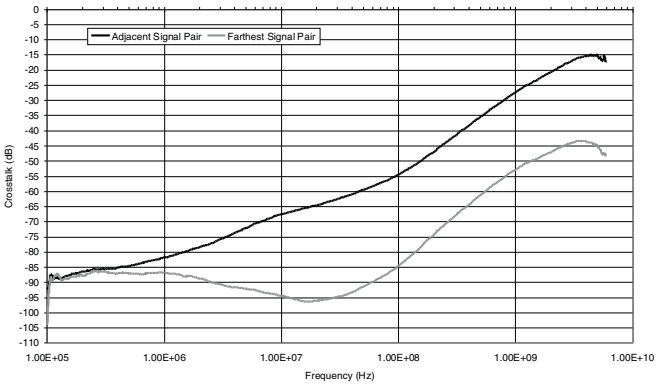


Figure 8. TPD6F003

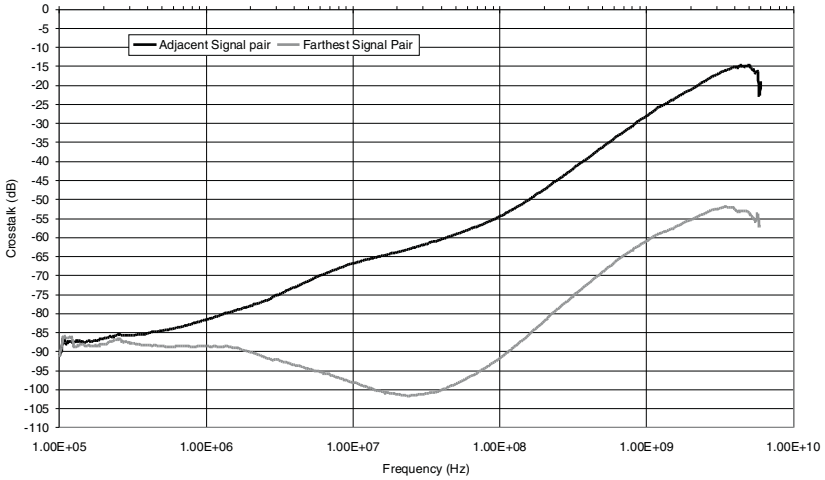


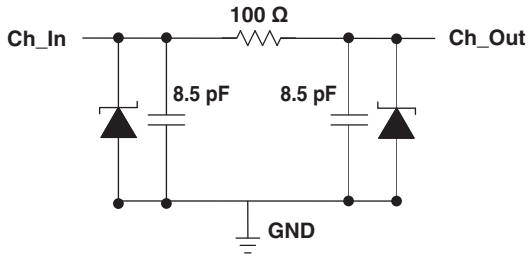
Figure 9. TPD8F003

7 Detailed Description

7.1 Overview

The TPDxF003 family is a series of highly integrated devices designed to provide EMI filtering in all systems subjected to electromagnetic interference. These filters also provide a Transient Voltage Suppressor (TVS) diode circuit for ESD protection which prevents damage to the application when subjected to ESD stress far exceeding IEC 61000-4-2 (Level 4).

7.2 Functional Block Diagram



7.3 Feature Description

The TPDxF003 family is a line of ESD and EMI filtering devices designed to reduce EMI emissions and provide system level ESD protection. Each device can dissipate ESD strikes above the maximum level specified by IEC 61000-4-2 international standard. Additionally, the EMI filtering structure reduces EMI emissions by providing high frequency roll-off.

7.3.1 Four-, Six-, and Eight-Channel EMI Filtering for Data Ports

These devices provide EMI filtering for four, six, or eight channels of data lines.

7.3.2 –3 dB Bandwidth of 200 MHz

These devices have a through –3dB bandwidth of 200 MHz.

7.3.3 Greater Than 25 dB Attenuation at 1 GHz

Signal attenuation is above 25dB at 1 GHz, which provides significant reduction in spurious emissions.

7.3.4 Robust ESD Protection Exceeds IEC 61000-4-2

The ESD protection on all pins exceeds the IEC 61000-4-2 level 4 standard. Contact ESD is rated at ±12 kV and Air-gap ESD is rated at ±20 kV.

7.3.5 Pi-Style (C-R-C) Filter Configuration

This family of devices has a pi-style filtering configuration composed of a series resistor and two capacitors in parallel with the I/O pins. The typical resistor value is 100 Ω and the typical capacitor values are 8.5 pF each.

7.3.6 Low 10-nA Leakage Current

The I/O pins feature an ultra-low leakage current of 10-nA (typical) with a bias of 3.3 V.

7.3.7 Easy Flow-Through Routing

The layout of this device makes it easy to add protection to existing layouts. The packages offer flow-through routing which requires minimal changes to existing layout for addition of these devices.

7.4 Device Functional Modes

The TPDxF003 family of devices are passive integrated circuits that passively filter EMI and trigger when voltages are above V_{BR} or below the lower diode voltage (–0.6 V). During ESD events, voltages as high as ±20 kV (air) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels, the device reverts to passive.

8 Applications and Implementation

8.1 Application Information

The TPDxF003 family are diode type TVS' integrated with series resistors for filtering emitted EMI. As signal passes through the device, higher frequency components are filtered out. This device also provides a path to ground during ESD events and isolates the protected IC. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. In particular, these filters are ideal for EMI filtering and protecting data lines from ESD at the display, keypad, and memory interfaces.

8.2 Typical Application

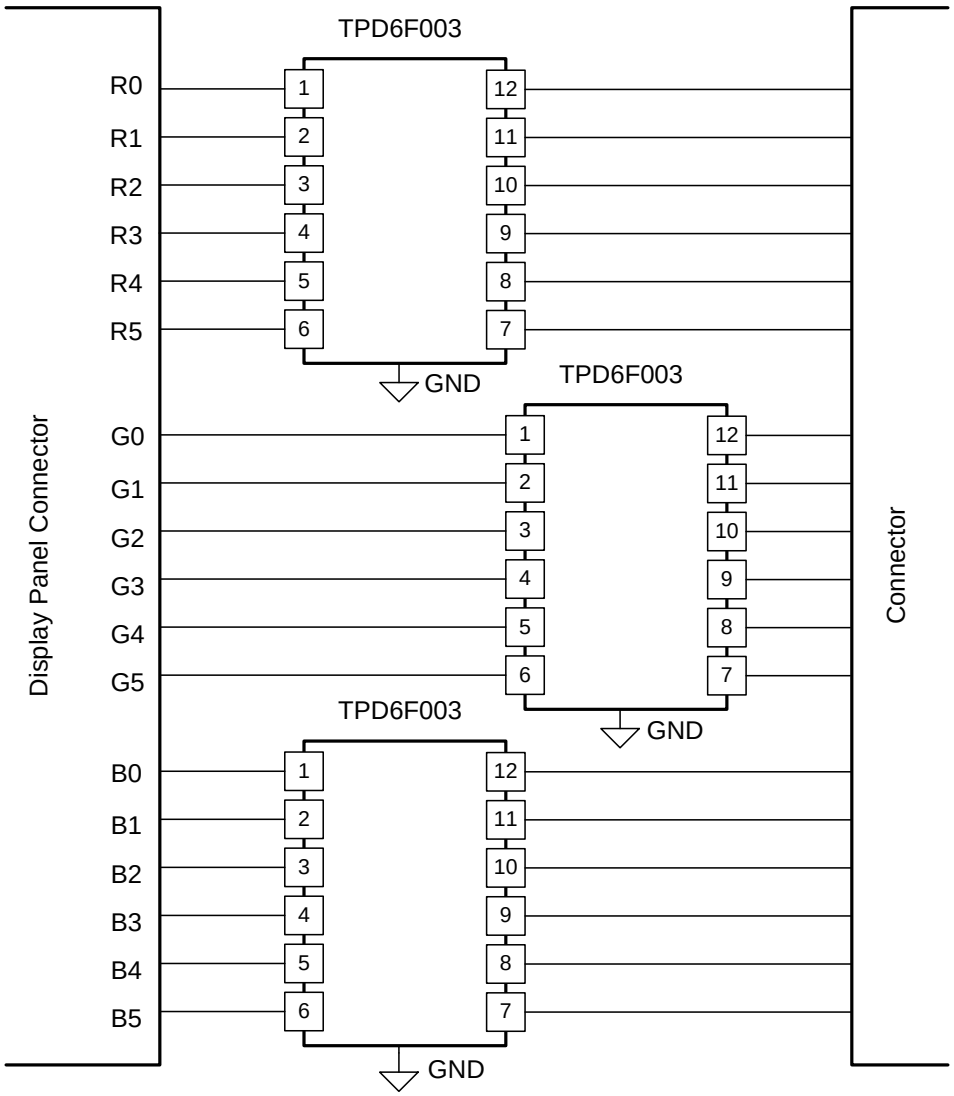


Figure 10. Display Panel Schematic

Typical Application (continued)

8.2.1 Design Requirements

For this design example, three TPD6F003 devices are used in an 18-bit display panel application. This will provide a complete ESD and EMI protection solution for the display connector.

Given the display panel application, the following parameters are known.

DESIGN PARAMETER	VALUE
Signal range on all pins except GND	0 V to 5 V
Operating Frequency	100 MHz

8.2.2 Detailed Design Procedure

To begin the design process, some design parameters must be decided; the designer need to know the following:

- Signal range on all the protected lines
- Operating frequency

8.2.2.1 Signal Range on All Protected Lines

The TPD6F003 has 8 identical protection channels for signal lines. All I/O pins will support a signal range from 0 to 5.5 V.

8.2.2.2 Operating Frequency

The TPD6F003 has a 200 MHz –3dB bandwidth, which supports the operating frequency for this display.

8.2.3 Application Curve

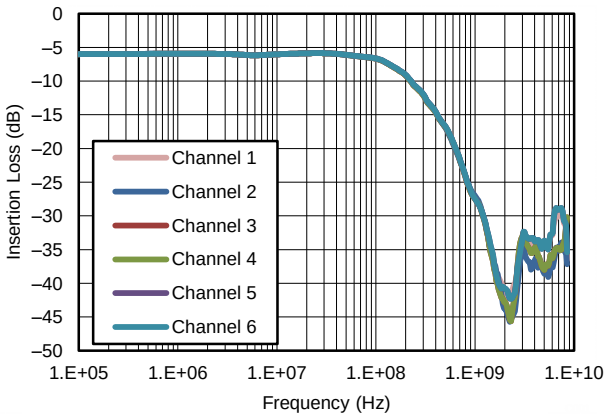


Figure 11. Frequency Response

9 Power Supply Recommendations

This family of devices are passive EMI and ESD devices so there is no need to power them. Care should be taken to not violate the recommended V_{IO} specification (5.5 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

This application is typical of an 18-bit RGB display panel layout.

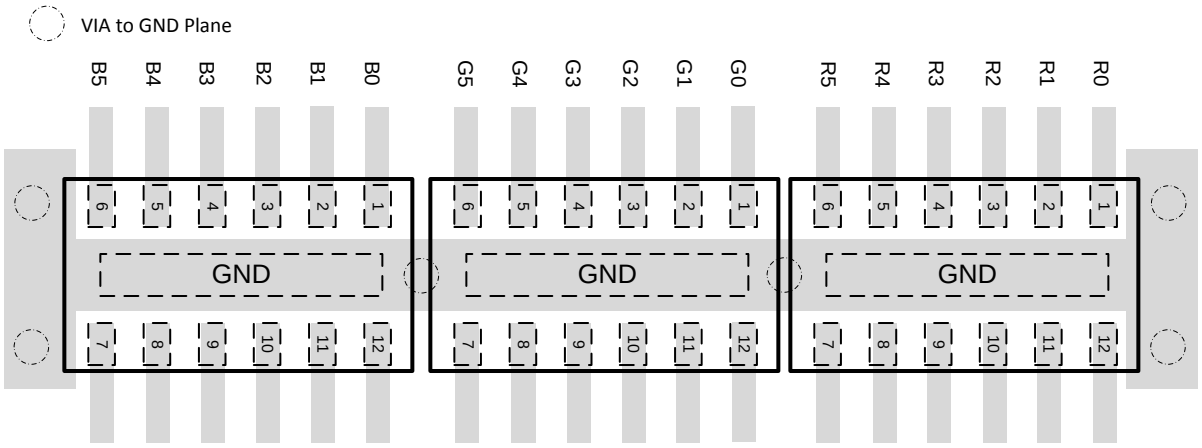


Figure 12. TPD6F003 Layout

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPD4F003	Click here	Click here	Click here	Click here	Click here
TPD6F003	Click here	Click here	Click here	Click here	Click here
TPD8F003	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4F003DQDR	ACTIVE	WSON	DQD	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5RS	Samples
TPD6F003DQDR	ACTIVE	WSON	DQD	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	47S	Samples
TPD8F003DQDR	ACTIVE	WSON	DQD	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5US	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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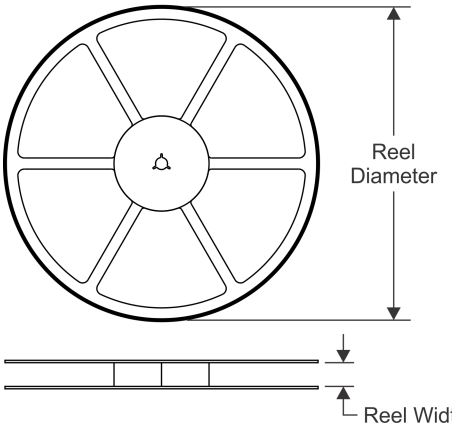
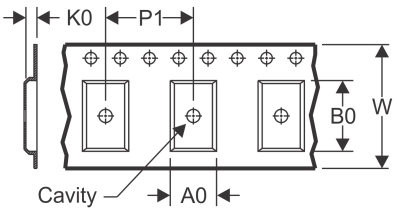
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

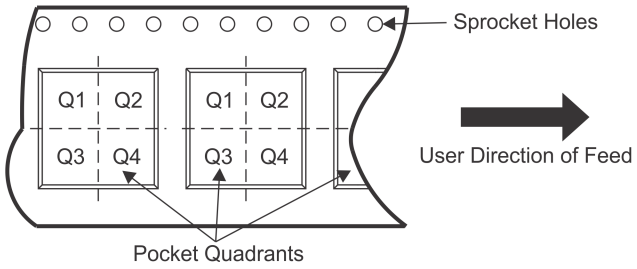


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

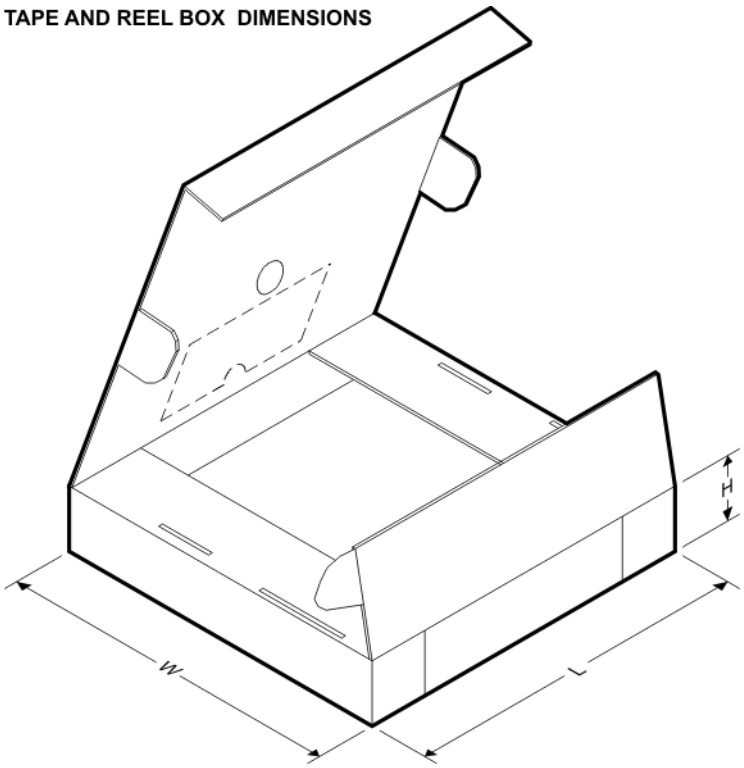
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4F003DQDR	WSON	DQD	8	3000	180.0	8.4	1.65	2.0	0.95	4.0	8.0	Q1
TPD6F003DQDR	WSON	DQD	12	3000	180.0	8.4	1.68	2.79	0.91	4.0	8.0	Q1
TPD8F003DQDR	WSON	DQD	16	3000	330.0	12.4	1.65	3.6	0.95	4.0	12.0	Q1

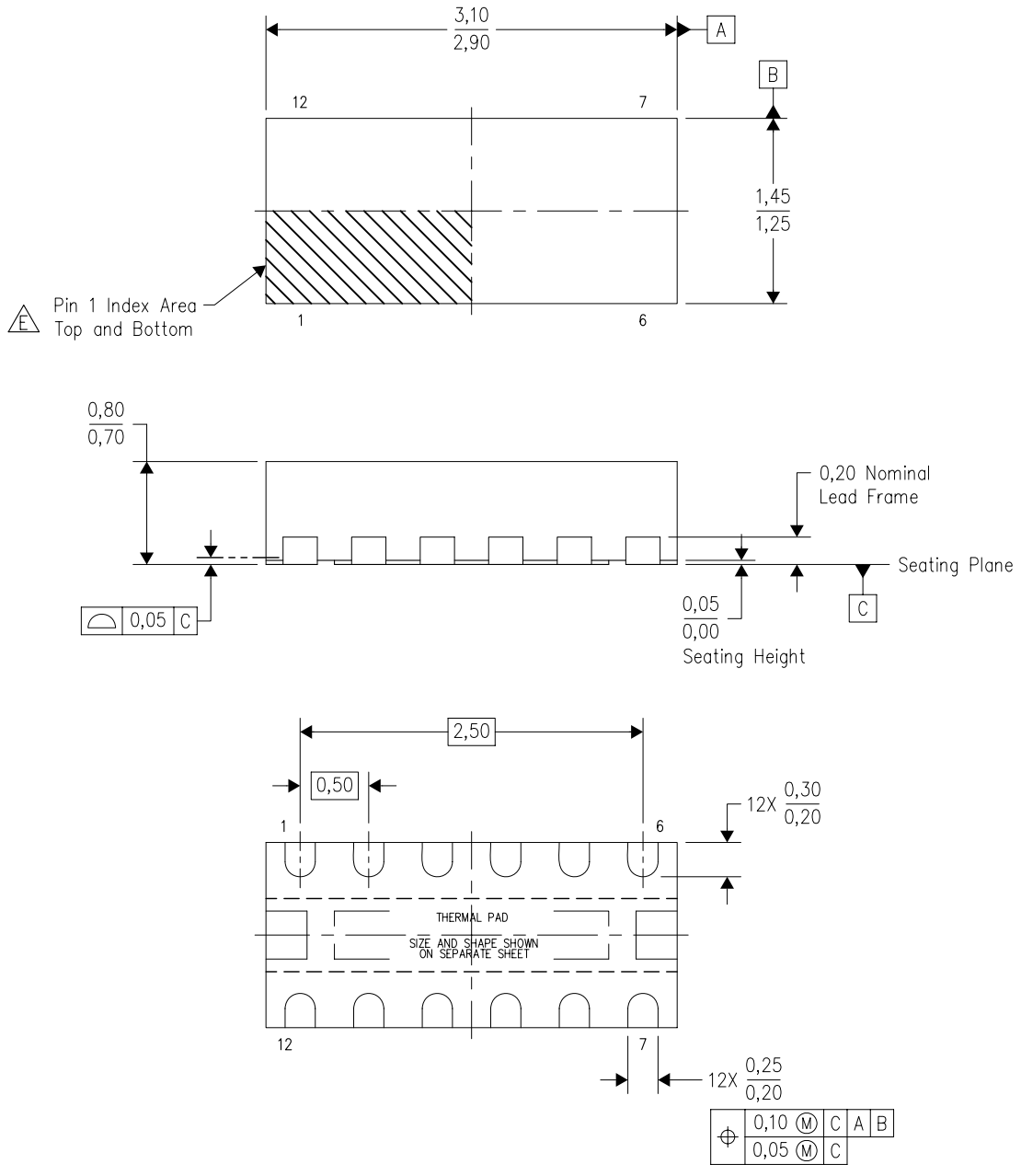
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

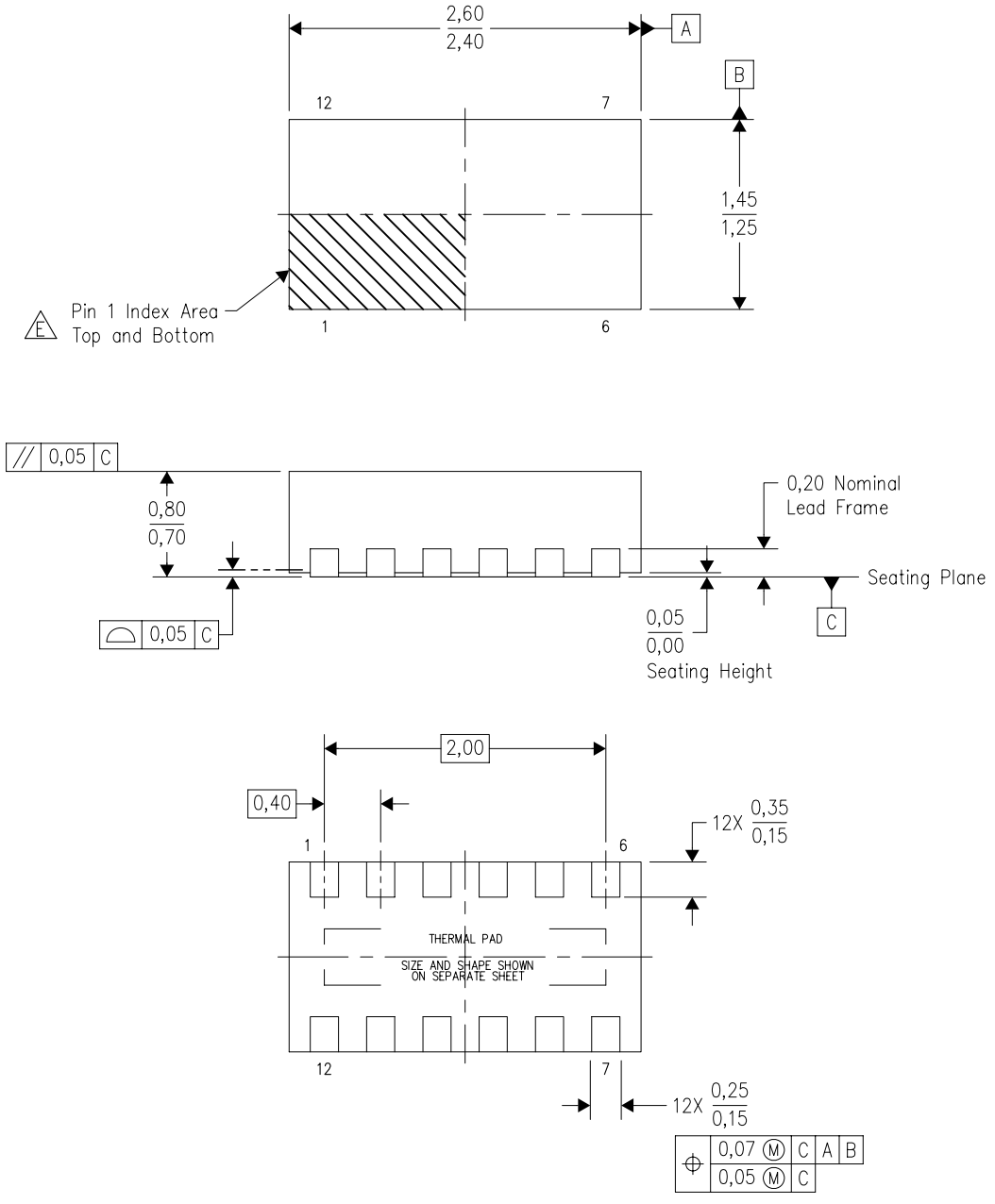
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4F003DQDR	WSON	DQD	8	3000	202.0	201.0	28.0
TPD6F003DQDR	WSON	DQD	12	3000	202.0	201.0	28.0
TPD8F003DQDR	WSON	DQD	16	3000	358.0	335.0	35.0

DSV (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

DQD (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



4209732–3/C 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

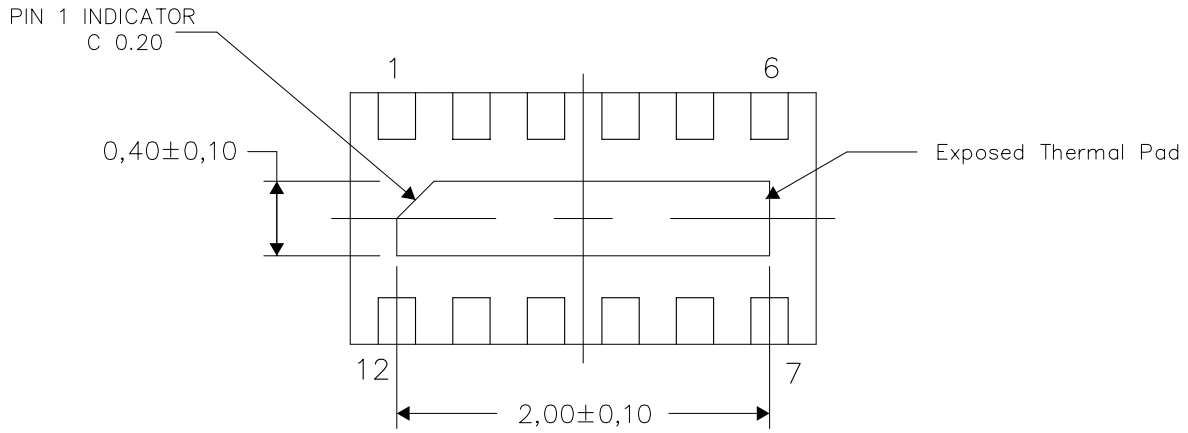
DQD (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



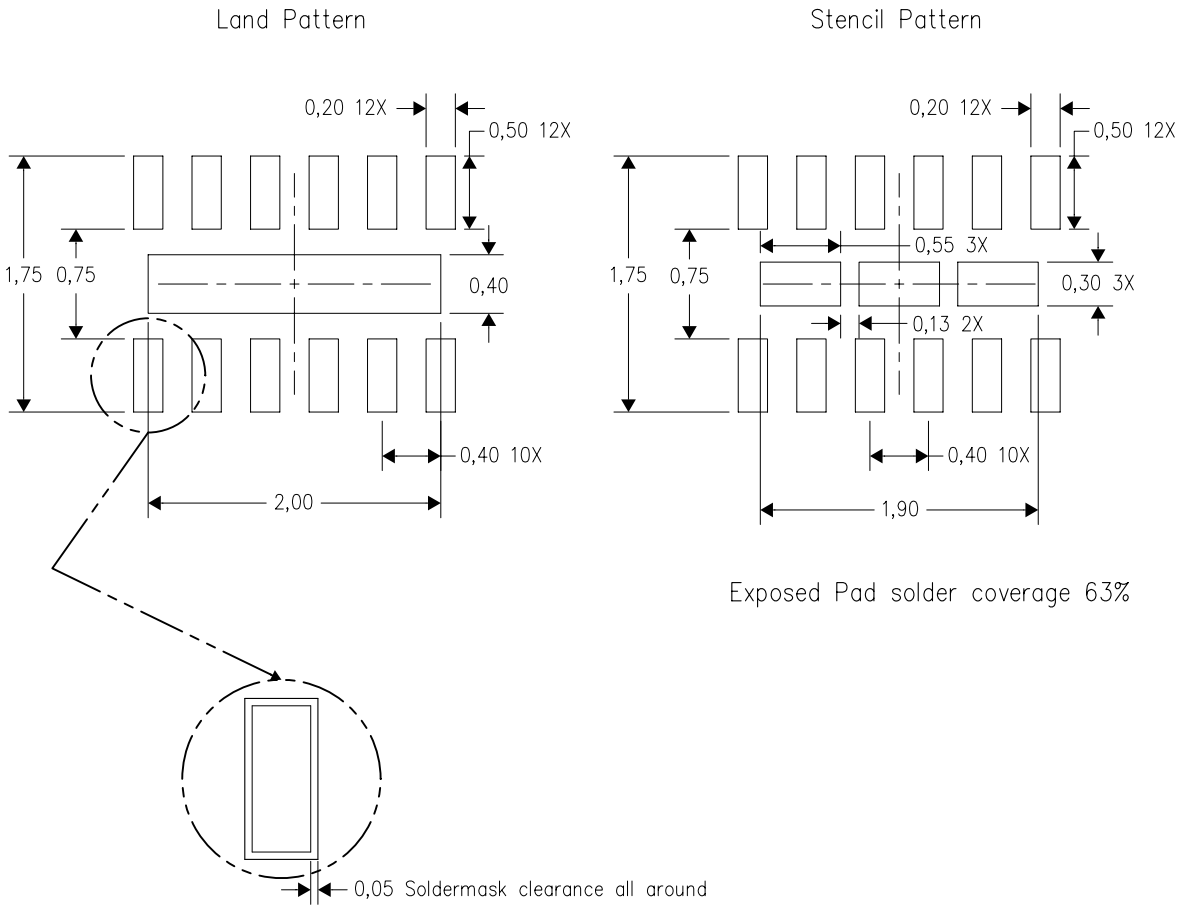
Bottom View

Exposed Thermal Pad Dimensions

4209733–3/C 12/11

NOTE: All linear dimensions are in millimeters

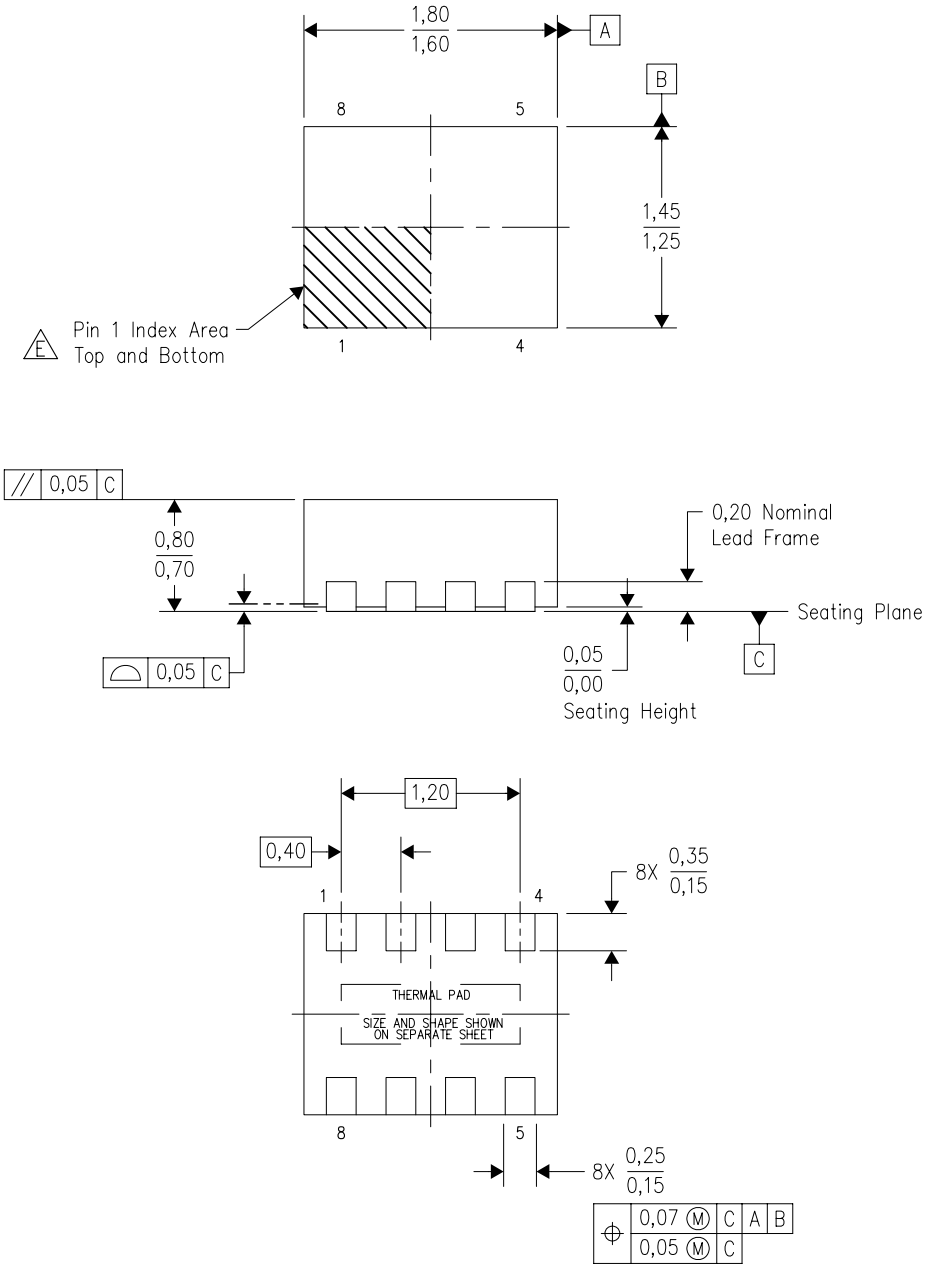
DQD (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



4211174–3/B 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DQD (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



Bottom View

4209732–2/C 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

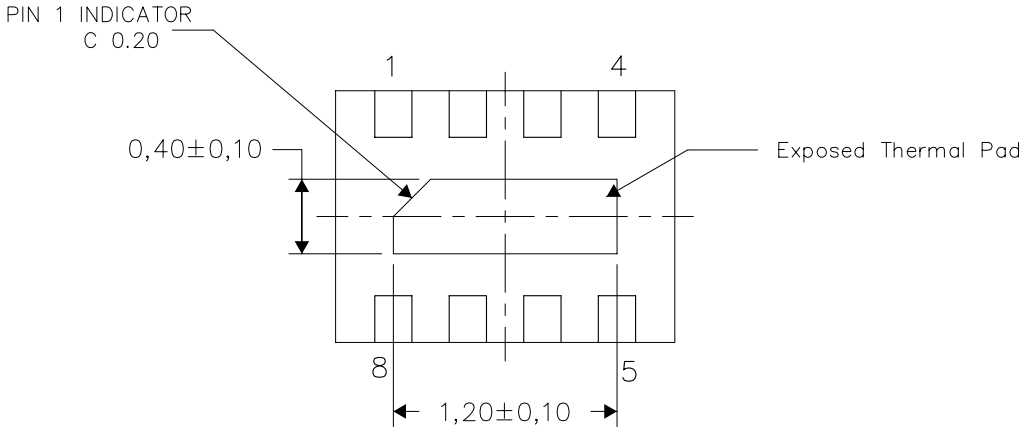
DQD (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

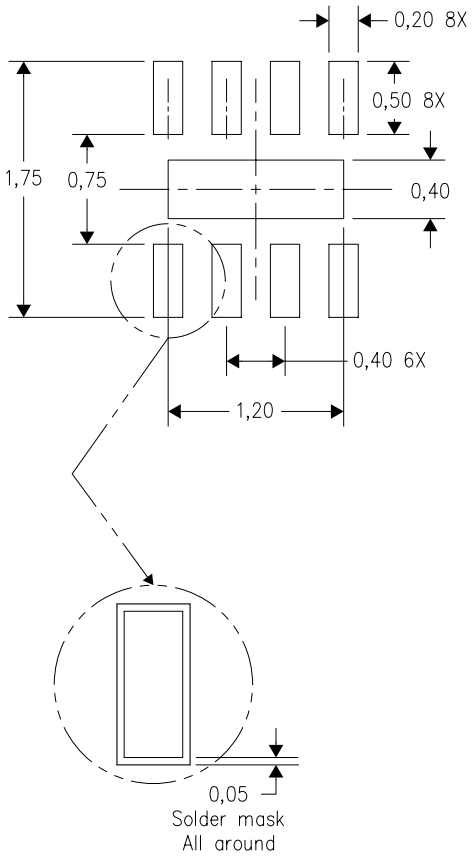
Exposed Thermal Pad Dimensions

4209733–2/C 12/11

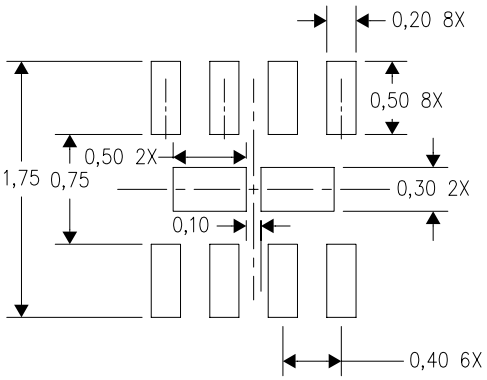
NOTE: All linear dimensions are in millimeters

DQD (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

Land Pattern



Stencil Pattern

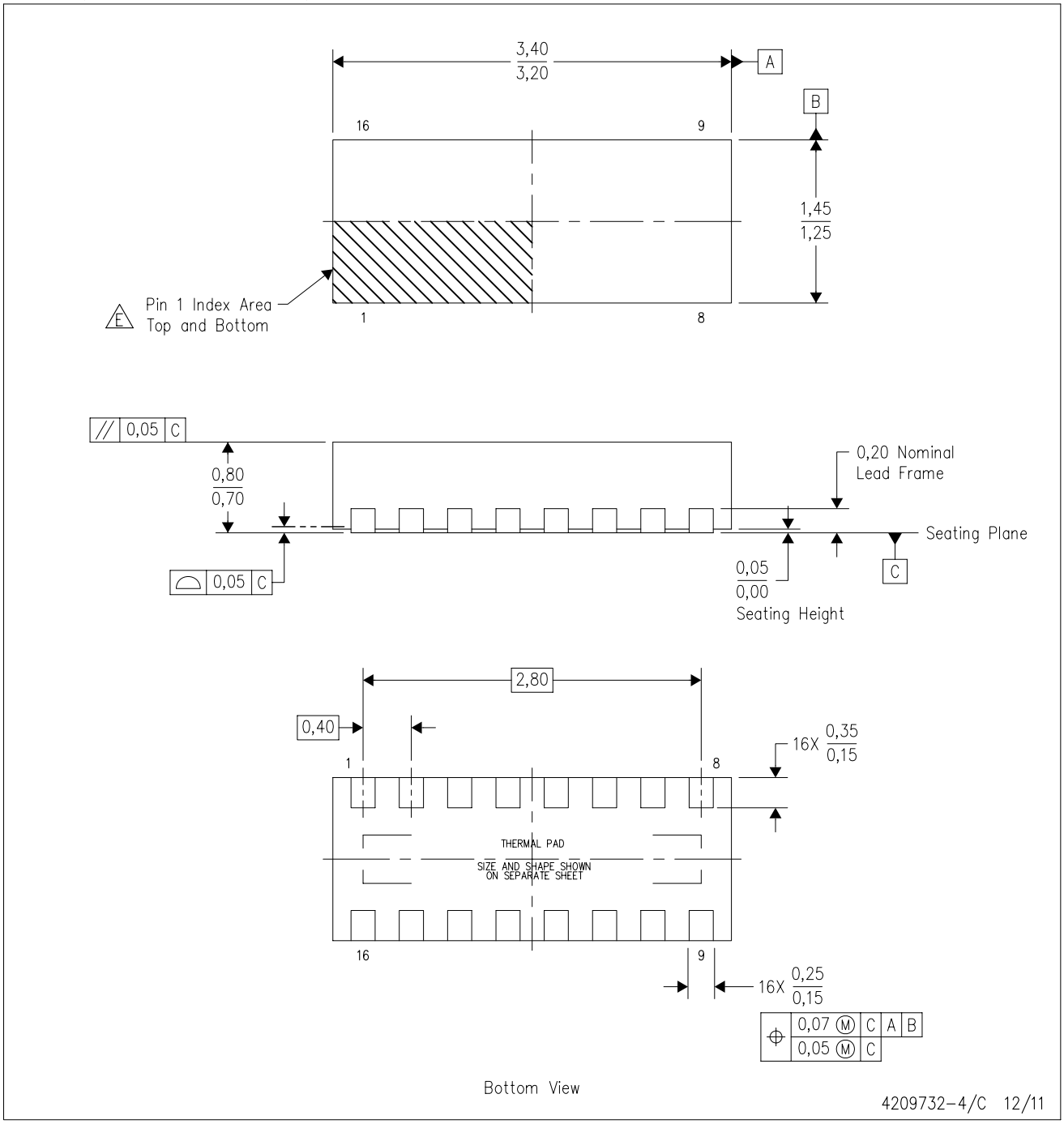


Exposed Pad solder coverage 62%

4211174–2/B 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DQD (R–PWSON–N16) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

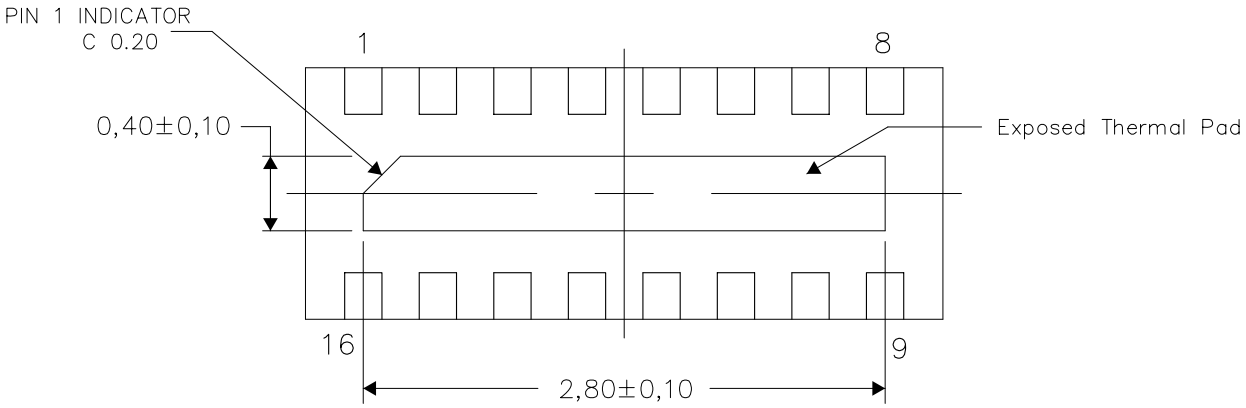
DQD (R–PWSON–N16) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



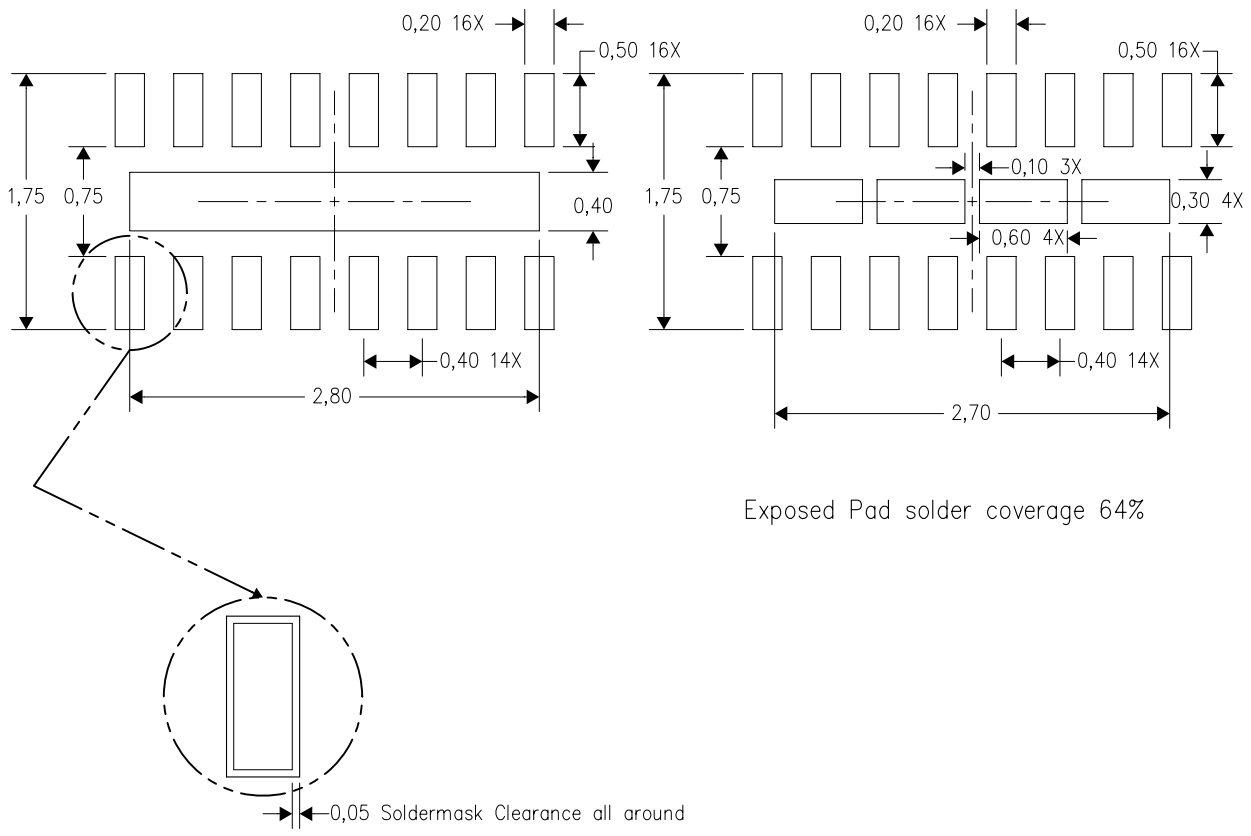
Bottom View

Exposed Thermal Pad Dimensions

4209733–4/C 12/11

NOTE: All linear dimensions are in millimeters

DQD (R–PWSON–N16) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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