

# 0.75-Ω DUAL SPDT ANALOG SWITCH WITH INPUT LOGIC TRANSLATION

Check for Samples: [TS5A26542](#)

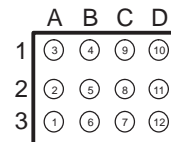
## FEATURES

- Specified Break-Before-Make Switching
- Low ON-State Resistance (0.75 Ω Max)
- Control Inputs Reference to  $V_{IO}$
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 2.25-V to 5.5-V Power Supply ( $V_+$ )
- 1.65-V to 1.95-V Logic Supply ( $V_{IO}$ )
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
  - 300-V Machine Model (A115-A)
- COM Inputs
  - 8000-V Human-Body Model (A114-B, Class II)
  - ±15-kV Contact Discharge (IEC 61000-4-2)

## APPLICATIONS

- Cell Phones
- PDA's
- Portable Instrumentation

YZT PACKAGE<sup>(1)</sup>  
(BOTTOM VIEW)


<sup>(1)</sup>The GND balls are internally connected.

	A	B	C	D
1	IN1	NO1	COM1	NC1
2	VIO	GND	GND	V+
3	IN2	NO2	COM2	NC2

## DESCRIPTION

The TS5A26542 is a dual single-pole double-throw (SPDT) analog switch that is designed to operate from 2.25 V to 5.5 V. The device offers a low ON-state resistance with an excellent channel-to-channel ON-state resistance matching, and the break-before-make feature to prevent signal distortion during the transferring of a signal from one path to the another. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

The TS5A26542 has a separate logic supply pin ( $V_{IO}$ ) that operates from 1.65 V to 1.95 V.  $V_{IO}$  powers the control circuitry, which allows the TS5A26542 to be controlled by 1.8-V signals.

**Table 1. ORDERING INFORMATION**

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZT (Pb-free) 0.625-mm max height	Reel of 3000	TS5A26542YZTR	___ JN_

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](#).

(2) YZT: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

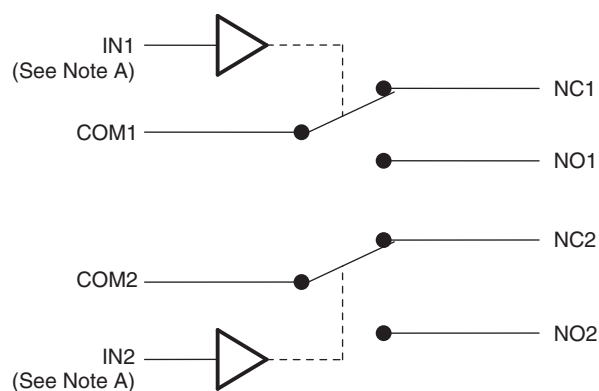
Copyright © 2006–2009, Texas Instruments Incorporated

**SUMMARY OF CHARACTERISTICS<sup>(1)</sup>**

Configuration	2:1 Multiplexer/Demultiplexer (2 × SPDT)
Number of channels	2
ON-state resistance ( $r_{on}$ )	0.75 $\Omega$ max
ON-state resistance match ( $\Delta r_{on}$ )	0.1 $\Omega$ max
ON-state resistance flatness ( $r_{on(flat)}$ )	0.1 $\Omega$ max
Turn-on/turn-off time ( $t_{ON}/t_{OFF}$ )	25 ns/20 ns
Charge injection ( $Q_C$ )	15 pC
Bandwidth (BW)	43 MHz
OFF isolation ( $O_{ISO}$ )	–63 dB at 1 MHz
Crosstalk ( $X_{TALK}$ )	–63 dB at 1 MHz
Total harmonic distortion (THD)	0.004%
Leakage current ( $I_{NO(OFF)}/I_{NC(OFF)}$ )	20 nA
Package option	12-pin WCSP

(1)  $V_+ = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ **FUNCTION TABLE**

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

**LOGIC DIAGRAM**A. IN1 and IN2 are control inputs referenced to  $V_{IO}$ .

## ABSOLUTE MAXIMUM RATINGS<sup>(1) (2)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_+$ $V_{IO}$	Supply voltage range <sup>(3)</sup>		–0.5	6.5	V
$V_{NC}$ $V_{NO}$ $V_{COM}$	Analog voltage range <sup>(3) (4) (5)</sup>		–0.5	$V_+ + 0.5$	V
$I_{I/O}$	Analog port diode current	$V_{NO}, V_{NC}, V_{COM} < 0$ or $V_{NO}, V_{NC}, V_{COM} > V_+$	–50	50	mA
$I_{NC}$ $I_{NO}$ $I_{COM}$	ON-state switch current	$V_{NO}, V_{NC}, V_{COM} = 0$ to $V_+$	–450	450	mA
	ON-state peak switch current <sup>(6)</sup>		–700	700	
$V_I$	Digital input voltage range <sup>(3) (4)</sup>		–0.5	6.5	V
$I_{IK}$	Digital input clamp current	$V_I < 0$	–50		mA
$I_+$ $I_{GND}$	Continuous current through $V_+$ or GND		–100	100	mA
$\theta_{JA}$	Package thermal impedance <sup>(7)</sup>			102	°C/W
$T_{stg}$	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration <10% duty cycle
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

**ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY<sup>(1)</sup>**
 $V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{IO} = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V <sub>COM</sub> , V <sub>NO</sub>					0		V <sub>+</sub>	V
ON-state resistance	r <sub>on</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 2.5 V, I <sub>COM</sub> = −100 mA,	Switch ON, See <a href="#">Figure 14</a>	25°C Full	4.5 V	0.5		0.75 0.8	Ω
ON-state resistance match between channels	Δr <sub>on</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 2.5 V, I <sub>COM</sub> = −100 mA,	Switch ON, See <a href="#">Figure 14</a>	25°C Full	4.5 V	0.05		0.1 0.1	Ω
ON-state resistance flatness	r <sub>on(flat)</sub>	0 ≤ (V <sub>NO</sub> or V <sub>NC</sub> ) ≤ V <sub>+</sub> , I <sub>COM</sub> = −100 mA,	Switch ON, See <a href="#">Figure 14</a>	25°C	4.5 V	0.1			Ω
		V <sub>NO</sub> or V <sub>NC</sub> = 1 V, 1.5 V, 2.5 V, I <sub>COM</sub> = −100 mA,	Switch ON, See <a href="#">Figure 14</a>	25°C		0.1	0.25		
				Full			0.25		
NO, NC OFF leakage current	I <sub>NO(OFF)</sub> , I <sub>NC (OFF)</sub>	V <sub>NO</sub> = 1 V, 4.5 V, V <sub>COM</sub> = 4.5 V, 1 V, V <sub>NC</sub> = Open, or V <sub>NC</sub> = 1 V, 4.5 V, V <sub>COM</sub> = 4.5 V, 1 V, V <sub>NO</sub> = Open,	Switch OFF, See <a href="#">Figure 15</a>	25°C Full	5.5 V	−20 −100	2 100	20 100	nA
NC, NO ON leakage current	I <sub>NO(ON)</sub>	V <sub>NO</sub> = 1 V, 4.5 V, V <sub>NC</sub> and V <sub>COM</sub> = Open, or V <sub>NC</sub> = 1V, 4.5 V, V <sub>NO</sub> and V <sub>COM</sub> = Open,	Switch ON, See <a href="#">Figure 16</a>	25°C Full	5.5 V	−20 −200	2 200	20 200	nA
COM ON leakage current	I <sub>COM(ON)</sub>	V <sub>COM</sub> = 1 V, V <sub>NO</sub> and V <sub>NC</sub> = Open, or V <sub>COM</sub> = 4.5 V, V <sub>NO</sub> and V <sub>NC</sub> = Open,	See <a href="#">Figure 16</a>	25°C Full	5.5 V	−20 −200	2 200	20 200	nA
Digital Control Inputs (IN1, IN2) <sup>(2)</sup>									
Input logic high	V <sub>IH</sub>	V <sub>IO</sub> = 1.65 V to 1.95 V		Full		0.65 × V <sub>IO</sub>		V <sub>IO</sub>	V
Input logic low	V <sub>IL</sub>	V <sub>IO</sub> = 1.65 V to 1.95 V		Full		0		0.35 × V <sub>IO</sub>	V
Input leakage current	I <sub>IH</sub> , I <sub>IL</sub>	V <sub>I</sub> = V <sub>IO</sub> or 0		25°C	5.5 V	−2		2	nA
				Full		−20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_{IO}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY<sup>(1)</sup> (continued)**
 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $V_{IO} = 1.65 \text{ V to } 1.95 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T <sub>A</sub>	V+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t <sub>ON</sub>	V <sub>COM</sub> = V <sub>+</sub> , R <sub>L</sub> = 50 Ω,	C <sub>L</sub> = 35 pF, See <a href="#">Figure 18</a>	25°C	5 V	1	12.5	25	ns
				Full	4.5 V			30	
Turn-off time	t <sub>OFF</sub>	V <sub>COM</sub> = V <sub>+</sub> , R <sub>L</sub> = 50 Ω,	C <sub>L</sub> = 35 pF, See <a href="#">Figure 18</a>	25°C	5 V	1	9.5	20	ns
				Full	4.5 V			25	
Break-before-make time	t <sub>BBM</sub>	V <sub>NC</sub> = V <sub>NO</sub> = V <sub>+</sub> /2, R <sub>L</sub> = 50 Ω,	C <sub>L</sub> = 35 pF, See <a href="#">Figure 19</a>	25°C	5 V	1	5	10	ns
				Full	4.5 V	1		12	
Charge injection	Q <sub>C</sub>	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0,	C <sub>L</sub> = 1 nF, See <a href="#">Figure 23</a>	25°C	5 V		15		pC
NO OFF capacitance	C <sub>NO(OFF)</sub>	V <sub>NO</sub> = V <sub>+</sub> or GND, Switch OFF,	See <a href="#">Figure 17</a>	25°C	5 V		37		pF
NC, NO ON capacitance	C <sub>NC(ON)</sub> , C <sub>NO(ON)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = V <sub>+</sub> or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	5 V		130		pF
COM ON capacitance	C <sub>COM(ON)</sub>	V <sub>COM</sub> = V <sub>+</sub> or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	5 V		130		pF
Digital input capacitance	C <sub>I</sub>	V <sub>I</sub> = V <sub>IO</sub> or GND,	See <a href="#">Figure 17</a>	25°C	5 V		6.5		pF
Bandwidth	BW	R <sub>L</sub> = 50 Ω, Switch ON,	See <a href="#">Figure 20</a>	25°C	5 V		43		MHz
OFF isolation	O <sub>ISO</sub>	R <sub>L</sub> = 50 Ω, f = 1 MHz,	See <a href="#">Figure 21</a>	25°C	5 V		−63		dB
Crosstalk	X <sub>TALK</sub>	R <sub>L</sub> = 50 Ω, f = 1 MHz,	See <a href="#">Figure 22</a>	25°C	5 V		−63		dB
Total harmonic distortion	THD	R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF,	f = 20 Hz to 20 kHz, See <a href="#">Figure 24</a>	25°C	5 V		0.004		%
Supply									
Positive supply current	I <sub>+</sub>	V <sub>I</sub> = V <sub>IO</sub> or GND		25°C	5.5 V		5.5	100	nA
				Full				750	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

## Electrical Characteristics for 3.3-V Supply<sup>(1)</sup>

$V_+ = 3\text{ V}$  to  $3.6\text{ V}$ ,  $V_{IO} = 1.65\text{ V}$  to  $1.95\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V
ON-state resistance	$r_{on}$	$V_{NO}$ or $V_{NC} = 2\text{ V}$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C Full	3 V	0.75		0.9 1.2	$\Omega$
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO}$ or $V_{NC} = 2\text{ V}$ , $0.8\text{ V}$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C Full	3 V	0.1		0.15 0.15	$\Omega$
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C Full	3 V	0.2 0.1		0.3 0.3	$\Omega$
NO, NC OFF leakage current	$I_{NO(OFF)}, I_{NC(OFF)}$	$V_{NO} = 1\text{ V}$ , $3\text{ V}$ , $V_{COM} = 3\text{ V}$ , $1\text{ V}$ , $V_{NC} = \text{Open}$ , or $V_{NC} = 1\text{ V}$ , $3\text{ V}$ , $V_{COM} = 3\text{ V}$ , $1\text{ V}$ , $V_{NO} = \text{Open}$ , Switch OFF, See <a href="#">Figure 15</a>	25°C Full	3.6 V	-20 -50	2	20 50	nA
NC, NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1\text{ V}$ , $3\text{ V}$ , $V_{NC}$ and $V_{COM} = \text{Open}$ , or $V_{NC} = 1\text{ V}$ , $3\text{ V}$ , $V_{NO}$ and $V_{COM} = \text{Open}$ , Switch ON, See <a href="#">Figure 16</a>	25°C Full	3.6 V	-10 30	2	10 30	nA
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}$ , $V_{NO}$ and $V_{NC} = \text{Open}$ , or $V_{COM} = 3\text{ V}$ , $V_{NO}$ and $V_{NC} = \text{Open}$ , See <a href="#">Figure 16</a>	25°C Full	3.6 V	-10 -30	2	10 30	nA
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>								
Input logic high	$V_{IH}$	$V_{IO} = 1.65\text{ V}$ to $1.95\text{ V}$	Full		$0.65 \times V_{IO}$		$V_{IO}$	V
Input logic low	$V_{IL}$	$V_{IO} = 1.65\text{ V}$ to $1.95\text{ V}$	Full		0		$0.35 \times V_{IO}$	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = V_{IO}$ or 0	25°C Full	3.6 V	-2 -20		2 20	nA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_{IO}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY<sup>(1)</sup> (continued)**
 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $V_{IO} = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T <sub>A</sub>	V+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t <sub>ON</sub>	V <sub>COM</sub> = V <sub>+</sub> , R <sub>L</sub> = 50 Ω,	C <sub>L</sub> = 35 pF, See <a href="#">Figure 18</a>	25°C	3.3 V	5	15	30	ns
				Full	3 V	3		35	
Turn-off time	t <sub>OFF</sub>	V <sub>COM</sub> = V <sub>+</sub> , R <sub>L</sub> = 50 Ω,	C <sub>L</sub> = 35 pF, See <a href="#">Figure 18</a>	25°C	3.3 V	1	9	20	ns
				Full	3 V	1		25	
Break-before-make time	t <sub>BBM</sub>	V <sub>NC</sub> = V <sub>NO</sub> = V <sub>+</sub> /2, R <sub>L</sub> = 50 Ω,	C <sub>L</sub> = 35 pF, See <a href="#">Figure 19</a>	25°C	3.3 V	1	8	13	ns
				Full	3 V	1		15	
Charge injection	Q <sub>C</sub>	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0,	C <sub>L</sub> = 1 nF, See <a href="#">Figure 23</a>	25°C	3.3 V		6.5		pC
NO OFF capacitance	C <sub>NO(OFF)</sub>	V <sub>NO</sub> = V <sub>+</sub> or GND, Switch OFF,	See <a href="#">Figure 17</a>	25°C	3.3 V		38		pF
NC, NO ON capacitance	C <sub>NC(ON)</sub> , C <sub>NO(ON)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = V <sub>+</sub> or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	3.3 V		133		pF
COM ON capacitance	C <sub>COM(ON)</sub>	V <sub>COM</sub> = V <sub>+</sub> or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	3.3 V		133		pF
Digital input capacitance	C <sub>I</sub>	V <sub>I</sub> = V <sub>IO</sub> or GND,	See <a href="#">Figure 17</a>	25°C	3.3 V		6.5		pF
Bandwidth	BW	R <sub>L</sub> = 50 Ω, Switch ON,	See <a href="#">Figure 20</a>	25°C	3.3 V		42		MHz
OFF isolation	O <sub>ISO</sub>	R <sub>L</sub> = 50 Ω, f = 1 MHz,	See <a href="#">Figure 21</a>	25°C	3.3 V		−63		dB
Crosstalk	X <sub>TALK</sub>	R <sub>L</sub> = 50 Ω, f = 1 MHz,	See <a href="#">Figure 22</a>	25°C	3.3 V		−63		dB
Total harmonic distortion	THD	R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF,	f = 20 Hz to 20 kHz, See <a href="#">Figure 24</a>	25°C	3.3 V		0.004		%
Supply									
Positive supply current	I <sub>+</sub>	V <sub>I</sub> = V <sub>IO</sub> or GND	25°C	3.6 V		10	50	nA	
			Full				300		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

**ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY<sup>(1)</sup>**
 $V_+ = 2.25\text{ V to }2.75\text{ V}$ ,  $V_{IO} = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V <sub>COM</sub> , V <sub>NO</sub>					0		V <sub>+</sub>	V
ON-state resistance	r <sub>on</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.8 V, I <sub>COM</sub> = −100 mA,	Switch ON, See <a href="#">Figure 14</a>	25°C	2.25 V	1		1.3	Ω
				Full			1.6		
ON-state resistance match between channels	Δr <sub>on</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.8 V, 0.8 V, I <sub>COM</sub> = −100 mA,	Switch ON, See <a href="#">Figure 14</a>	25°C	2.25 V	0.15		0.2	Ω
				Full			0.2		
ON-state resistance flatness	r <sub>on(flat)</sub>	0 ≤ (V <sub>NO</sub> or V <sub>NC</sub> ) ≤ V <sub>+</sub> , I <sub>COM</sub> = −100 mA,	Switch ON, See <a href="#">Figure 14</a>	25°C	2.25 V	0.5			Ω
				25°C		0.25	0.5		
		V <sub>NO</sub> or V <sub>NC</sub> = 0.8 V, 1 V, 1.8 V, I <sub>COM</sub> = −100 mA,	Full			0.6			
NO, NC OFF leakage current	I <sub>NO(OFF)</sub> , I <sub>NC (OFF)</sub>	V <sub>NO</sub> = 0.5 V, 2.2 V, V <sub>COM</sub> = 2.2 V, 0.5 V, V <sub>NC</sub> = Open, or V <sub>NC</sub> = 0.5 V, 2.2 V, V <sub>COM</sub> = 2.2 V, 0.5 V, V <sub>NO</sub> = Open,	Switch OFF, See <a href="#">Figure 15</a>	25°C	2.75 V	−20	2	20	nA
				Full		−50		50	
NC, NO ON leakage current	I <sub>NO(ON)</sub>	V <sub>NO</sub> = 0.5 V, 2.2 V, V <sub>NC</sub> and V <sub>COM</sub> = Open, or V <sub>NC</sub> = 0.5 V, 2.2 V, V <sub>NO</sub> and V <sub>COM</sub> = Open,	Switch ON, See <a href="#">Figure 16</a>	25°C	2.75 V	−10	2	10	nA
				Full		−20		20	
COM ON leakage current	I <sub>COM(ON)</sub>	V <sub>COM</sub> = 0.5 V, V <sub>NO</sub> and V <sub>NC</sub> = Open, or V <sub>COM</sub> = 2.2 V, V <sub>NO</sub> and V <sub>NC</sub> = Open,	Switch ON, See <a href="#">Figure 16</a>	25°C	2.75 V	−10	2	10	nA
				Full		−50		50	
Digital Control Inputs (IN1, IN2) <sup>(2)</sup>									
Input logic high	V <sub>IH</sub>	V <sub>IO</sub> = 1.65 V to 1.95 V		Full		0.65 × V <sub>IO</sub>		V <sub>IO</sub>	V
Input logic low	V <sub>IL</sub>	V <sub>IO</sub> = 1.65 V to 1.95 V		Full		0		0.35 × V <sub>IO</sub>	V
Input leakage current	I <sub>IH</sub> , I <sub>IL</sub>	V <sub>I</sub> = V <sub>IO</sub> or 0		25°C	2.75 V	−2		2	nA
				Full		−20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_{IO}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

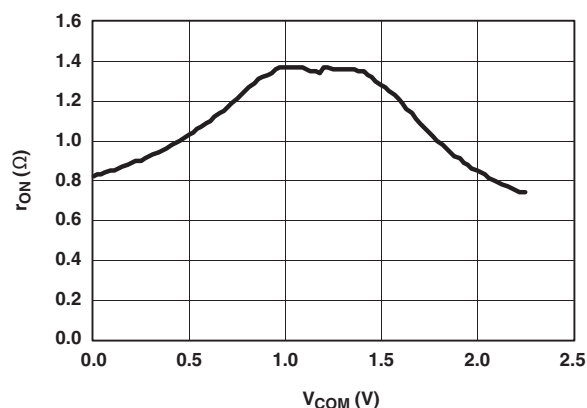
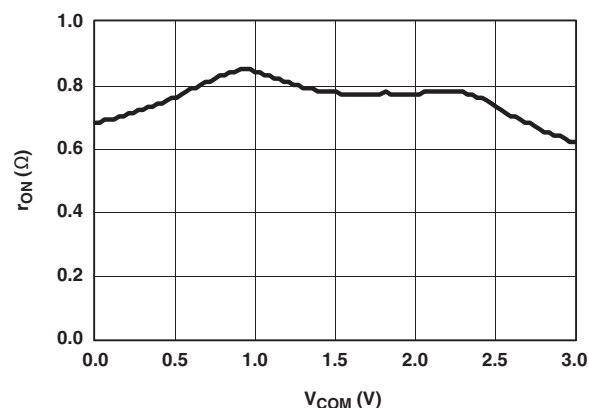
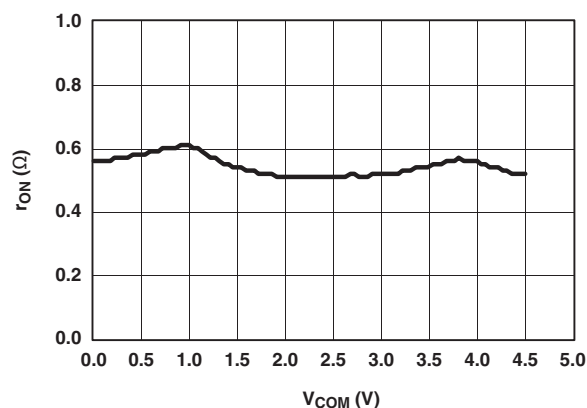
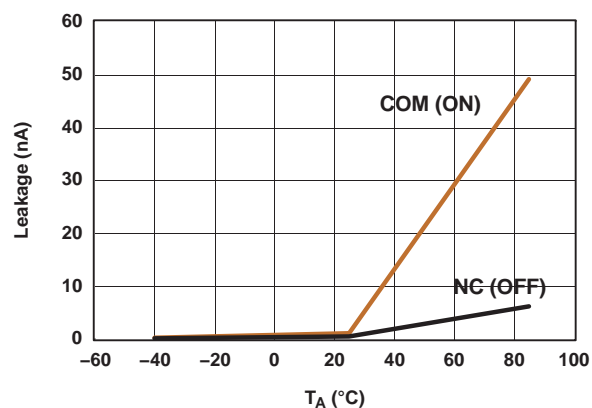
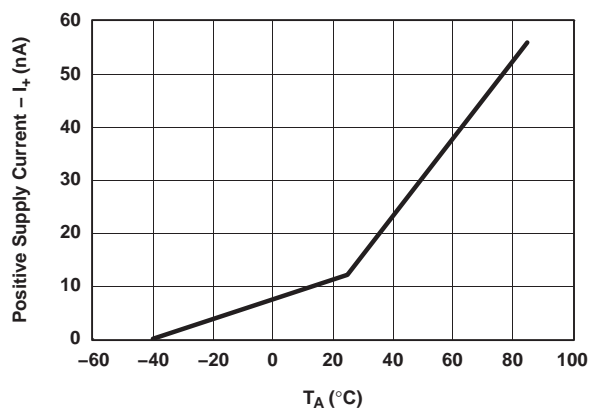
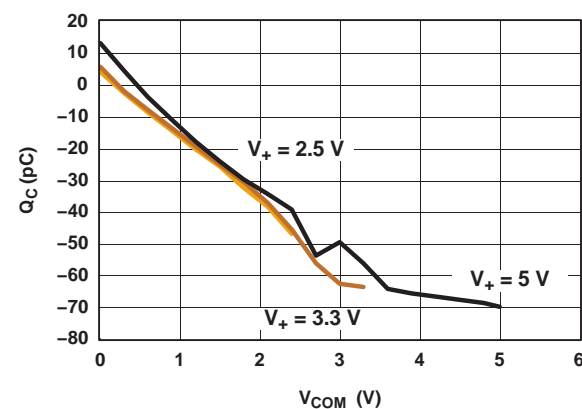


**ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY<sup>(1)</sup> (continued)**
 $V_+ = 2.25\text{ V to }2.75\text{ V}$ ,  $V_{IO} = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T <sub>A</sub>	V+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t <sub>ON</sub>	V <sub>COM</sub> = V <sub>+</sub> , R <sub>L</sub> = 50 Ω,	C <sub>L</sub> = 35 pF, See <a href="#">Figure 18</a>	25°C	2.5 V	5	20	35	ns
				Full	2.25 V	5		40	
Turn-off time	t <sub>OFF</sub>	V <sub>COM</sub> = V <sub>+</sub> , R <sub>L</sub> = 50 Ω,	C <sub>L</sub> = 35 pF, See <a href="#">Figure 18</a>	25°C	2.5 V	2	10	20	ns
				Full	2.25 V	2		25	
Break-before-make time	t <sub>BBM</sub>	V <sub>NC</sub> = V <sub>NO</sub> = V <sub>+</sub> /2, R <sub>L</sub> = 50 Ω,	C <sub>L</sub> = 35 pF, See <a href="#">Figure 19</a>	25°C	2.5 V	1	11	20	ns
				Full	2.25 V	1		25	
Charge injection	Q <sub>C</sub>	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0,	C <sub>L</sub> = 1 nF, See <a href="#">Figure 23</a>	25°C	2.5 V		5		pC
NO OFF capacitance	C <sub>NO(OFF)</sub>	V <sub>NO</sub> = V <sub>+</sub> or GND, Switch OFF,	See <a href="#">Figure 17</a>	25°C	2.5 V		38		pF
NC, NO ON capacitance	C <sub>NC(ON)</sub> , C <sub>NO(ON)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = V <sub>+</sub> or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	2.5 V		135		pF
COM ON capacitance	C <sub>COM(ON)</sub>	V <sub>COM</sub> = V <sub>+</sub> or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	2.5 V		135		pF
Digital input capacitance	C <sub>I</sub>	V <sub>I</sub> = V <sub>IO</sub> or GND,	See <a href="#">Figure 17</a>	25°C	2.5 V		6.5		pF
Bandwidth	BW	R <sub>L</sub> = 50 Ω, Switch ON,	See <a href="#">Figure 20</a>	25°C	2.5 V		40		MHz
OFF isolation	O <sub>ISO</sub>	R <sub>L</sub> = 50 Ω, f = 1 MHz,	See <a href="#">Figure 21</a>	25°C	2.5 V		−63		dB
Crosstalk	X <sub>TALK</sub>	R <sub>L</sub> = 50 Ω, f = 1 MHz,	See <a href="#">Figure 22</a>	25°C	2.5 V		−63		dB
Total harmonic distortion	THD	R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF,	f = 20 Hz to 20 kHz, See <a href="#">Figure 24</a>	25°C	2.5 V		0.008		%
Supply									
Positive supply current	I <sub>+</sub>	V <sub>I</sub> = V <sub>IO</sub> or GND		25°C	2.75 V		10	25	nA
				Full				100	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

## TYPICAL PERFORMANCE

Figure 1.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 2.5$  V)Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3.3$  V)Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 5$  V)Figure 4. Leakage Current vs Temperature ( $V_+ = 5$  V)Figure 5.  $I_+$  vs Temperature ( $V_+ = 5$  V)Figure 6. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

## TYPICAL PERFORMANCE (continued)

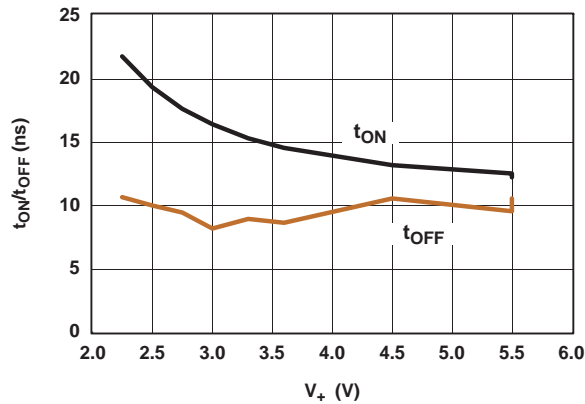


Figure 7.  $t_{ON}/t_{OFF}$  vs Supply Voltage

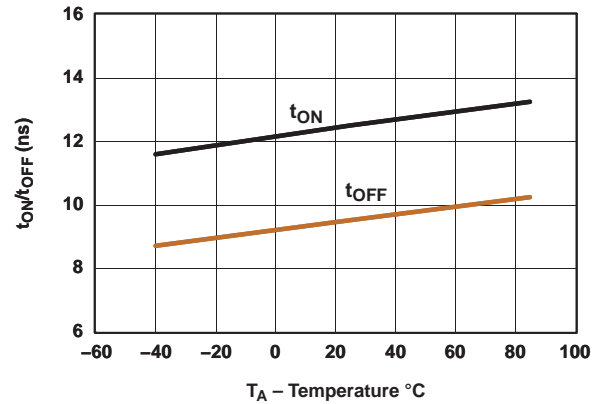


Figure 8.  $t_{ON}/t_{OFF}$  vs Temperature ( $V_+ = 5$  V)

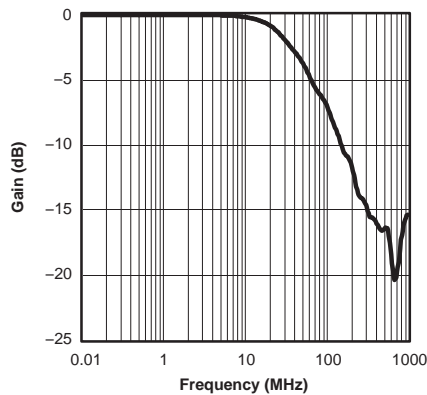


Figure 9. Gain vs Frequency ( $V_+ = 5$  V)

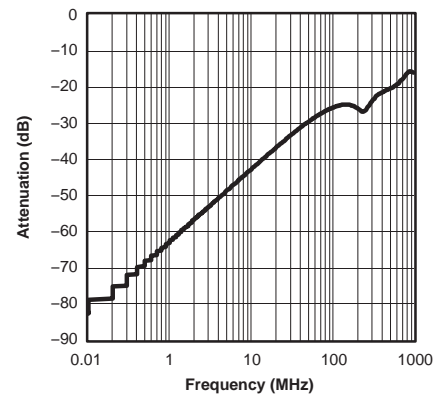


Figure 10. Crosstalk vs Frequency ( $V_+ = 5$  V)

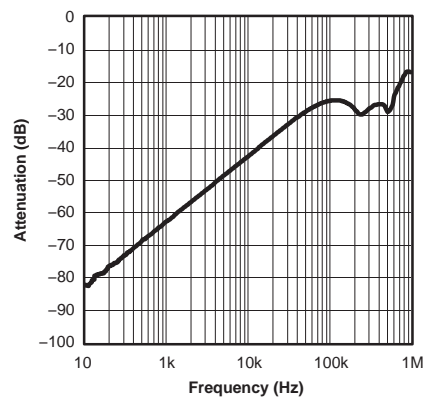


Figure 11. OFF Isolation vs Frequency ( $V_+ = 5$  V)

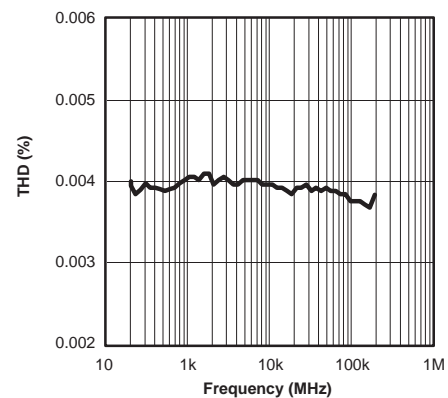
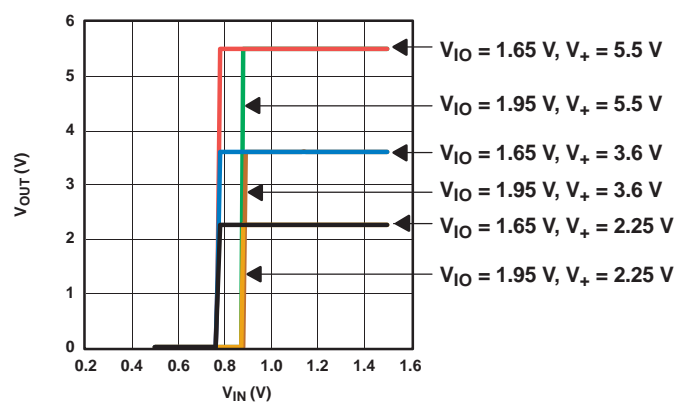
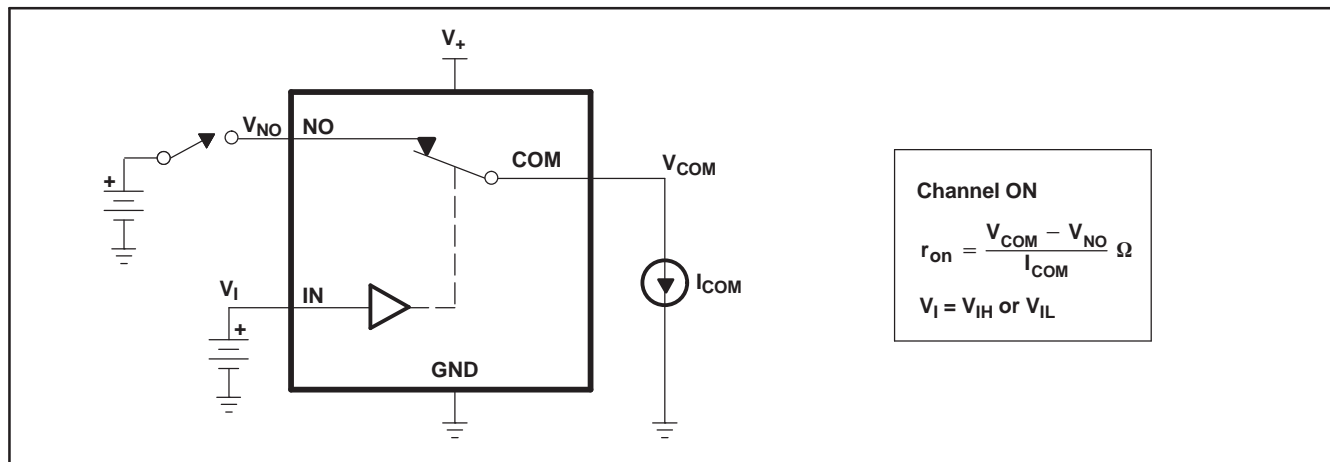


Figure 12. Total Harmonic Distortion vs Frequency ( $V_+ = 2.5$  V)

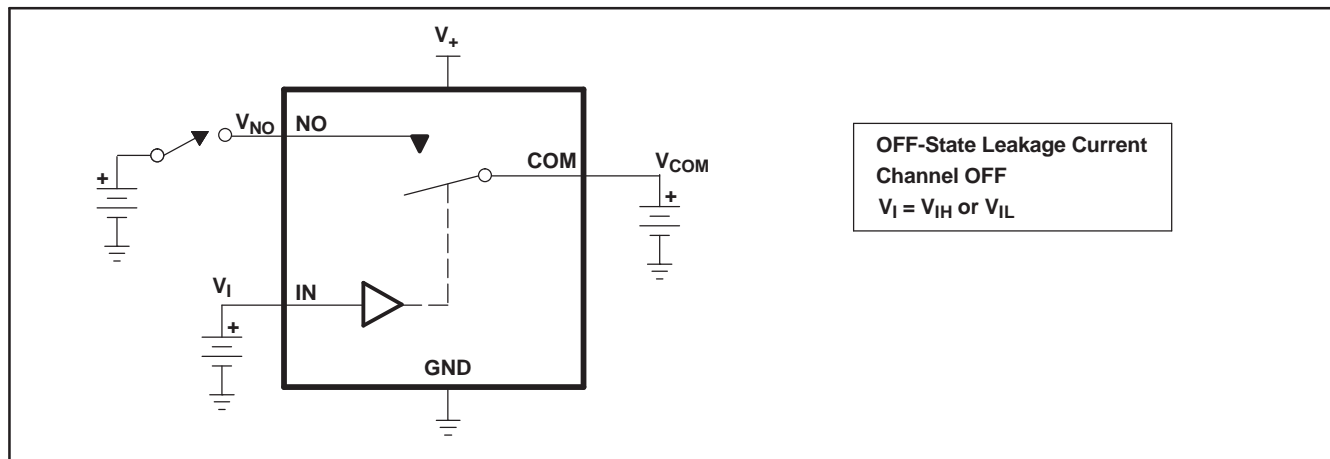
## TYPICAL PERFORMANCE (continued)

Figure 13.  $V_{IO}$  Thresholds

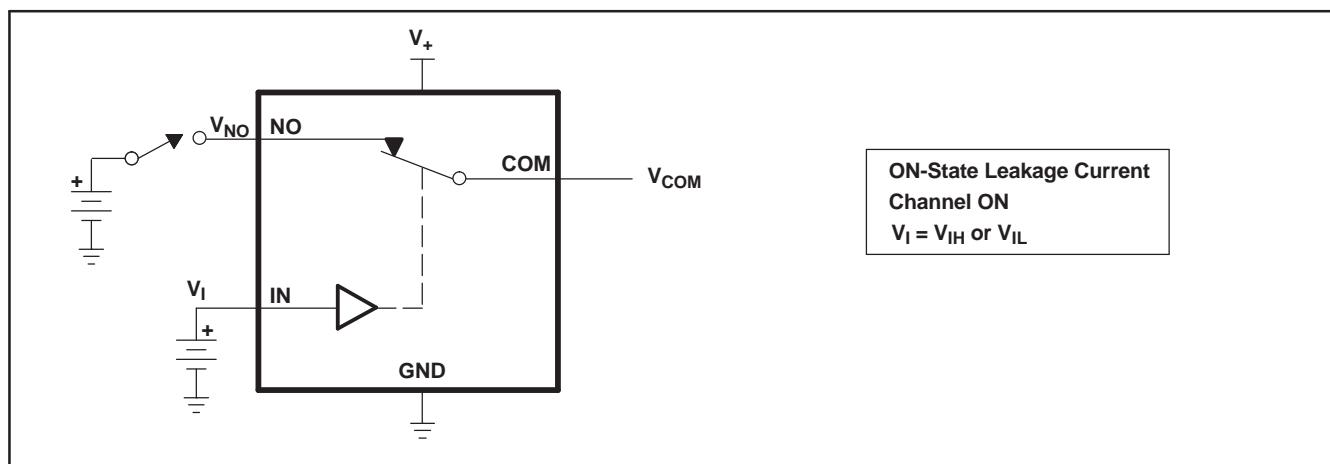
## PARAMETER MEASUREMENT INFORMATION



**Figure 14. ON-State Resistance ( $r_{on}$ )**



**Figure 15. OFF-State Leakage Current ( $I_{COM(OFF)}$ ,  $I_{NC(OFF)}$ ,  $I_{COM(PWROFF)}$ ,  $I_{NC(PWRFF)}$ )**



**Figure 16. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NC(ON)}$ )**

## PARAMETER MEASUREMENT INFORMATION (continued)

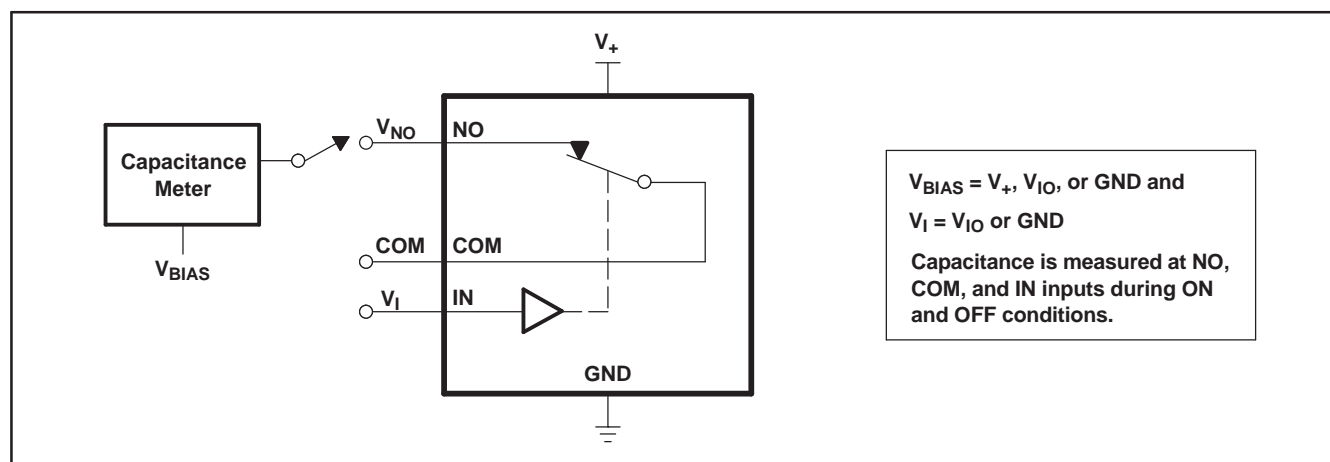
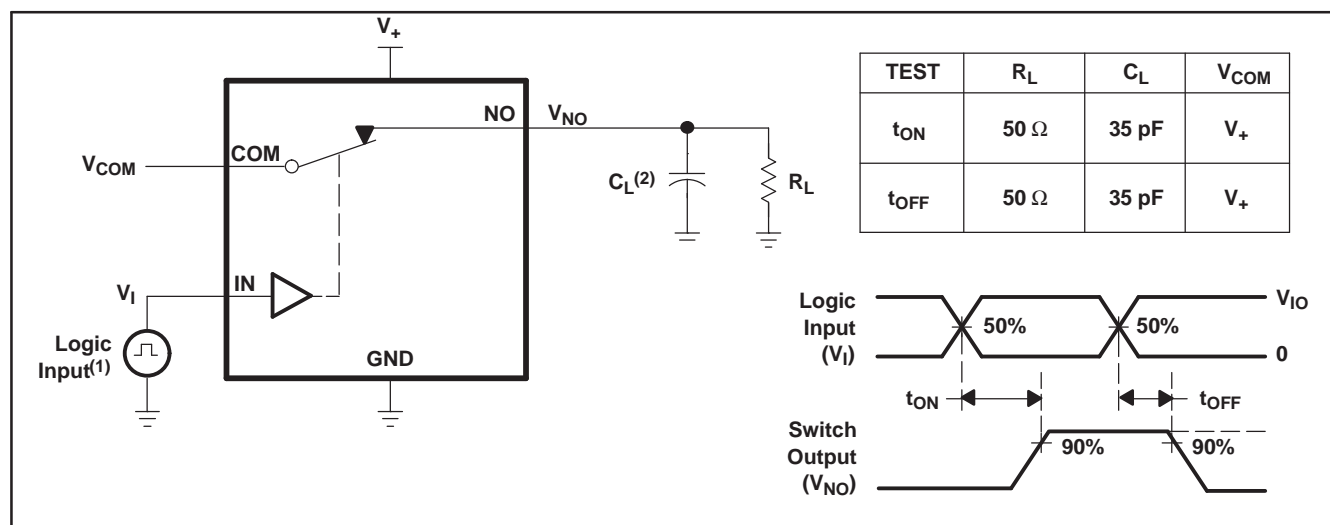


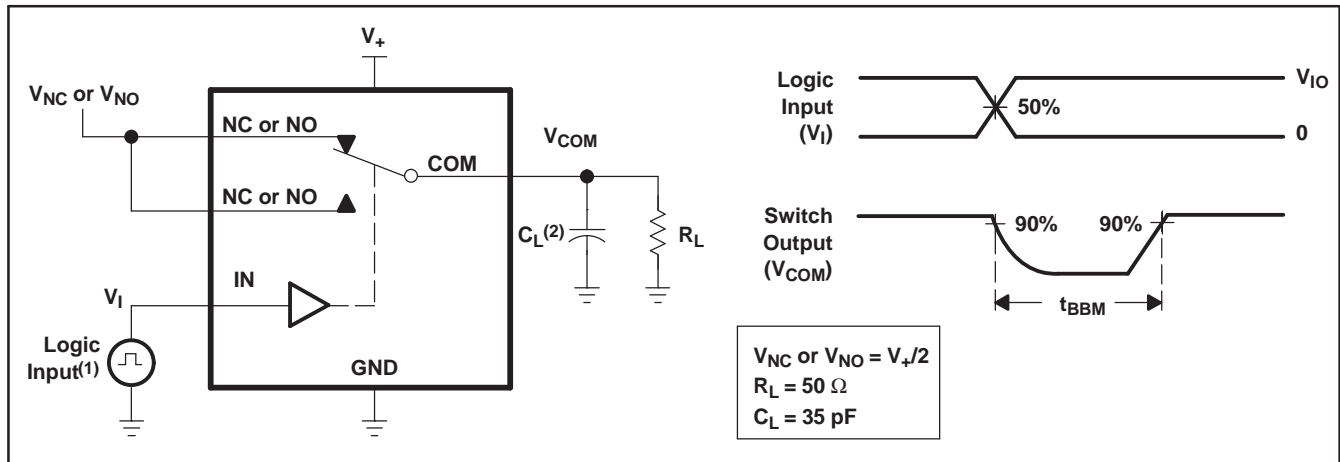
Figure 17. Capacitance ( $C_I$ ,  $C_{COM(OFF)}$ ,  $C_{COM(ON)}$ ,  $C_{NC(OFF)}$ ,  $C_{NC(ON)}$ )



NOTES: A. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\ \text{MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r < 5\ \text{ns}$ ,  $t_f < 5\ \text{ns}$ .  
 B.  $C_L$  includes probe and jig capacitance.

Figure 18. Turn-On ( $t_{ON}$ ) and Turn-Off Time ( $t_{OFF}$ )

## PARAMETER MEASUREMENT INFORMATION (continued)



NOTES: A. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 19. Break-Before-Make Time ( $t_{BBM}$ )

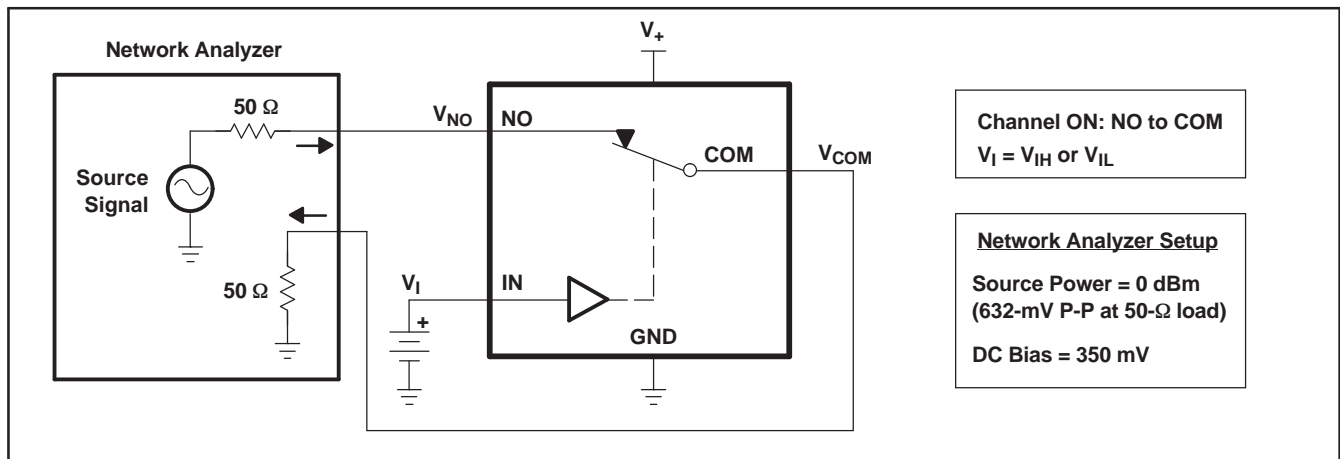
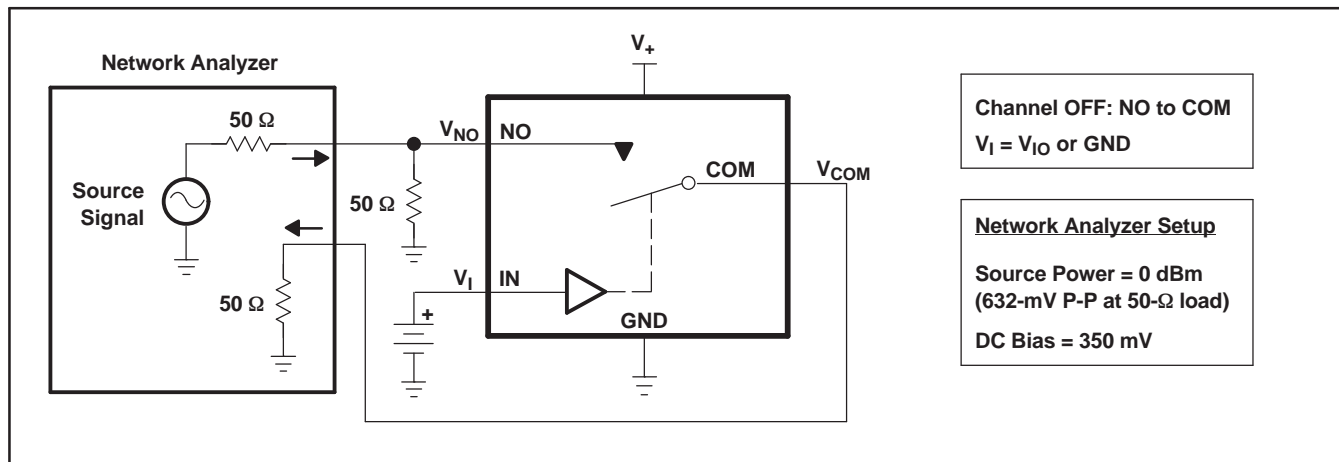
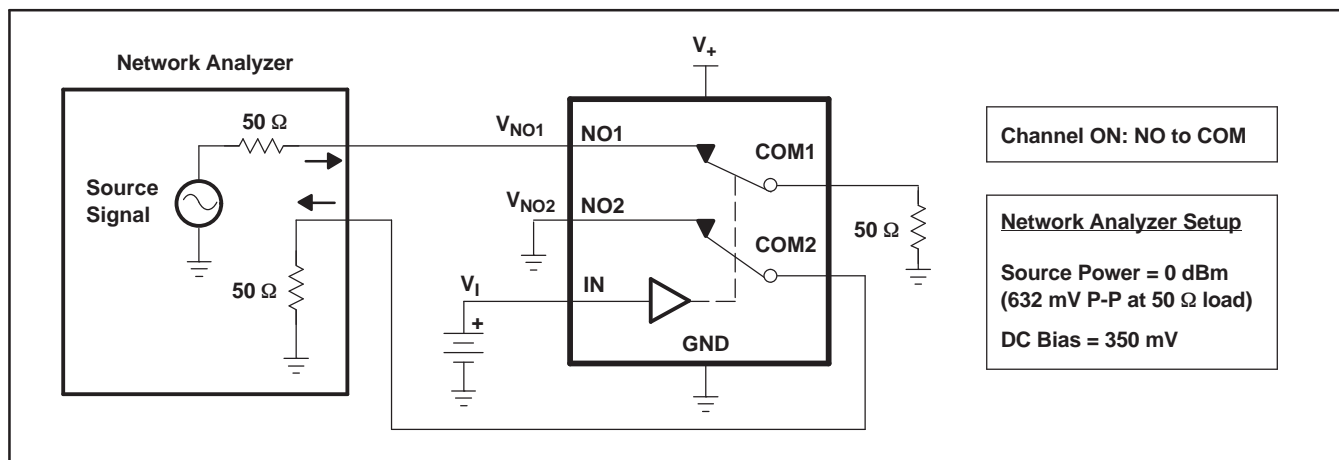


Figure 20. Bandwidth (BW)

### PARAMETER MEASUREMENT INFORMATION (continued)



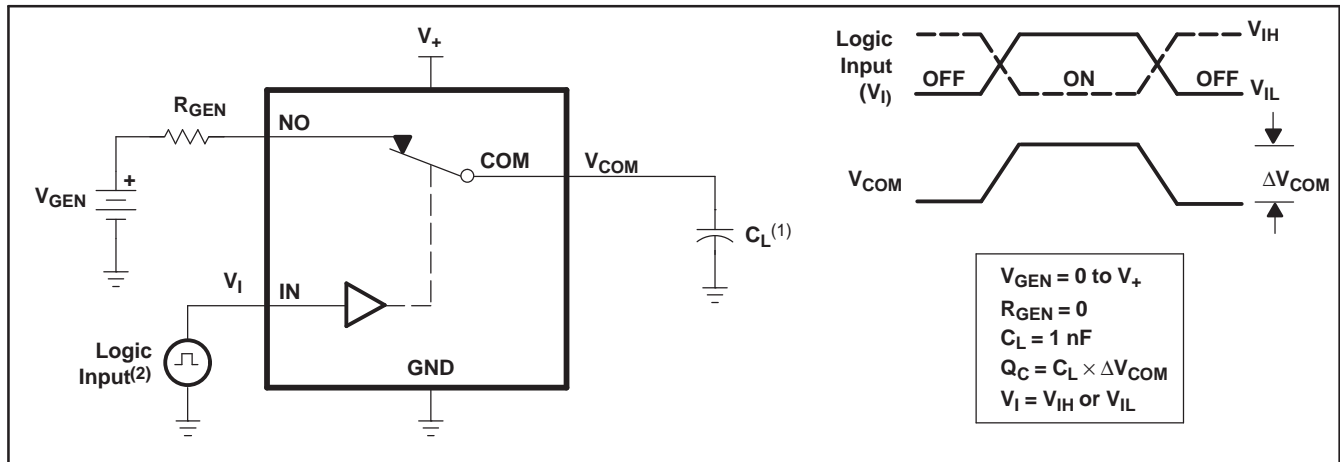
**Figure 21. OFF Isolation ( $O_{ISO}$ )**



**Figure 22. Crosstalk ( $X_{TALK}$ )**

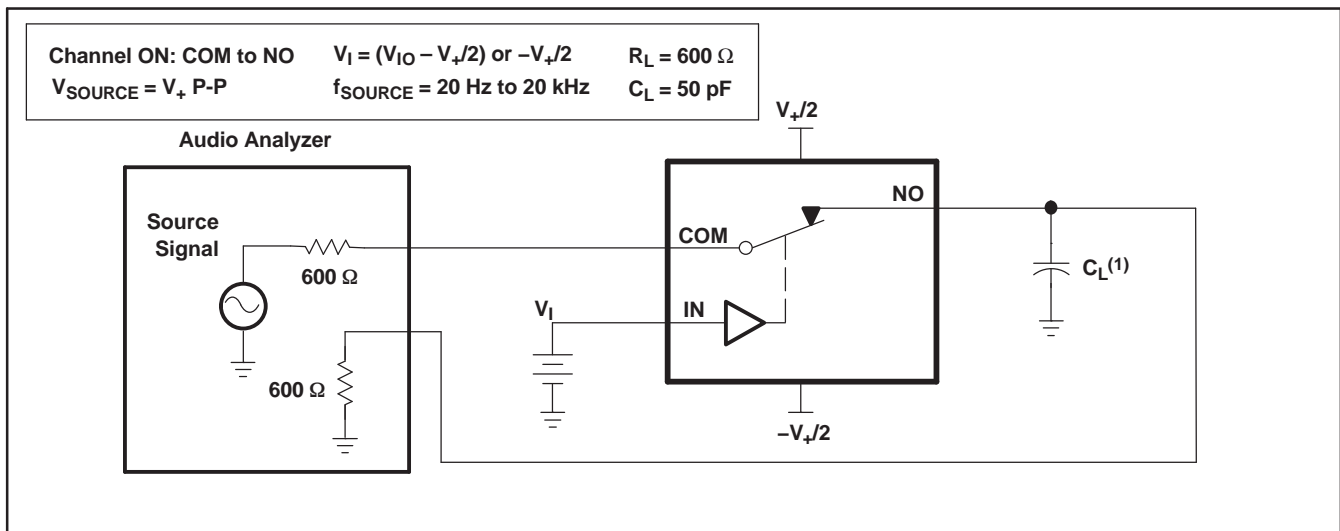


## PARAMETER MEASUREMENT INFORMATION (continued)



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .

Figure 23. Charge Injection ( $Q_C$ )



NOTES: A.  $C_L$  includes probe and jig capacitance.

Figure 24. Total Harmonic Distortion (THD)

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TS5A26542YZTR	ACTIVE	DSBGA	YZT	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(JN2 ~ JN7 ~ JNN)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

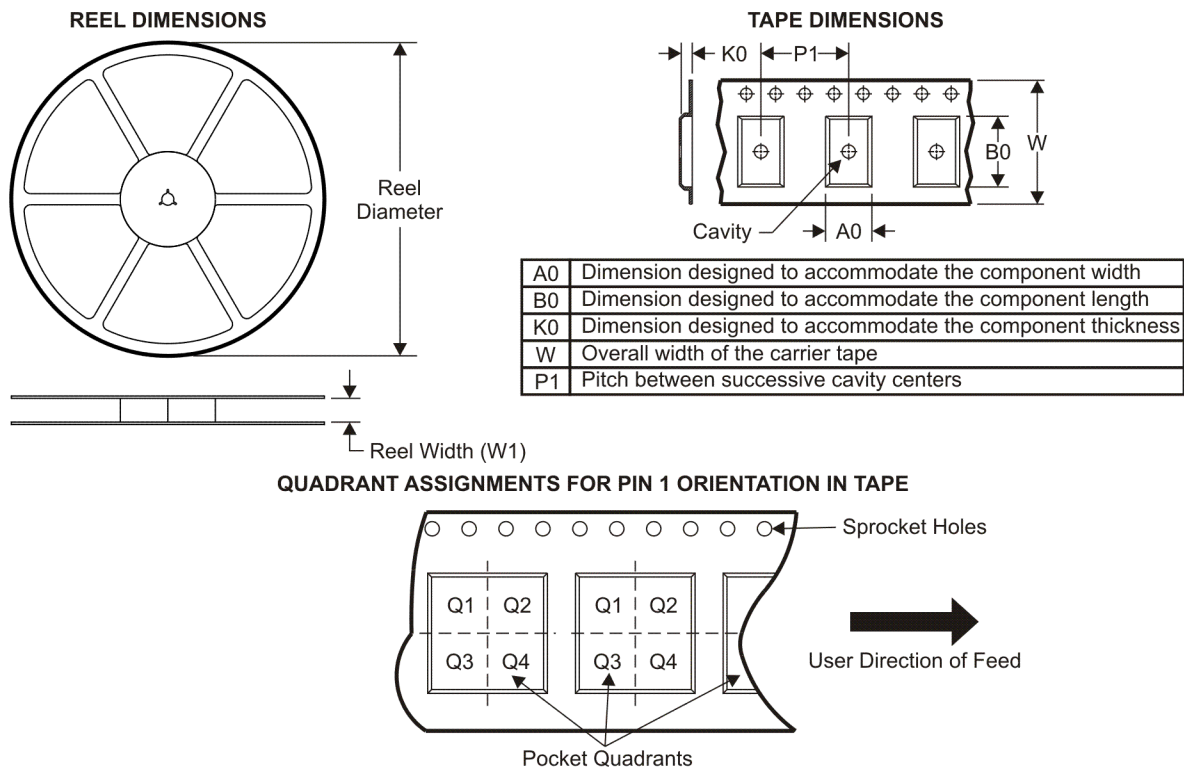
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A26542YZTR	DSBGA	YZT	12	3000	178.0	9.2	1.49	1.99	0.75	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS

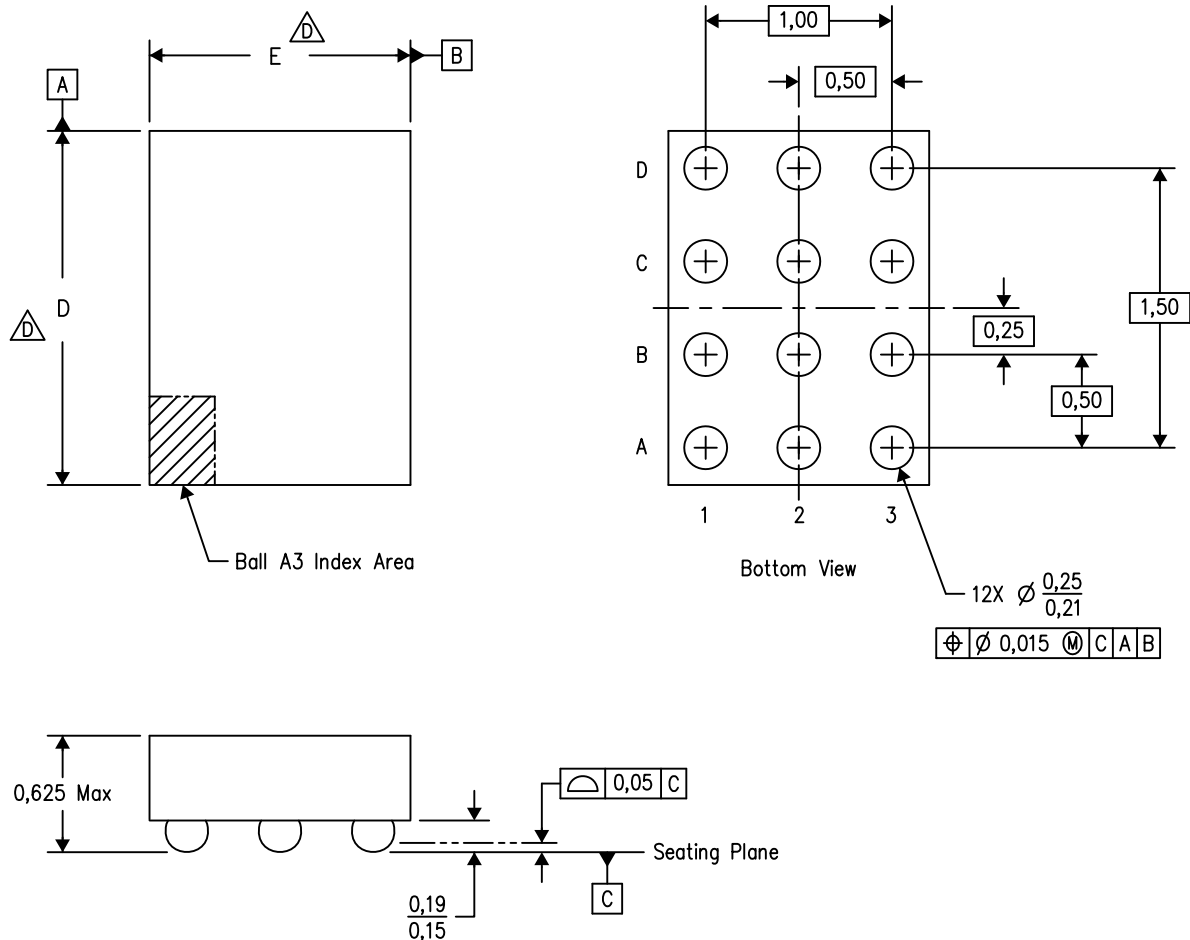


\*All dimensions are nominal


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A26542YZTR	DSBGA	YZT	12	3000	220.0	220.0	35.0

YZT (R-XBGA-N12)

(CUSTOM) DIE-SIZE BALL GRID ARRAY



4205418-6/G 04/13

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  -  D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
  - E. Reference Product Data Sheet for array population.  
3 x 4 matrix pattern is shown for illustration only.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)

# AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit [www.ameya360.com](http://www.ameya360.com)

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd  
Minhang District, Shanghai , China

➤ Sales :

Direct    +86 (21) 6401-6692  
Email     amall@ameya360.com  
QQ        800077892  
Skype     ameyasales1 ameyasales2

➤ Customer Service :

Email     service@ameya360.com

➤ Partnership :

Tel        +86 (21) 64016692-8333  
Email     mkt@ameya360.com