POSITIVE HIGH-VOLTAGE POWER-LIMITING HOTSWAP CONTROLLER

Check for Samples: TPS2490, TPS2491

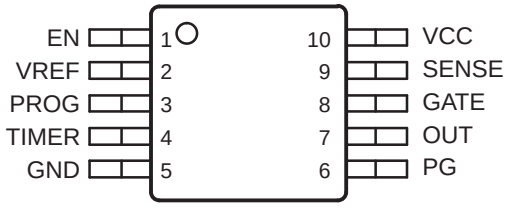
FEATURES

- **Programmable Power Limiting and Current Limiting for Complete SOA Protection**
- **Wide Operating Range: +9 V to +80 V**
- **Latched Operation (TPS2490) and Automatic Retry (TPS2491)**
- **High-side Drive for Low-$R_{DS(on)}$ External N-channel MOSFET**
- **Programmable Fault Timer to Protect the MOSFET and Eliminate Nuisance Shutdowns**
- **Power Good Open-Drain Output for Downstream DC/DC Coordination**
- **Enable can be used as a Programmable Undervoltage Lockout or Logic Control**
- **Small, Space-saving 10-pin MSOP Package**
- **Calculator Tool Available (SLVC033)**

APPLICATIONS

- **Server Backplanes**
- **Storage Area Networks (SAN)**
- **Medical Systems**
- **Plug-in Modules**
- **Base Stations**

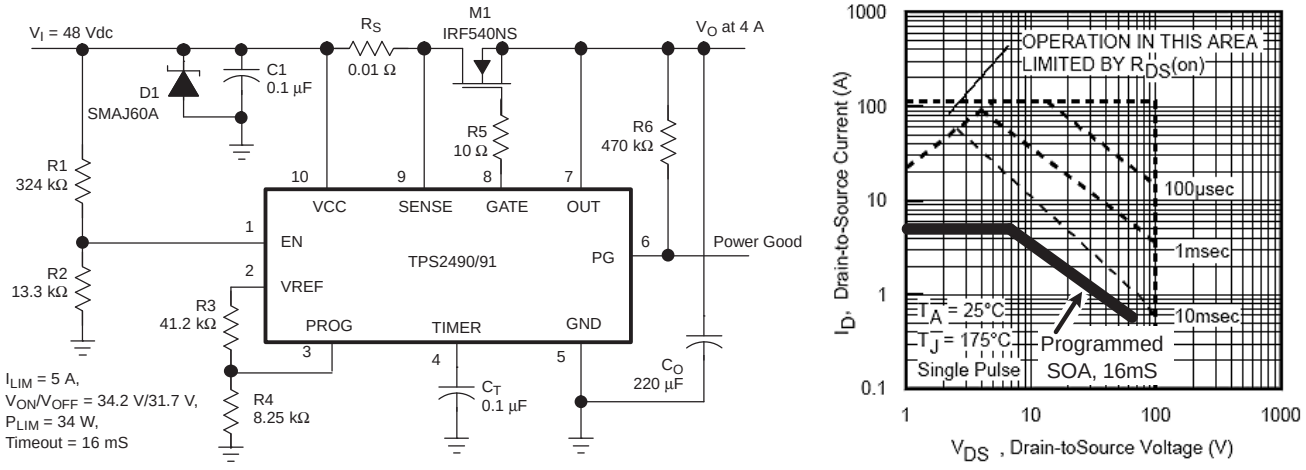
DGS Package
(Top View)



DESCRIPTION

The TPS2490 and TPS2491 are easy-to-use, positive high voltage, 10-pin Hot Swap Power Manager™ devices that safely drive an external N-channel MOSFET switch. The power limit and current limit (both are adjustable and independent of each other) ensure that the external MOSFET operates inside a selected safe operating area (SOA) under the harshest operating conditions. Applications include inrush current limiting, electronic circuit breaker protection, controlled load turn-on, interfacing to down-stream dc-to-dc converters, and power feed protection. These devices are available in a small, space-saving 10-pin MSOP package and significantly reduce the number of external devices, saving precious board space. The TPS2490/91 is supported by application notes, an evaluation module, and a design tool.

Figure 1. Typical Application and Corresponding SOA



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

TA	FUNCTION	PACKAGE	PART NUMBER(1)	SYMBOL
-40°C to 85°C	Latched	VSSOP-10 (MSOP)	TPS2490DGS	BIY
	Retry		TPS2491DGS	BIX

(1) Add an R suffix to the device type for tape and reel packaging.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		UNIT
Input voltage range, VCC, SENSE, EN	–0.3 to 100	V
Input voltage range, OUT(2)	–1 to 100	V
Output voltage range, GATE, PG	–0.3 to 100	V
Input voltage range, PROG	–0.3 to 6	V
Output voltage range, TIMER, VREF	–0.3 to 6	V
Sink current, PG	10	mA
Source current, VREF	0 to 2	mA
Sink Current, PROG	2	mA
ESD - human body model	2	kV
ESD - charged device model	500	V
Maximum junction temperature, T_J	150	°C
Storage temperature, T_{ST}	–65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) OUT will withstand transients to –2 V for 1 ms or less.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{VCC}	Input voltage range	9		80	V
V_{PROG}	Input voltage range	0.4(1)		4	V
V_{OUT}	Operating voltage range	0		80	V
I_{VREF}	Operating current range (sourcing), V_{REF}	0		1	mA
T_J	Operating junction temperature	–40		125	°C
T_A	Operating free-air temperature	–40		85	°C

(1) V_{PROG} may be set below this minimum with reduced accuracy.

DISSIPATION RATING TABLE

PACKAGE	T_A <25°C POWER RATING mW	DERATING FACTOR ABOVE T_A= 25°C (mW/°C)	T_A = 70°C POWER RATING (mW)	T_A = 85°C POWER RATING (mW)
VSSOP-10 (MSOP)	376	3.76	207	150

ELECTRICAL CHARACTERISTICS

unless otherwise noted, minimum and maximum limits apply across the recommended operating junction temperature and voltage range, V_{TIMER} = 0 V, and all outputs unloaded; typical specifications are at T_J = 25°C, V_{VCC} = 48 V, V_{TIMER} = 0 V, and all outputs unloaded; positive currents are into pins.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT (VCC)						
	Enabled	V_{EN} = Hi, V_{SENSE} = V_{OUT} = V_{VCC}		450	1000	µA
	Disabled	V_{EN} = Lo, V_{SENSE} = V_{VCC} = V_{OUT}		90	250	µA
CURRENT SENSE INPUT (SENSE)						
I_{SENSE}	Input bias current	V_{SENSE} = V_{VCC}, V_{OUT} = V_{VCC}		7.5	20	µA
REFERENCE VOLTAGE OUTPUT (VREF)						
V_{REF}	Reference voltage	0 < I_{VREF} < 1 mA	3.9	4	4.1	V
POWER LIMITING INPUT (PROG)						
I_{PROG}	Input bias current, device enabled, sourcing or sinking	0 < V_{PROG} < 4 V, V_{EN} = 48 V			5	µA
R_{PROG}	Pulldown resistance, device disabled	I_{PROG} = 200 µA, V_{EN} = 0 V		375	600	Ω
POWER LIMITING AND CURRENT LIMITING (SENSE)						
V_{CL}	Current sense threshold $V_{(VCC-SENSE)}$ with power limiting trip	V_{PROG} = 2.4 V, V_{OUT} = 0 V or V_{PROG} = 0.9 V, V_{OUT} = 30 V, V_{VCC} = 48 V	17	25	33	mV
V_{SENSE}	Current sense threshold $V_{(VCC-SENSE)}$ without power limiting trip	V_{PROG} = 4 V, V_{SENSE} = V_{OUT}	45	50	55	mV
t_{F_TRIP}	Large overload response time to GATE low	V_{PROG} = 4 V, V_{OUT} = V_{SENSE}, $V_{(VCC-SENSE)}$: 0 → 200 mV, $C_{(GATE-OUT)}$ = 2 nF, $V_{(GATE-OUT)}$ = 1 V			1.2	µs
TIMER OPERATION (TIMER)						
	Charge current (sourcing)	V_{TIMER} = 0 V	15.0	25.0	34.0	µA
		V_{TIMER} = 0 V, T_J = 25°C	20.0	25.0	30.0	µA
	Discharge current (sinking)	V_{TIMER} = 5 V	1.50	2.5	3.70	µA
		V_{TIMER} = 5 V, T_J = 25°C	2.10	2.5	3.10	µA
	TIMER upper threshold voltage		3.9	4	4.1	V
	TIMER lower reset threshold voltage	TPS2491 only	0.96	1.0	1.04	V
D_{RETRY}	Fault retry duty cycle	TPS2491 only	0.5%	0.75%	1.0%	
GATE DRIVE OUTPUT (GATE)						
I_{GATE}	GATE sourcing current	V_{SENSE} = V_{VCC}, $V_{(GATE-OUT)}$ = 7 V, V_{EN} = Hi	15	22	35	µA
	GATE sinking current	V_{EN} = Lo, V_{GATE} = V_{VCC}	1.8	2.4	2.8	mA
		V_{EN} = Hi, V_{GATE} = V_{VCC}, $V_{(VCC-SENSE)}$ ≥ 200 mV	75	125	250	mA
	GATE output voltage, $V_{(GATE-OUT)}$		12		16	V
t_{D_ON}	Propagation delay: EN going true to GATE output high	V_{EN} = 0 → 2.5 V, 50% of V_{EN} to 50% of V_{GATE}, V_{OUT} = V_{VCC}, $R_{(GATE-OUT)}$= 1 MΩ		25	40	µs
t_{D_OFF}	Propagation delay: EN going false (0 V) to GATE output low	V_{EN} = 2.5 V → 0, 50% of V_{EN} to 50% of V_{GATE}, V_{OUT} = V_{VCC}, $R_{(GATE-OUT)}$= 1 MΩ, t_{FALL} < 0.1 µs		0.5	1	µs
	Propagation delay: TIMER expires to GATE output low	V_{TIMER}: 0 → 5 V, t_{RISE} < 0.1 µs, 50% of V_{TIMER} to 50% of V_{GATE}, V_{OUT} = V_{VCC}, $R_{(GATE-OUT)}$ = 1 MΩ,		0.8	1	µs

ELECTRICAL CHARACTERISTICS (continued)

unless otherwise noted, minimum and maximum limits apply across the recommended operating junction temperature and voltage range, V_{TIMER} = 0 V, and all outputs unloaded; typical specifications are at T_J = 25°C, V_{VCC} = 48 V, V_{TIMER} = 0 V, and all outputs unloaded; positive currents are into pins.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD OUTPUT (PG)						
V_{PG_L}	Low voltage (sinking)	I_{PG} = 2 mA		0.1	0.25	V
		I_{PG} = 4 mA		0.25	0.5	V
V_{PGTL}	PG threshold voltage, V_{OUT} rising, PG goes open drain	V_{SENSE} = V_{VCC}, measure $V_{(VCC-OUT)}$	0.8	1.25	1.7	V
VPGTH	PG threshold voltage, V_{OUT} falling, PG goes low	V_{SENSE} = V_{VCC}, measure $V_{(VCC-OUT)}$	2.2	2.7	3.2	V
ΔV_{PGT}	PG threshold hysteresis voltage, $V_{(SENSE-OUT)}$	V_{SENSE} = V_{VCC}		1.4		V
t_{DPG}	PG deglitch delay, detection to output, rising and falling edges	V_{SENSE} = V_{VCC}	5	9	15	ms
	Leakage current, PG false, open drain				10	µA
OUTPUT VOLTAGE FEEDBACK INPUT (OUT)						
I_{OUT}	Bias current	V_{OUT} = V_{VCC}, V_{EN} = Hi, sinking		8	20	µA
		V_{OUT} = GND, V_{EN} = Lo, sourcing		18	40	µA
ENABLE INPUT (EN)						
V_{EN_H}	Threshold, V_{EN} going high		1.32	1.35	1.38	V
V_{EN_L}	Threshold, V_{EN} going low		1.22	1.25	1.28	V
	V_{EN} hysteresis			100		mV
	Leakage current	V_{EN} = 48 V			1	µA
INPUT SUPPLY UVLO (VCC)						
	V_{VCC} turn on	Rising		8.4	8.8	V
	V_{VCC} turn off	Falling	7.5	8.3		V
	Hysteresis			75		mV

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

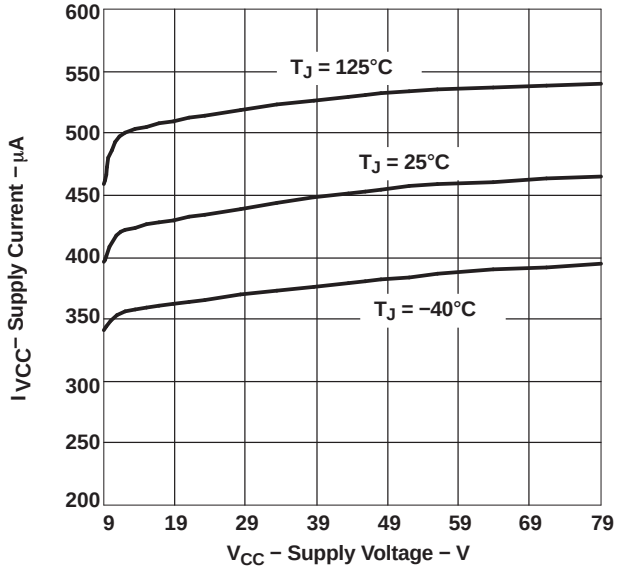


Figure 2.

CURRENT LIMIT TRIP vs SUPPLY VOLTAGE

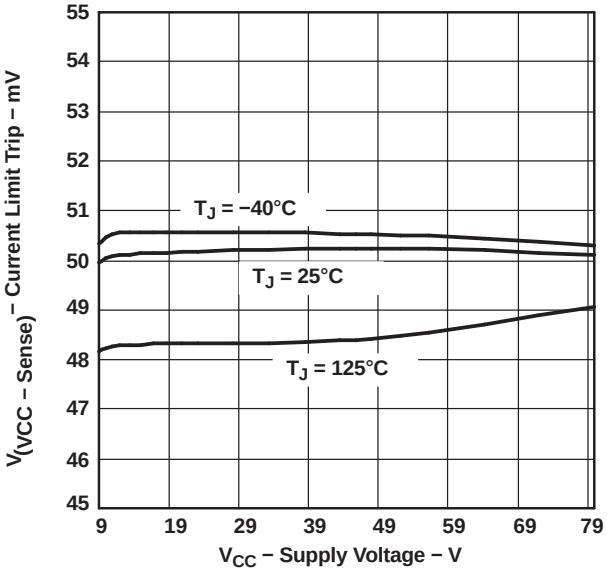


Figure 3.

GATE PULLUP CURRENT vs SUPPLY VOLTAGE

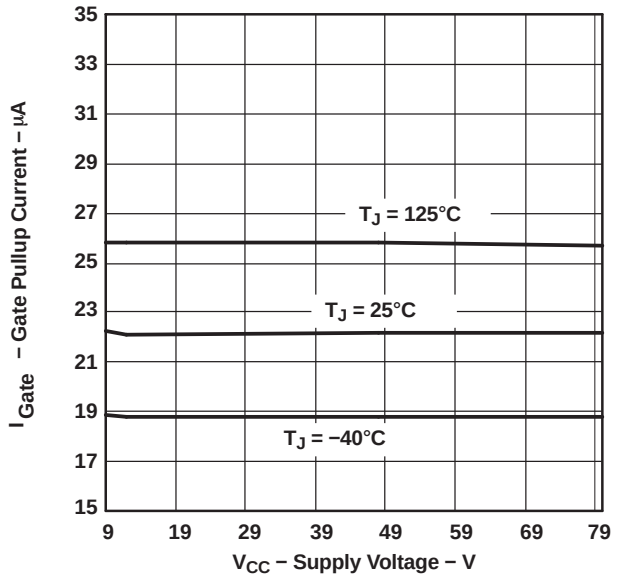


Figure 4.

GATE PULLDOWN CURRENT(EN = 0 V) vs SUPPLY VOLTAGE

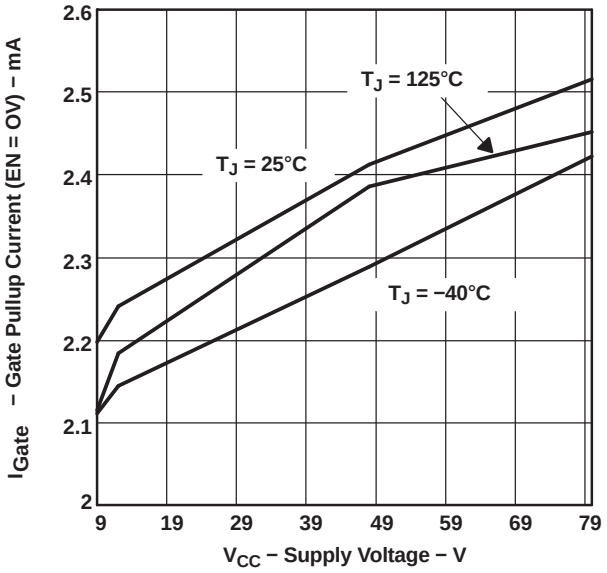


Figure 5.

TYPICAL CHARACTERISTICS (continued)

GATE PULLDOWN CURRENT vs SUPPLY VOLTAGE (EN = 4 V, V(vcc – sense) = 200 mV)

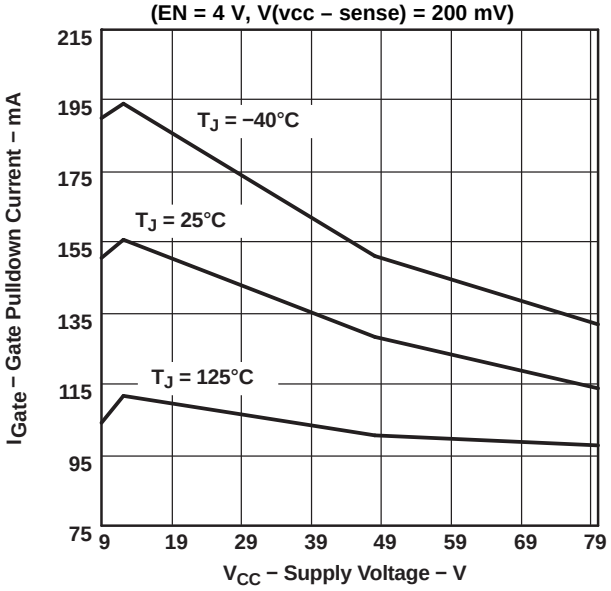


Figure 6.

CURRENT LIMIT RESPONSE TIME vs SUPPLY VOLTAGE (EN = 4 V, V(vcc – sense) = 200 mV)

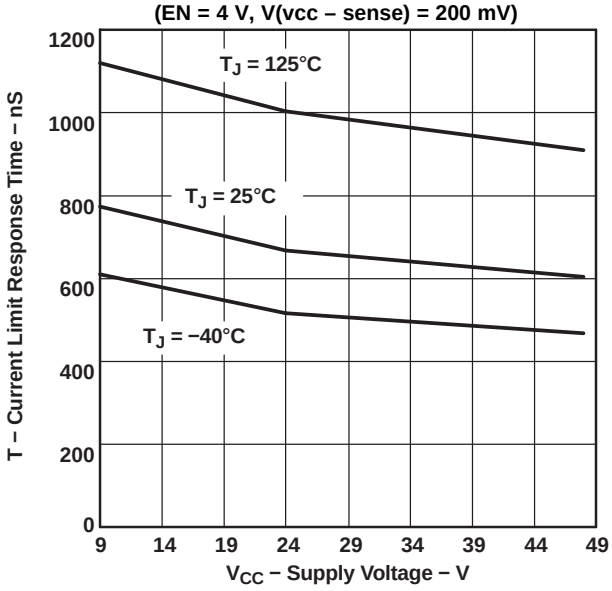


Figure 7.

GATE OUTPUT VOLTAGE vs SUPPLY VOLTAGE

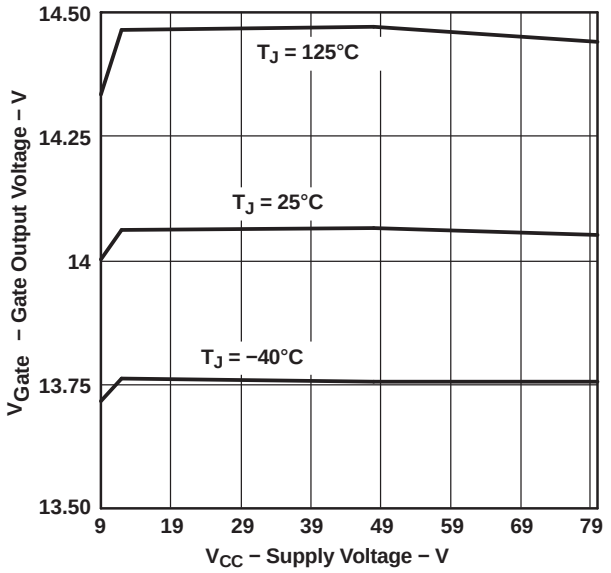


Figure 8.

TIMER PULLUP CURRENT vs SUPPLY VOLTAGE

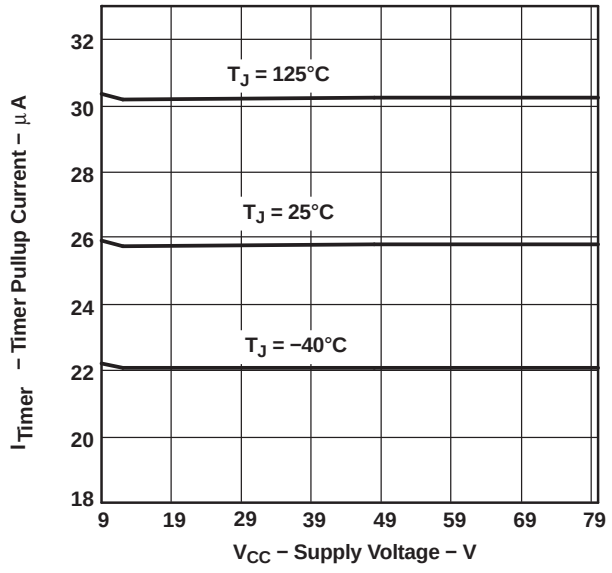


Figure 9.

TYPICAL CHARACTERISTICS (continued)

TIMER CHARGE/DISCHARGE RATIO
vs
SUPPLY VOLTAGE AND TEMPERATURE

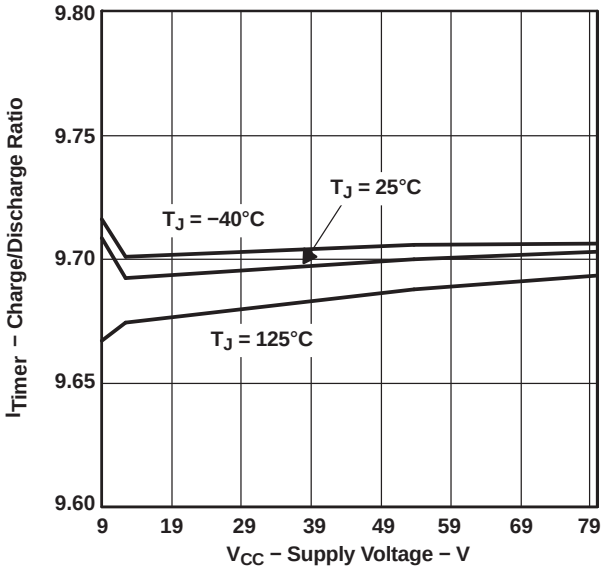


Figure 10.

EN THRESHOLD VOLTAGE (FALLING)
vs
SUPPLY VOLTAGE

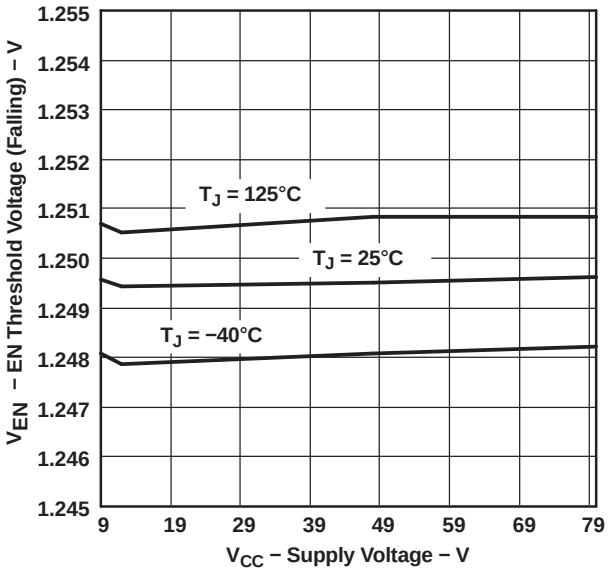


Figure 11.

EN THRESHOLD VOLTAGE (RISING)
vs
SUPPLY VOLTAGE

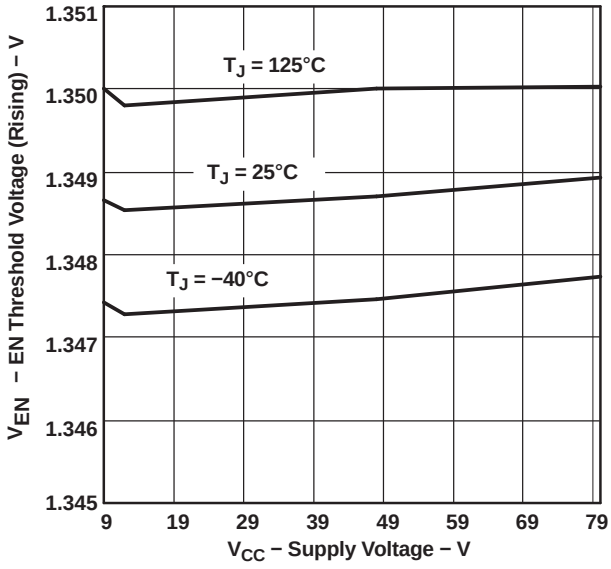
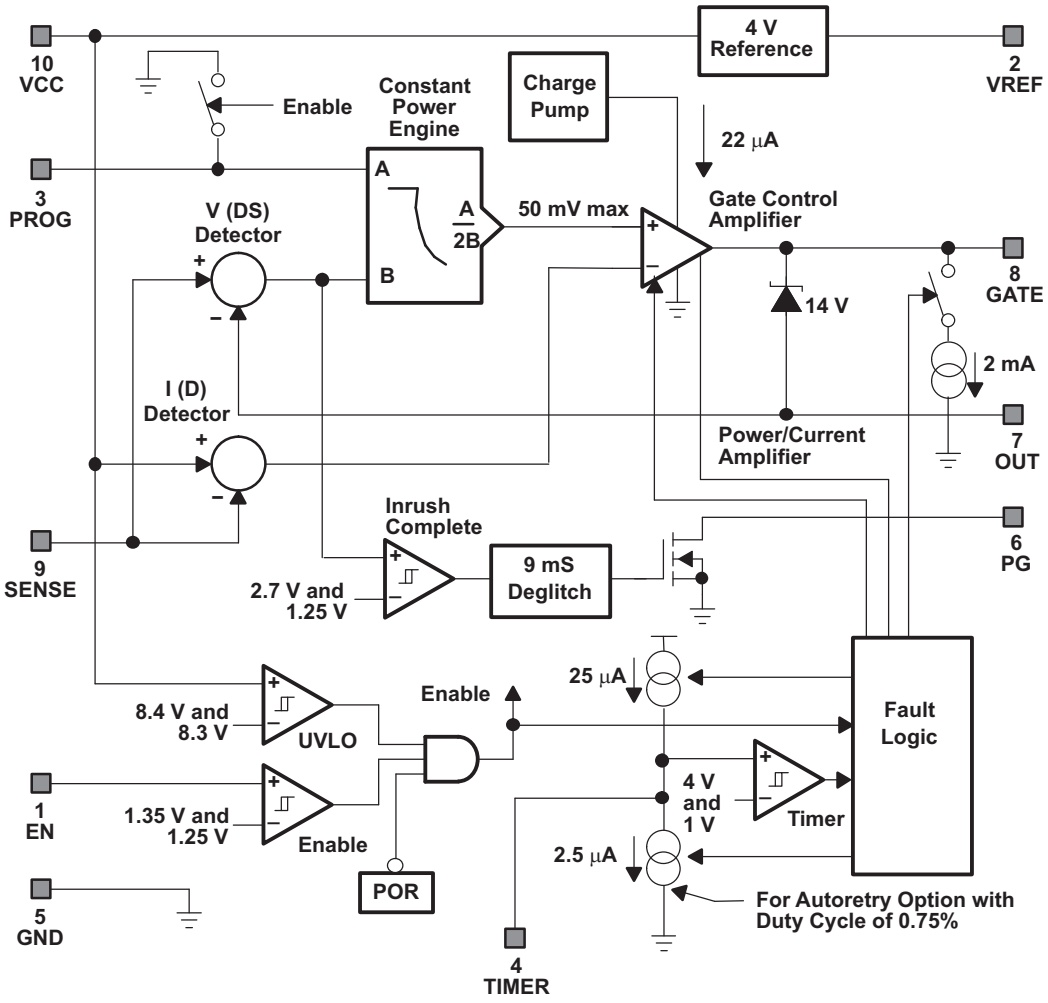


Figure 12.

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Device enable
VREF	2	O	Reference voltage output, used to set power threshold on PROG pin
PROG	3	I	Power-limit setting input
TIMER	4	I/O	Fault timing capacitor
GND	5		Ground
PG	6	O	Power good reporting output, open-drain
OUT	7	I	Output voltage feedback
GATE	8	O	Gate output
SENSE	9	I	Current-limit sense input
VCC	10	I	Supply input

DETAILED PIN DESCRIPTION

The following description relies on the *Typical Application and Corresponding SOA* circuit, and the functional block diagram.

VCC: This pin is associated with three functions: 1) biasing power to the integrated circuit, 2) input to power on reset (POR) and under voltage lockout (UVLO) functions, and 3) voltage sense at one terminal of R_S for M1 current measurement. The voltage must exceed the POR (about 6 V for approximately 400 µs) and the internal UVLO (about 8 V) before normal operation (driving the GATE) may begin. Connections to VCC should be designed to minimize R_S voltage sensing errors and to maximize the effect of C1 and D1; place C1 at R_S rather than at the IC pin to eliminate transient sensing errors. GATE, PROG, PG, and TIMER are held low when either UVLO or POR are active.

SENSE: Monitors the voltage at the drain of M1, and the downstream side of R_S providing the constant power limit engine with feedback of both M1 current (I_D) and voltage (V_{DS}). Voltage is determined by the difference between SENSE and OUT, while the current analog is the difference between VCC and SENSE. The constant power engine uses V_{DS} to compute the allowed I_D and is clamped to 50 mV, acting like a traditional current limit at low V_{DS}. The current limit is set by the following equation:

$$I_{LIM} = \frac{50\ mV}{R_S} \quad (1)$$

Design the connections to SENSE to minimize R_S voltage sensing errors. Don't drive SENSE to a large voltage difference from VCC because it is internally clamped to VCC. The current limit function can be disabled by connecting SENSE to VCC.

GATE: Provides the high side (above VCC) gate drive for M1. It is controlled by the internal gate drive amplifier, which provides a pull-up of 22 µA from an internal charge pump and a strong pull-down to ground of 75 mA (min). The pull-down current is a non-linear function of the amplifier overdrive; it provides small drive for small overloads, but large overdrive for fast reaction to an output short. There is a separate pull-down of 2 mA to shut M1 off when EN or UVLO cause this to happen. An internal clamp protects the gate of M1 (to OUT) and generally eliminates the need for an external clamp in almost all cases for devices with 20 V $V_{GS(MAX)}$ ratings; an external Zener may be required to protect the gate of devices with $V_{GS(MAX)}$ < 16 V. A small series resistance (R5) of 10 Ω should be inserted in the gate lead if the C_{ISS} of M1 > 200 pF, otherwise use 33 Ω for small MOSFETs.

A capacitor can be connected from GATE to ground to create a slower inrush with a constant current profile without affecting the amplifier stability. Add a series resistor of about 1 kΩ to the gate capacitor to maintain the gate clamping and current limit response time. Adding capacitance across M1 gate to source requires some series damping resistance to avoid high-frequency oscillations.

OUT: This input pin is used by the constant power engine and the PG comparator to measure V_{DS} of M1 as $V_{(SENSE-OUT)}$. Internal protection circuits leak a small current from this pin when it is low. If the load circuit can drive OUT below ground, connect a clamp (or freewheel) diode such as an S1B from OUT (cathode) to GND (anode).

EN: The GATE driver is enabled if the positive threshold is exceeded and the internal POR and UVLO thresholds have been satisfied. EN can be used as a logic control input, an analog input voltage monitor as illustrated by R1/R2 in the *Typical Application and Corresponding SOA* circuit, or it can be tied to VCC to always enable the TPS2490/91. The hysteresis associated with the internal comparator makes this a stable method of detecting a low input condition and shutting the downstream circuits off. A TPS2490 that has latched off can be reset by cycling EN below its negative threshold and back high.

VREF: Provides a 4.0-V reference voltage for use in conjunction with R3/R4 of the typical application circuit to set the voltage on the PROG pin. The reference voltage is available once the internal POR and UVLO thresholds have been met. It is not designed as a supply voltage for other circuitry, therefore ensure that no more than 1 mA is drawn. Bypass capacitance is not required, but if a special application requires one, less than 1000 pF can be placed on this pin.

PROG: The voltage applied to this pin (0.4 – 4 V) programs the power limit used by the constant power engine. Normally, a resistor divider R3/R4 is connected from VREF to PROG to set the power limit according to the following equation:

$$V_{PROG} = \frac{P_{LIM}}{10 \times I_{LIM}} \quad (2)$$

where P_{LIM} is the desired power limit of M1 and I_{LIM} is the current limit setpoint (see SENSE). P_{LIM} is determined by the desired thermal stress on M1:

$$P_{LIM} < \frac{T_{J(MAX)} - T_{S(MAX)}}{R_{\theta JC(MAX)}} \quad (3)$$

where $T_{J(MAX)}$ is the maximum desired transient junction temperature of M1 and $T_{S(MAX)}$ is the maximum case temperature prior to a start or restart.

V_{PROG} is used in conjunction with V_{DS} to compute the (scaled) current, $I_{D\_ALLOWED}$, by the constant power engine. $I_{D\_ALLOWED}$ is compared by the gate amplifier to the actual I_D, and used to generate a gate drive. If $I_D < I_{D\_ALLOWED}$, the amplifier turns the gate of M1 fully on because there is no overload condition; otherwise GATE is regulated to maintain the $I_D = I_{D\_ALLOWED}$ relationship.

A capacitor may be tied from PROG to ground to alter the natural constant power inrush current shape. If properly designed, the effect is to cause the leading step of current in Figure 13 to look like a ramp.

PROG is internally pulled to ground whenever EN, POR, or UVLO are not satisfied or the TPS2490 is latched off. This feature serves to discharge any capacitance connected to the pin. Do not apply voltages greater than 4 V to PROG. If the constant power limit is not used, PROG should be tied to VREF through a 47-kΩ resistor.

TIMER: An integrating capacitor, C_T, connected to the TIMER pin provides a timing function that controls the fault-time for both versions and the restart interval for the TPS2491. The timer charges at 25 µA whenever the TPS2490/91 is in power limit or current limit and discharges at 2.5 µA otherwise. The charge-to-discharge current ratio is constant with temperature even though there is a positive temperature coefficient to both. If TIMER reaches 4 V, the TPS2490 pulls GATE to ground, latch off, and discharge C_T. The TPS2491 pulls GATE to ground and attempt a restart (re-enable GATE) after a timing sequence consisting of discharging C_T down to 1 V followed by 15 more charge and discharge cycles. The TPS2490 can be reset by either cycling the EN pin or the UVLO (e.g. power cycling). TIMER discharges when EN is low or UVLO or POR are active. The TIMER pin should be tied to ground if this feature is not used.

PG: This open-drain output is intended to interface to downstream dc/dc converters or monitoring circuits. PG goes open-drain (high voltage with a pull-up) after V_{DS} of M1 has fallen to about 1.25 V and a 9 ms deglitch time period has elapsed. PG is false (low or low resistance to ground) whenever V_{DS} of M1 has not been less than 1.25 V, V_{DS} of M1 is above 2.7 V, or UVLO is active. Both V_{DS} rising and falling are deglitched while entering UVLO sets PG low immediately. PG can also be viewed as having an input and output voltage monitor function. The 9-ms deglitch circuit operates to filter short events that could cause PG to go inactive (low) such as a momentary overload or input voltage step. V_{PG} voltage can be greater than V_{VCC} because it's ESD protection is only with respect to ground.

GND: This pin is connected to system ground.

APPLICATION INFORMATION

BASIC OPERATION

The TPS2490/91 provides all the features needed for a positive hotswap controller. These features include: 1) under-voltage lockout; 2) adjustable (system-level) enable; 3) turn-on inrush limit; 4) high-side gate drive for an external N-channel MOSFET; 5) MOSFET protection (power limit and current limit); 6) adjustable overload timeout—also called an electronic circuit breaker; 7) charge-complete indicator for downstream converter coordination; and 8) an optional automatic restart mode. The TPS2490/91 features superior power-limiting MOSFET protection that allows independent control of current limit (to set maximum full-load current), power limit (to control junction temperature rise), and overload time (to control case temperature rise).

The typical application circuit, and oscilloscope plots of Figure 13 through Figure 17 demonstrate many of the functions described above.

Board Plug-In (Figure 13)

Only the bypass capacitor charge current and small bias currents are evident when a board is first plugged in. The TPS2490/91 is held inactive, and GATE, PROG, TIMER, and PG are held low for less than 1 ms while internal voltages stabilize. A startup cycle is ready to take place after the stabilization.

GATE, PROG, TIMER, and PG are released after stabilization in this example because both the internal UVLO threshold and the external EN (enable) thresholds have been exceeded. The part begins sourcing current from the GATE pin and M1 begins to turn on while the voltage across it, $V_{(SENSE–OUT)}$, and current through it, $V_{(VCC–SENSE)}$, are monitored. Current initially rises to the value which satisfies the power limit engine ($P_{LIM} \div V_{VCC}$) since the output capacitor was discharged.

TIMER and PG Operation (Figure 13)

The TIMER pin charges C_T as long as limiting action continues, and discharges at a 1/10 charge rate when limiting stops. If the voltage on C_T reaches 4 V before the output is charged, M1 is turned off and either a latch-off or restart cycle commences, depending on the part type. The open-drain PG output provides a deglitched end-of-charge indication which is based on the voltage across M1. PG is useful for preventing a downstream dc/dc converter from starting while C_O is still charging. PG goes active (open drain) about 9 ms after C_O is charged. This delay allows M1 to fully turn on and any transients in the power circuits to end before the converter starts up. The resistor pull-up shown on pin PG in the typical application diagram only demonstrates operation; the actual connection to the converter depends on the application. Timing can appear to terminate early in some designs if operation transitions out of the power limit mode into a gate charge limited mode at low V_{DS} values.

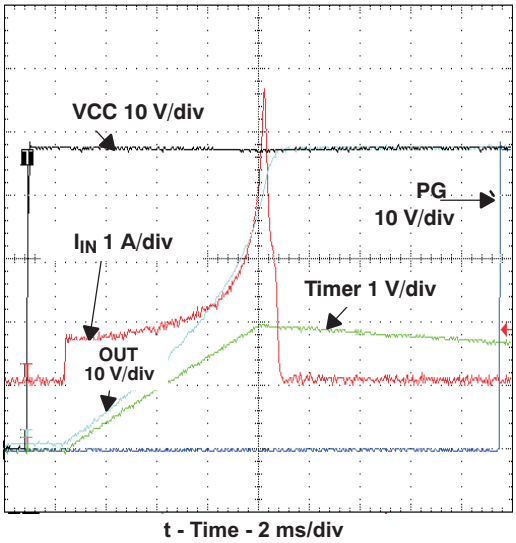


Figure 13. Basic Board Insertion

Action of the Constant Power Engine (Figure 14)

The calculated power dissipated in M1, $V_{DS} \times I_D$, is computed under the same startup conditions as Figure 13 . The current of M1, labeled I_{IN}, initially rises to the value that satisfies the constant power engine; in this case it is 34 W ÷ 48 V = 0.7 A. The 34 W value is programmed into the engine by setting the PROG voltage using the equation given in the PROG pin description. V_{DS} of M1, which is calculated as $V_{(SENSE–OUT)}$, falls as C_O charges, thus allowing the M1 drain current to increase . This is the result of the internal constant power engine adjusting the current limit reference to the GATE amplifier as C_O charges and V_{DS} falls. The calculated device power in Figure 14, labeled FET PWR, is seen to be flat-topped and constant within the limitations of circuit tolerance and acquisition noise. A fixed current limit is implemented by clamping the constant power engine's output to 50 mV when V_{DS} is low. This protection technique can be viewed as a specialized form of foldback limiting; the benefit over linear foldback is that it yields the maximum output current from a device over the full range of V_{DS} and still protects the device.

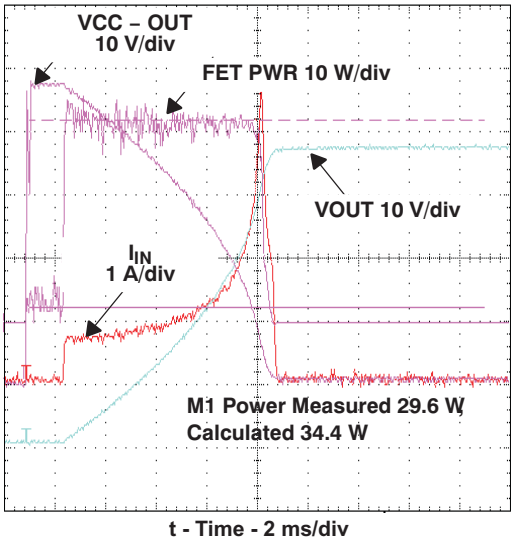


Figure 14. Computation of M1 Stress During Startup

Response to a Hard Output Short (Figure 15 and Figure 16)

Figure 15 shows the short circuit response over the full time-out period. The period begins when the output voltage falls and ends when M1 is turned off. M1 current is actively controlled by the constant power engine and gate amplifier circuit while the TIMER pin charges C_T to the 4 V threshold causing M1 to be turned off. The TPS2490 latches off after the threshold is reached until either the input voltage drops below the UVLO threshold or EN cycles through the false (low) state. The TPS2491 goes through a timing sequence before attempting a restart.

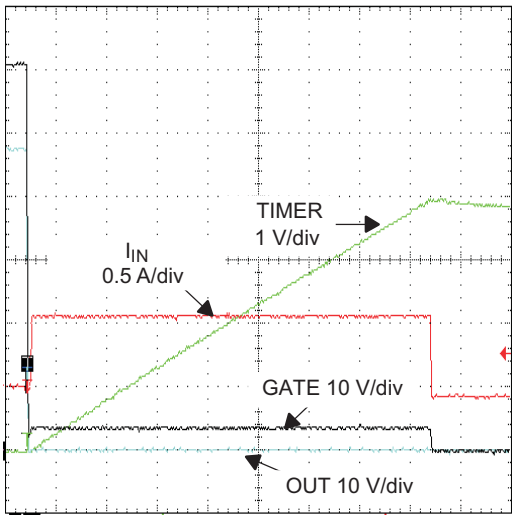


Figure 15. Current Limit Overview

The TPS2490/91 responds rapidly to the short circuit as seen in Figure 16. The falling OUT voltage is the result of M1 and C_O currents through the short's impedance at this time scale. The internal GATE clamp causes the GATE voltage to follow the output voltage down and subsequently limits the negative V_{DS} to 1–2 V. The rapidly rising fault current overdrives the GATE amplifier causing it to overshoot and rapidly turn M1 off by sinking current to ground. M1 slowly turns back on as the GATE amplifier recovers; M1 then settles to an equilibrium operating point determined by the power limiting circuit.

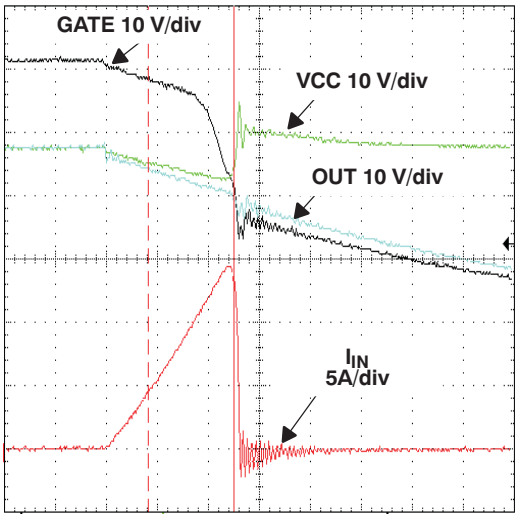


Figure 16. Current Limit Onset

Minimal input voltage overshoot appears in Figure 16 because a local 100-µF bypass capacitor and very short input leads were used. The input voltage would overshoot as the input current abruptly drops in a typical application due to the stored energy in the input distribution's inductance. The exact waveforms seen in an application depend upon many factors including parasitics of the voltage distribution, circuit layout, and the short itself.

Automatic Restart (Figure 17)

The TPS2491 automatically initiates a restart after a fault has caused it to turn off M1. Internal control circuits use C_T to count 16 cycles before re-enabling M1. This sequence repeats if the fault persists. The TIMER has a 1:10 charge-to-discharge current ratio, and uses a 1-V lower threshold. The fault-retry duty cycle specification quantifies this behavior. This small duty cycle often reduces the average short-circuit power dissipation to levels associated with normal operation and eliminates special thermal considerations for surviving a prolonged output short.

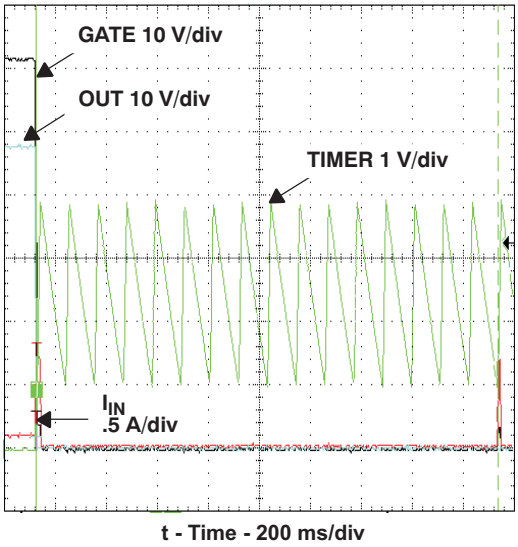


Figure 17. TPS2491 Restart Cycle Timing

DESIGN PROCEDURE

This design procedure seeks to control the junction temperature of M1 under both static and transient conditions by selecting the device's package, cooling, $R_{DS(on)}$, current limit, fault timeout, and power limit. The following procedure assumes that a unit running at full load and maximum ambient temperature experiences a brief input power interruption sufficient to discharge C_O, but short enough to keep M1 from cooling. A full C_O recharge then takes place. Adjust this procedure to fit your application and design criteria. See SLVC033 for a calculation tool to help with this process.

This procedure assumes that C_O is the only load during inrush. Only simple first-order thermal models, natural convection and a large PCB pad for M1 are assumed. The assumptions build generous safety margins into the design to allow for the inherent inaccuracies of the models and variations of real-world conditions.

Other tools and applications information are available on the TI website that supplement the following procedure.

STEP 1. Choose R_S

Given the maximum operating current, I_{MAX}, compute the current sense resistance, R_S.

$$R_S = \frac{0.05}{1.2 \times I_{MAX}} \quad (4)$$

This equation allows for minimum current limit, a sense resistor tolerance of 5%, and 5% margin. Round the result down to the nearest available standard value.

STEP 2. Choose M1

First select a V_{DS} rating that allows for the maximum input voltage and transients. Next select an operating $R_{DS(on)}$, package, and cooling to control operating temperature. The following equation computes the value of $R_{DS(on)(MAX)}$at a junction temperature of $T_{J(MAX)}$. Most manufacturers list $R_{DS(on)(MAX)}$ at 25°C and provide a derating curve from which values at other temperatures can be derived. Compute the maximum allowable on-resistance, $R_{DS(on)(MAX)}$, using the equation:

$$R_{DSON(MAX)} \leq \frac{T_{J(MAX)} - T_{A(MAX)}}{R_{\theta JA} \times I^2_{MAX}} \quad (5)$$

where $T_{J(MAX)}$ is the desired maximum steady-state junction temperature (typically 125°C), and $T_{A(MAX)}$ is the maximum ambient temperature. $R_{\theta JA}$, the junction-to-ambient thermal resistance, depends upon the package style chosen and the details of heat-sinking and cooling. Note the $R_{\theta JC}$ and $R_{\theta JA}$ for use below.

STEP 3. Choose P_{LIM}, R3, R4

M1 dissipates large amounts of power during power-up or output short circuit. The power limit P_{LIM} of the TPS2940/91 should be set to prevent the die temperature from exceeding a short term maximum temperature, $T_{J(MAX)2}$. The short-term $T_{J(MAX)2}$ could be set as high as 150°C while still leaving ample margin to the usual manufacturer's rating of 175°C. An expression for calculating P_{LIM} is:

$$P_{LIM} \leq 0.7 \times \frac{T_{J(MAX)2} - \left[\left(I^2_{MAX} \times R_{DSON} \times R_{\theta CA}\right) + T_{A(MAX)}\right]}{R_{\theta JC}} \quad (6)$$

where $R_{\theta JC}$ is M1 junction-to-case thermal resistance, $R_{DS(on)}$ is the channel resistance at the maximum operating temperature, and the factor of 0.7 represents the tolerance of the constant power engine. Next calculate V_{PROG} and the divider resistors R3 and R4. R3 must be greater than 4 kΩ, but it is recommended that 10 kΩ or greater be used.

$$V_{PROG} = \frac{P_{LIM}}{10 \times I_{LIM}} \text{ where } I_{LIM} = \frac{0.05}{R_S}$$

$$\frac{R4}{R3 + R4} = \frac{V_{PROG}}{V_{REF}} \quad (7)$$

STEP 4. Choose t_{ON}, C_T

The on-time, t_{ON}, set by capacitor C_T must suffice to fully charge the load capacitance C_O without triggering the fault circuitry. Assuming that only the load capacitance draws current during startup:

$$t_{ON} = \begin{cases} \frac{C_O \times P_{LIM}}{2 \times I^2_{LIM}} + \frac{C_O \times V^2_{VCC(MAX)}}{2 \times P_{LIM}} & \text{if } P_{LIM} < I_{LIM} V_{VCC(MAX)} \\ \frac{C_O \times V_{VCC(MAX)}}{I_{LIM}} & \text{if } P_{LIM} \geq I_{LIM} V_{VCC(MAX)} \end{cases} \quad (8)$$

Using this value of t_{ON}, $C_T$is computed as:

$$C_T = 8.5 \times 10^{-6} \times t_{ON} \times \left(1 + C_{OUT\_TOL} + C_{T\_TOL}\right) \quad (9)$$

where C_{T_TOL} and C_{OUT_TOL} are the tolerances associated with each capacitor. Assuming C_O is a 20% tolerance part, C_{OUT_TOL} has a value of 0.2. This expression assures the worst case set of parts will always start.

STEP 5. Choose The Turn On Voltage, R1 and R2

Assuming that EN is used as an analog input, the turn-on voltage, V_{ON} and turn-off voltage, V_{OFF} are defined as:

$$V_{ON} = \frac{1.35\ V}{\left(\frac{R2}{R1+R2}\right)} \qquad V_{OFF} = \frac{1.25\ V}{\left(\frac{R2}{R1+R2}\right)} \quad (10)$$

Use caution in selecting large values of R1 and R2 because the leakage current causes errors in the threshold voltages.

STEP 6. Choose R5, R6, and C1

R5 is intended to suppress high-frequency oscillations; a resistor of 10Ω will serve for most applications but if M1 has a C_{ISS} below 200 pF, then use 33 Ω. Applications with larger MOSFETs and short wiring may not require R5. R6 is required only if the PG output drives a circuit that requires it. It is recommended that the sink current be less than 2 mA. C1 is a bypass capacitor to help with control of transient voltages, unit emissions, and local supply noise while in the disabled state. Where acceptable, a value in the range of 0.001 µF to 0.1 µF is recommended.

STEP 7. Choose D1

Transient voltage suppressor D1 is required in applications where there will be enough energy in the distribution inductance to cause a voltage surge above the TPS2490/91 rated maximum. Such transients can be caused by card insertions or shorts on the input or output of the TPS2490/91.

ALTERNATIVE INRUSH DESIGNS

Gate Capacitor (dV/dt) Control

The TPS2490/91 can be used with applications that require constant turn-on currents. The current is controlled by a single capacitor from the GATE terminal to ground with a series resistor. M1 appears to operate as a source follower (following the gate voltage) in this implementation. Choose a time to charge, Δt, based on the output capacitor, input voltage V_I, and desired charge current, I_{CHARGE}. Select I_{CHARGE} to be less than $P_{LIM} \div V_{VCC}$ if the power limit feature is kept. See SLVC033 for a calculation tool.

$$\Delta t = \frac{C_O \times V_{VCC}}{I_{CHARGE}} \tag{11}$$

To select the gate capacitance:

$$C_G = \left(I_{GATE} \times \frac{\Delta t}{V_{VCC}} \right) - C_{RS} \tag{12}$$

I_{GATE} is the nominal gate charge current. This equation assumes that the MOSFET C_{GD} is the controlling element as the gate and output voltage rise. C_{GD} is non-linear with applied V_{DG}. An averaged estimate may be made using the MOSFET V_{GS} vs Q_G curve. Divide the charge accumulated during the plateau region by the plateau V_{GS} to get C_{RS}.

Since neither power nor current-limit faults are invoked during turn on, C_T can be chosen for fast transient turn off response using the M1 SOA curve. Choose the single pulse time conservatively from the M1 SOA curve using maximum operating voltage and maximum trip current. A series resistor of about 1 kΩ should be used in conjunction with C_G.

PROG Inrush Control

A capacitor can be connected from the PROG pin to ground to reduce the initial current step seen in Figure 13 based on the *Typical Application and Corresponding SOA* circuit. This method maintains a relatively fast turn-on time without the drawbacks of a gate-to-ground capacitor that include increased short circuit response time and less predictable gate clamping.

ADDITIONAL DESIGN CONSIDERATIONS

Use of PG

Use the PG pin to control and coordinate a downstream dc/dc converter. A long time delay is needed to allow C_O to fully charge before the converter starts if this is not done. An undesirable latchup condition can be created between the TPS2490 output characteristic and the dc/dc converter input characteristic if the converter starts while C_O is still charging; the PG pin is one way to avoid this.

Faults and Backplane Voltage Droop

A hard short at the output of the TPS2490/91 during normal operation could result in activation of the enable or UVLO circuit instead of the current limit if the input voltage droops sufficiently. The lower GATE drive in this condition will cause a prolonged, larger over-current spike. This can be eliminated by filtering EN, or distributing capacitance on the bus itself. Capacitance from adjacent plugged-in units may help with this as well.

Output Clamp Diode

Inductive loads on the output may drive the OUT pin below GND when the circuit is unplugged or during a current limit. The OUT pin ratings can be maintained with a small diode, such as an S1B, across TPS2490/91 OUT to GND.

Gate Clamp Diode

The TPS2490/91 has a relatively well-regulated gate voltage of 12–16 V, even with low supply voltages. A small clamp Zener from gate to source of M1, such as a BZX84C7V5, is recommended if V_{GS} of M1 is rated below this.

High Gate Capacitance Applications

Gate voltage overstress and abnormally large fault current spikes can be caused by large gate capacitance. An external gate clamp Zener diode is recommended to assist the internal Zener if the total gate capacitance of M1 exceeds about 4000 pF. When gate capacitor dv/dt control is used, a 1-kΩ resistor in series with C_G is recommended. If the series R-C combination is used for MOSFETs with C_{ISS} less than 3000 pF, then a Zener is not necessary.

Input Bypass

C1 should be present for control of external noise at VCC and as a low-impedance source for high-speed circuits.

Output Short Circuit Measurements

Repeatable short-circuit testing results are difficult to obtain. The many details of source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to obtaining different results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet—every setup differs.

Layout Considerations

Good layout practice places the power devices D1, R_S, M1, and C_O so power flows in a sequential fashion, and preferably in a straight line. A ground plane under the power and the TPS2490/91 is desirable. The TPS2490/91 should be placed close to the sense resistor and the MOSFET; a Kelvin connection is recommended to achieve accurate current sensing across R_S. A low-impedance GND connection is required because the TPS2490/91 can momentarily sink upwards of 100 mA from the gate of M1. The GATE amplifier has high bandwidth while active, so keep the gate trace length short. The PROG, TIMER, and EN pins have high input impedances, therefore keep their input leads short. Oversize power traces and power device connections to assure low voltage drop and good thermal performance.

REVISION HISTORY

Note: Page numbers of current version may differ from page numbers of previous versions.

Changes from Original (November 2003) to Revision A — **Page**

- Deleted Lead temperature spec. from Abs Max Ratings table 2
- Changed V_{PROG} MIN voltage spec. from: 0 to: 0.4; added footnote (1) to the RECOMMENDED OPERATING CONDITIONS table 2
- Deleted footnote - Not tested in production from t_{F_TRIP} 3
- Added clarification sentence to the GATE pin description, regarding adding capacitance. 9
- Changed $V_{(VCC-OUT).}$ to $V_{(SENSE-OUT)}$ in the OUT pin description. 9
- Changed from: (0–4 V) to: (0.4 – 4 V) in the PROG pin description 9
- Changed from: 2.5 V to: 2.7 V in the PG pin description. 10
- Added text to the PG pin description. 10
- Changed from: $V_{(VCC–OUT)}$ to: $V_{(SENSE–OUT)}$ 12
- Added text to the Gate Capacitor (dV/dt) Control section description 16
- Added text to the High Gate Capacitance Applications section description 17
- Added The Input Bypass section description. 17

Changes from Revision A (March 2010) to Revision B — **Page**

- Added Feature: Calculator Tool Available (SLVC033) 1
- Added a sentence to the first paragraph of the DESIGN PROCEDURE section - See SLVC033 for a calculation tool to help with this process. 14
- Added the Gate Capacitor (dV/dt) Control section: Revised text and Equation 12 16

Changes from Revision B (March 2010) to Revision C — **Page**

- Changed Figure 15, From: I_{IN} = 5 A/div To: I_{IN} = 0.5 A/div 13

Changes from Revision C (September 2011) to Revision D — **Page**

- Added Input voltage range, OUT as an individual line in the Abs Max Table 2
- Added Operating voltage range to the RECOMMENDED OPERATING CONDITIONS table 2
- Changed Supply Current Disabled Test Conditions From: V_{EN} = Lo, V_{SENSE} = V_{VCC} = V_{OUT} = 0 To: V_{EN} = Lo, V_{SENSE} = V_{VCC} = V_{OUT} 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2490DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BIY	Samples
TPS2490DGSG4	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIY	Samples
TPS2490DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BIY	Samples
TPS2490DGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIY	Samples
TPS2491DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BIX	Samples
TPS2491DGSG4	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIX	Samples
TPS2491DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BIX	Samples
TPS2491DGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

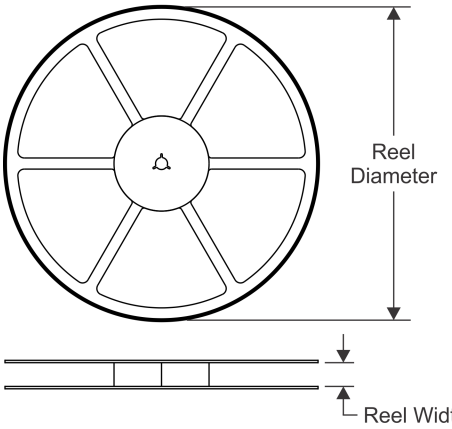
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

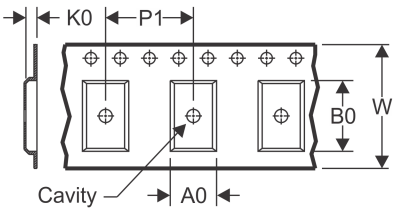
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

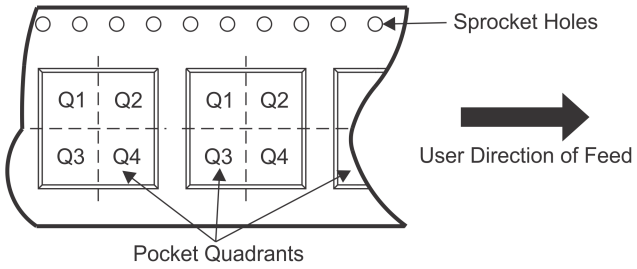


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

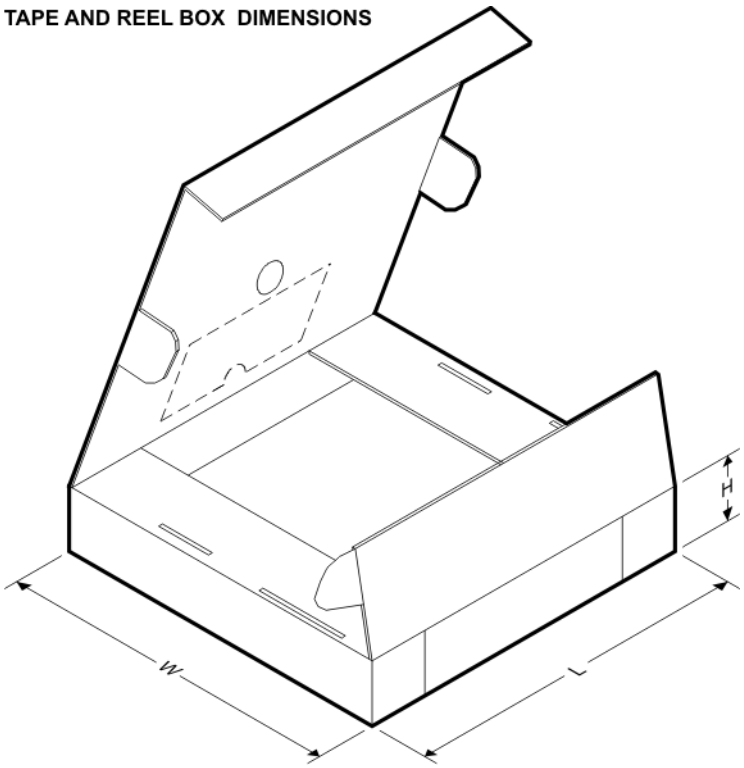
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2490DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2491DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

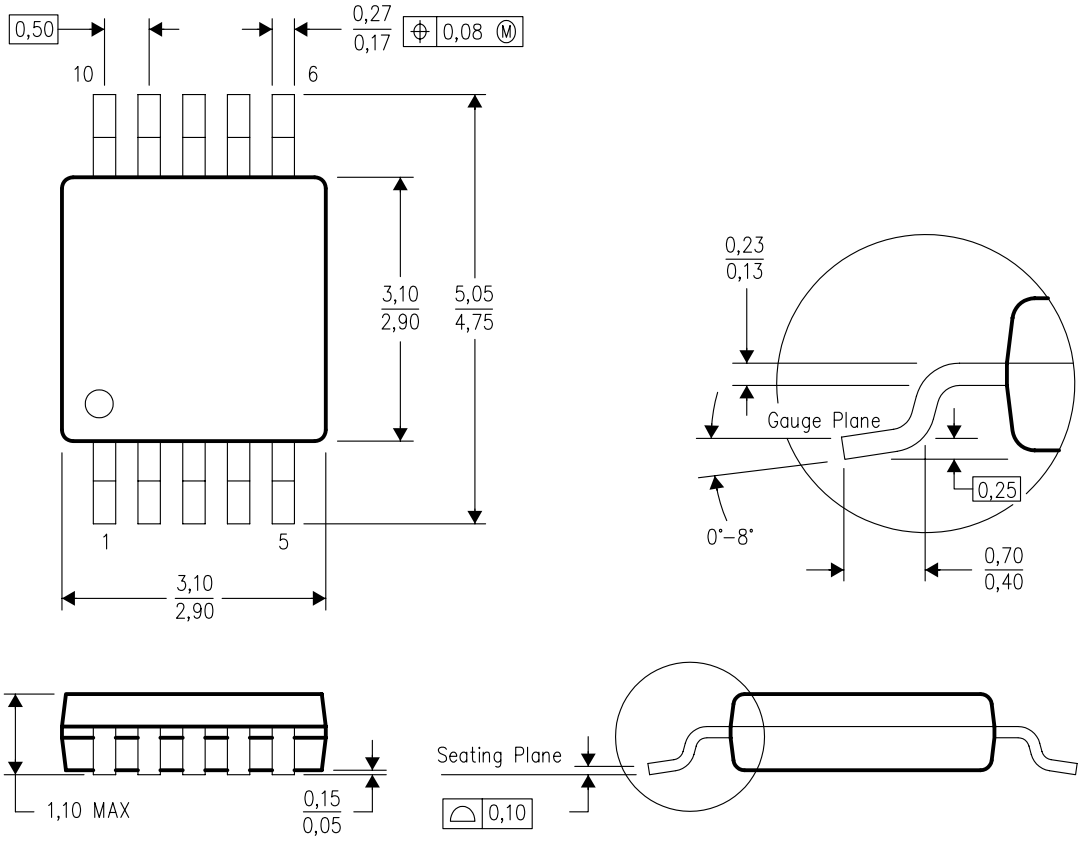
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2490DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TPS2491DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0

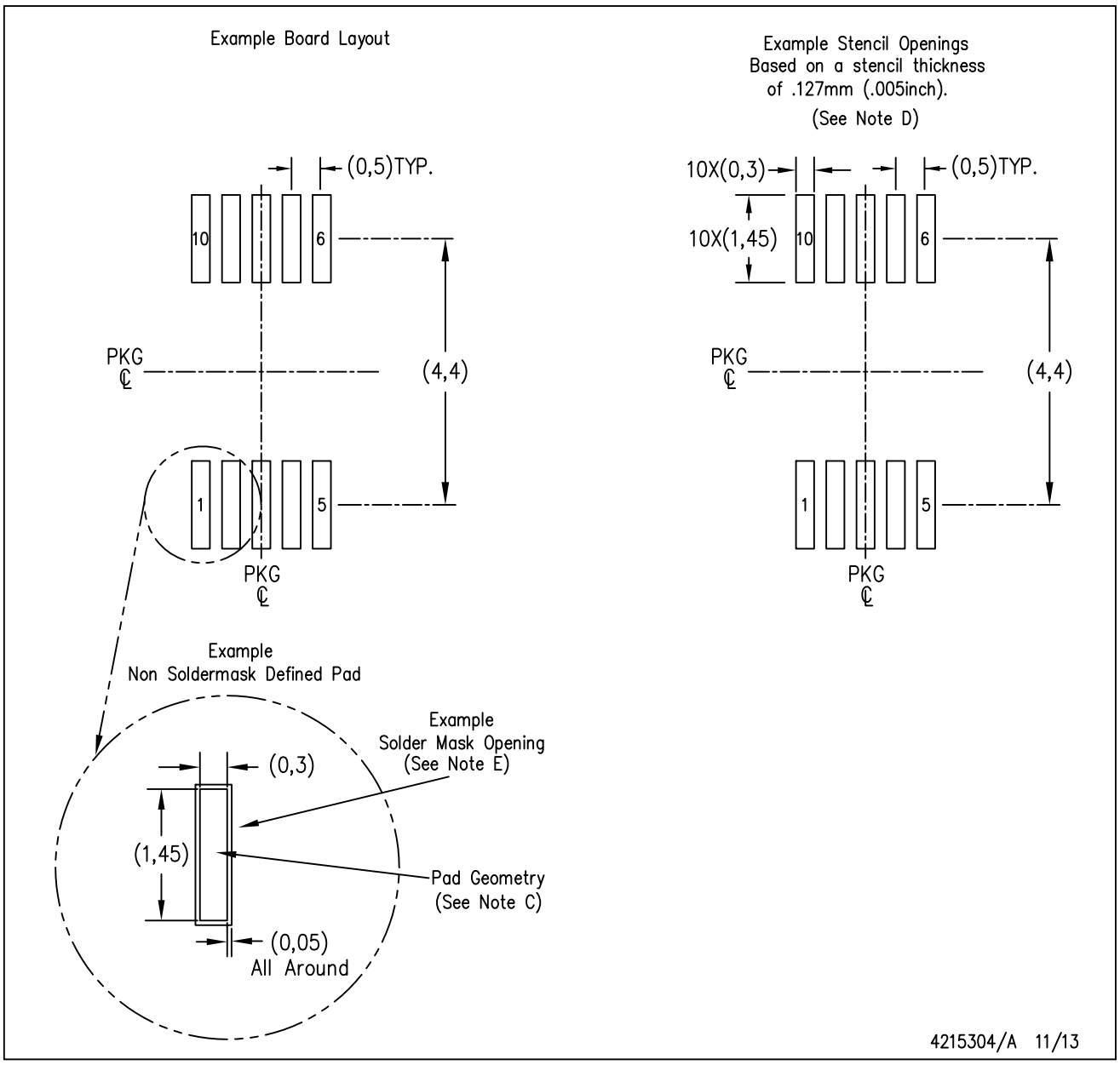
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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