



# PCA9511A

Hot swappable I<sup>2</sup>C-bus and SMBus bus buffer

Rev. 04 — 19 August 2009

Product data sheet

## 1. General description

The PCA9511A is a hot swappable I<sup>2</sup>C-bus and SMBus buffer that allows I/O card insertion into a live backplane without corrupting the data and clock buses. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the PCA9511A provides bidirectional buffering, keeping the backplane and card capacitances isolated.

The PCA9511A rise time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements. The PCA9511A incorporates a digital ENABLE input pin, which enables the device when asserted HIGH and forces the device into a low current mode when asserted LOW, and an open-drain READY output pin, which indicates that the backplane and card sides are connected together (HIGH) or not (LOW).

During insertion, the PCA9511A SDA and SCL lines are precharged to 1 V to minimize the current required to charge the parasitic capacitance of the chip.

## 2. Features

- Bidirectional buffer for SDA and SCL lines increases fan out and prevents SDA and SCL corruption during live board insertion and removal from multipoint backplane systems
- Compatible with I<sup>2</sup>C-bus Standard-mode, I<sup>2</sup>C-bus Fast-mode, and SMBus standards
- Built-in  $\Delta V/\Delta t$  rise time accelerators on all SDA and SCL lines (0.6 V threshold) requires the bus pull-up voltage and supply voltage ( $V_{CC}$ ) to be the same
- Active HIGH ENABLE input
- Active HIGH READY open-drain output
- High-impedance SDA and SCL pins for  $V_{CC} = 0$  V
- 1 V precharge on all SDA and SCL lines
- Supporting clock stretching and multiple master arbitration/synchronization
- Operating power supply voltage range: 2.7 V to 5.5 V
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8 (MSOP8)

### 3. Applications

- cPCI, VME, AdvancedTCA cards and other multipoint backplane cards that are required to be inserted or removed from an operating system

### 4. Feature selection

**Table 1. Feature selection chart**

Feature	PCA9510A	PCA9511A	PCA9512A	PCA9513A	PCA9514A
idle detect	yes	yes	yes	yes	yes
high-impedance SDA, SCL pins for $V_{CC} = 0\text{ V}$	yes	yes	yes	yes	yes
rise time accelerator circuitry on SDA <sub>n</sub> and SCL <sub>n</sub> lines	-	yes	yes	yes	yes
rise time accelerator circuitry hardware disable pin for lightly loaded systems	-	-	yes	-	-
rise time accelerator threshold 0.8 V versus 0.6 V improves noise margin	-	-	-	yes	yes
ready open-drain output	yes	yes	-	yes	yes
two $V_{CC}$ pins to support 5 V to 3.3 V level translation with improved noise margins	-	-	yes	-	-
1 V precharge on all SDA and SCL lines	in only	yes	yes	-	-
92 $\mu\text{A}$ current source on SCLIN and SDAIN for PICMG applications	-	-	-	yes	-

### 5. Ordering information

**Table 2. Ordering information**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Type number	Topside mark	Package		
		Name	Description	Version
PCA9511AD	PA9511A	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9511ADP	9511A	TSSOP8 <sup>[1]</sup>	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

[1] Also known as 'MSOP8'.

6. Block diagram

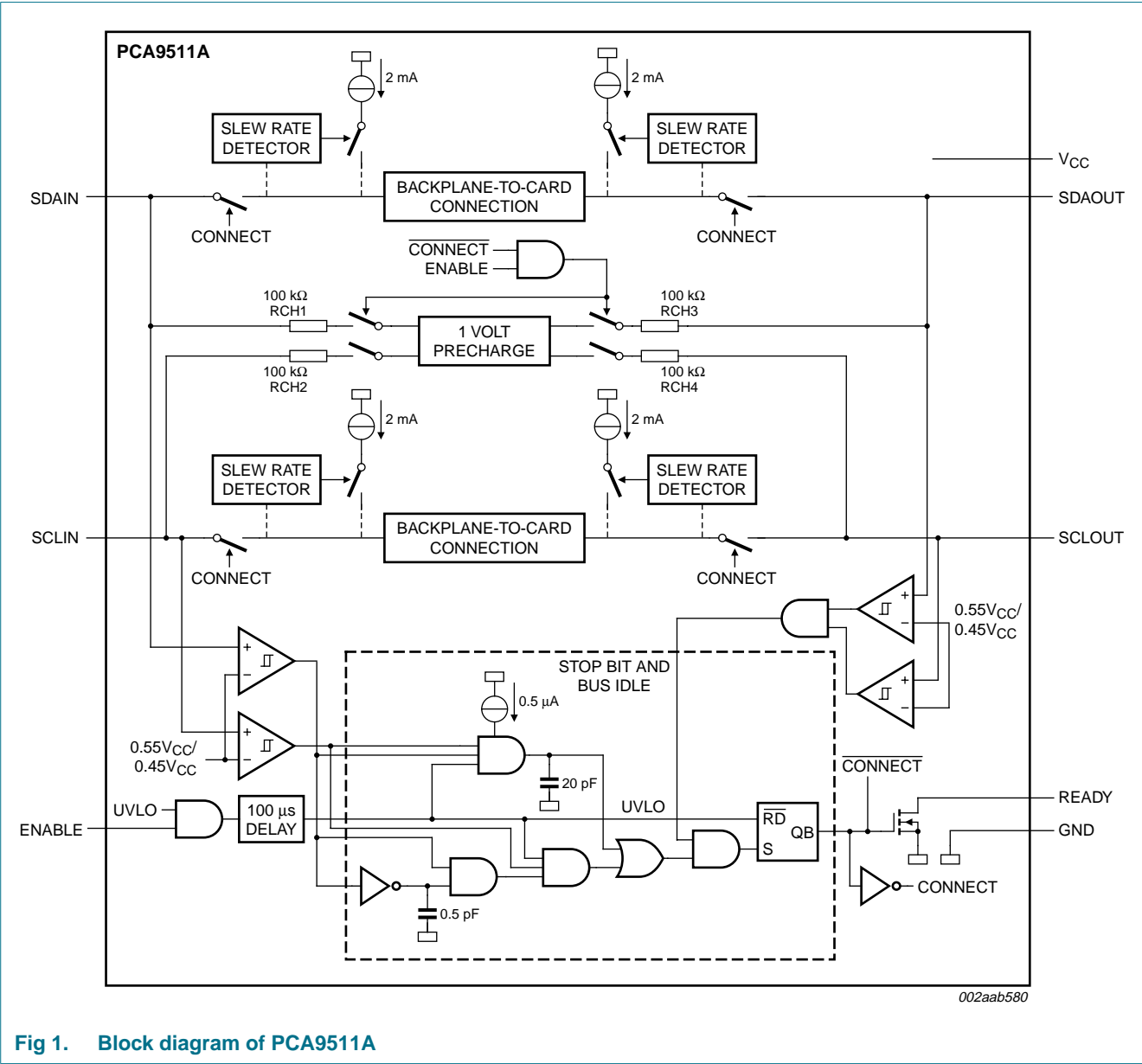
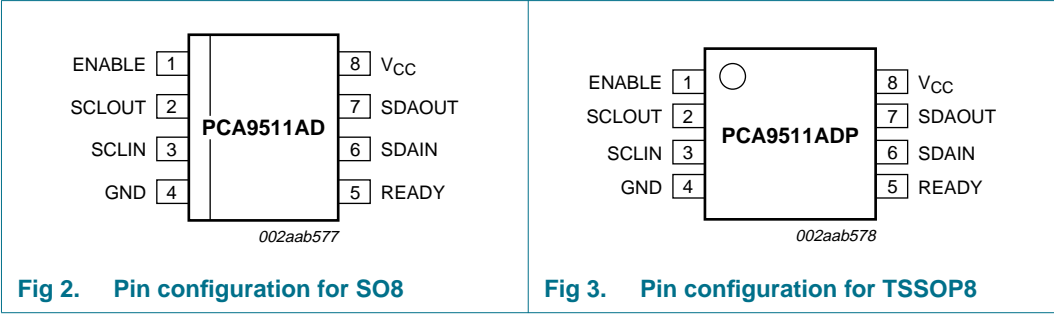


Fig 1. Block diagram of PCA9511A

7. Pinning information

7.1 Pinning



7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
ENABLE	1	Chip enable. Grounding this input puts the part in a low current (< 1 $\mu$ A) mode. It also disables the rise time accelerators, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT.
SCLOUT	2	serial clock output to and from the SCL bus on the card
SCLIN	3	serial clock input to and from the SCL bus on the backplane
GND	4	Ground. Connect this pin to a ground plane for best results.
READY	5	open-drain output which pulls LOW when SDAIN and SCLIN are disconnected from SDAOUT and SCLOUT, and goes HIGH when the two sides are connected
SDAIN	6	serial data input to and from the SDA bus on the backplane
SDAOUT	7	serial data output to and from the SDA bus on the card
V <sub>CC</sub>	8	power supply

8. Functional description

Refer to [Figure 1 “Block diagram of PCA9511A”](#).

8.1 Start-up

An undervoltage/initialization circuit holds the parts in a disconnected state which presents high-impedance to all SDA and SCL pins during power-up. A LOW on the ENABLE pin also forces the parts into the low current disconnected state when the I<sub>CC</sub> is essentially zero. As the power supply is brought up and the ENABLE is HIGH or the part is powered and the ENABLE is taken from LOW to HIGH it enters an initialization state where the internal references are stabilized and the precharge circuit is enabled. At the end of the initialization state the ‘Stop Bit And Bus Idle’ detect circuit is enabled. With the ENABLE pin HIGH long enough to complete the initialization state (t<sub>en</sub>) and remaining HIGH when all the SDA and SCL pins have been HIGH for the bus idle time or when all pins are HIGH and a STOP condition is seen on the SDAIN and SCLIN pins, SDAIN is connected to SDAOUT and SCLIN is connected to SCLOUT. The 1 V precharge circuitry

is activated during the initialization and is deactivated when the connection is made. The precharge circuitry pulls up the SDA and SCL pins to 1 V through individual 100 k $\Omega$  nominal resistors. This precharges the pins to 1 V to minimize the worst case disturbances that result from inserting a card into the backplane where the backplane and the card are at opposite logic levels.

## 8.2 Connect circuitry

Once the connection circuitry is activated, the behavior of SDAIN and SDAOUT as well as SCLIN and SCLOUT become identical with each acting as a bidirectional buffer that isolates the input capacitance from the output bus capacitance while communicating the logic levels. A LOW forced on either SDAIN or SDAOUT will cause the other pin to be driven to a LOW by the part. The same is also true for the SCL pins. Noise between  $0.7V_{CC}$  and  $V_{CC}$  is generally ignored because a falling edge is only recognized when it falls below  $0.7V_{CC}$  with a slew rate of at least 1.25 V/ $\mu$ s. When a falling edge is seen on one pin, the other pin in the pair turns on a pull-down driver that is referenced to a small voltage above the falling pin. The driver will pull the pin down at a slew rate determined by the driver and the load initially, because it does not start until the first falling pin is below  $0.7V_{CC}$ . The first falling pin may have a fast or slow slew rate, if it is faster than the pull down slew rate then the initial pull-down rate will continue. If the first falling pin has a slow slew rate then the second pin will be pulled down at its initial slew rate only until it is just above the first pin voltage then they will both continue down at the slew rate of the first.

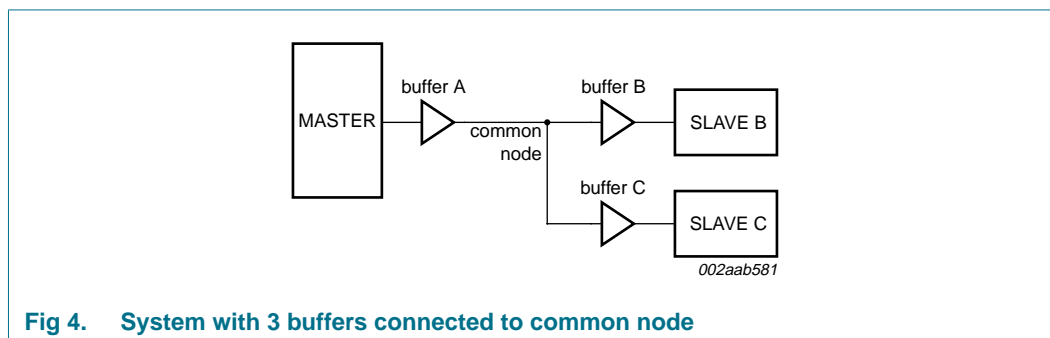
Once both sides are LOW they will remain LOW until all the external drivers have stopped driving LOWs. If both sides are being driven LOW to the same value for instance, 10 mV by external drivers, which is the case for clock stretching and is typically the case for acknowledge, and one side external driver stops driving that pin will rise until the internal driver pulls it down to the offset voltage. When the last external driver stops driving a LOW, that pin will rise up and settle out just above the other pin as both rise together with a slew rate determined by the internal slew rate control and the RC time constant. As long as the slew rate is at least 1.25 V/ $\mu$ s, when the pin voltage exceeds 0.6 V for the PCA9511A, the rise time accelerator's circuits are turned on and the pull-down driver is turned off.

## 8.3 Maximum number of devices in series

Each buffer adds about 0.1 V dynamic level offset at 25 °C with the offset larger at higher temperatures. Maximum offset ( $V_{offset}$ ) is 0.150 V with a 10 k $\Omega$  pull-up resistor. The LOW level at the signal origination end (master) is dependent upon the load and the only specification point is that the I<sup>2</sup>C-bus specification of 3 mA will produce  $V_{OL} < 0.4$  V, although if lightly loaded the  $V_{OL}$  may be  $\sim 0.1$  V. Assuming  $V_{OL} = 0.1$  V and  $V_{offset} = 0.1$  V, the level after four buffers would be 0.5 V, which is only about 0.1 V below the threshold of the rising edge accelerator (about 0.6 V). With great care a system with four buffers may work, but as the  $V_{OL}$  moves up from 0.1 V, noise or bounces on the line will result in firing the rising edge accelerator thus introducing false clock edges. Generally it is recommended to limit the number of buffers in series to two, and to keep the load light to minimize the offset.

The PCA9510A (rise time accelerator is permanently disabled) and the PCA9512A (rise time accelerator can be turned off) are a little different with the rise time accelerator turned off because the rise time accelerator will not pull the node up, but the same logic that turns

on the accelerator turns the pull-down off. If the  $V_{IL}$  is above  $\sim 0.6$  V and a rising edge is detected, the pull-down will turn off and will not turn back on until a falling edge is detected.



Consider a system with three buffers connected to a common node and communication between the Master and Slave B that are connected at either end of buffer A and buffer B in series as shown in Figure 4. Consider if the  $V_{OL}$  at the input of buffer A is 0.3 V and the  $V_{OL}$  of Slave B (when acknowledging) is 0.4 V with the direction changing from Master to Slave B and then from Slave B to Master. Before the direction change you would observe  $V_{IL}$  at the input of buffer A of 0.3 V and its output, the common node, is  $\sim 0.4$  V. The output of buffer B and buffer C would be  $\sim 0.5$  V, but Slave B is driving 0.4 V, so the voltage at Slave B is 0.4 V. The output of buffer C is  $\sim 0.5$  V. When the Master pull-down turns off, the input of buffer A rises and so does its output, the common node, because it is the only part driving the node. The common node will rise to 0.5 V before buffer B's output turns on, if the pull-up is strong the node may bounce. If the bounce goes above the threshold for the rising edge accelerator  $\sim 0.6$  V the accelerators on both buffer A and buffer C will fire contending with the output of buffer B. The node on the input of buffer A will go HIGH as will the input node of buffer C. After the common node voltage is stable for a while the rising edge accelerators will turn off and the common node will return to  $\sim 0.5$  V because the buffer B is still on. The voltage at both the Master and Slave C nodes would then fall to  $\sim 0.6$  V until Slave B turned off. This would not cause a failure on the data line as long as the return to 0.5 V on the common node ( $\sim 0.6$  V at the Master and Slave C) occurred before the data setup time. If this were the SCL line, the parts on buffer A and buffer C would see a false clock rather than a stretched clock, which would cause a system error.

## 8.4 Propagation delays

The delay for a rising edge is determined by the combined pull-up current from the bus resistors and the rise time accelerator current source and the effective capacitance on the lines. If the pull-up currents are the same, any difference in rise time is directly proportional to the difference in capacitance between the two sides. The  $t_{PLH}$  may be negative if the output capacitance is less than the input capacitance and would be positive if the output capacitance is larger than the input capacitance, when the currents are the same.

The  $t_{PHL}$  can never be negative because the output does not start to fall until the input is below  $0.7V_{CC}$ , and the output turn on has a non-zero delay, and the output has a limited maximum slew rate, and even if the input slew rate is slow enough that the output catches up it will still lag the falling voltage of the input by the offset voltage. The maximum  $t_{PHL}$  occurs when the input is driven LOW with zero delay and the output is still limited by its

turn-on delay and the falling edge slew rate. The output falling edge slew rate is a function of the internal maximum slew rate which is a function of temperature,  $V_{CC}$  and process, as well as the load current and the load capacitance.

### 8.5 Rise time accelerators

During positive bus transitions a 2 mA current source is switched on to quickly slew the SDA and SCL lines HIGH once the input level of 0.6 V for the PCA9511A is exceeded. The rising edge rate should be at least 1.25 V/ $\mu$ s to guarantee turn on of the accelerators. The built-in  $\Delta V/\Delta t$  rise time accelerators on all SDA and SCL lines requires the bus pull-up voltage and supply voltage ( $V_{CC}$ ) to be the same.

### 8.6 READY digital output

This pin provides a digital flag which is LOW when either ENABLE is LOW or the start-up sequence described earlier in this section has not been completed. READY goes HIGH when ENABLE is HIGH and start-up is complete. The pin is driven by an open-drain pull-down capable of sinking 3 mA while holding 0.4 V on the pin. Connect a resistor of 10 k $\Omega$  to  $V_{CC}$  to provide the pull-up.

### 8.7 ENABLE low current disable

Grounding the ENABLE pin disconnects the backplane side from the card side, disables the rise time accelerators, drives READY LOW, disables the bus precharge circuitry, and puts the part in a low current state. When the pin voltage is driven all the way to  $V_{CC}$ , the part waits for data transactions on both the backplane and card sides to be complete before reconnecting the two sides.

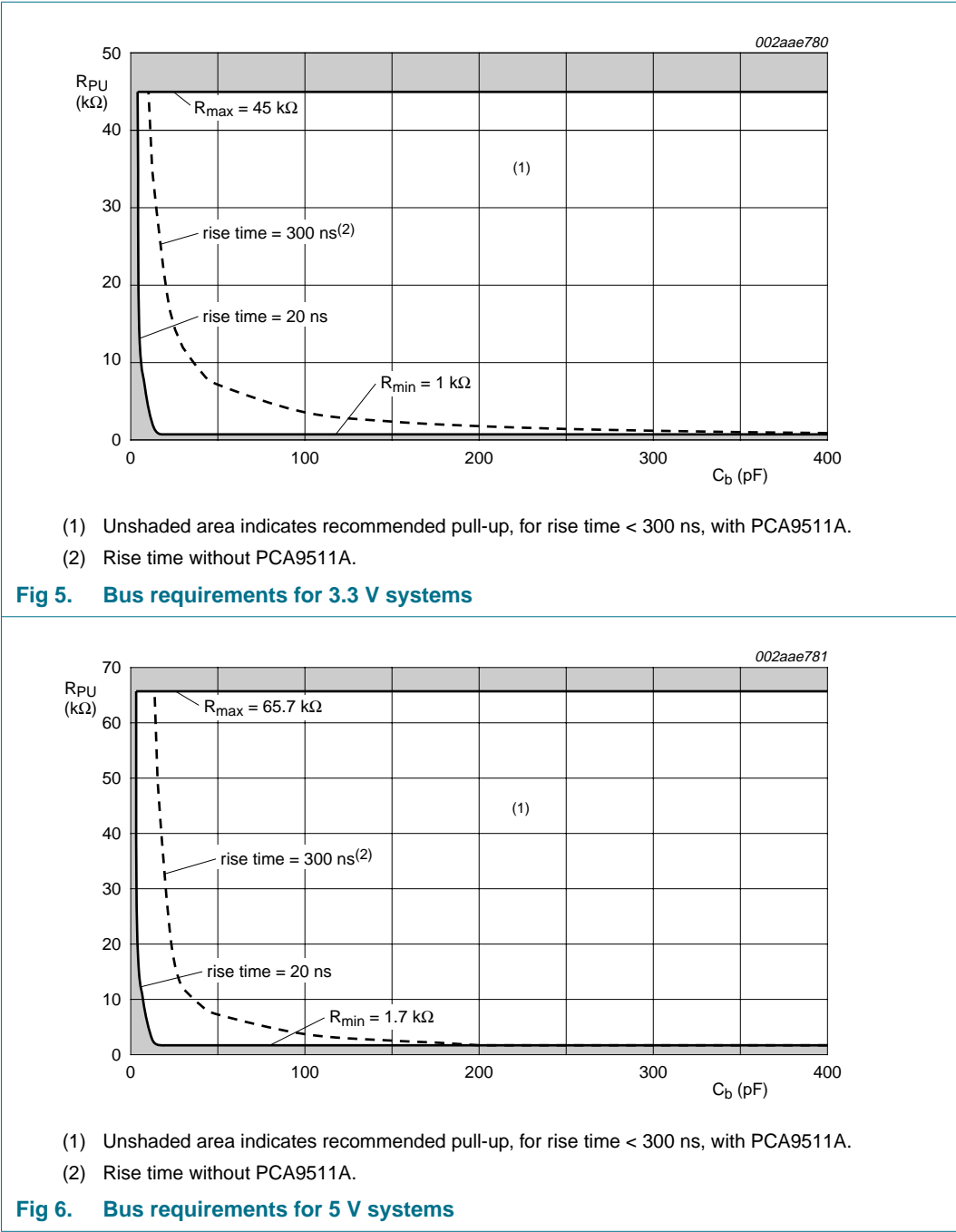
### 8.8 Resistor pull-up value selection

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25 V/ $\mu$ s on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value using the formula given in [Equation 1](#):

$$R \leq 800 \times 10^3 \left( \frac{V_{CC(min)} - 0.6}{C} \right) \quad (1)$$

where R is the pull-up resistor value in  $\Omega$ ,  $V_{CC(min)}$  is the minimum  $V_{CC}$  voltage in volts, and C is the equivalent bus capacitance in picofarads (pF).

In addition, regardless of the bus capacitance, always choose  $R \leq 65.7$  k $\Omega$  for  $V_{CC} = 5.5$  V maximum,  $R \leq 45$  k $\Omega$  for  $V_{CC} = 3.6$  V maximum. The start-up circuitry requires logic HIGH voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the precharge voltage. See the curves in [Figure 5](#) and [Figure 6](#) for guidance in resistor pull-up selection.

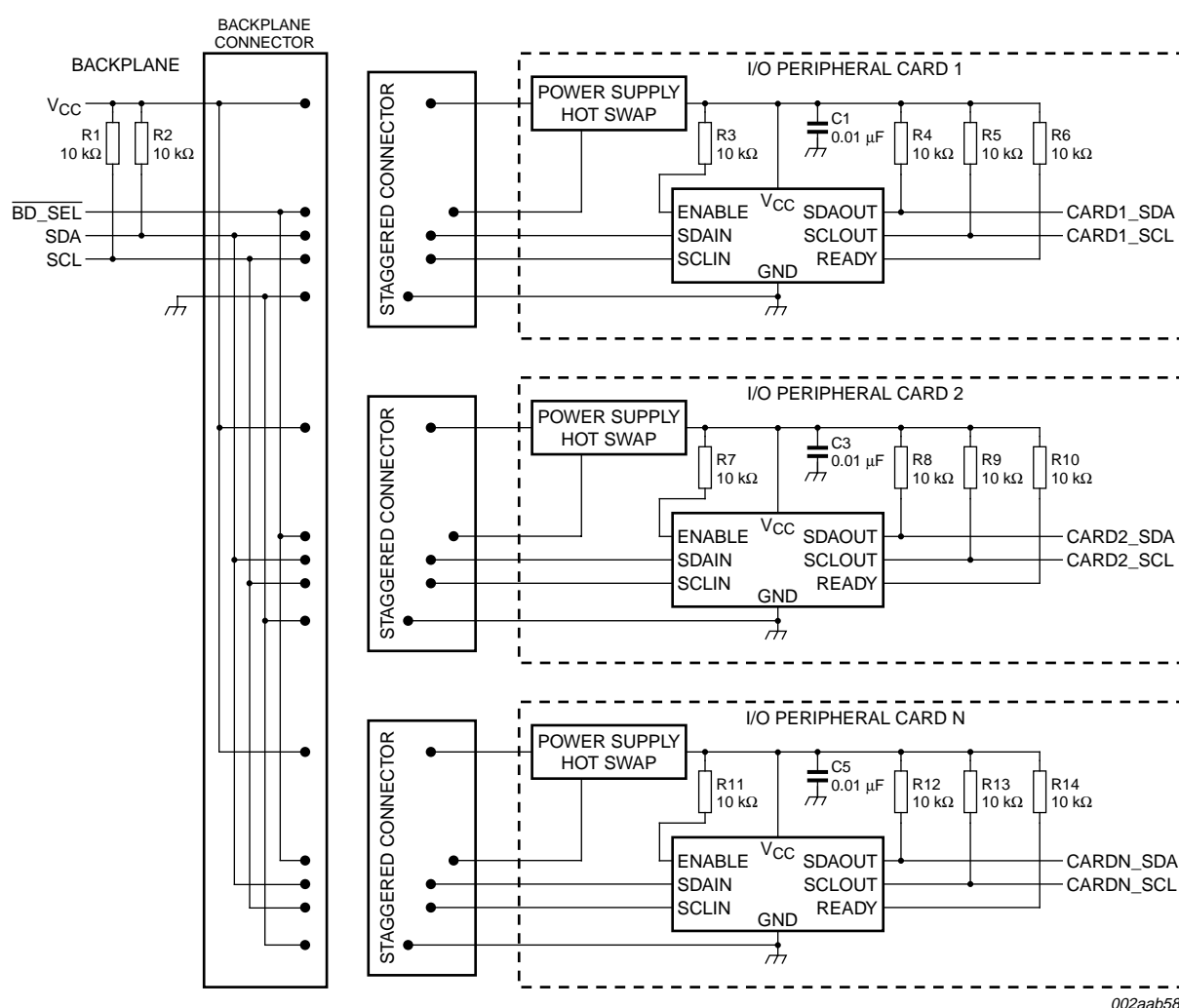




## 8.9 Hot swapping and capacitance buffering application

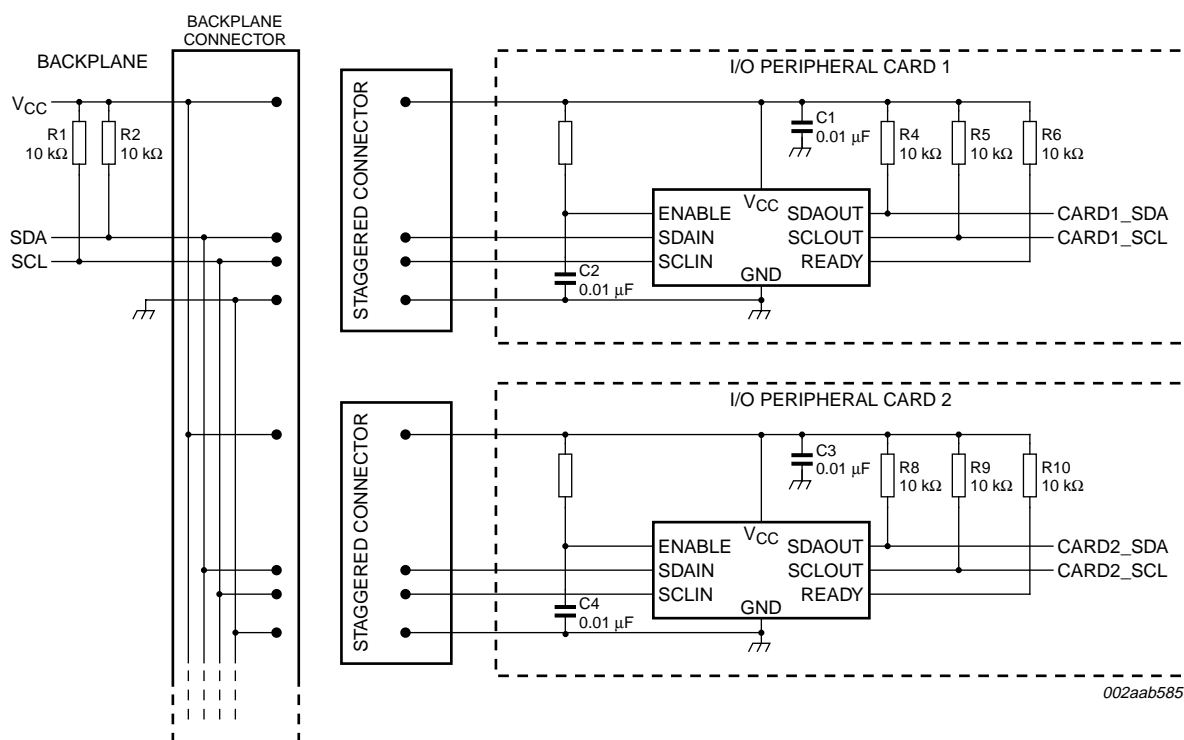
Figure 7 through Figure 10 illustrate the usage of the PCA9511A in applications that take advantage of both its hot swapping and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise time and fall time requirements difficult to meet. Placing a bus buffer on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the PCA9511A drives the capacitance of everything on the card and the backplane must drive only the capacitance of the bus buffer, which is less than 10 pF, the connector, trace, and all additional cards on the backplane.

See Application Note AN10160, 'Hot Swap Bus Buffer' for more information on applications and technical assistance.

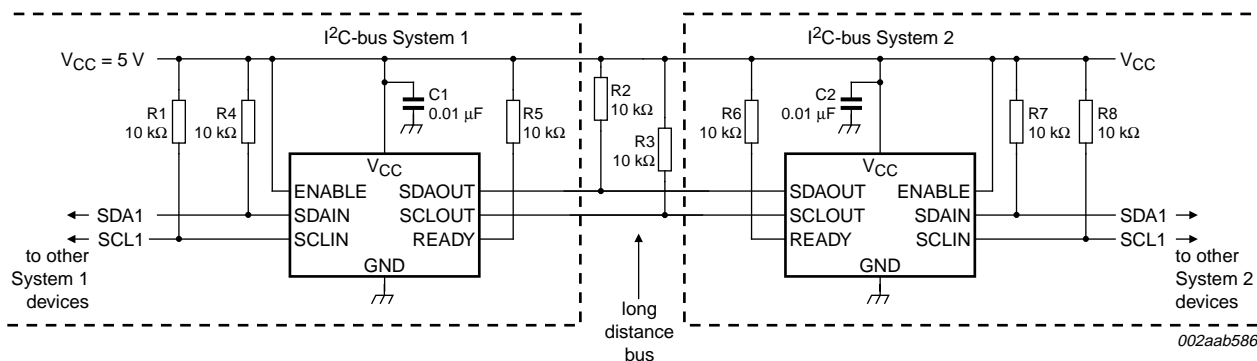


**Remark:** The PCA9511A can be used in any combination depending on the number of rise time accelerators that are needed by the system. Normally only one PCA9511A would be required per bus.

**Fig 7. Hot swapping multiple I/O cards into a backplane using the PCA9511A in a cPCI, VME, and AdvancedTCA system**



**Fig 8. Hot swapping multiple I/O cards into a backplane using the PCA9511A in a PCI system**



**Remark:** See Application Note AN255, 'I<sup>2</sup>C repeaters, hubs, and expanders' for more information on other devices better optimized for long distance transmission of the I<sup>2</sup>C-bus or SMBus.

**Fig 9. Repeater/bus extender application using the PCA9511A**

[illegible]

## 9. Application design-in information

The diagram shows a 74VHC00 inverter chip with the following connections:

- Pin 1 (ENABLE):** Connected to a common ground rail.
- Pin 4 (GND):** Connected to a common ground rail.
- Pin 5 (READY):** Connected to a common ground rail.
- Pin 8:** Connected to the  $V_{CC}$  supply (2.7 V to 5.5 V).
- Input Stage (Pins 3 and 6):**
  - Pin 3 (SCLIN):** Connected to  $V_{CC}$  through a pull-up resistor  $R1$  (10 k $\Omega$ ).
  - Pin 6 (SDAIN):** Connected to  $V_{CC}$  through a pull-up resistor  $R2$  (10 k $\Omega$ ).
- Output Stage (Pins 2 and 7):**
  - Pin 2 (SCLOUT):** Connected to  $V_{CC}$  through a pull-up resistor  $R5$  (10 k $\Omega$ ).
  - Pin 7 (SDAOUT):** Connected to  $V_{CC}$  through a pull-up resistor  $R3$  (10 k $\Omega$ ) and a pull-down resistor  $R4$  (10 k $\Omega$ ).
- Capacitors:** A capacitor  $C1$  (0.01  $\mu$ F) is connected between pins 8 and 5.

The circuit is labeled with the part number 002aab579.

## 10. Limiting values

#### Table 4. Limiting values

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		[1] −0.5	+7	V
V <sub>n</sub>	voltage on SDAIN, SCLIN, SDAOUT, SCLOUT, READY, ENABLE		[1] −0.5	+7	V
T <sub>oper</sub>	operating temperature		−40	+85	°C
T <sub>stg</sub>	storage temperature		−65	+150	°C
T <sub>sp</sub>	solder point temperature	10 s max.	-	+300	°C
T <sub>j(max)</sub>	maximum junction temperature		-	+125	°C

[1] Voltages with respect to pin GND.

## 11. Characteristics

**Table 5. Characteristics**

$V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Power supply</b>						
$V_{CC}$	supply voltage		[1] 2.7	-	5.5	V
$I_{CC}$	supply current	$V_{CC} = 5.5\text{ V}$ ; $V_{SDAIN} = V_{SCLIN} = 0\text{ V}$	[1] -	3.5	6	mA
$I_{CC(sd)}$	Shut-down mode supply current	$V_{ENABLE} = 0\text{ V}$ ; all other pins at $V_{CC}$ or GND	-	0.1	-	$\mu\text{A}$
<b>Start-up circuitry</b>						
$V_{pch}$	precharge voltage	SDA, SCL floating	[1] 0.8	1.1	1.2	V
$V_{IH(ENABLE)}$	HIGH-level input voltage on pin ENABLE		-	$0.5 \times V_{CC}$	$0.7 \times V_{CC}$	V
$V_{IL(ENABLE)}$	LOW-level input voltage on pin ENABLE		$0.3 \times V_{CC}$	$0.5 \times V_{CC}$	-	V
$I_{I(ENABLE)}$	input current on pin ENABLE	$V_{ENABLE} = 0\text{ V to }V_{CC}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$t_{en}$	enable time		[2] -	110	-	$\mu\text{s}$
$t_{idle(READY)}$	bus idle time to READY active		[1] 50	105	200	$\mu\text{s}$
$t_{dis(EN-RDY)}$	disable time (ENABLE to READY)		-	30	-	ns
$t_{stp(READY)}$	SDAIN to READY delay after STOP		[3] -	1.2	-	$\mu\text{s}$
$t_{READY}$	SCLOUT/SDAOUT to READY delay		[3] -	0.8	-	$\mu\text{s}$
$I_{LZ(READY)}$	off-state leakage current on pin READY	$V_{ENABLE} = V_{CC}$	-	$\pm 0.3$	-	$\mu\text{A}$
$C_{i(ENABLE)}$	input capacitance on pin ENABLE	$V_I = V_{CC}$ or GND	[4] -	1.9	4.0	pF
$C_{o(READY)}$	output capacitance on pin READY	$V_I = V_{CC}$ or GND	[4] -	2.5	4.0	pF
$V_{OL(READY)}$	LOW-level output voltage on pin READY	$I_{pu} = 3\text{ mA}$ ; $V_{ENABLE} = V_{CC}$	[1] -	-	0.4	V
<b>Rise time accelerators</b>						
$I_{trt(pu)}$	transient boosted pull-up current	positive transition on SDA, SCL; $V_{CC} = 2.7\text{ V}$ ; slew rate = $1.25\text{ V}/\mu\text{s}$	[5][6] 1	2	-	mA

**Table 5. Characteristics ...continued** $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input-output connection</b>						
$V_{offset}$	offset voltage	10 k $\Omega$ to $V_{CC}$ on SDA, SCL; $V_{CC} = 3.3\text{ V}$	[1][7][9] 0	110	175	mV
$t_{PLH}$	LOW to HIGH propagation delay	SCL to SCL and SDA to SDA; 10 k $\Omega$ to $V_{CC}$ ; $C_L = 100\text{ pF}$ each side	-	0	-	ns
$t_{PHL}$	HIGH to LOW propagation delay	SCL to SCL and SDA to SDA; 10 k $\Omega$ to $V_{CC}$ ; $C_L = 100\text{ pF}$ each side	-	70	-	ns
$C_{I(SCL/SDA)}$	SCL and SDA input capacitance		[4] -	5	7	pF
$V_{OL}$	LOW-level output voltage	$V_I = 0\text{ V}$ ; SDA <sub>n</sub> , SCL <sub>n</sub> pins; $I_{sink} = 3\text{ mA}$ ; $V_{CC} = 2.7\text{ V}$	[1] 0	-	0.4	V
$I_{LI}$	input leakage current	SDA <sub>n</sub> , SCL <sub>n</sub> pins; $V_{CC} = 5.5\text{ V}$	-1	-	+1	$\mu\text{A}$
<b>System characteristics</b>						
$f_{SCL}$	SCL clock frequency		[4] 0	-	400	kHz
$t_{BUF}$	bus free time between a STOP and START condition		[4] 1.3	-	-	$\mu\text{s}$
$t_{HD,STA}$	hold time (repeated) START condition		[4] 0.6	-	-	$\mu\text{s}$
$t_{SU,STA}$	set-up time for a repeated START condition		[4] 0.6	-	-	$\mu\text{s}$
$t_{SU,STO}$	set-up time for STOP condition		[4] 0.6	-	-	$\mu\text{s}$
$t_{HD,DAT}$	data hold time		[4] 300	-	-	ns
$t_{SU,DAT}$	data set-up time		[4] 100	-	-	ns
$t_{LOW}$	LOW period of the SCL clock		[4] 1.3	-	-	$\mu\text{s}$
$t_{HIGH}$	HIGH period of the SCL clock		[4] 0.6	-	-	$\mu\text{s}$
$t_f$	fall time of both SDA and SCL signals		[4][8] $20 + 0.1 \times C_b$	-	300	ns
$t_r$	rise time of both SDA and SCL signals		[4][8] $20 + 0.1 \times C_b$	-	300	ns

[1] This specification applies over the full operating temperature range.

[2] The enable time can slow considerably for some parts when temperature is  $< -20\text{ }^{\circ}\text{C}$ .

[3] Delays that can occur after ENABLE and/or idle times have passed.

[4] Guaranteed by design, not production tested.

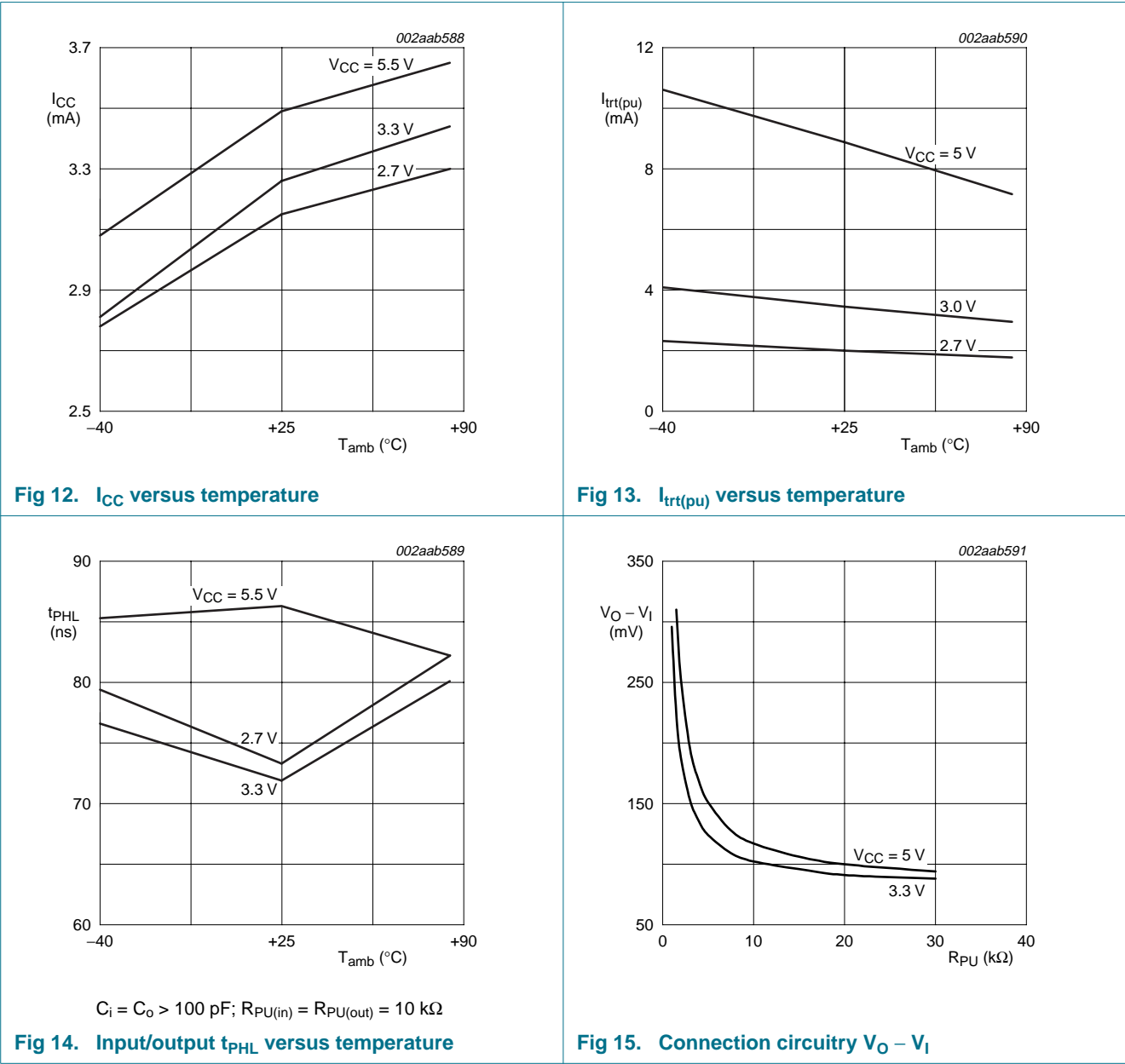
[5]  $I_{trt(pu)}$  varies with temperature and  $V_{CC}$  voltage, as shown in [Section 11.1 "Typical performance characteristics"](#).

[6] Input pull-up voltage should not exceed power supply voltage in operating mode because the rise time accelerator will clamp the voltage to the positive supply rail.

[7] The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pull-up resistor and  $V_{CC}$  voltage is shown in [Section 11.1 "Typical performance characteristics"](#).[8]  $C_b$  = total capacitance of one bus line in pF.

[9] Force  $V_{SDAIN} = V_{SCLIN} = 0.1\text{ V}$ , tie SDAOUT and SCLOUT through 10 k $\Omega$  resistor to  $V_{CC}$  and measure the SDAOUT and SCLOUT output.

### 11.1 Typical performance characteristics



11.2 Timing diagrams

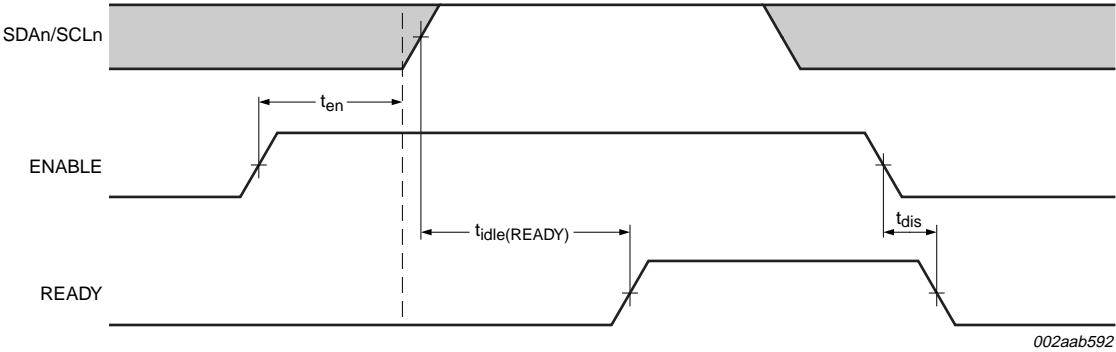
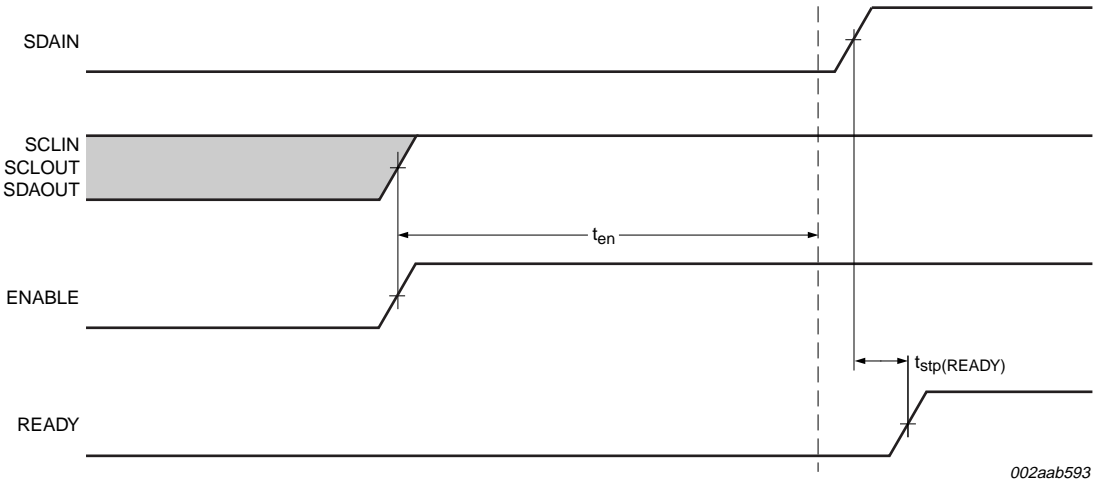
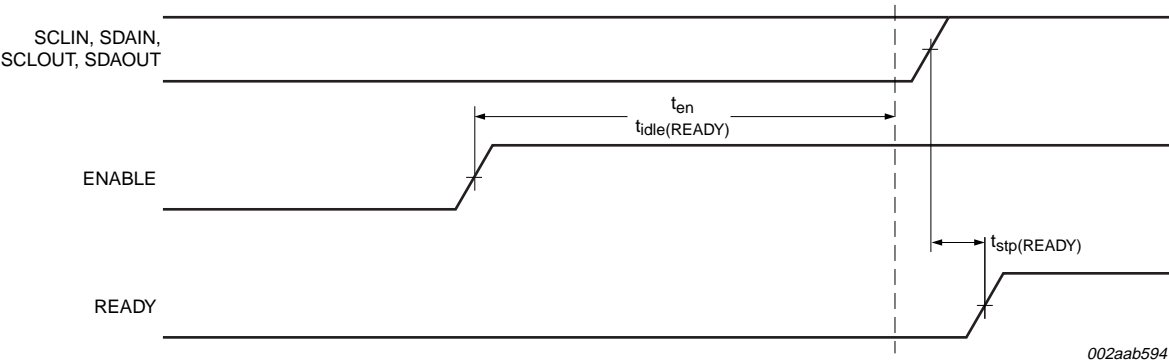


Fig 16. Timing for  $t_{en}$ ,  $t_{idle(READY)}$ , and  $t_{dis}$



$t_{stp(READY)}$  is only applicable after the  $t_{en}$  delay.

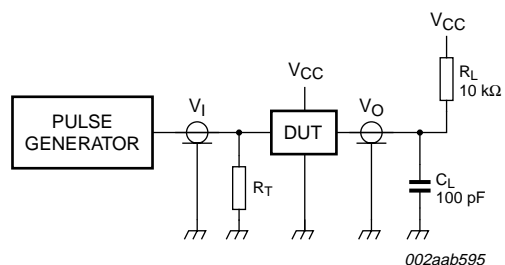
Fig 17.  $t_{stp(READY)}$  that can occur after  $t_{en}$



$t_{stp(READY)}$  is only applicable after the  $t_{en}$  delay.

Fig 18.  $t_{stp(READY)}$  delay that can occur after  $t_{en}$  and  $t_{idle(READY)}$

## 12. Test information



$R_L$  = load resistor

$C_L$  = load capacitance includes jig and probe capacitance

$R_T$  = termination resistance should be equal to the output impedance  $Z_0$  of the pulse generators.

**Fig 19. Test circuitry for switching times**



13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm SOT96-1

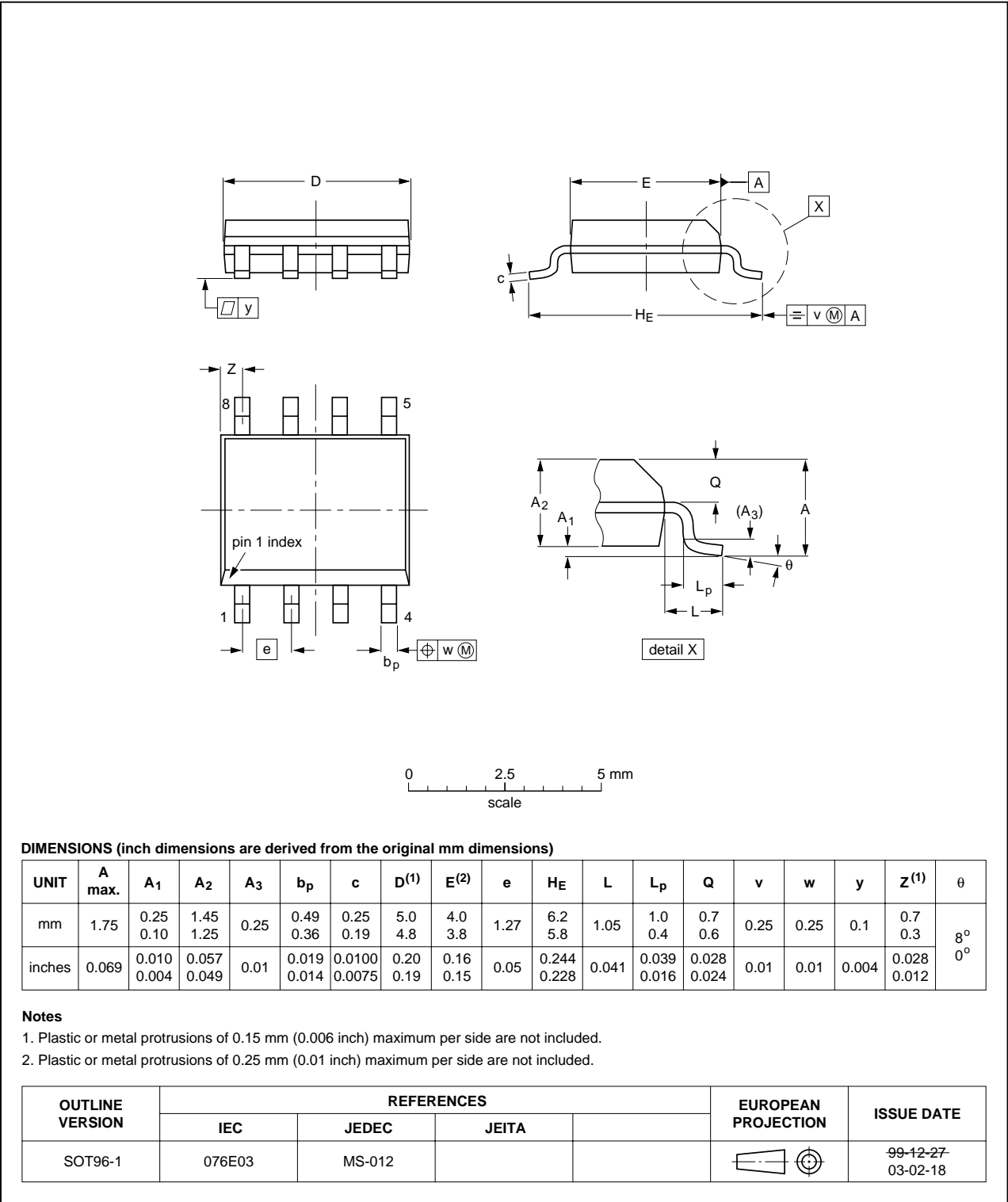


Fig 20. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

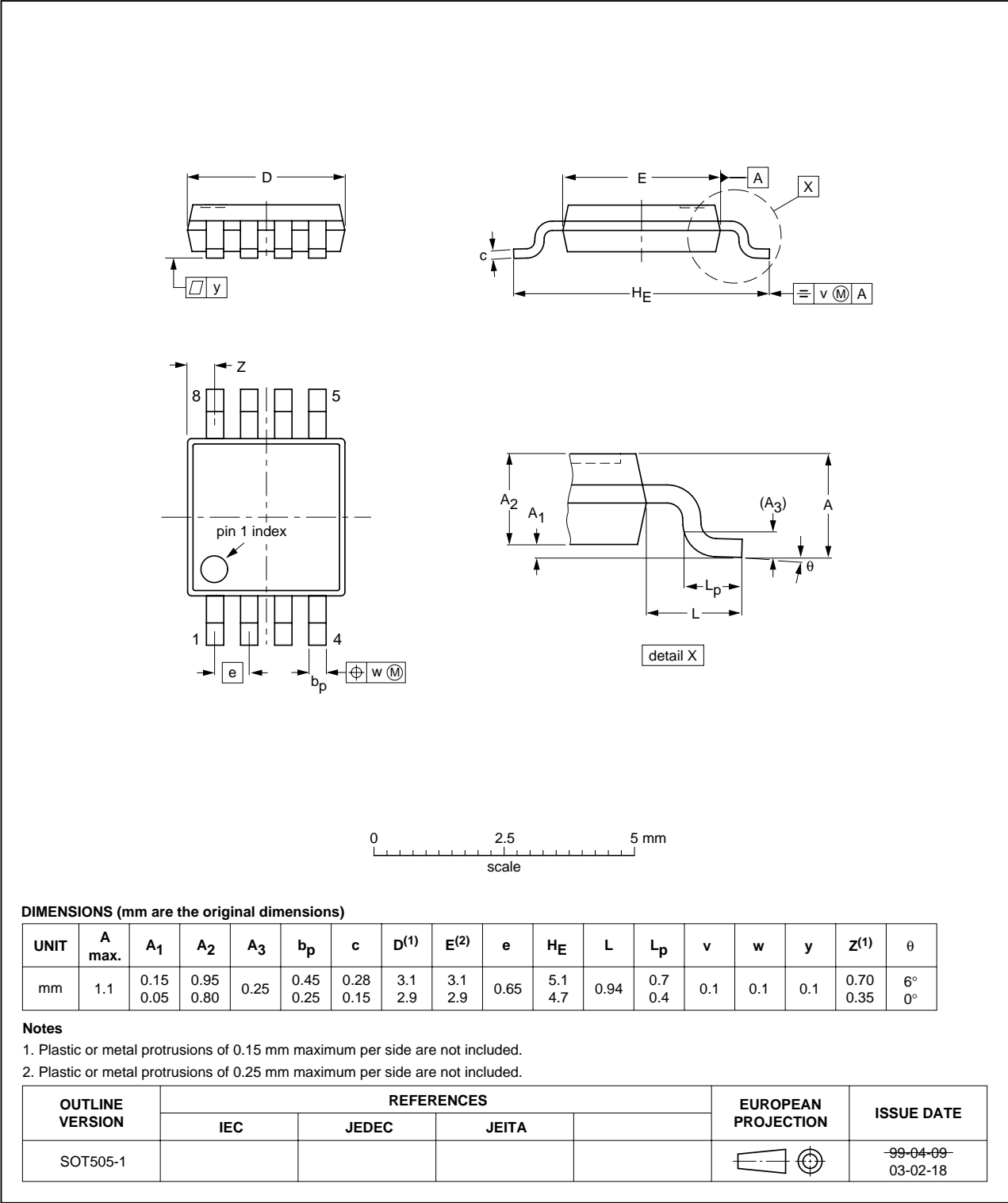


Fig 21. Package outline SOT505-1 (TSSOP8)

## 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leadless or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leadless SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leadless packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 22](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 6](#) and [7](#)

**Table 6. SnPb eutectic process (from J-STD-020C)**

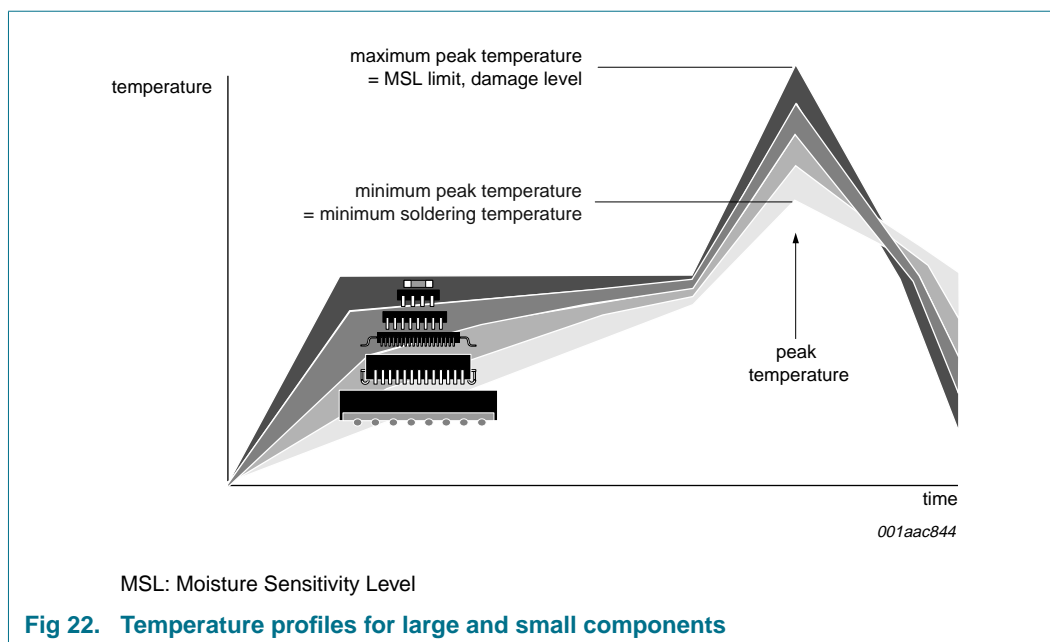
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 7. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 22](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

## 15. Abbreviations

**Table 8. Abbreviations**

Acronym	Description
AdvancedTCA	Advanced Telecommunications Computing Architecture
CDM	Charged Device Model
cPCI	compact Peripheral Component Interface
ESD	Electrostatic Discharge
HBM	Human Body Model
I <sup>2</sup> C-bus	Inter IC bus
MM	Machine Model
PCI	Peripheral Component Interface
PICMG	PCI Industrial Computer Manufacturers Group
SMBus	System Management Bus
VME	VERSAModule Eurocard

## 16. Revision history

**Table 9.** Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9511A_4	20090819	Product data sheet	-	PCA9511A_3
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 8.8 "Resistor pull-up value selection"</a>, 2<sup>nd</sup> paragraph, 1<sup>st</sup> sentence: changed from "... always choose <math>R \leq 16 \text{ k}\Omega</math> for <math>V_{CC} = 5.5 \text{ V}</math> maximum, <math>R \leq 24 \text{ k}\Omega</math> for <math>V_{CC} = 3.6 \text{ V}</math> maximum." to "... always choose <math>R \leq 65.7 \text{ k}\Omega</math> for <math>V_{CC} = 5.5 \text{ V}</math> maximum, <math>R \leq 45 \text{ k}\Omega</math> for <math>V_{CC} = 3.6 \text{ V}</math> maximum."</li> <li>• <a href="#">Figure 5 "Bus requirements for 3.3 V systems"</a> updated: <ul style="list-style-type: none"> <li>– changed from "rise time &gt; 300 ns" to "rise time = 300 ns"</li> <li>– changed from "rise time &lt; 20 ns" to "rise time = 20 ns"</li> </ul> </li> <li>• <a href="#">Figure 6 "Bus requirements for 5 V systems"</a> updated: <ul style="list-style-type: none"> <li>– changed from "rise time &gt; 300 ns" to "rise time = 300 ns"</li> <li>– changed from "rise time &lt; 20 ns" to "rise time = 20 ns"</li> </ul> </li> </ul>			
PCA9511A_3	20090720	Product data sheet	-	PCA9511A_2
PCA9511A_2	20090528	Product data sheet	-	PCA9511A_1
PCA9511A_1 (9397 750 13269)	20050815	Product data sheet	-	-

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 19. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features</b> .....	<b>1</b>
<b>3</b>	<b>Applications</b> .....	<b>2</b>
<b>4</b>	<b>Feature selection</b> .....	<b>2</b>
<b>5</b>	<b>Ordering information</b> .....	<b>2</b>
<b>6</b>	<b>Block diagram</b> .....	<b>3</b>
<b>7</b>	<b>Pinning information</b> .....	<b>4</b>
7.1	Pinning .....	4
7.2	Pin description .....	4
<b>8</b>	<b>Functional description</b> .....	<b>4</b>
8.1	Start-up .....	4
8.2	Connect circuitry .....	5
8.3	Maximum number of devices in series .....	5
8.4	Propagation delays .....	6
8.5	Rise time accelerators .....	7
8.6	READY digital output .....	7
8.7	ENABLE low current disable .....	7
8.8	Resistor pull-up value selection .....	7
8.9	Hot swapping and capacitance buffering application .....	9
<b>9</b>	<b>Application design-in information</b> .....	<b>11</b>
<b>10</b>	<b>Limiting values</b> .....	<b>11</b>
<b>11</b>	<b>Characteristics</b> .....	<b>12</b>
11.1	Typical performance characteristics .....	14
11.2	Timing diagrams .....	15
<b>12</b>	<b>Test information</b> .....	<b>16</b>
<b>13</b>	<b>Package outline</b> .....	<b>17</b>
<b>14</b>	<b>Soldering of SMD packages</b> .....	<b>19</b>
14.1	Introduction to soldering .....	19
14.2	Wave and reflow soldering .....	19
14.3	Wave soldering .....	19
14.4	Reflow soldering .....	20
<b>15</b>	<b>Abbreviations</b> .....	<b>21</b>
<b>16</b>	<b>Revision history</b> .....	<b>22</b>
<b>17</b>	<b>Legal information</b> .....	<b>23</b>
17.1	Data sheet status .....	23
17.2	Definitions .....	23
17.3	Disclaimers .....	23
17.4	Trademarks .....	23
<b>18</b>	<b>Contact information</b> .....	<b>23</b>
<b>19</b>	<b>Contents</b> .....	<b>24</b>

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