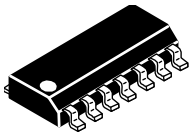
Document Number: MC33897
Rev. 18.0, 4/2012

RoHS

Single Wire CAN Transceiver

33897

SINGLE-WIRE CAN TRANSCEIVER



EF (PB-FREE) SUFFIX
98ASB42565B
14-PIN SOICN

The 33897 series provides a physical layer for digital communication using a Carrier Sense Multiple Access/Collision Resolution (CSMA/CR) data link operating over a single wire medium. This is more commonly referred to as single-wire Controller Area Network (SWCAN).

The 33897 series operates directly from a vehicle's 12 V battery system or a broad range of DC-power sources. It can operate at low or high (33.33 kbps or 83.33 kbps) data rates. A high-voltage wake-up feature allows the device to control the regulator used in support of the MCU and other logic. The device includes a control pin that can be used to put the module regulator into Sleep mode. The presence of a defined wake-up voltage level on the bus will reactivate the control line to turn the regulator and the system back ON.

The device complies with the GMW3089v2.4 General Motors Corporation specification.

Features

- Waveshaping for low Electromagnetic Interference (EMI)
- Detects and automatically handles loss of ground
- Worst-case Sleep mode current of only 60 μA
- Current limit prevents damage due to bus shorts
- Built-in thermal shutdown on bus output
- Protected against vehicular electrical transients
- Under-voltage lockout prevents false data with low battery

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MCZ33897TEF/R2	-40 to 125 °C	14 SOICN
*MC33897CTEF/R2		

*Recommended device for all new designs

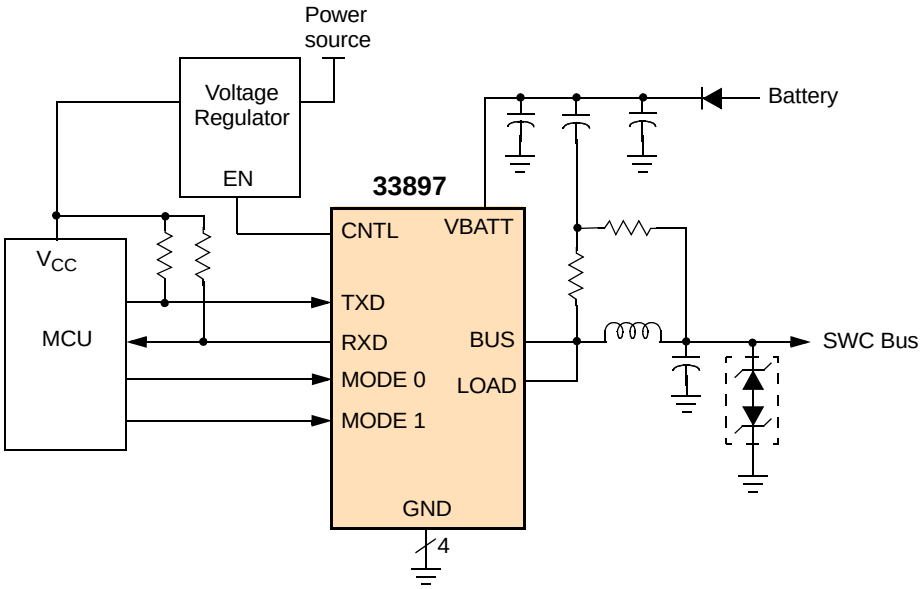


Figure 1. 33897 Simplified Application Diagram

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DEVICE VARIATIONS

Table 1. Device Variations

Part No.	Load Voltage Sleep Mode	See Page
33897T	1.0 V Max	7
*33897CT	0.1 V Max	7

*Recommended device for all new designs

INTERNAL BLOCK DIAGRAM

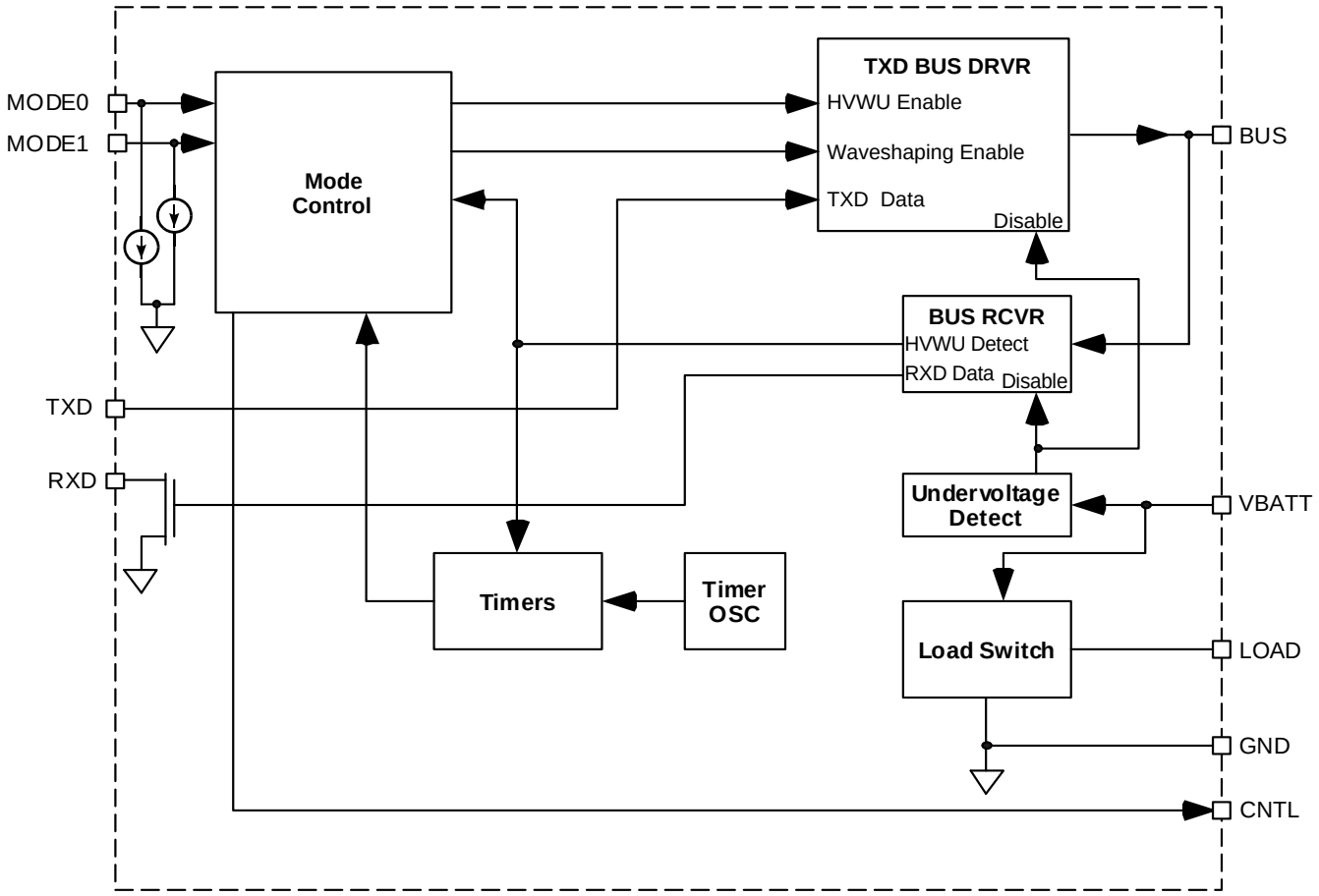


Figure 2. 33897 Simplified Internal Block Diagram

PIN CONNECTIONS

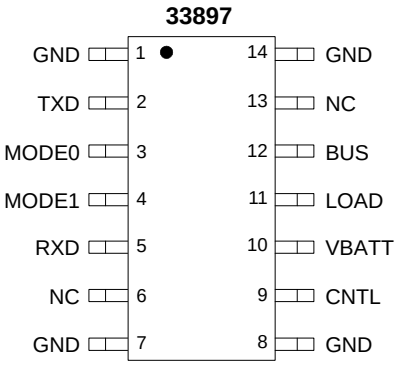


Figure 3. 33897 Pin Connections

Table 2. Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section, beginning on page 12.

33897 Pin	Pin Name	Formal Name	Definition
1, 7, 8, 14	GND	Ground	Electrical Common Ground and Heat removal. A good thermal path will also reduce the die temperature.
2	TXD	Transmit Data	Data input here will appear on the BUS pin. A logic [0] will assert the bus, a logic [1] will make the bus go to the recessive state.
3, 4	MODE0, MODE1	Mode Control	These Pins control Sleep mode, Transmit Level, and Speed. They have weak pull-downs.
5	RXD	Receive Data	Open drain output of the data on BUS. A recessive bus = a logic [1], a dominant bus = logic [0]. An external pull-up is required.
6, 13	NC	No Connect	No internal connection to these Pins. Pin 13 can be connected to GND.
9	CNTL	Control	Provides a battery level logic signal.
10	VBATT	Battery	Power input. An external diode is needed for reverse battery protection.
11	LOAD	Load	The external bus load resistor connects here to prevent bus pull-up in the event of loss of module ground.
12	BUS	Bus	This pin connects to the bus through external components.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Electrical Ratings			
Supply Voltage	V_{BATT}	-0.3 to 40	V
Input Logic Voltage	V_{IN}	-0.3 to 7.0	V
RXD Pin Voltage	V_{RXD}	-0.3 to 7.0	V
CNTL Pin Voltage	V_{CNTL}	-0.3 to 40	V
ESD Voltage[1] Human Body Model All Pins Except BUS BUS Pin Machine Model	V_{ESD}	 ±2000 ±4000 ±100	V
Thermal Ratings			
Ambient Operating Temperature[1]	T_A	-40 to 125	°C
Junction Operating Temperature	T_J	-40 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	150	°C/W
Peak Package Reflow Temperature During Reflow [2], [3]	T_{PPRT}	Note 3.	°C

Notes

1. ESD testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions of -40 °C ≤ T_A ≤ 125 °C, unless otherwise stated. Voltages are relative to GND, unless otherwise noted. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
GENERAL					
Quiescent Current					
Sleep					
5.0 V ≤ V_{BATT} ≤ 13 V (4)	I_{QSLP}	–	45	60	µA
Awake with Transmitter Disabled					
5.0 V ≤ V_{BATT} ≤ 26.5 V	I_{QATDIS}	–	–	4.0	mA
Awake with Transmitter Enabled					
5.0 V ≤ V_{BATT} ≤ 26.5 V	I_{QATEN}	–	–	9.0	mA
Under-voltage Shutdown	V_{BATTUV}	4.0	–	5.0	V
Under-voltage Hysteresis	V_{UVHYS}	0.1	–	0.5	V
Thermal Shutdown (5)	T_{SD}				°C
5.0 V ≤ V_{BATT} ≤ 26.5 V		150	–	190	
Thermal Shutdown Hysteresis (5)	T_{SDHYS}				°C
5.0 V ≤ V_{BATT} ≤ 26.5 V		10	–	20	
LOGIC I/O, MODE0, MODE1, TXD, RXD					
Logic Input Low Level (MODE0, MODE1, and TXD)	V_{IL}				V
5.0 V ≤ V_{BATT} ≤ 26.5 V		–	–	0.8	
Logic Input High Level (MODE0, MODE1, and TXD)	V_{IH}				V
5.0 V ≤ V_{BATT} ≤ 26.5 V		2.0	–	–	
Mode Pin Pull-down Current (MODE0 and MODE1)	I_{PD}				µA
Pin Voltage = 0.8 V, 5.0 V ≤ V_{BATT} ≤ 26.5 V		10	–	50	
Receiver Output Low (RXD)	V_{OL}				V
I_{IN} = 2.0 mA, 5.0 V ≤ V_{BATT} ≤ 26.5 V		–	–	0.45	
CNTL					
CNTL Output Low	V_{OLCNTL}				V
I_{IN} = 5.0 µA, 5.0 V ≤ V_{BATT} ≤ 26.5 V		–	–	0.8	
CNTL Output High	V_{OHCNTL}				V
I_{OUT} = 180 µA, 5.0 V ≤ V_{BATT} ≤ 26.5 V		V_{BATT} - 0.8	–	V_{BATT}	

Notes

4. After $t_{CNTLFDLY}$
5. Thermal shutdown causes the BUS output driver to be disabled. Guaranteed by characterization.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions of -40 °C ≤ T_A ≤ 125 °C, unless otherwise stated. Voltages are relative to GND, unless otherwise noted. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
LOAD					
LOAD Voltage Rise [6]	V_{LDRISE}				V
Normal Speed and Voltage Mode, Transmit High-Voltage Mode, Transmit High Speed Mode					
I_{IN} = 1.0 mA, 5.0 V ≤ V_{BATT} ≤ 26.5 V		–	–	0.1	
Sleep Mode					
I_{IN} = 7.0 mA 33897T		–	–	1.0	
I_{IN} = 7.0 mA [7] 33897CT		–	–	0.1	
Loss of Battery					
I_{IN} = 7.0 mA		–	–	1.0	
LOAD Leakage During Loss of Module Ground [8]	I_{LDLEAK}				µA
0.0 V ≤ V_{BATT} ≤ 18 V 33897T		0.0	–	-90	
0.0 V ≤ V_{BATT} ≤ 18 V 33897CT		-10	–	10	
BUS					
Passive Out BUS Leakage					µA
Passive In	I_{LEAK}				
0.0 V ≤ V_{BATT} ≤ 26.5 V, -1.5 V ≤ V_{BUS} < 0 V		-5.0	–	5.0	
Active In	I_{LKAI}				
0.0 V ≤ V_{BATT} ≤ 26.5 V, 0 V < V_{BUS} ≤ 12.5 V		-5.0	–	5.0	
BUS Leakage During Loss of Module Ground [9]					
0.0 V ≤ V_{BATT} ≤ 18 V 33897T	I_{BLKLOG}	-10	–	10	
0.0 V ≤ V_{BATT} ≤ 18 V 33897CT		0.0	–	-90	
High Voltage Wake-up Mode Output High Voltage					V
12 V ≤ V_{BATT} ≤ 26.5 V, 200 Ω ≤ R_L ≤ 3332 Ω					
33897T	$V_{HVWUOHF}$	9.7	–	12.5	
33897CT	$V_{HVWUOHO}$	9.9	–	12.5	
5.0 V ≤ V_{BATT} < 12 V, 200 Ω ≤ R_L ≤ 3332 Ω		Lesser of V_{BAT} - 1.5 or 9.7	–	V_{BATT}	
High Speed Mode Output High Voltage	V_{OHHS}				V
8.0 V ≤ V_{BATT} ≤ 16 V, 75 Ω ≤ R_L ≤ 135 Ω		4.2	–	5.1	
Normal Mode Output High Voltage					V
6.0 V ≤ V_{BATT} ≤ 26.5 V, 200 Ω ≤ R_L ≤ 3332 Ω	V_{NOHF}	4.4	–	5.1	
5.0 V ≤ V_{BATT} < 6.0 V, 200 Ω ≤ R_L ≤ 3332 Ω	V_{NOHO}	Lesser of V_{BATT} - 1.6 or 4.4	–	Lesser of V_{BATT} or 5.1	

Notes

6. GMW3089V2.4 specifies the maximum load voltage rise to be 0.1 V whenever module battery is intact, including when in Sleep mode. The maximum load voltage rise of 1.0 V in Sleep mode is a GM-approved exception to GMW3089V2.4.
7. 33897CT removes the diode drop during Sleep mode.
8. LOAD pin is at system ground voltage.
9. BUS pin is at system ground voltage

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions of -40 °C ≤ T_A ≤ 125 °C, unless otherwise stated. Voltages are relative to GND, unless otherwise noted. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS (CONTINUED)					
BUS Low Voltage 5.0 V ≤ V_{BATT} ≤ 26.5 V, 200 Ω ≤ R_L ≤ 3332 Ω	V_{OL}	-0.2	–	0.2	V
Short-circuit BUS Output Current Dominant State, 5.0 V ≤ V_{BATT} ≤ 26.5 V	I_{BSC}	-350	–	-100	mA
Input Threshold					V
Awake 5.0 V ≤ V_{BATT} ≤ 26.5 V	V_{BIA}	2.0	–	2.2	
Sleep 12 V ≤ V_{BATT} ≤ 26.5 V	V_{BISF}	6.6	–	7.9	
Sleep 5.0 V ≤ V_{BATT} < 12 V	V_{BISO}	Lesser of 6.6 V or V_{BATT} - 4.3	–	Lesser of 7.9 V or V_{BATT} - 3.25	

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions of -40 °C ≤ T_A ≤ 125 °C, unless otherwise stated. Voltages are relative to GND unless otherwise noted. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS					
Normal Speed Rising Output Delay 200 Ω ≤ R_L ≤ 3332 Ω, 1.0 µs ≤ Load Time Constants ≤ 4.0 µs Measured from TXD = V_{IL} to V_{BUS} as follows: Max Time to V_{BUSMOD} = 3.7 V, 6.0 V ≤ V_{BATT} ≤ 26.5 V (10) Min Time to V_{BUSMOD} = 1.0 V, 6.0 V ≤ V_{BATT} ≤ 26.5 V (10) Max Time to V_{BUSMOD} = 2.7 V, V_{BATT} = 5.0 V (10) Min Time to V_{BUSMOD} = 1.0 V, V_{BATT} = 5.0 V (10)	$t_{DLYNORMRO}$	2.0	–	6.3	µs
Normal Speed Falling Output Delay 200 Ω ≤ R_L ≤ 3332 Ω, 1.0 µs ≤ Load Time Constants ≤ 4.0 µs Measured from TXD = V_{IH} to V_{BUS} as follows: Max Time to V_{BUSMOD} = 1.0 V, 6.0 V ≤ V_{BATT} ≤ 26.5 V (10) Min Time to V_{BUSMOD} = 3.7 V, 6.0 V ≤ V_{BATT} ≤ 26.5 V (10) Max Time to V_{BUSMOD} = 1.0 V, V_{BATT} = 5.0 V (10) Min Time to V_{BUSMOD} = 2.7 V, V_{BATT} = 5.0 V (10)	$t_{DLYNORMFO}$	1.8	–	8.5	µs
High Speed Rising Output Delay 75 Ω ≤ R_L ≤ 135 Ω, 0.0 µs ≤ Load Time Constants ≤ 1.5 µs, 8.0 V ≤ V_{BATT} ≤ 16 V Measured from TXD = V_{IL} to V_{BUS} as follows: Max Time to V_{BUS} = 3.7 V (11) Min Time to V_{BUS} = 1.0 V (11)	$t_{DLYHSRO}$	0.1	–	1.7	µs
High Speed Falling Output Delay 75 Ω ≤ R_L ≤ 135 Ω, 0.0 µs ≤ Load Time Constants ≤ 1.5 µs, 8.0 V ≤ V_{BATT} ≤ 16 V Measured from TXD = V_{IH} to V_{BUS} as follows: Max Time to V_{BUS} = 1.0 V (11) Min Time to V_{BUS} = 3.7 V (11)	$t_{DLYHSFO}$	0.04	–	3.0	µs

Notes

10. V_{BUSMOD} is the voltage at the BUSMOD node in Figure 6, page 13.
11. V_{BUS} is the voltage at the BUS pin in Figure 7, page 14.

Table 5. Dynamic Electrical Characteristics (continued)

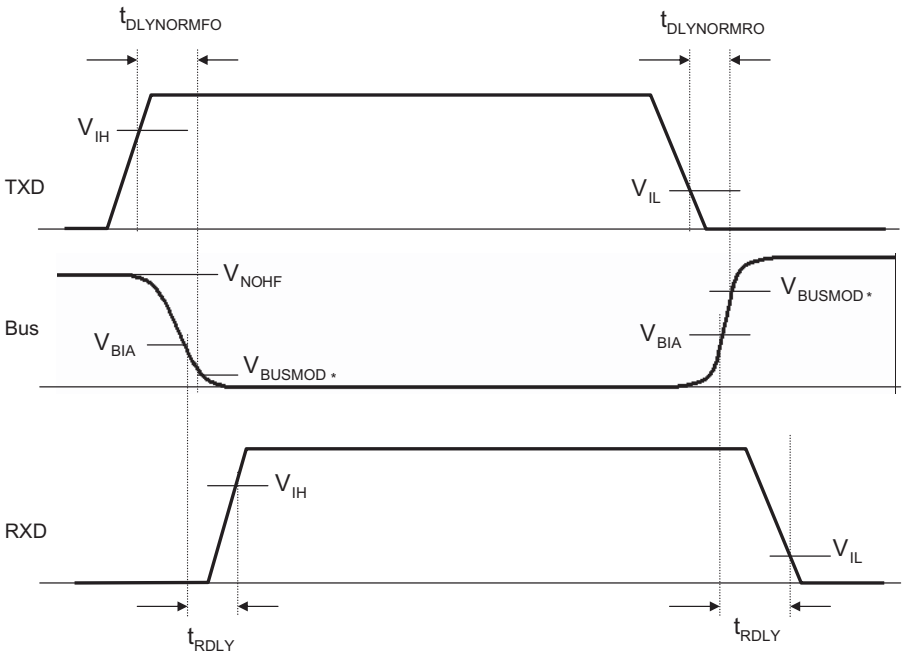
Characteristics noted under conditions of -40 °C ≤ T_A ≤ 125 °C, unless otherwise stated. Voltages are relative to GND unless otherwise noted. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS (CONTINUED)					
High Voltage Rising Output Delay 200 Ω ≤ R_L ≤ 3332 Ω, 1.0 µs ≤ Load Time Constants ≤ 4.0 µs Measured from TXD=V_{IL} to V_{BUS} as follows: Max Time to V_{BUSMOD} = 3.7 V, 6.0 V ≤ V_{BATT} ≤ 26.5 V (12) Min Time to V_{BUSMOD} = 1.0 V, 6.0 V ≤ V_{BATT} ≤ 26.5 V (12) Max Time to V_{BUSMOD} = 9.4 V, 12.0 V ≤ V_{BATT} ≤ 26.5 V (12)	$t_{DLYHVRO}$	 2.0 2.0 2.0	 – – –	 6.3 6.3 18	µs
High Voltage Falling Output Delay 200 Ω ≤ R_L ≤ 3332 Ω, 1.0 µs ≤ Load Time Constants ≤ 4.0 µs, 12.0 V ≤ V_{BATT} ≤ 26.5 V Measured from TXD=V_{IH} to V_{BUS} as follows: Max Time to V_{BUSMOD} = 1.0 V (12) Min Time to V_{BUSMOD} = 3.7 V (12)	$t_{DLYHVFO}$	 1.8 1.8	 – –	 14 14	µs
RECEIVER RXD					
Receive Delay Time (5.0 V ≤ V_{BATT} ≤ 26.5 V) Awake	t_{RDLY}	0.2	–	1.0	µs
Receive Delay Time (BUS Rising to RXD Falling, 5.0 V ≤ V_{BATT} ≤ 26.5 V) Sleep	t_{RDLYSL}	10	–	70	µs
CNTL					
CNTL Falling Delay Time (5.0 V ≤ V_{BATT} ≤ 26.5 V)	$t_{CNTLFDLY}$	300	–	1000	ms

Notes

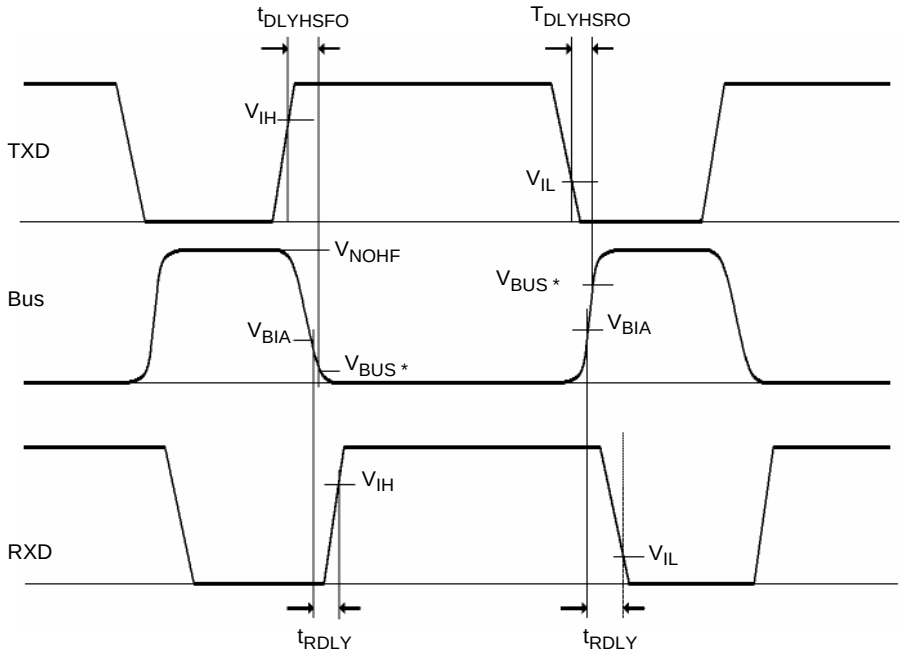
12. V_{BUSMOD} is the voltage at the BUSMOD node in Figure 6, page 13.

TIMING DIAGRAMS



* V_{BUSMOD} is the voltage at the BUSMOD node in Figure 7.

Figure 4. TXD, Bus and RXD Waveforms in Normal Mode



* V_{BUS} is the voltage at the BUS pin in Figure 8.

Figure 5. TXD, Bus and RXD Waveforms in High Speed Mode

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33897 Series is intended for use as a physical layer device in a Single Wire CAN communications bus. Communications takes place from a single pin over a single wire using a common ground for a current return path. Two data rates are available, with the high rate used for factory or assembly line communications and the lower for actual system communications where the radiated EMI of the higher rate could be an issue.

Two pins control the mode of operation (sleep, low speed, high speed, and high voltage wake-up).

FUNCTIONAL PIN DESCRIPTION

The 33897 Series is intended to be used with an MCU to control its operation and to process and generate the data for the bus.

GROUND PINS

The four ground pins are not only for electrical conduction, their number and locations at each of the four corners serve also to remove heat from the IC. The biggest benefit of this is obtained by putting a lot of copper on the PCB in this area and, if ground is an internal layer, by adding numerous plated-through connections to it with the largest diameter holes the layout can use.

TXD DATA

The data driven onto the SWCAN bus is inverted from the TXD pin. A “1” driven on TXD will result in an undriven (recessive) state (bus at near zero volts). When the TXD pin is low, the output goes to a driven state. The voltage and waveshaping in the driven state is determined by the levels on the MODE0 and MODE1 Pins (refer to Table 6).

Table 6. Mode Control Logic Levels

Logic Level		Operation
MODE0	MODE1	
0	0	Sleep mode
0	1	High voltage wake-up mode
1	0	High speed mode
1	1	Normal mode

MODE CONTROL

The MODE pins control the transmitter filtering and BUS voltage and the IC Sleep mode operation. Table 6 shows the mode versus the logic levels on MODE0 and MODE1.

The MODE0 and MODE1 pins have a weak pull-down in the IC so that in case the pins are not driven, the device will enter the Sleep mode. This is usually the situation as the MCU comes out of reset, before the driving signals have been configured as outputs.

RXD DATA

The data received on the bus is translated to logic levels on this pin. This pin is a logic high when the bus is in the recessive state (near zero volts) and is logic low when the bus is in either the normal or high voltage dominant state.

This is an open-drain type of output that requires an external resistor to pull it up. When the device is in sleep mode, the output will be off unless a high voltage wake-up level is detected on the bus. If the wake-up level is detected, the output will be driven by the data on the bus. If the level of the data returns to normal level, the output will return to off after a short delay unless a non-sleep mode condition is set by the MCU.

LOAD SWITCH

This switch is ON in all operating modes unless a loss of ground is detected. If this happens, the switch is opened and the resistor normally attached to its pin will no longer pass current to or from the bus.

CNTL OUTPUT

This logic level signal is used to control a V_{CC} regulator. When the output is low, the V_{CC} regulator is expected to shutdown. This is normally used to shut down the MCU and all the devices powered by V_{CC} when the IC is in Sleep mode. This is done to save power. When the part is taken out of the Sleep mode by the higher than normal bus voltage, this pin is asserted high and the V_{CC} regulator brings its output up to the regulated level. This starts the MCU, which controls the mode of the IC. The MCU must change the mode signals to non-Sleep mode levels in order to keep this pin from going low. There is a delay to allow the MCU to fully wake-up and take control after the high voltage signaling is removed before the level on this output returns low. After a delay time, even if the bus is at high voltage, the IC will return to Sleep mode if both MODE pins are low.

VBATT INPUT

This power input is not reverse battery protected and should use an external diode to protect it from damage due to reverse battery if this protection is desired. The voltage drop of the diode must be taken into consideration when the operating range of the system is being determined. This diode is generally used to protect the entire module from reverse battery and should be selected accordingly.

BUS I/O

This input/output may require electrostatic discharge (ESD) and/or EMI external circuitry. A set of components is shown in the simplified application diagrams on page 15. The value of the capacitor should be adjusted downward in direct proportion to the added capacitance of the ESD or EMI circuits. The series resistance of the inductor should be kept below 3.5 Ω to prevent its voltage drop from significantly degrading system noise margins.

FUNCTIONAL BLOCK DIAGRAM COMPONENTS

TIMER OSC

This circuit generates a 500 kHz signal to be used for internal logic. It is the reference for some of the required delays.

TIMERS

This circuit contains the timing logic used to hold the CNTL active for the required time after the conditions for sleep mode have been met. It is also used to keep the TXD driver active for a period of time after it has generated a passive level on the bus.

MODE CONTROL

This circuit contains the control logic for the various operating modes and conditions required for the IC.

BUS RCVR

This circuit translates the levels on the BUS pin to a CMOS level indicating the presence of a logic [0] or a logic [1]. It also determines the presence of a high voltage wake-up (HVWU) signal that is passed to Mode Control and Timers circuits. An analog filter is used to “de-glitch” the high voltage wake-up signal and prevent false exits from the Sleep mode.

TXD BUS DRVR

This circuit drives the BUS. It can drive it with the higher voltage wake-up signals when enabled by the Mode Control circuit. It can also provide waveshaping for reduced EMI or not provide it for the higher data rate mode. The actual data is received on TXD at CMOS logic levels, then translated by this circuit to the necessary operating voltages.

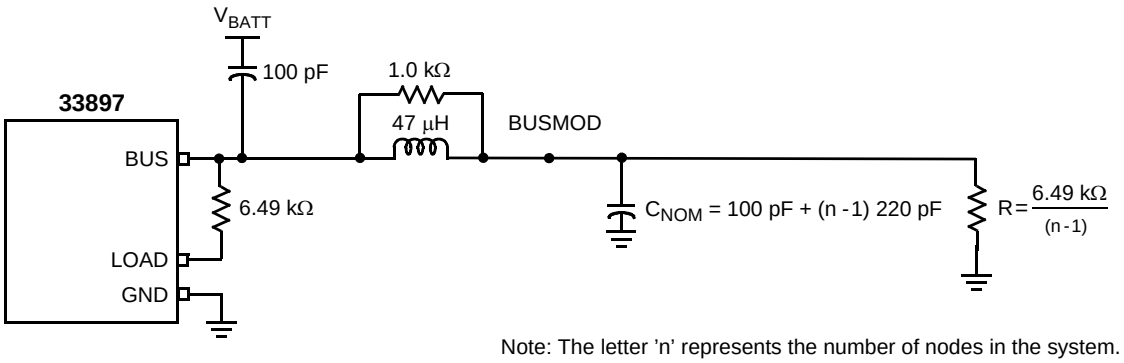
UNDER-VOLTAGE DETECT

This circuit monitors internal operating voltage to assure proper operation of the part. If a low-voltage condition is detected, it sends a signal to disable the BUS RCVR and TXD BUS DRVR circuits. This prevents incorrect data from being put on the bus or sent to the MCU.

LOAD SWITCH

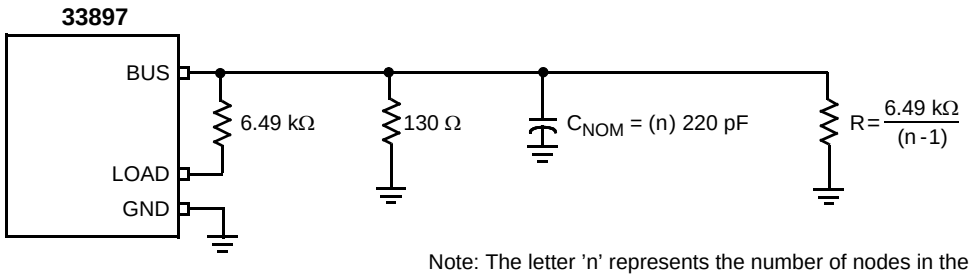
The LOAD switch provides a path for an external resistor connected to the BUS to be connected to ground. When a loss of ground is detected, this switch is opened to prevent the current that would normally be flowing to the ground from the module from going back through the load resistor and raising the bus level. The circuit is opened when the voltage between GND and VBATT becomes too low as would be the case if module ground were lost.

BUS LOADING PARAMETERS



Note: The letter ’n’ represents the number of nodes in the system.

Figure 6. Transmitter Delays in Normal and Transmit High Voltage Wake-up Modes



Note: The letter 'n' represents the number of nodes in the system.

Figure 7. Transmitter Delays in Transmit High Speed Mode

TYPICAL APPLICATIONS

The 33897 can be used in applications where the module includes a regulator that has the capability of going into Sleep mode by having an Enable pin. See Figure 8. When the module's regulator is in Sleep mode, the module is turned off. The module waits for a defined wake-up voltage level on the bus. This wake-up voltage will activate the CNTL line, which enables the regulator and turns the module back ON. This feature allows the module to be more energy efficient since the current consumption is significantly lowered when it goes into sleep mode.

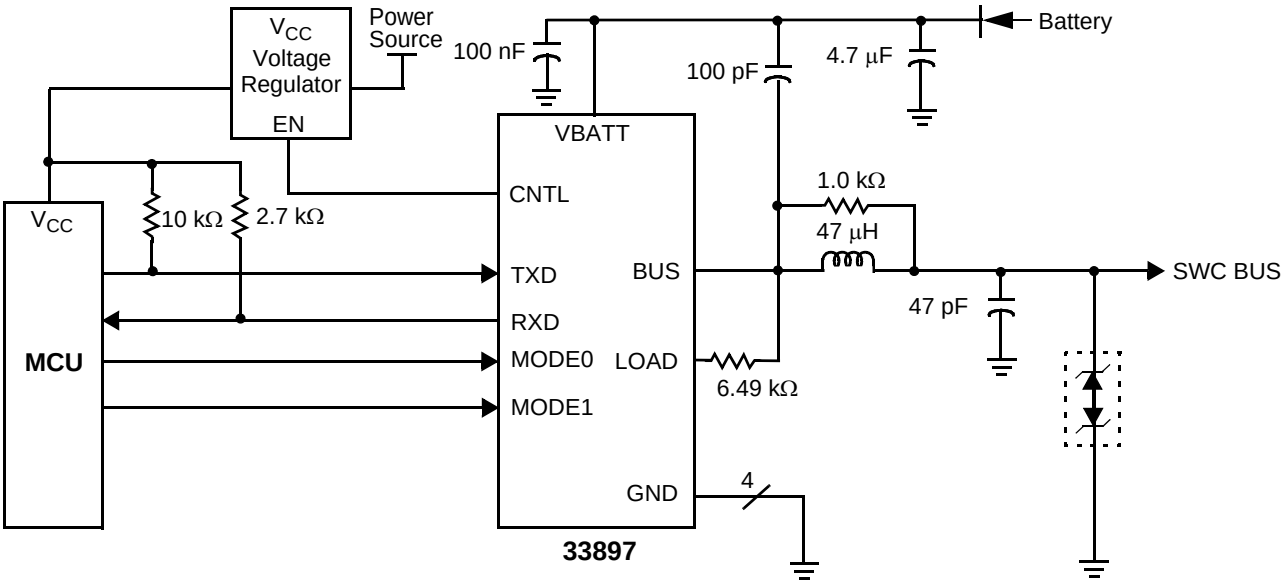
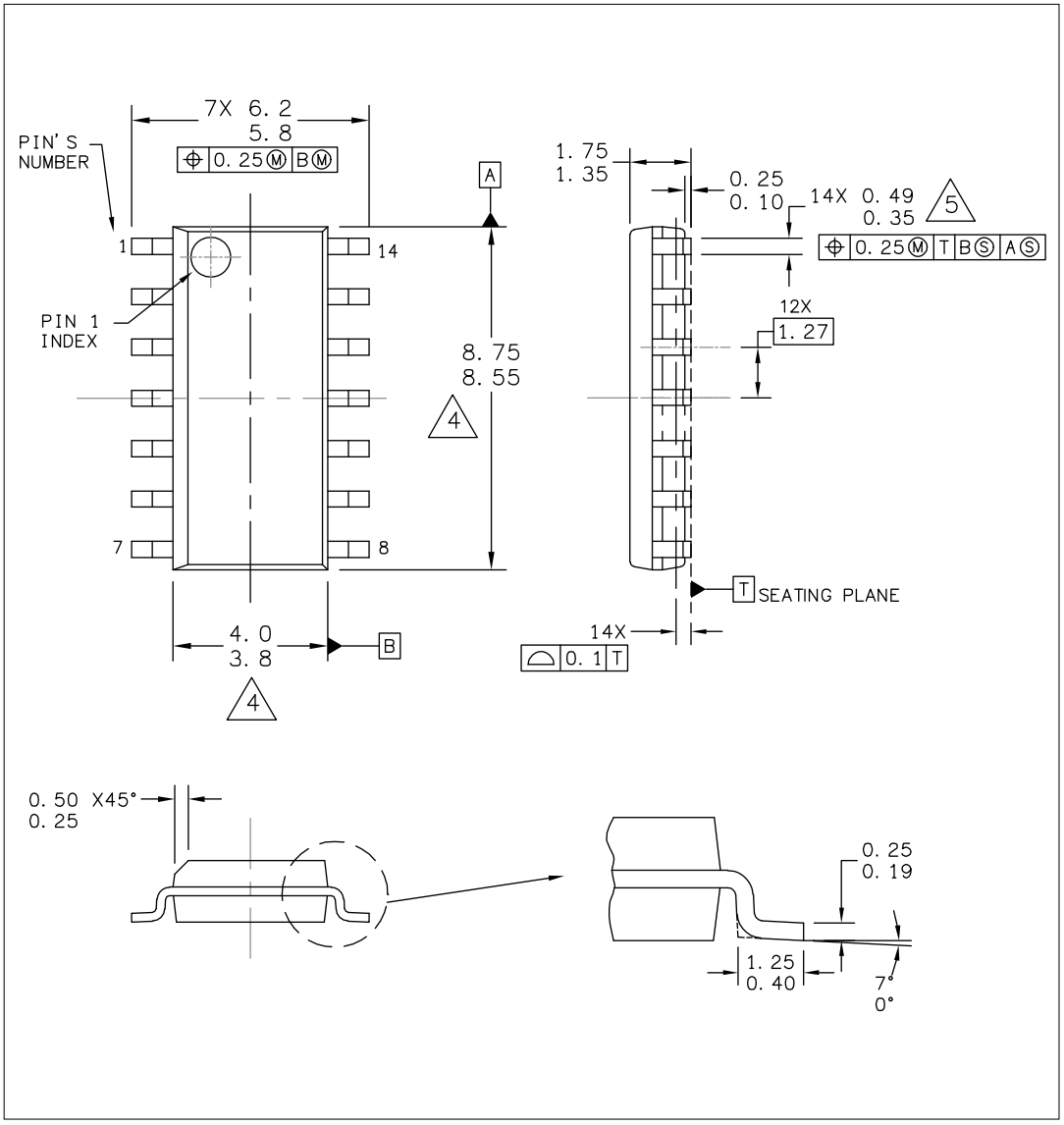


Figure 8. 33897 Typical Application Schematic

PACKAGING

PACKAGE DIMENSIONS

Important: For the most current Package revision, visit www.freescale.com and perform a Keyword Search on the 98ASB42565B drawing number below. Dimensions shown are provided for reference ONLY.



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TITLE: 14LD SOIC N/B, 1.27 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASB42565B	REV: J
	CASE NUMBER: 751A-04	04 DEC 2007
	STANDARD: JECDEC MS-012AB	

EF (Pb-FREE) SUFFIX
14-pin SOICN
98ASB42565B
ISSUE J

33897

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY. DATUM T IS A SURFACE.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTOAL IN EXCESS OF THE LEAD WIDTH AT MAXIMUM MATERIAL CONDITION.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 14LD SOIC N/B, 1.27 PITCH CASE–OUTLINE	DOCUMENT NO: 98ASB42565B	REV: J
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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
9.0	5/2005	• Converted to Freescale format • Added A & B Versions • Updated Device Variation Table, and Note "* Recommended device for all new designs" • Added EF (Pb-Free) Devices, and higher soldering temperature
10.0	8/2005	• Implemented Revision History page • Updated Simplified Application Diagrams • Updated Typical Application Schematic
11.0	12/2005	• Added 33897C and D versions and Timing Diagrams
12.0	1/2006	• Updated Table 4, Static Electrical Characteristics - LOAD and BUS parameters • Updated Ordering Information.
13.0	6/2006	• Removed "Unless otherwise noted" from Static Electrical Characteristics & Dynamic Electrical Characteristics table introductions
14.0	8/2006	• Added Part Numbers MC33897TD and MC33897TEF to Ordering Information on Page 1. • Added 33897T to Table 1, Device Variations on Page 3, Referencing Electrical Changes per Errata MC33897TER, Revision 3 and specifying ESD variations
15.0	10/2006	• Removed Part Numbers MC33897TD/R2, MC33897TEF/R2, MC33897CLEF/R2, PC33897CLEF/R2, MC33897DLEF/R2, and PC33897DLEF/R2 • Added Part Numbers MCZ33897EF/R2, MCZ33897TEF/R2, MCZ33897AEF/R2, MCZ33897CEF/R2, MCZ33897BEF/R2, and MCZ33897DEF/R2 to the Ordering Information block on Page 1. • Updated Device Variations on page 2 for "T" suffix products • Split out Human Body Model on page 5 to differentiate between T and non-T versions • Added Under-voltage Hysteresis on page 6 • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 5. Added note with instructions to obtain this information from www.freescale.com.
16.0	6/2007	• Removed watermark, "Advance Information" from page 1.
17.0	1/2011	• Improved HBM ESD All Pins Except BUS to ±2.0 kV on MC33897CT • Added MC33897CTEKF/R2 to the ordering information • Removed all 8-Pin SOICN device information • Changed Short-circuit BUS Output Current to -100 mA (Approved by GM)
18.0	4/2012	• Updated Quiescent Current I_{QSLP} to 60 μA max.

How to Reach Us:

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4/2012

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