Two-Channel SATA 6-Gb/s Redriver

Check for Samples: SN75LVCP601

FEATURES

- **1.5-, 3-, or 6-Gbps Two-Channel Redriver**
- **Integrated Output Squelch**
- **Programmable Rx/Tx Equalization and De-Emphasis Width Control**
- **Power-Save Feature Lowers Power by >80% in Auto Low-Power Mode**
- **Low Power**
  - **<220 mW Typ.**
  - **<50 mW (in Auto Low-Power Mode)**
  - **<5 mW (in Standby Mode)**
- **Excellent Jitter and Loss Compensation Capability to Over 24-Inch (61-cm) FR4 Trace**
- **20-Pin 4-mm × 4-mm QFN Package**
- **High Protection Against ESD Transient**
  - **HBM: 10,000 V**
  - **CDM: 1,500 V**
  - **MM: 200 V**
- **Pin-Compatible to LVCP412A and MAX4951**

APPLICATIONS

- **Notebooks, Desktops, Docking Stations, Servers, and Workstations**

DESCRIPTION

The SN75LVCP601 is a dual-channel, single-lane SATA redriver and signal conditioner supporting data rates up to 6 Gbps. The device complies with SATA physical link 2m and 3i specifications. The SN75LVCP601 operates from a single 3.3-V supply and has 100-Ω line termination with a self-biasing feature, making the device suitable for ac coupling. The inputs incorporate an out-of-band (OOB) detector, which automatically squelches the output while maintaining a stable common-mode voltage compliant to the SATA link. The device design also handles spread-spectrum clocking (SSC) transmission per the SATA specification.

The SN75LVCP601 handles interconnect losses at both its input and output. The input stage of each channel offers selectable equalization settings that are programmable to match the loss in the channel. The differential outputs provide selectable de-emphasis to compensate for the expected distortion that the SATA signal experiences. The level of equalization and de-emphasis settings depends on the length of interconnect and its characteristics. The setting of signal control pins EQ1, EQ2, DE1, and DE2 controls both equalization and de-emphasis levels.

The device is hot-plug capable (requires the use of ac-coupling capacitors at differential inputs and outputs), preventing device damage under device *hot*-insertion, such as async signal plug or removal, unpowered plug or removal, powered plug or removal, or surprise plug or removal.

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
SN75LVCP601RTJR	LVC601	20-pin RTJ, reel (large)
SN75LVCP601RTJT	LVC601	20-pin RTJ, reel (small)

(1) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

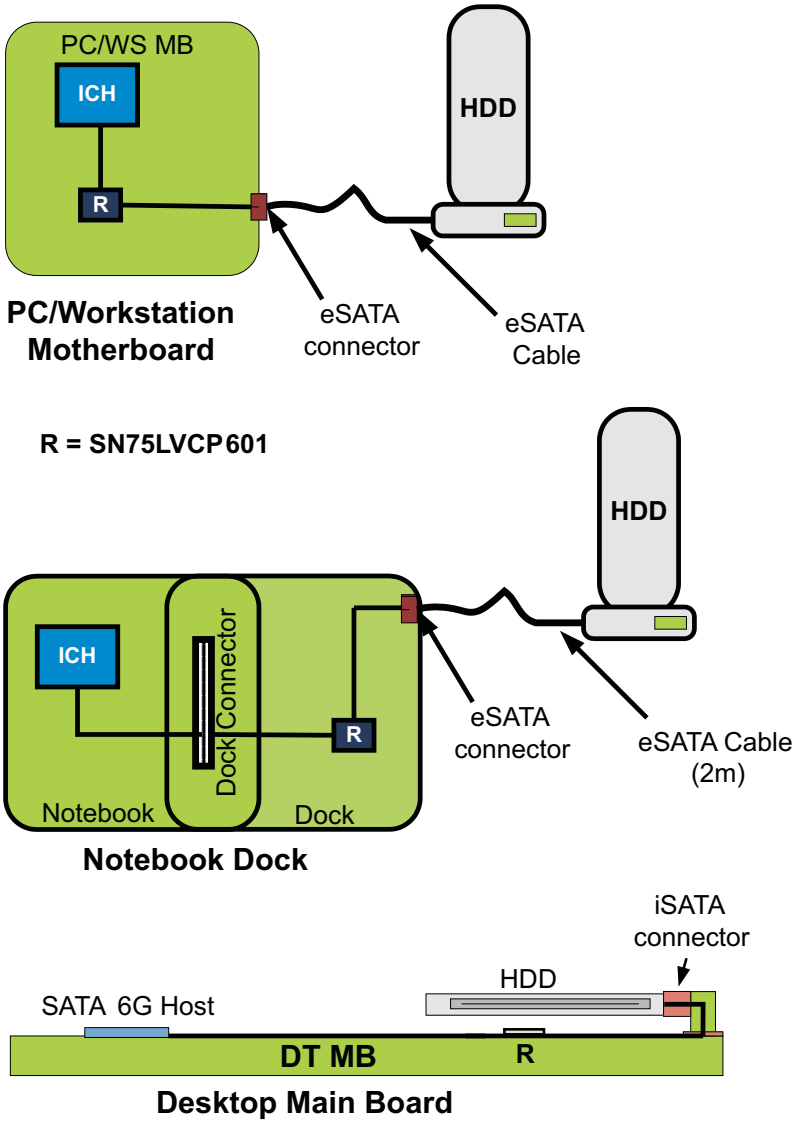

Figure 1. Typical Application

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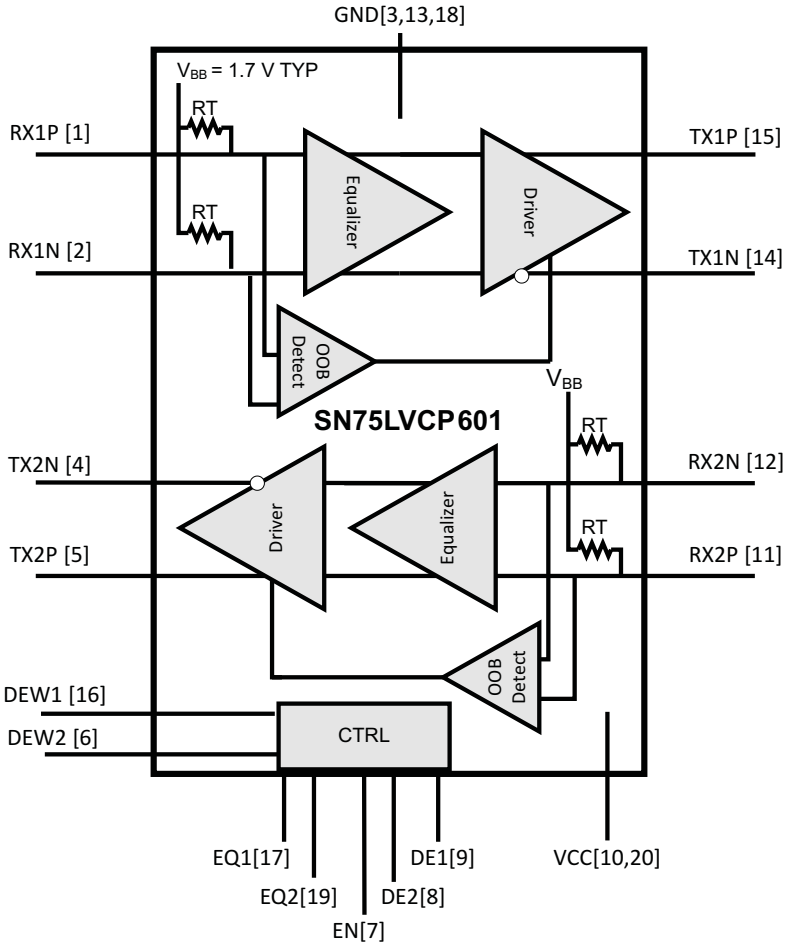

Figure 2. Data Flow Block Diagram

PIN TABLE

NAME	PIN	DESCRIPTION	NAME	PIN	DESCRIPTION
RX1P	1	Input 1, non-inverting	RX2P	11	Input 2, non-inverting
RX1N	2	Input 1, inverting	RX2N	12	Input 2, inverting
GND	3	Ground	GND	13	Ground
TX2N	4	Output 2, inverting	TX1N	14	Output 1, inverting
TX2P	5	Output 2, non-inverting	TX1P	15	Output 1, non-inverting
DEW2 (1)	6	De-emphasis width cntrl.-CH 2	DEW1 (1)	16	De-emphasis width cntrl.-CH 1
EN (1)	7	Enable	EQ1 (2)	17	EQ control CH 1
DE2 (2)	8	De-emphasis CH2	GND	18	Ground
DE1 (2)	9	De-emphasis CH1	EQ2 (2)	19	EQ control CH 2
Vcc	10	3.3-V supply	Vcc	20	3.3-V supply

(1) DEW1, DEW2, and EN tied to Vcc via internal PU resistor
(2) DE1, DE2, EQ1, EQ2 connect to Vcc / 2 via internal resistor

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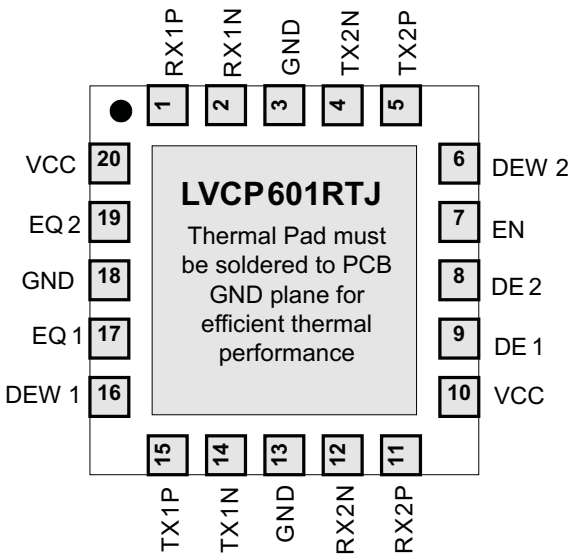
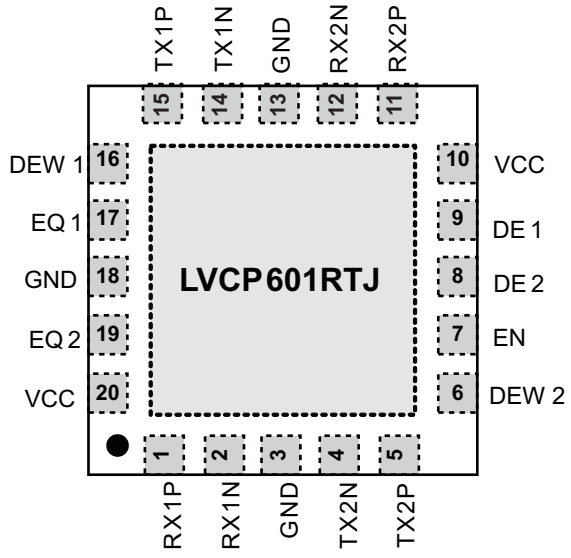
PACKAGE PINOUT

Bottom View



Top View



PIN FUNCTIONS

PIN		PIN TYPE	DESCRIPTION
NO.	NAME		
HIGH-SPEED DIFFERENTIAL I/O			
2	RX1N	I, CML	Non-inverting and inverting CML differential input for CH 1 and CH 2. These pins connect to an internal voltage bias via a dual-termination resistor circuit.
1	RX1P	I, CML	
12	RX2N	I, CML	
11	RX2P	I, CML	
14	TX1N	O, VML	Non-inverting and inverting VML differential output for CH 1 and CH 2. These pins connect internally to voltage bias via termination resistors.
15	TX1P	O, VML	
4	TX2N	O, VML	
5	TX2P	O, VML	
CONTROL PINS			
7	EN	I, LVCMOS	Device enable/disable pin, internally pulled to V_{CC}. See Table 2.
8, 9	DE1, DE2 (1)	I, LVCMOS	Selects de-emphasis settings for CH 1 and CH 2 per Table 1. Internally tied to V_{CC} / 2
17, 19	EQ1, EQ2 (1)	I, LVCMOS	Selects equalization settings for CH 1 and CH 2 per Table 1. Internally tied to V_{CC} / 2
16, 6	DEW1, DEW2	I, LVCMOS	De-emphasis width control for CH 1 and CH 2. See Table 2.
POWER			
10, 20	Vcc	Power	Positive supply should be 3.3 V ± 10%.
3, 13, 18	GND	Power	Supply ground

(1) Internally biased to Vcc/2 with >200-kΩ pullup/pulldown. When 3-state pins are left as NC, board leakage at the pin pad must be <1 µA; otherwise, drive to Vcc/2 to assert mid-level state.

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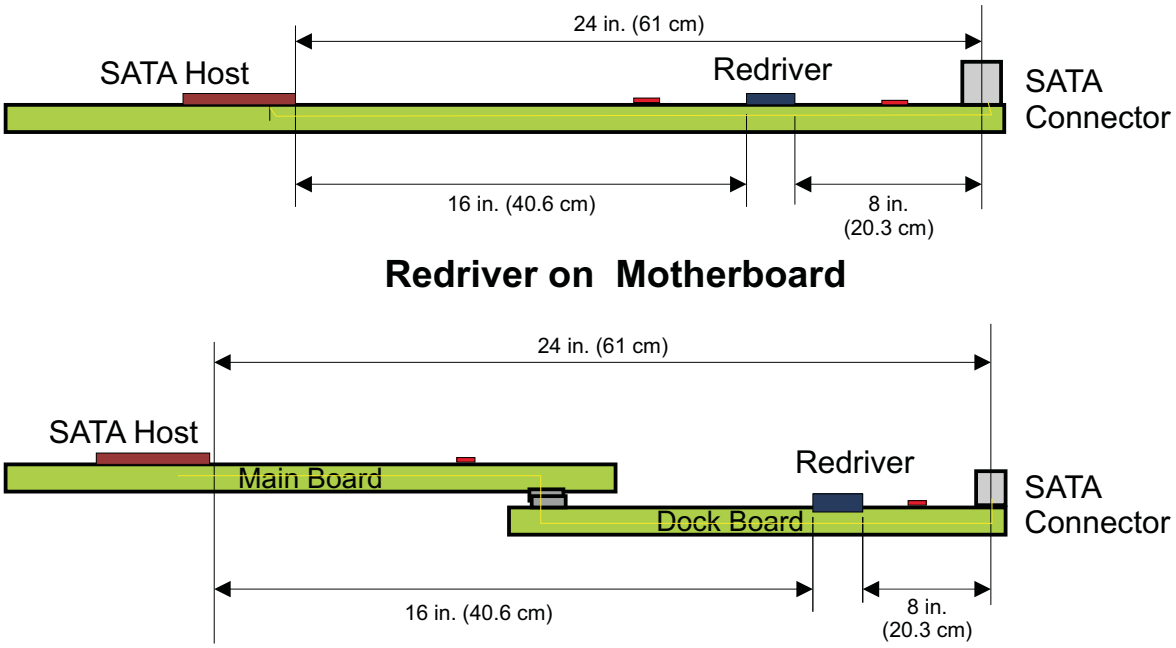
Table 1. Tx/Rx EQ and DE Pulse-Duration Settings

DE1 or DE2	CH1 or CH2 De-Emphasis dB (at 6Gbps)	EQ1 or EQ2	CH1 or CH2 Equalization dB (at 6Gbps)
NC (***default***)	–4	NC (***default***)	0
0	0	0	7
1	–2	1	14

DEW1 or DEW2	Device Function → DE Width for CH1/CH2
0	De-emphasis pulse duration, short
1 (***default***)	De-emphasis pulse duration, long

Table 2. Control Pin Settings

EN	Device Function → Standby Mode
0	Device in standby mode
1 (***default***)	Device enabled



NOTE: *Suggested trace-length values are values based on TI spice simulations (done over programmable limits of input EQ and output de-emphasis) to meet SATA loss and jitter spec.

Actual trace length supported by the LVCP601 may be more or less than suggested values and depends on board layout, trace widths, and number of connectors used in the SATA signal path.

Figure 3. Trace Length Example* for LVCP601

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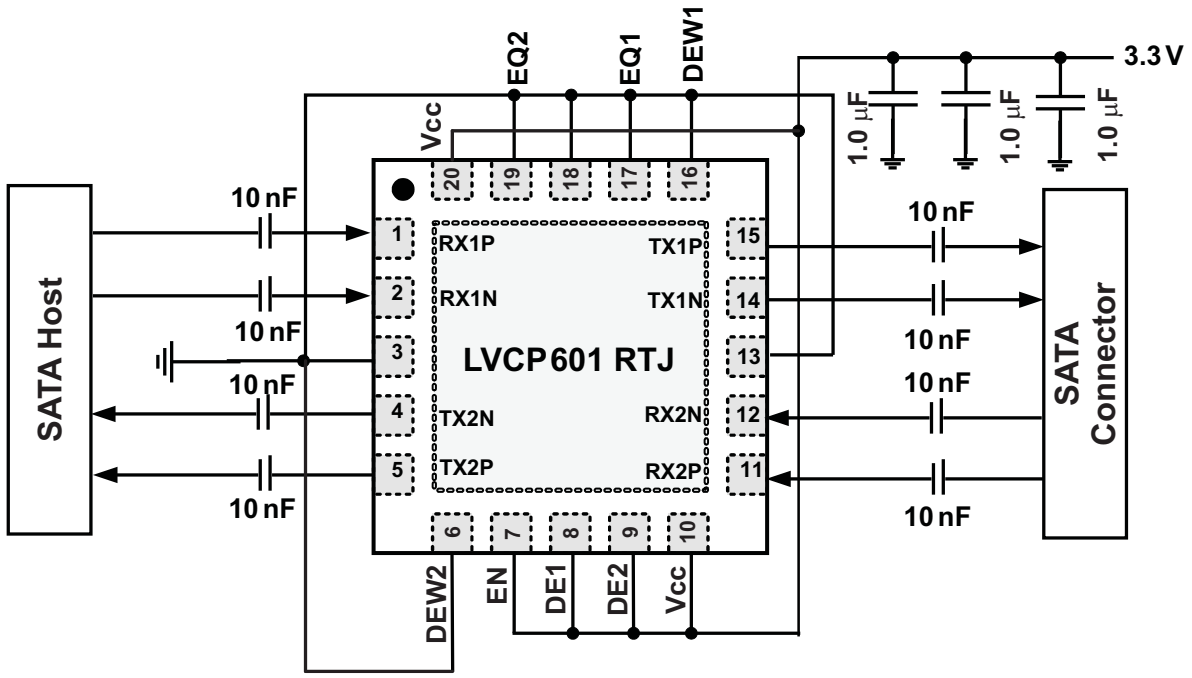

(1) Place supply capacitors close to device pin.

(2) With no external control is implemented, one can leave EN open or tie it to the supply .

(3) Output de-emphasis setting is for –2 dB, EQ for 7 dB, and DE duration for SATA I/II/III operation for both channels.

(4) Actual EQ/DE duration settings depend on device placement relative to host and SATA connector.

Figure 4. Typical Device Implementation

OPERATION DESCRIPTION

INPUT EQUALIZATION

Each differential input of the SN75LVCP601 has programmable equalization in its front stage. Table 1 shows the equalization. The input equalizer design recovers a signal even when no eye is present at the receiver, and effectively supports FR4 trace at the input anywhere from 4 in. (10.2 cm) to 20 in. (50.8 cm) at SATA 6G speed.

OUTPUT DE-EMPHASIS

The SN75LVCP601 provides the de-emphasis settings shown in Table 1. De-emphasis control is independent for each channel, controlled by the DE1 and DE2 pin settings as shown in Table 1. The reference for the de-emphasis settings available in the device is the transition bit amplitude for each given configuration; this transition bit amplitude is different at 0 dB than the –2-dB and –4-dB settings by design. DEW1 and DEW2 control the DE durations for channels one and two, respectively. Table 1 lists the recommended settings for these control pins. Output de-emphasis is capable of supporting FR4 trace at the output anywhere from 2 in. (5.1 cm) to 12 in. (30.5 cm) at SATA 3G/6G speed.

LOW-POWER MODE

There are two low-power modes supported by the SN75LVCP601, listed as follows:

1. Standby mode (triggered by the EN pin, EN = 0 V)
   - The enable (EN) pin controls th low-power mode. Pulling this pin LOW puts the device in standby mode within 2 µs (max). In this mode, the device drives all its active components to their quiescent level, and differential outputs Hi-Z (open). Maximum power dissipation in this mode is 5 mW. Exiting from this mode to normal operation requires a maximum latency of 5 µs.
2. Auto low-power mode (triggered when a given channel is in the electrically idle state for more than 100 µs and EN = Vcc)

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– The device enters and exits low-power mode by actively monitoring the input signal (VIDp-p) level on each of its channels independently. When the input signal on either or both channels is in the electrically idle state, that is, VIDp-p < 50 mV and stays in this state for >100 µs, the associated channel enters into the low-power state. In this state, output of the associated channel goes to VCM and the device selectively shuts off some circuitry to lower power by >80% of its normal operating power. Exit time from the auto low-power mode is <50 ns.

Out-of-Band (OOB) SUPPORT

The squelch detector circuit within the device enables full detection of OOB signaling as specified in the SATA specification. The device does not detect differential signal amplitude at the receiver input of 50 mVpp or less an activity, and hence does not passed it to the output. The device detects differential signal amplitude of 150 mVp-p or more as an activity and therefore passes it to the output, providing an indication of the activity. Squelch circuit ON or OFF time is 5 ns, maximum. While in squelch mode, outputs are held to VCM.

DEVICE POWER

The design of SN75LVCP601 is for operation from a single 3.3-V supply. Always practice proper power-supply sequencing procedure. Apply Vcc first, before application of any input signals to the device. The power-down sequence is in reverse order.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
Supply voltage range(2)	V_{CC}	–0.5 to 4	V
Voltage range	Differential I/O	–0.5 to 4	V
	Control I/O	–0.5 to Vcc + 0.5	V
Electrostatic discharge	Human-body model(3)	±10,000	V
	Charged-device model(4)	±1500	V
	Machine model(5)	±200	V
Continuous power dissipation		See Thermal Table	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A.
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

THERMAL INFORMATION

THERMAL METRIC(1)		SN75LVCP601 QFN 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	38	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	40	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	10	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

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THERMAL INFORMATION (continued)

THERMAL METRIC[1]		SN75LVCP601 QFN 20 PINS	UNITS
ψ_{JB}	Junction-to-board characterization parameter[6]	0.9	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	15.2	°C/W
P_D	Device power dissipation in active mode	215 to 288	mW
P_{SD}	Device power dissipation under standby mode	5	mW

(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

(Typical values for all parameters are at V_{CC} = 3.3V and T_A = 25°C. All temp limits are specified by design)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage		3	3.3	3.6	V
$C_{COUPLING}$	Coupling capacitor			12		nF
	Operating free-air temperature		0		85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
P_D	Power dissipation in active mode	DEWx = EN = Vcc, EQx = DEx = NC, K28.5 pattern at 6 Gbps, V_{ID} = 700 mV_{p-p}		215	288	mW
P_{SD}	Power dissipation in standby mode	EN = 0 V, DEWx = EQx = DEx = NC, K28.5 pattern at 6 Gbps, V_{ID} = 700 mV_{p-p}			5	mW
I_{CC}	Active-mode supply current	EN = 3.3 V, DEWx = 0 V, EQx = DEx = NC, K28.5 pattern at 6 Gbps, V_{ID} = 700 mV_{p-p}		65	80	mA
I_{CC_ALP}	Acive power-save mode I_{CC}	When device is enabled and auto low-power conditions are met		6.5	10	mA
I_{CC_STDBY}	Standby mode supply current	EN = 0 V			1	mA
	Maximum data rate			1	6	Gbps
t_{PDelay}	Propagation delay	Measured using K28.5 pattern. See Figure 8.		323	400	ps
$AutoLP_{ENTRY}$	Auto low-power entry time	Electrical idle at input; see Figure 9.	80	105	130	µs
$AutoLP_{EXIT}$	Auto low-power exit time	After first signal activity; see Figure 9.		42	50	ns
t_{ENB}	Device enable time	EN 0 → 1			5	µs
t_{DIS}	Device disable time	EN 1 → 0			2	µs

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT-OF-BAND (OOB)						
V_{OOB}	Input OOB threshold	f = 750 MHz	50	78	150	mVpp
$D_{VdiffOOB}$	OOB differential delta				25	mV
D_{VCMOOB}	OOB common-mode delta				50	mV
t_{OOB1}	OOB mode enter	See Figure 9.		3	5	ns
t_{OOB2}	OOB mode exit			3	5	ns
CONTROL LOGIC						
V_{IH}	Input high voltage	For all control pins	1.4			V
V_{IL}	Input low voltage				0.5	V
VIN_{HYS}	Input hysteresis			115		mV
I_{IH}	High-level input current	EQx, DEx = Vcc			30	µA
		EN, DEWx = Vcc			1	
I_{IL}	Low-level input current	EQx, DEx = GND	–30			µA
		EN, DEWx = GND	–10			
RECEIVER AC/DC						
Z_{DIFFRX}	Differential-input impedance		85	100	115	Ω
Z_{SERX}	Single-ended input impedance		40			Ω
VCM_{RX}	Common-mode voltage			1.8		V
RL_{DiffRX}	Differential-mode return loss (RL)	f = 150 MHz–300 MHz	18	28		dB
		f = 300 MHz–600 MHz	14	17		
		f = 600 MHz–1.2 GHz	10	12		
		f = 1.2 GHz–2.4 GHz	8	9		
		f = 2.4 GHz–3 GHz	3	9		
$RX_{DiffRLSlope}$	Differential-mode RL slope	f = 300 MHz–6 GHz (See Figure 5.)		–13		dB/dec
RL_{CMRX}	Common-mode return loss	f = 150 MHz–300 MHz	5	10		dB
		f = 300 MHz–600 MHz	5	17		
		f = 600 MHz–1.2 GHz	2	23		
		f = 1.2 GHz–2.4 GHz	1	16		
		f = 2.4 GHz–3 GHz	1	12		
V_{diffRX}	Differential input voltage PP	f = 1.5 GHz and 3 GHz	120		1600	mVppd
IB_{RX}	Impedance balance	f = 150 MHz–300 MHz	30	41		dB
		f = 300 MHz–600 MHz	30	38		
		f = 600 MHz–1.2 GHz	20	32		
		f = 1.2 GHz–2.4 GHz	10	26		
		f = 2.4 GHz–3 GHz	10	25		
		f = 3 GHz–5 GHz	4	20		
		f = 5 GHz–6.5 GHz	4	17		
$t_{20\text{-}80RX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal. SATA 6-Gbps speed measured 1 in, (2.5 cm) from device pin	62		75	ps
t_{skewRX}	Differential skew	Difference between the single-ended midpoint of the RX+ signal rising or falling edge, and the single-ended midpoint of the RX– signal falling or rising edge			30	ps

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSMITTER AC/DC						
Z_{diffTX}	Pair differential impedance		85	100	122	Ω
Z_{SETX}	Single-ended impedance		40			Ω
$V_{TXtrans}$	Sequencing transient voltage	Transient voltages on the serial data bus during power sequencing (lab load)	–1.2		1.2	V
RL_{DiffTX}	Differential-mode return loss	f = 150 MHz–300 MHz	14	24		dB
		f = 300 MHz–600 MHz	8	19		
		f = 600 MHz–1.2 GHz	6	14		
		f = 1.2 GHz–2.4 GHz	6	10		
		f = 2.4 GHz–3 GHz	3	10		
$TX_{DiffRLSlope}$	Differential-mode RL slope	f = 300 MHz–3 GHz (SeeFigure 5.)		–13		dB/dec
RL_{CMTX}	Common-mode return loss	f = 150 MHz–300 MHz	5	20		dB
		f = 300 MHz–600 MHz	5	19		
		f = 600 MHz–1.2 GHz	2	17		
		f = 1.2 GHz–2.4 GHz	1	12		
		f = 2.4 GHz–3.0 GHz	1	11		
IB_{TX}	Impedance balance	f = 150 MHz–300 MHz	30	41		dB
		f = 300 MHz–600 MHz	30	38		
		f = 600 MHz–1.2 GHz	20	33		
		f = 1.2 GHz–2.4 GHz	10	24		
		f = 2.4 GHz–3 GHz	10	26		
		f = 3 GHz–5 GHz	4	22		
		f = 5 GHz–6.5 GHz	4	21		
DE	Output de-emphasis (relative to transition bit)	f = 3 GHz, DE1 or DE2 = 0		0		dB
		f = 3 GHz, DE1 or DE2 = 1		–2		
		f = 3 GHz, DE1 or DE2 = NC		–4		
$Diff_{VppTX\_DE}$	Differential output-voltage swing dc level	f = 3 GHz, DE1 or DE2 = 0		550		mV
		f = 3 GHz, DE1 or DE2 = 1		830		
		f = 3 GHz, DE1or DE2 = NC		630		
t_{DE}	De-emphasis duration	DEW1 or DEW2 = 0		94		ps
		DEW1 or DEW2 = 1		215		
VCM_{AC_TX}	TX AC CM voltage	At 1.5 GHz		20	50	mVppd
		At 3 GHz		12	26	dBmV (rms)
		At 6 GHz		13	30	
VCM_{TX}	Common-mode voltage			1.8		V
$t_{20\text{-}80TX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal. At 6Gbps under no load conditions	42	55	75	ps
t_{skewTX}	Differential skew	Difference between the single-ended mid-point of the TX+ signal rising or falling edge, and the single-ended mid-point of the TX- signal falling or rising edge.		6	20	ps
TxR/F_{Imb}	TX rise-fall imbalance	At 3 Gbps		6%	20%	
$TxAmp_{Imb}$	TX amplitude imbalance			2%	10%	

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSMITTER JITTER						
DJ_{TX}	Deterministic jitter(1) at CP in Figure 6	VID = 500 mVpp, UI = 333 ps, K28.5 control character		0.06	0.07	UIp-p
RJ_{TX}	Residual random jitter(1)	VID = 500 mVpp, UI = 333 ps, K28.7 control character		0.01	2	ps-rms
DJ_{TX}	Deterministic jitter(1) at CP in Figure 6	VID = 500 mVpp, UI = 167 ps, K28.5 control character		0.08	0.16	UIp-p
RJ_{TX}	Residual random jitter(1)	VID = 500 mVpp, UI = 167 ps, K28.7 control character		0.09	2	ps-rms

(1) TJ = (14.1 × RJ_{SD} + DJ), where RJ_{SD} is one standard deviation value of RJ Gaussian distribution. Jitter measurement is at the SATA connector and includes jitter generated at the package connection on the printed circuit board, and at the board interconnect as shown in Figure 6.

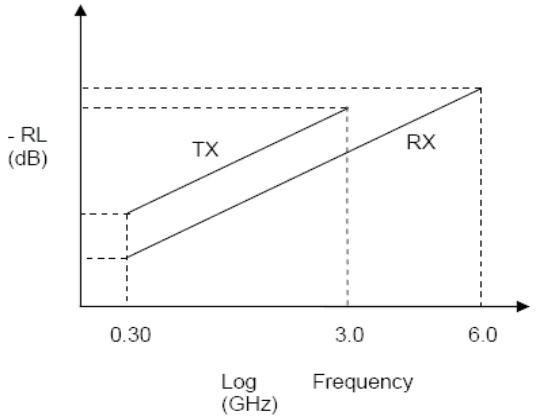

Figure 5. TX, RX Differential Return Loss Limits

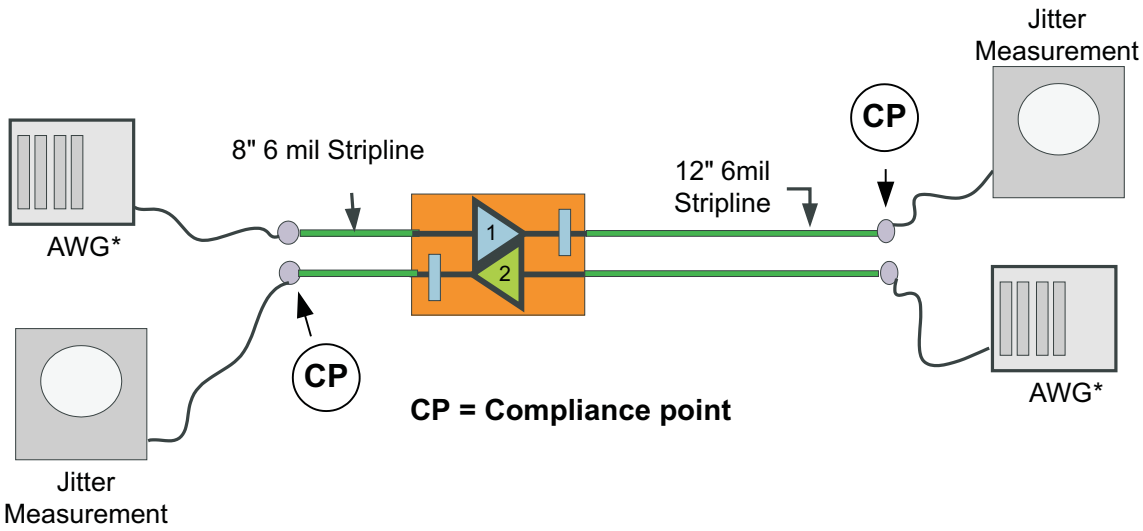

Figure 6. Jitter Measurement Test Condition

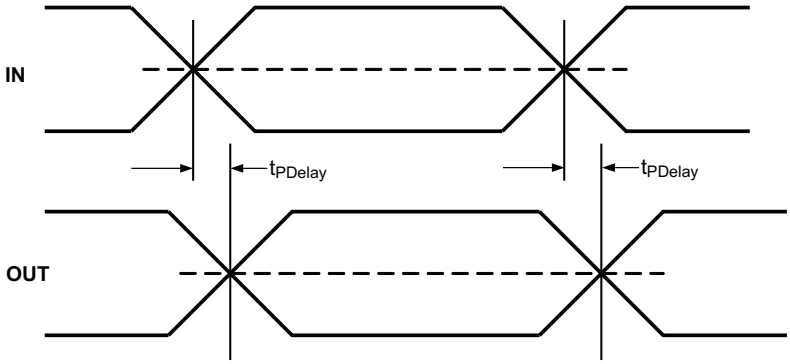

Figure 7. Propagation Delay Timing Diagram

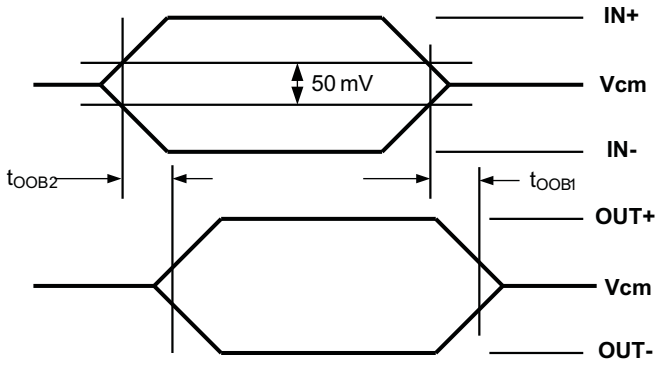

Figure 8. OOB Enter and Exit Timing

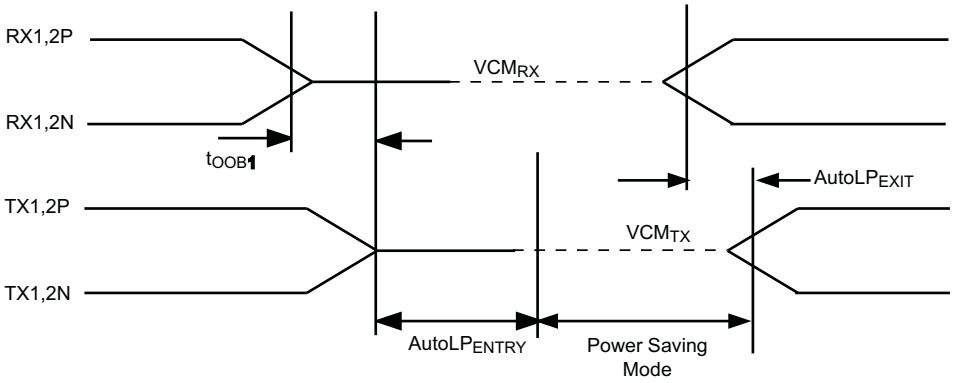

Figure 9. Auto Low-Power Mode Enter and Exit Timing

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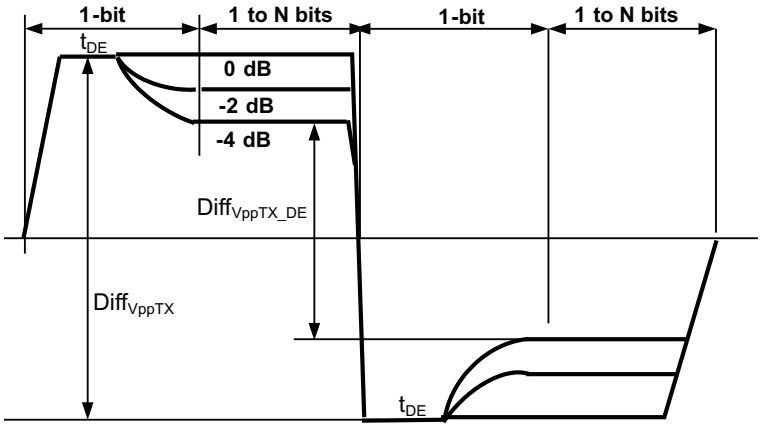


Figure 10. TX Differential Output

SN75LVCP601 TYPICAL PERFORMANCE CURVE

- Input signal characteristics
  - Data rate = 6 Gbps, 3 Gbps, 1.5 Gbps
  - Amplitude = 500 mVp-p
  - Data pattern = K28.5
- SN75LVCP601 device setup
  - Temperature = 25°C
  - Voltage = 3.3 V
  - De-emphasis duration = 117 ps (short)
  - Equalization and de-emphasis set to optimize performance at 6 Gbps

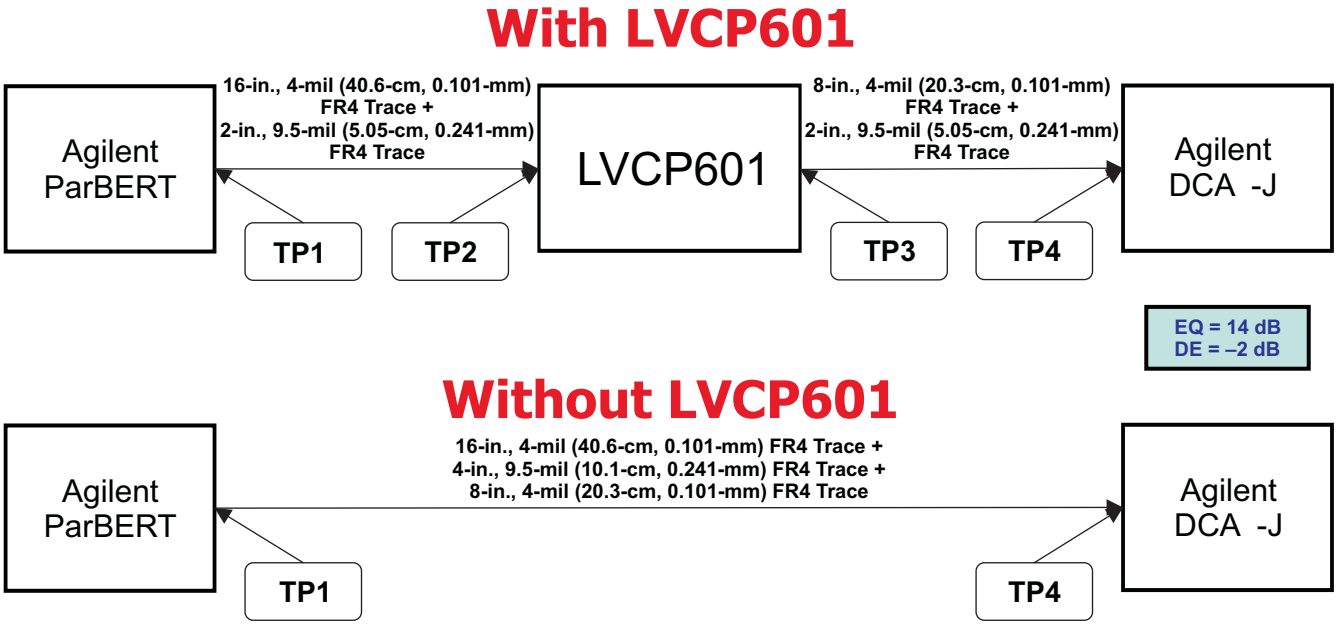


Figure 11. Performance Curve Measurement Setup

SN75LVCP601 TYPICAL PERFORMANCE CURVE (continued)

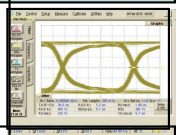
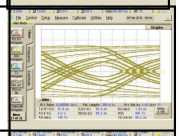
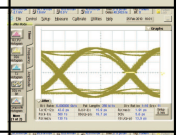
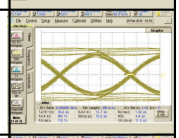
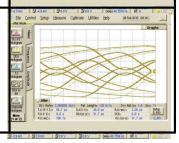
Test Point	TJ (1e-12) ps	DJ (δ-δ) ps	RJ (rms) ps	Eye Amplitude mV	Eye Width ps	Eye Opening mV	Eye Diagram
TP1	29.0	3.3	1.88	412.4	159.2	350.52	
TP2	91.8	65.4	1.93	240	28.9	81.24	
TP3	42.0	15.9	1.91	788.8	141.3	623.02	
TP4 **With** LVCP601	39.0	12.7	1.92	557.1	149.7	459.62	
TP4 **Without** LVCP601	56.7	29.8	2.00	165.4	101	13.24	

Figure 12. Jitter and VOD Results: Case 1 at 6 Gbps

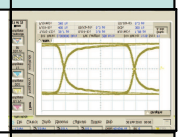
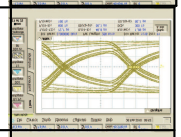
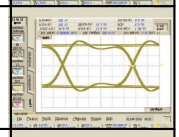
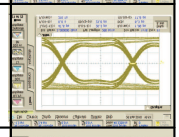
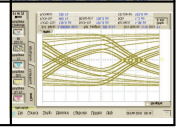
Test Point	TJ (1e-12) ps	DJ (δ-δ) ps	RJ (rms) ps	Eye Amplitude mV	Eye Width ps	Eye Opening mV	Eye Diagram
TP1	29.7	3.8	1.89	430.9	326	392.84	
TP2	72.7	46.8	1.89	314.9	237	222.36	
TP3	39.6	12.8	1.96	714.5	321	611.62	
TP4 **With** LVCP601	47.9	20.3	1.99	615.3	305.0	463.42	
TP4 **Without** LVCP601	128.6	101.8	1.96	258.8	118	122.26	

Figure 13. Jitter and VOD Results: Case 2 at 3 Gbps

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SN75LVCP601 TYPICAL PERFORMANCE CURVE (continued)

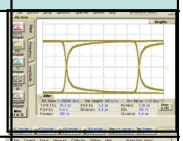
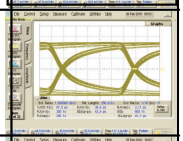
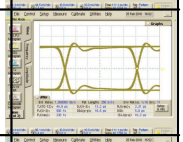
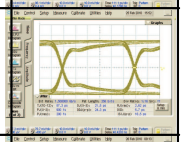
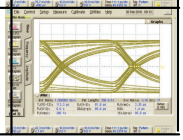
Test Point	TJ (1e-12) ps	DJ (δ-δ) ps	RJ (rms) ps	Eye Amplitude mV	Eye Width ps	Eye Opening mV	Eye Diagram
TP1	34.3	3.4	2.26	448	659	417.28	
TP2	67.5	38.6	2.11	363.4	589	318.48	
TP3	44.9	13.2	2.31	753.1	649	604.02	
TP4 **With** LVCP601	57.3	21.5	2.62	672.8	632.0	442.42	
TP4 **Without** LVCP601	113.3	81.9	2.30	322.8	493	217.46	

Figure 14. Jitter and VOD Results: Case 3 at 1.5 Gbps

TYPICAL CHARACTERISTICS

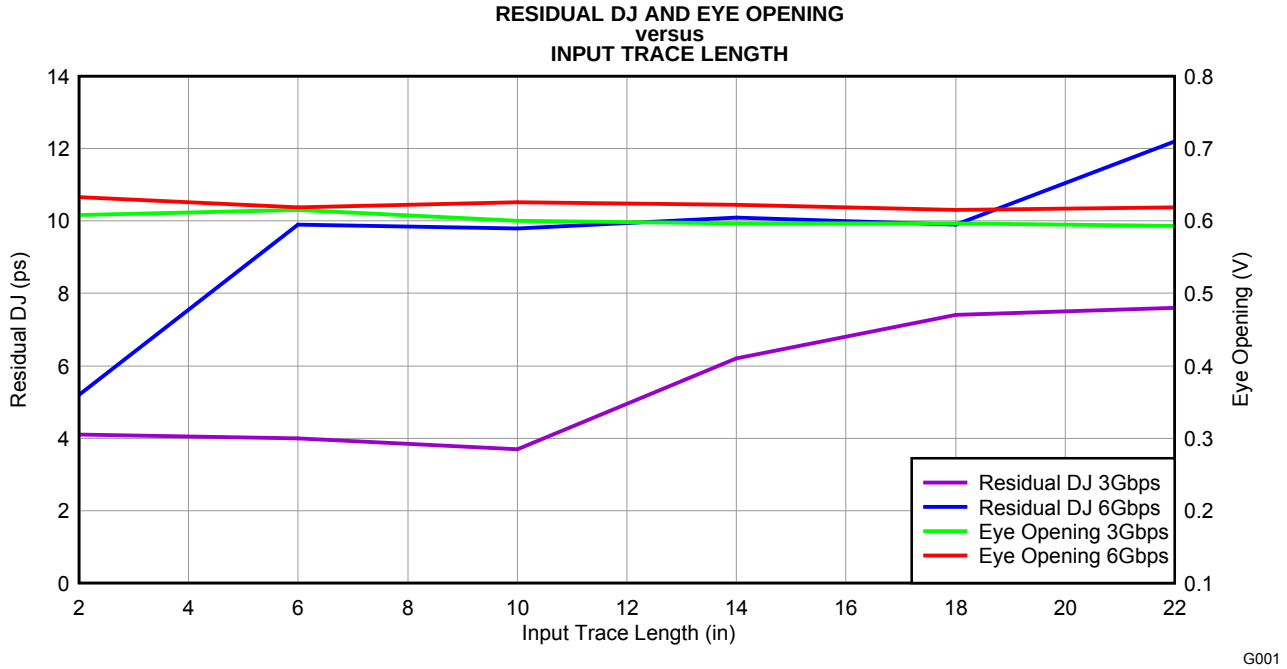


Figure 15.

TYPICAL CHARACTERISTICS (continued)

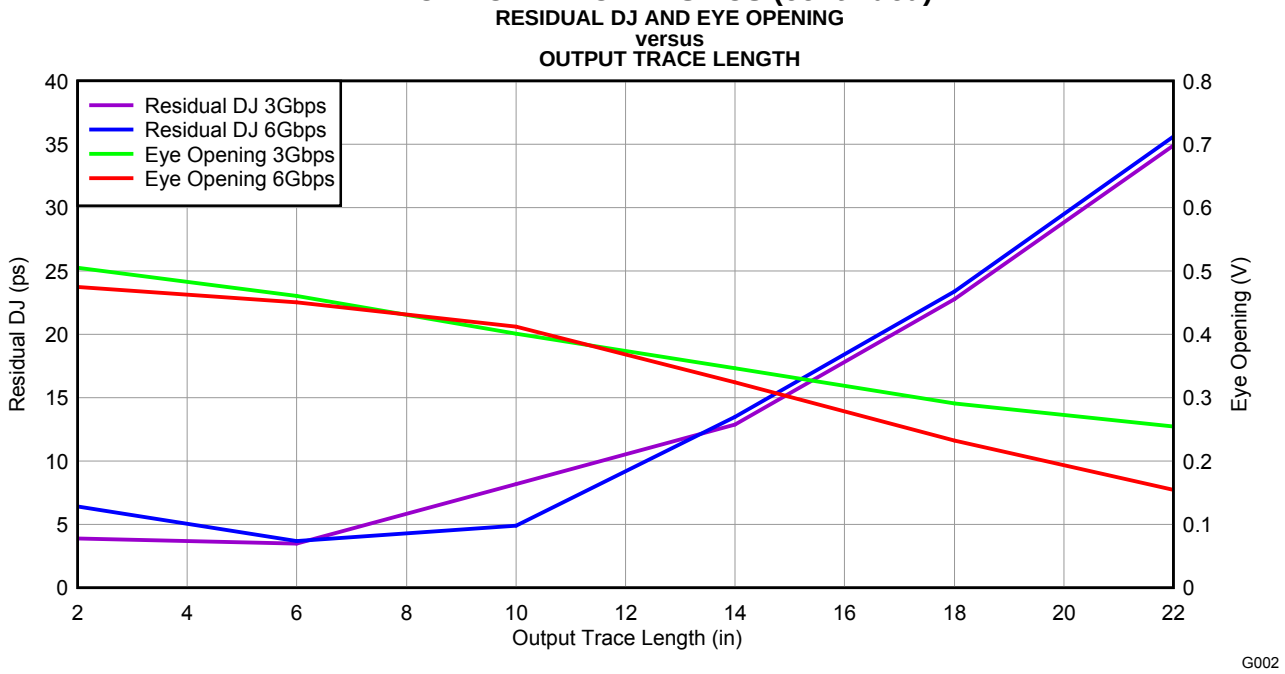


Figure 16.

REVISION HISTORY

Changes from Revision D (January 2013) to Revision E **Page**

- Changed DJ_{TX} (UI = 333 ps) From: Max = 0.19 To: Max = 0.07 11
- Changed DJ_{TX} (UI = 167 ps) From: Max = 0.34 To: Max = 0.16 11

Changes from Revision C (October 2012) to Revision D **Page**

- Corrected formatting of the Differential output-voltage swing dc level section of the Electrical Characteristics table 10

Changes from Revision B (February 2012) to Revision C **Page**

- Deleted setting recommendations on pulse durations for DEW1 and DEW2 5
- Revised text of the Output Ed-Emphasis section 6
- Deleted $Diff_{VppTX}$ row 10
- Inserted $Diff_{VppTX\_DE}$ row 10
- Changed Figure 10 caption 13

Changes from Revision A (October 2011) to Revision B **Page**

- Changed pin type from CML to VML for pins 4, 5, 14, 15 4

Changes from Original (June 2010) to Revision A **Page**

- Changed pin EN number From: 4 To: 7 4

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVCP601RTJR	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	0 to 85	LVC601	Samples
SN75LVCP601RTJT	ACTIVE	QFN	RTJ	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	0 to 85	LVC601	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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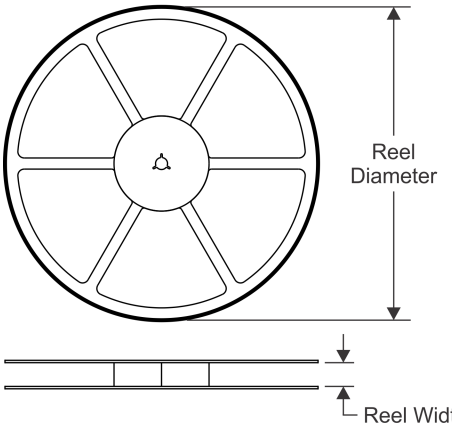
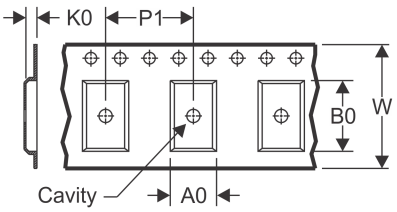
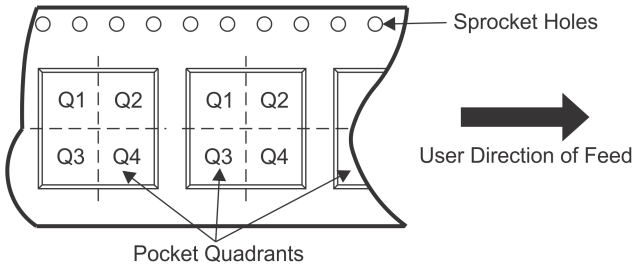


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

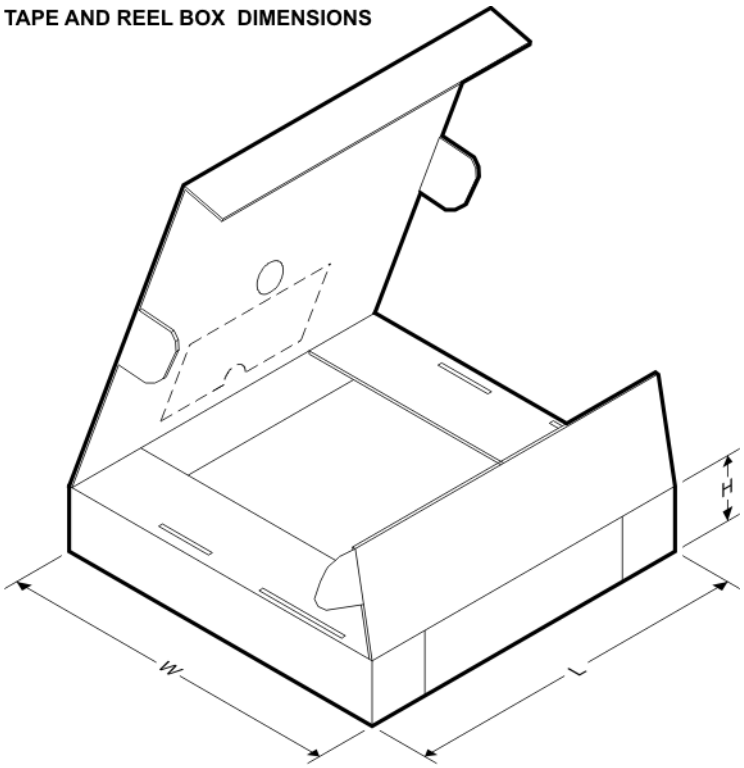
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVCP601RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN75LVCP601RTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

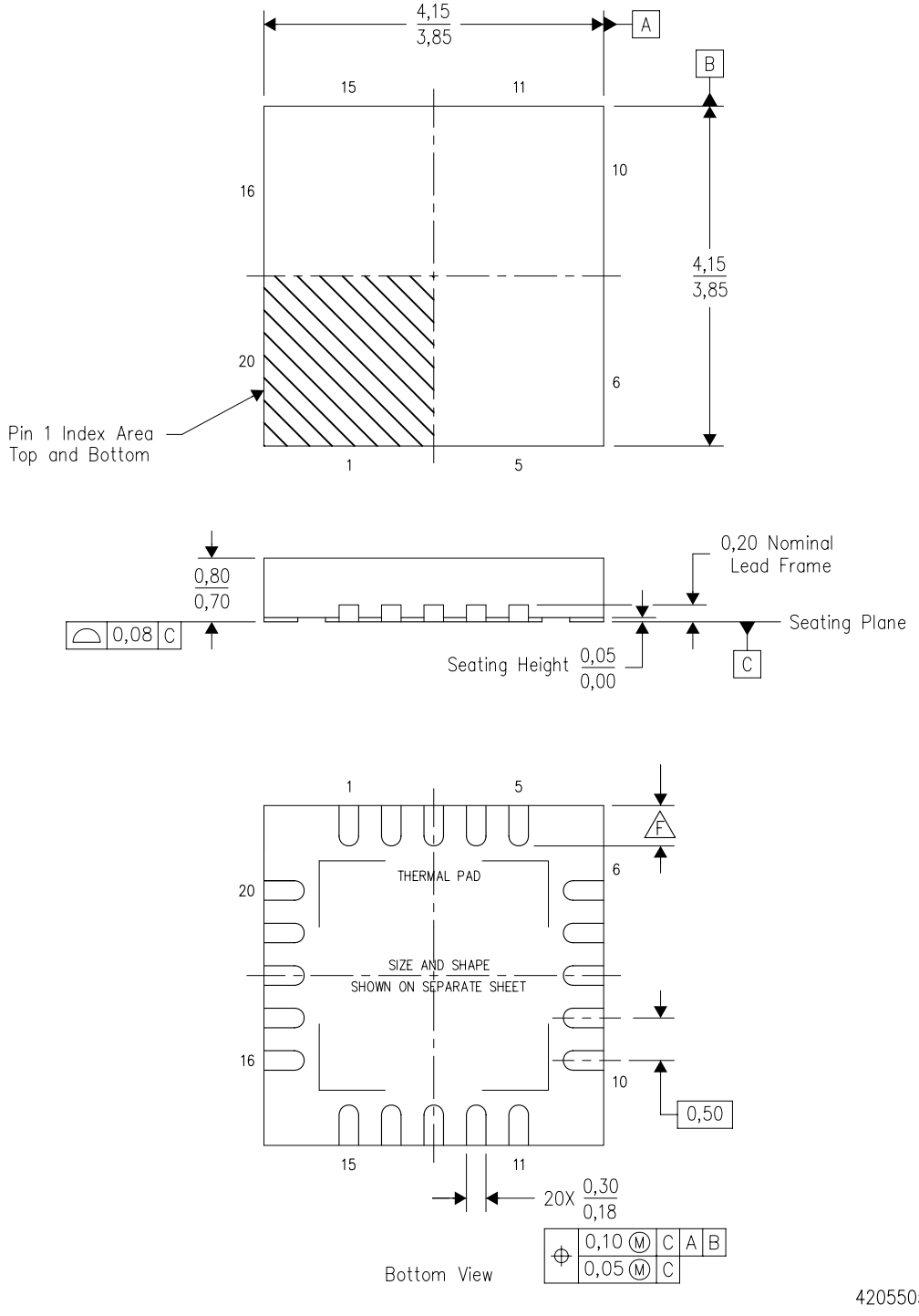
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVCP601RTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
SN75LVCP601RTJT	QFN	RTJ	20	250	210.0	185.0	35.0

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

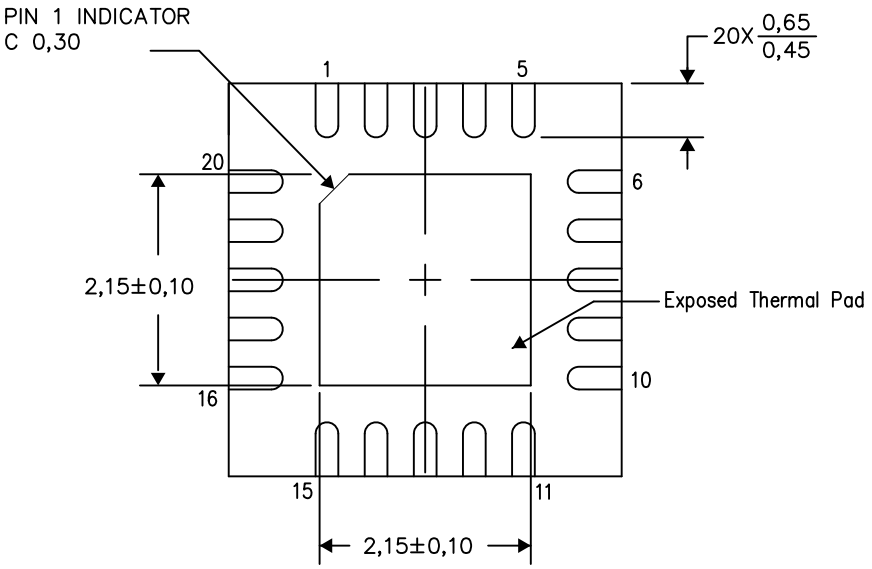
RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



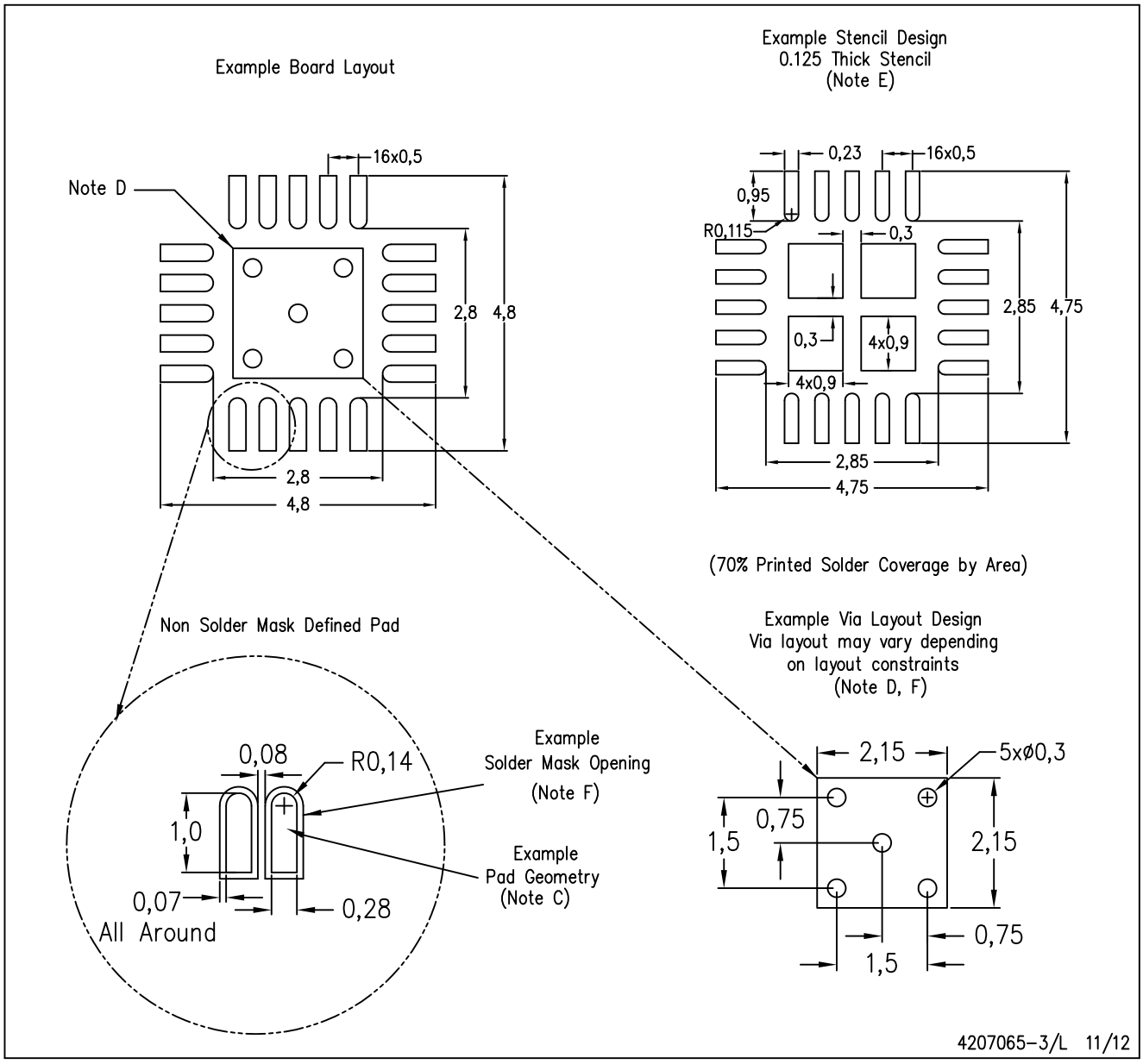
Bottom View

Exposed Thermal Pad Dimensions

4206256–3/S 08/13

NOTE: All linear dimensions are in millimeters

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com