# 50 mA, 3 V TO 50 V, MICROPOWER, LOW-DROPOUT LINEAR REGULATOR

**Check for Samples: TPS79801-Q1, TPS79850-Q1**

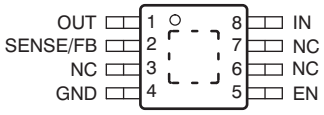
## FEATURES

- **Qualified for Automotive Applications**
- **Wide Input Voltage Range: 3 V to 50 V**
- **Low Quiescent Current: 40 µA (Typ)**
- **Low Dropout Voltage: 300 mV (Typ)**
- **Output Current: 50 mA**
- **No Input Protection Diodes Needed**
- **Adjustable Output From 1.275 V to 28 V**
- **1-µA Quiescent Current in Shutdown**
- **Stable With 1-µF Output Capacitor**
- **Stable With Aluminum, Tantalum, or Ceramic Capacitors**
- **Reverse Input-Battery Protection**
- **Reverse Output Current Flow Protection**
- **Thermal Limiting**
- **Available in MSOP-8 Package**

## APPLICATIONS

- **Low-Current, High-Voltage Regulators**
- **Regulators for Battery-Powered Systems**
- **Telecom**
- **Automotive**

**DGN PACKAGE**
**MSOP-8 PowerPAD™**
**(TOP VIEW)**




Note: The exposed thermal pad is connected to ground via pin 4 (GND).

## DESCRIPTION

The TPS798xx is the first device in a line of 50-V high-voltage micropower low-dropout (LDO) linear regulators. This device is capable of supplying 50-mA output current with a dropout voltage of only 300 mV. Designed for low quiescent current high voltage (50 V) applications, 40 µA operating and 1 µA in shutdown makes the TPS798xx an ideal choice for battery-powered or high-voltage systems. Quiescent current is also well-controlled in dropout.

Other features of the TPS798xx include the ability to operate with low equivalent series resistance (ESR) ceramic output capacitors. This device is stable with only 1 µF on the output; most older devices require between 10-µF and 100-µF tantalum capacitors for stability. Small ceramic capacitors can be used without the necessary addition of ESR, as is common with other regulators. Internal protection circuitry includes reverse input-battery protection, reverse output current protection, current limiting, and thermal limiting to protect the device in various fault conditions.

This device is available in a fixed output voltage of 5 V (TPS79850) and with an adjustable output voltage with a 1.275-V reference voltage (TPS79801). The TPS798xx regulator is available in a 8-lead MSOP (DGN) package with an exposed pad for enhanced thermal management capability.

### ORDERING INFORMATION(1)

| $T_J$ | $V_{OUT}$ (NOM) | PACKAGE(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|---|
| –40°C to 125°C | Adjustable(3) | MSOP – DGN | Reel of 2500 | TPS79801QDGNRQ1 | PMRQ |
| | 5 V | | | TPS79850QDGNRQ1 | OOLQ |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) For fixed 1.275 V, tie FB to out.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

| | | | |
|---|---|---|---|
| $V_{IN}$ | Input voltage range | IN(2) | –65 V to 60 V |
| | | OUT | –0.3 V to 28 V |
| | | FB | –0.3 V to 7 V |
| | | EN(2) | –65 V to 60 V |
| | | Enable to IN differential | 0.6 V < $V_{IN}$ |
| $\theta_{JA}$ | Thermal impedance, junction to free air | JEDEC 51-5(3) | 60°C/W |
| | | JEDEC 51-7(4) | 130°C/W |
| $T_J$ | Junction temperature range(5) | | –40°C to 125°C |
| $T_{STG}$ | Storage temperature range | | –65°C to 150°C |
| | ESD rating | Human-Body Model (HBM) | 2000 V |
| | | Charged-Device Model (CDM) | 1000 V |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient: 500 ms for $V_{IN}$ > 50 V
(3) The thermal data is based on using JEDEC 51-5. The copper pad is soldered to the thermal land pattern and using 5 by 8 thermal array (vias). Correct attachment procedure must be incorporated.
(4) The thermal data is based on using JEDEC 51-7. The copper pad is soldered to the thermal land. No thermal vias. Correct attachment procedure must be incorporated.
(5) The junction temperature must not exceed 125ºC. See Figure 1 to determine the maximum ambient operating temperature versus the supply voltage and load current. The safe operating area curves assume a 50ºC/W thermal impedance and may need to be adjusted to match actual system thermal performance.

## DISSIPATION RATINGS(1)

| BOARD | PACKAGE | $R_{\theta JC}$ | $R_{\theta JA}$ | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A \le 25°C$ POWER RATING | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|---|---|---|
| High-K(2) | DGN | 8.2°C/W | 60°C/W | 16.6 mW/°C | 1.83 W | 1.08 W | 0.833 W |

(1) See Thermal Considerations in the *Applications Information* section for more information related to thermal design.
(2) The JEDEC High-K (1s) board design used to derive this data was a 4.5-inch x 3-inch, 2-layer board with 2-ounce copper traces on top of the board.

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | IN | –65 | 50 | V |
| | | OUT | –0.3 | 28 | |
| | | FB | –0.3 | 7 | |
| | | EN | –65 | 50 | |
| $I_{OUT}$ | Output current | | | 50 | mA |
| $T_J$ | Operating junction temperature(1) (2) (3) | | –40 | 125 | °C |
| $T_A$ | Ambient free-air temperature | | –40 | 105 | °C |

(1) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.
(2) The TPS798xxQ is specified to meet performance specifications from –40°C to 125°C operating junction temperature. Specifications over the full operating junction temperature range are specified by design, characterization, and correlation with statistical process controls.
(3) This device includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature exceeds 125°C (min) when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

## ELECTRICAL CHARACTERISTICS

$V_{IN}$ = $V_{OUT(NOM)}$ + 1.0 V or 4.0 V (whichever is greater for either fixed or adjustable versions), $I_{LOAD}$ = 1.0 mA, $V_{EN}$ = 3.0 V, $C_{OUT}$ = $C_{IN}$ = 2.2 µF (unless otherwise noted). For TPS79801, FB pin tied to $V_{OUT}$. Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | | $T_J$[1] | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Minimum input voltage | $I_{LOAD}$ = 50 mA | | Full range | | 3 | 4 | V |
| Fixed $V_{OUT}$ | Initial output voltage accuracy | $V_{IN}$ = $V_{OUT}$ nom + 0.5 V | | 25°C | -1.5 | | +1.5 | % |
| | Output voltage accuracy over line, load, and full temperature range | $V_{IN}$ = $V_{OUT}$ nom + 1 V to 50 V, $I_{LOAD}$ = 1 mA to 50 mA | | Full range | -3.0 | | +3.0 | |
| Adjustable $V_{OUT}$ | Initial output voltage accuracy | $V_{IN}$ = 3 V | | 25°C | 1.256 | 1.275 | 1.294 | V |
| | Output voltage accuracy over line, load, and full temperature range | $V_{IN}$ = 4 V to 50 V, $I_{LOAD}$ = 1 mA to 50 mA | | Full range | 1.237 | 1.275 | 1.313 | |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation, adjustable $V_{OUT}$ | $\Delta V_{IN}$ = 3 V to 50 V | | Full range | | | 13 | mV |
| | Line regulation, TPS79850 | $V_{IN}$ = $V_{OUT}$ nom + 0.5 V to 50 V | | | | | 15 | |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation, adjustable $V_{OUT}$ | $\Delta I_{LOAD}$ = 1 mA to 50 mA | | 25°C | | | 20 | mV |
| | | | | Full range | | | 32 | |
| | Load regulation, fixed $V_{OUT}$ | $\Delta I_{LOAD}$ = 1 mA to 50 mA | | 25°C | | | 50 | |
| | | | | Full range | | | 90 | |
| Adjustable $V_{OUT}$ | Output voltage range[2] [3] | | | Full range | 1.275 | | 28 | V |
| $V_{DO}$ | Dropout voltage[4] [5] | $V_{IN}$ = $V_{OUT(NOM)}$ – 0.1 V | | 25°C | | 85 | 150 | mV |
| | | | | Full range | | | 190 | mV |
| | | $I_{LOAD}$ = 10 mA, $V_{IN}$ = $V_{OUT(NOM)}$ – 0.1 V | | 25°C | | 170 | 260 | mV |
| | | | | Full range | | | 350 | mV |
| | | $I_{LOAD}$ = 50 mA, $V_{IN}$ = $V_{OUT(NOM)}$ – 0.1 V | | 25°C | | 300 | 370 | mV |
| | | | | Full range | | | 550 | mV |
| $I_{GND}$ | GND pin current[6] | $V_{IN}$ = $V_{OUT(NOM)}$ | $I_{LOAD}$ = 0 mA | Full range | | 30 | 80 | µA |
| | | | $I_{LOAD}$ = 1 mA | Full range | | 100 | 180 | µA |
| | | | $I_{LOAD}$ = 10 mA | Full range | | 400 | 700 | µA |
| | | | $I_{LOAD}$ = 50 mA | Full range | | 1.8 | 3.3 | mA |
| $V_N$ | Output voltage noise | $C_{OUT}$ = 10µF, $I_{LOAD}$ = 50 mA, BW = 10 Hz to 100 kHz, $V_{IN}$ = 4.3 V, $V_{OUT}$ = 3.3 V (adjustable used) | | 25°C | | 100 | | $\mu V_{RMS}$ |
| $I_{FB}$ | FB pin bias current[7] | $V_{IN}$ = 3.0 V | | 25°C | | 0.05 | 0.2 | µA |
| $V_{EN}$ | EN pin high (enabled)[8] | OFF to ON, $V_{IN}$ = 6.0 V | | Full range | | | 1.5 | V |
| | EN pin low (shutdown)[8] | ON to OFF, $V_{IN}$ = 6.0 V | | 25°C | 0.4 V | | | V |
| | EN pin low (shutdown)[8] | ON to OFF, $V_{IN}$ = 6.0 V | | Full range | 0.2 V | | | V |
| $I_{EN}$ | EN pin current[8] | $V_{EN}$ = 0 V $V_{IN}$ = 6.0 V, $I_{LOAD}$ = 0 mA | | Full range | | 0.4 | 2.0 | µA |
| | | $V_{EN}$ = 3 V, $V_{IN}$ = 6.0 V, $I_{LOAD}$ = 0 mA | | Full range | | 0.4 | 0.5 | µA |
| $I_{shutdown}$ | GND pin current[6] | $V_{IN}$ = 6 V, $V_{EN}$ = 0 V, $I_{LOAD}$ = 0 mA | | Full range | | 3 | 25 | µA |
| PSRR | Power-supply rejection ratio | $V_{IN}$ = 4.3 V, $V_{OUT}$ 3.3-V $V_{RIPPLE}$ = 0.5 $V_{PP}$, $f_{RIPPLE}$ = 120 Hz, $I_{LOAD}$ = 50 mA | | 25°C | | 65 | | dB |
| $I_{LIMIT}$ | Fixed current limit[9] | $\Delta V_{OUT}$ = $V_{OUT(NOM)}$ – 0.1 V | | Full range | 60 | | 200 | mA |
| | Adjustable current limit | $\Delta V_{OUT}$ = $V_{OUT(NOM)}$ – 0.1 V | | Full range | 60 | | 200 | mA |

(1) Full range $T_J$ = –40°C to 125°C
(2) This parameter is tested and specified under pulse load conditions such that $T_J$ = $T_A$. This device is 100% production tested at $T_A$ = 25°C. Performance at full range is specified by design, characterization, bench to ATE correlation testing, and other statistical process controls.
(3) This device is limited by a maximum junction temperature of $T_J$ = 125°C. The regulated output voltage specification cannot be applied to all combinations of various $V_{IN}$, $V_{OUT}$, ambient temperature, and $I_{OUT}$ conditions. When operating with large voltage differentials across the device, the output load must be limited so as not to violate the maximum junction temperature for a given ambient temperature.
(4) In the adjustable version test, the output uses an external voltage divider. This resistor voltage divider is made up of $R_1$ = 215 kΩ and R2 (bottom resistor) = 340 kΩ. This configuration preloads the output with 6.0µA.
(5) By definition, dropout voltage is the minimum input voltage needed to maintain a given output voltage at a specific load current. For dropout testing, minimum $V_{IN}$ = $V_{OUT(NOM)}$ × 0.96. This specification ensures that the device is in dropout and takes into account the output voltage tolerance over the full temperature range.
(6) Ground pin current is tested with $V_{IN}$ = $V_{OUT(NOM)}$ or 3 V, whichever is greater.
(7) FB pin current flows into the FB pin.
(8) EN pin current flows into the EN pin.
(9) Current limit is tested with $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 3.0 V, whichever is greater. $V_{OUT}$ is forced to $V_{OUT(NOM)}$ – 0.1 V and the output current is measured.

## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 1.0 V or 4.0 V (whichever is greater for either fixed or adjustable versions), $I_{LOAD}$ = 1.0 mA, $V_{EN}$ = 3.0 V, $C_{OUT}$ = $C_{IN}$ = 2.2 µF (unless otherwise noted). For TPS79801, FB pin tied to $V_{OUT}$. Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | $T_J$(1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{RL}$ | Input reverse leakage current(reverse battery test) | $V_{IN}$ = –60 V, $V_{OUT}$ = open, $C_{IN}$ open | Full range | | | 6 | mA |
| $I_{RO}$ | Reverse output current(10) | $V_{OUT}$ = $V_{OUT(NOM)}$, $V_{IN}$ = ground | 25°C | | 19 | 25 | µA |
| $T_{SD}$ | Thermal shutdown temperature ($T_J$)(11) | Shutdown, temperature increasing | | 135 | | | ˚C |
| | | Reset, temperature decreasing | | 135 | | | °C |

(10) Reverse output current is tested with the IN pin tied to ground and the output forced to $V_{OUT(NOM)}$ +0.1 V. This current flows into the OUT pin and out of the GND pin and then measured.
(11) Specified by design

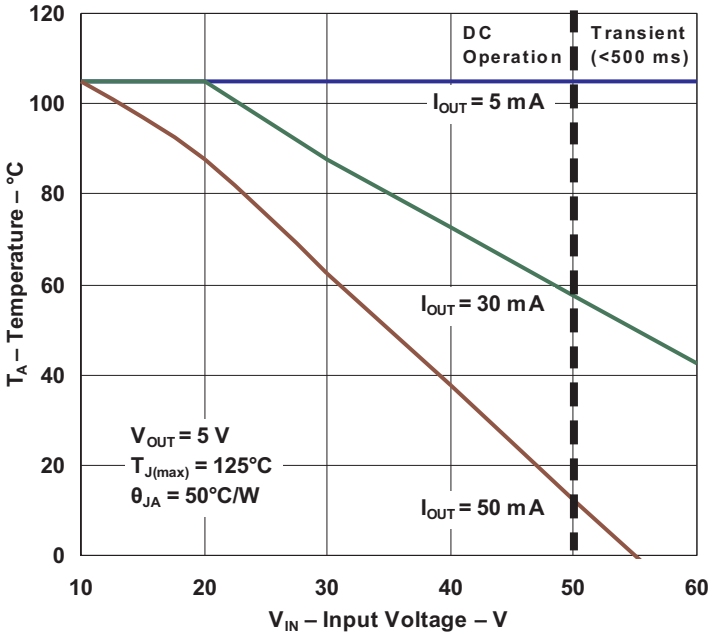



**Figure 1. Safe Operating Area**

## FUNCTIONAL BLOCK DIAGRAMS

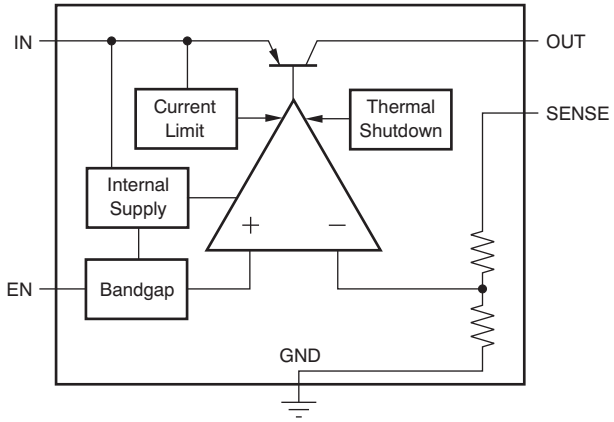



**Figure 2. Fixed Voltage Output Version**

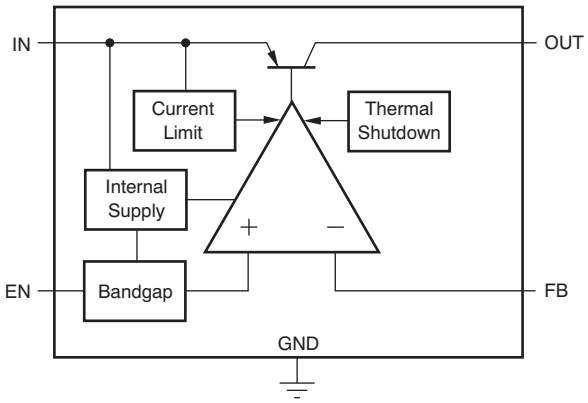
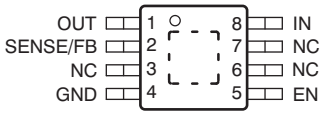



**Figure 3. Adjustable Voltage Output Version**

## PIN CONFIGURATIONS

**DGN PACKAGE**
**MSOP-8 PowerPAD**
**(TOP VIEW)**




Note: The exposed thermal pad is connected to ground via pin 4 (GND).

## PIN DESCRIPTIONS

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | DGN | |
| EN | 5 | Enable pin. Driving the EN pin high turns on the regulator over full operating range. Driving this pin low puts the regulator into shutdown mode over full operating range. |
| IN | 8 | Input pin. A 0.1-µF ceramic or greater capacitor is recommended from this pin to ground to assure stability. Both input and output capacitor grounds should be tied back to the IC ground with no significant impedance between them. |
| GND | 4 | Ground. The exposed thermal pad is connected to ground via this pin. |
| OUT | 1 | Regulated output voltage pin. A small (1 µF) capacitor is needed from this pin to ground to assure stability. |
| SENSE/FB | 2 | This pin is the input to the control loop error amplifier; it is used to set the output voltage of the device. |
| NC | 3, 6, 7 | No internal connection |

## TYPICAL CHARACTERISTICS

**LINE REGULATION vs INPUT VOLTAGE**

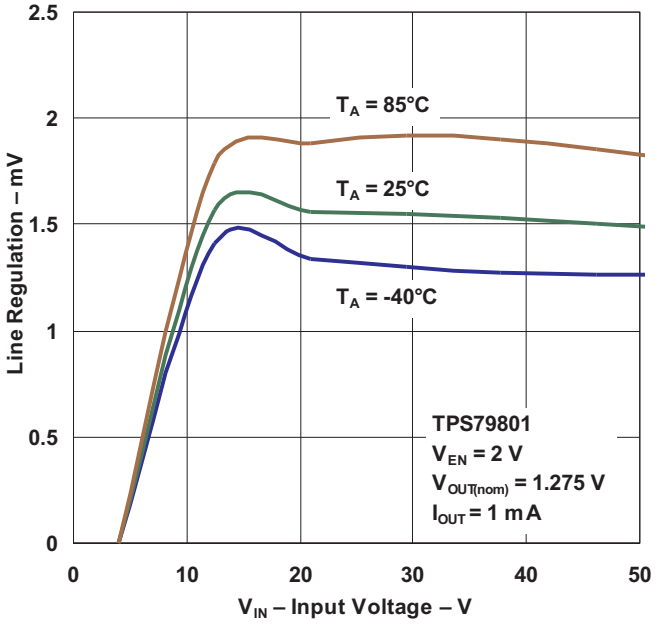



Figure 4.

**LINE REGULATION vs INPUT VOLTAGE**

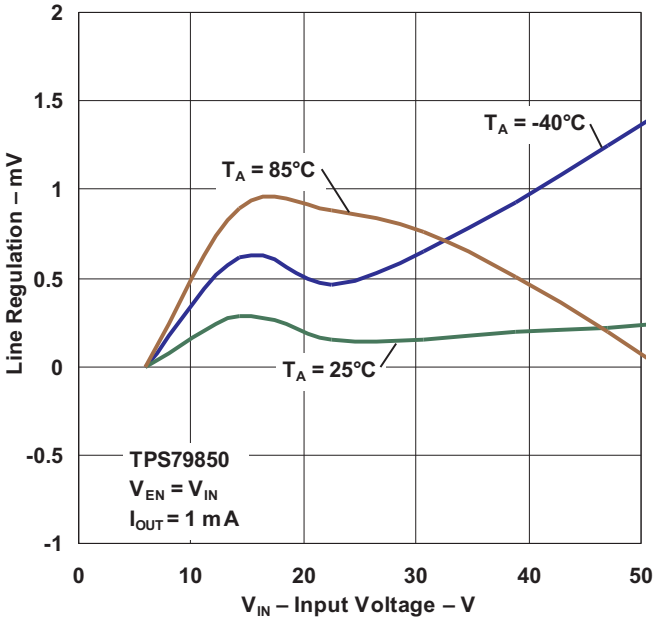



Figure 5.

**DROPOUT VOLTAGE vs OUTPUT CURRENT**

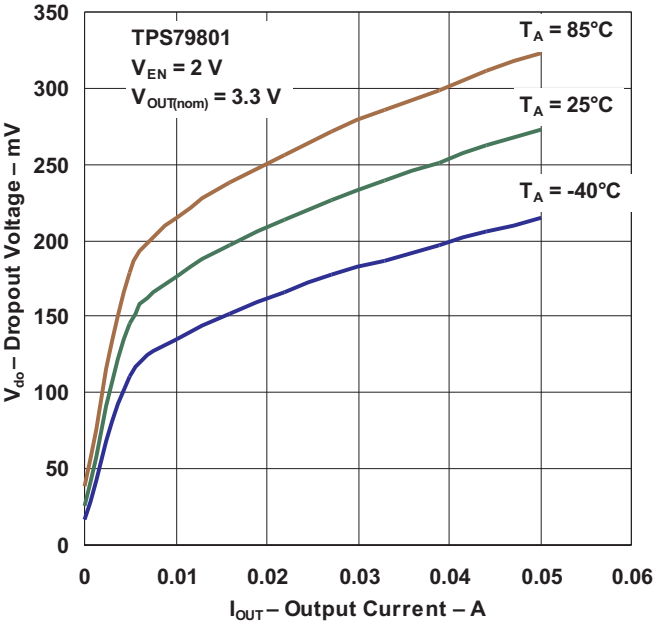



Figure 6.

**DROPOUT VOLTAGE vs OUTPUT CURRENT**

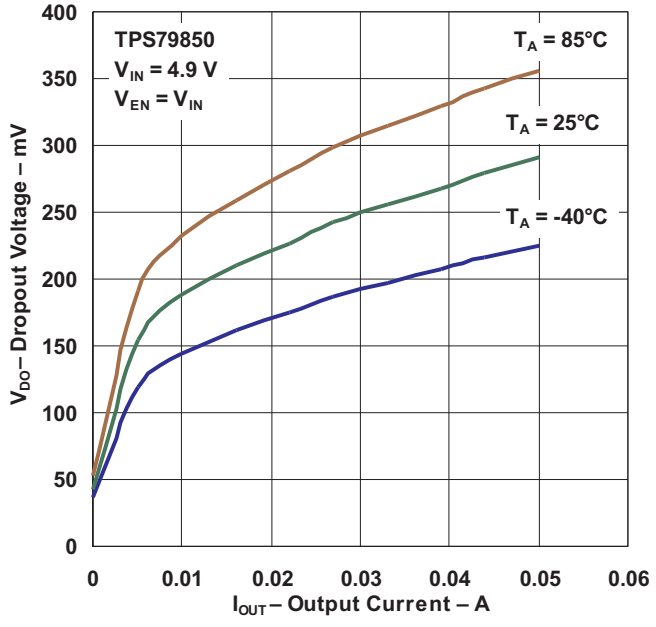



Figure 7.

## TYPICAL CHARACTERISTICS (continued)

**QUIESCENT CURRENT vs TEMPERATURE**

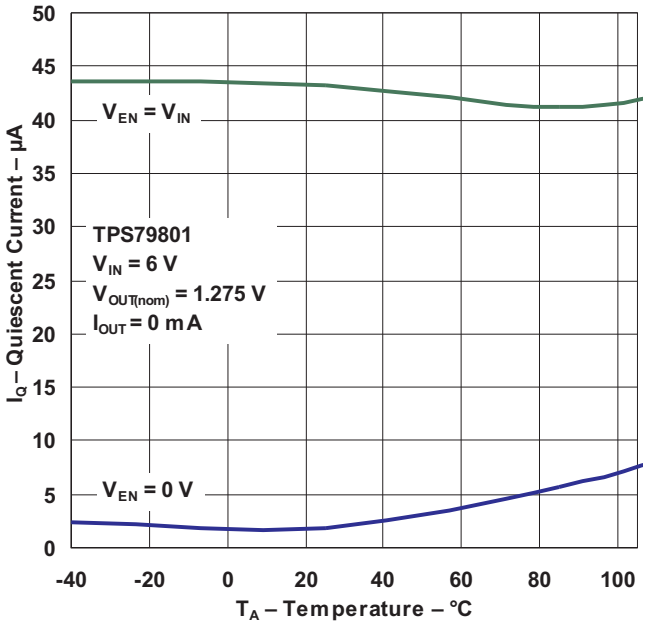



Figure 8.

**QUIESCENT CURRENT vs TEMPERATURE**

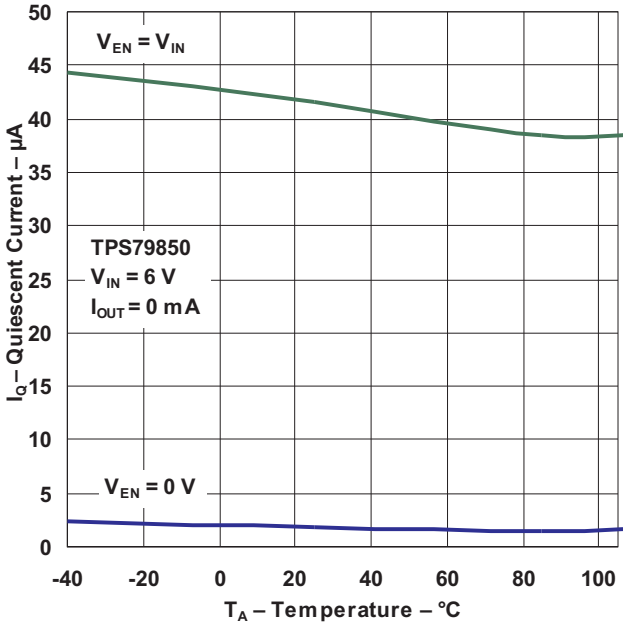



Figure 9.

**QUIESCENT CURRENT vs INPUT VOLTAGE**

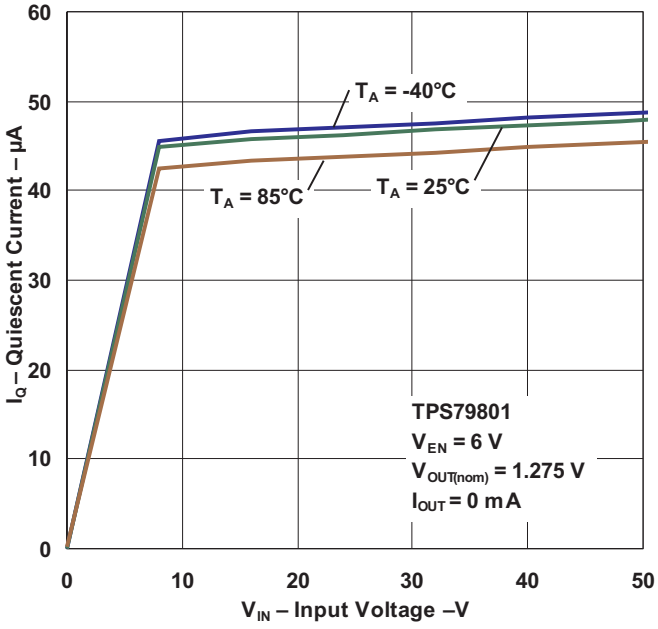



Figure 10.

**QUIESCENT CURRENT vs INPUT VOLTAGE**

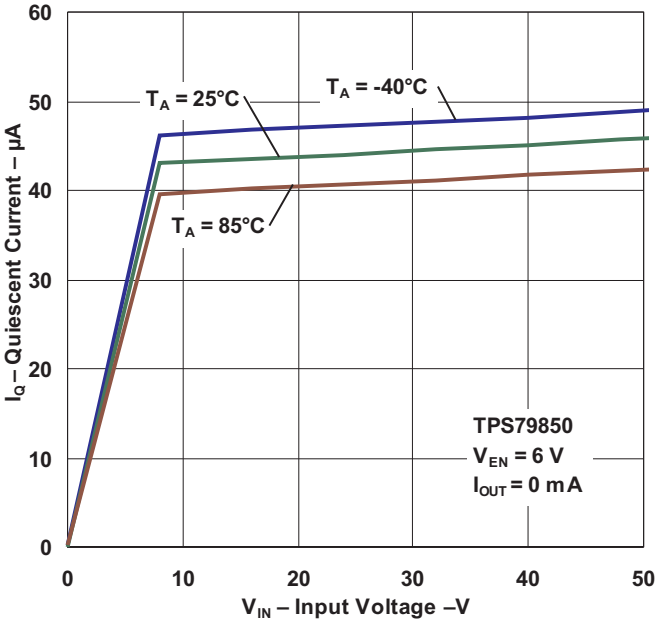



Figure 11.

## TYPICAL CHARACTERISTICS (continued)

**QUIESCENT CURRENT vs OUTPUT CURRENT**

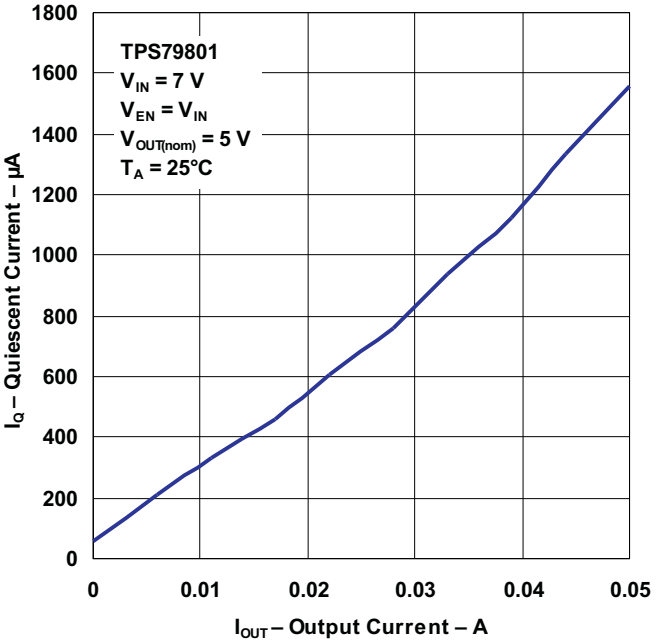



Figure 12.

**QUIESCENT CURRENT vs OUTPUT CURRENT**

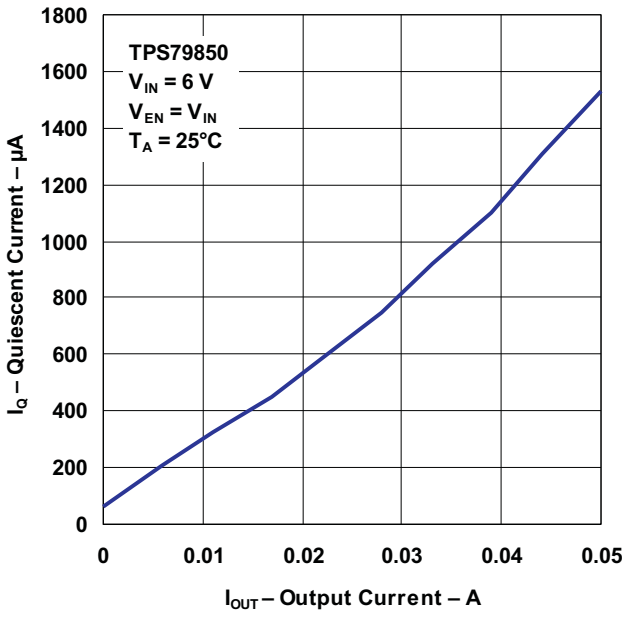



Figure 13.

**REVERSE BATTERY LEAKAGE vs INPUT VOLTAGE**

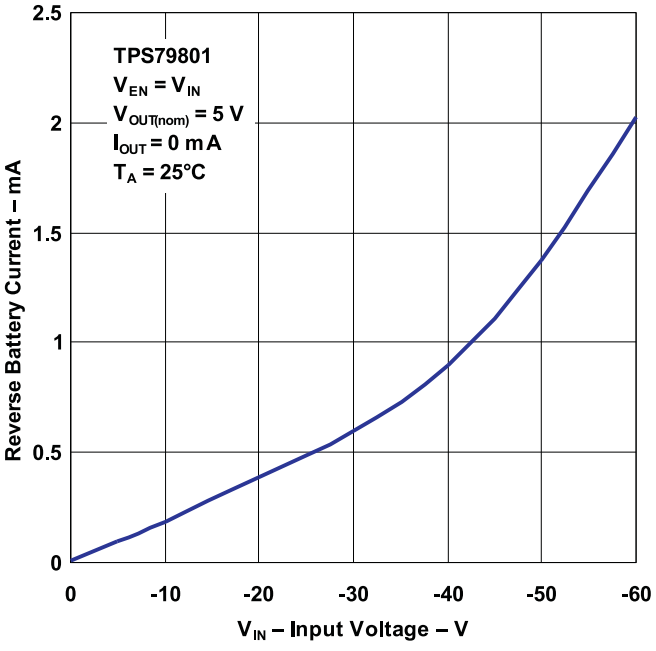



Figure 14.

**POWER SUPPLY RIPPLE REJECTION vs FREQUENCY**

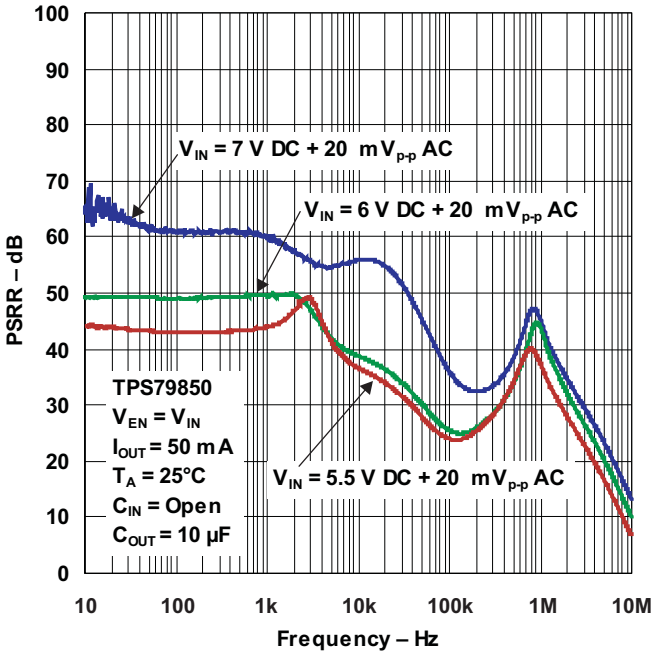
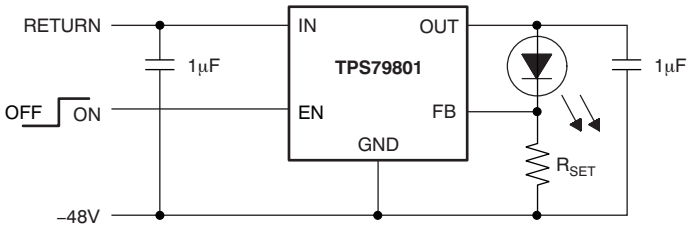



Figure 15.

## APPLICATION INFORMATION

The TPS798xx is a 50-mA high-voltage LDO regulator with micropower quiescent current and shutdown. The device is capable of supplying 50 mA at a dropout voltage of 300 mV (typ). The low operating quiescent current (40 µA) drops to 1 µA in shutdown. In addition to the low quiescent current, the TPS798xx incorporates several protection features that make it ideal for battery-powered applications.

The device is protected against both reverse-input and reverse-output voltages. In battery-backup applications, where the output can be held up by a backup battery when the input is pulled to ground, the TPS798xx acts as if it has a diode in series with its output and prevents reverse current flow. Figure 16 and Figure 17 illustrate two typical applications.




Note: $I_{LED} = 1.275\ V/R_{SET}$
–48 V can vary from –4 V to –50 V

**Figure 16. Constant Brightness for Indicator LED Over Wide Input Voltage Range**

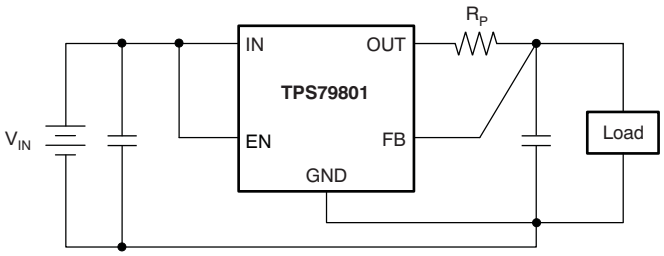
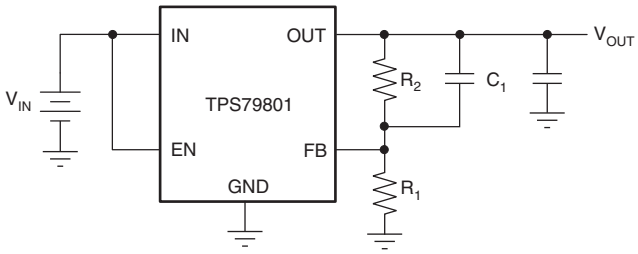



**Figure 17. Kelvin Sense Connection**

### Adjustable Operation

The TPS798xx has an output voltage range of 1.275 V to 28 V. The output voltage is set by the ratio of two external resistors as shown in Figure 18. The feedback loop monitors the output to maintain the voltage at the adjust pin at 1.275 V referenced to ground. The current in $R_1$ is then equal to 1.275 V/$R_1$, and the current in $R_2$ is the current in $R_1$ plus the FB pin bias current. The FB pin bias current, 0.2 µA at 25°C, flows through $R_2$ into the FB pin. The output voltage can be calculated using the formula in Figure 18. The value of $R_1$ should be less than 250 kΩ to minimize errors in the output voltage caused by the FB pin bias current. Note that in shutdown, the output is turned off and the divider current is zero.




$V_{OUT} = 1.275\ V\ (1 + R_2 / R_1) + I_{FB}R_2$
$V_{FB} = 1.275\ V$
$I_{FB} = 0.2\ \mu A$ at 25°C
Output Range = 1.275 V to 28 V

**Figure 18. Adjustable Operation**

A 100-pF capacitor ($C_1$) placed in parallel with the top resistor ($R_2$) of the output divider is necessary for stability and transient performance of the adjustable TPS798xx. The impedance of $C_1$ at 10 kHz should be less than the value of $R_2$.

The adjustable device is tested and specified with the FB pin tied to the OUT pin and a 1 mA dc load (unless otherwise specified) for an output voltage of 1.275 V. Specifications for output voltages greater than 1.275 V are proportional to the ratio of the desired output voltage to 1.275 V ($V_{OUT}$/1.275 V). For example, load regulation for an output current change of 1 mA to 50 mA is –10 mV (typ) at $V_{OUT}$ = 1.275 V.

At $V_{OUT}$ = 12 V, load regulation is:

(12 V/1.275 V) × (–10 mV) = –94 mV

## Output Capacitance and Transient Response

The TPS798xx is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 1 µF with an ESR of 3 Ω or less is recommended to prevent oscillations. The TPS798xx is a micropower device, and output transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TPS798xx, increase the effective output capacitor value.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectrics used are Z5U, Y5 V, X5R, and X7R. The Z5U and Y5 V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients. When used with a 5 V regulator, a 10µF Y5 V capacitor can exhibit an effective value as low as 1µF to 2µF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals because of mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

## Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125°C). The power dissipated by the device consists of two components:

- Output current multiplied by the input/output voltage differential: $I_{OUT} \times (V_{IN} - V_{OUT})$
- GND pin current multiplied by the input voltage: $I_{GND} \times V_{IN}$

The GND pin current can be found by examining the GND pin current curves in the *Typical Characteristics* . Power dissipation is equal to the sum of the two components listed previously.

The TPS798xx series regulators have internal thermal limiting designed to protect the device during overload conditions. Do not exceed the maximum junction temperature rating of 125°C. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface-mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the printed circuit board (PCB) and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

## Calculating Junction Temperature

Given an output voltage of 5 V, an input voltage range of 15 V to 24 V, an output current range of 0 mA to 50 mA, and a maximum ambient temperature of 50°C, the maximum junction temperature is calculated as follows.

The power dissipated ($P_{DISS}$) by the DGN package is equal to:

$I_{OUT(MAX)}(V_{IN(MAX)} – V_{OUT}) + I_{GND}(V_{IN(MAX)})$

Where:

$I_{OUT(MAX)}$ = 50 mA
$V_{IN(MAX)}$ = 24 V
$V_{OUT}$ = 5 V
$I_{GND}$ at ($I_{OUT}$ = 50 mA, $V_{IN}$ = 24 V) = 1 mA

Therefore,

$P_{DISS}$ = 50 mA (24 V – 5 V) + 1 mA (24 V) = 0.974 W

The thermal resistance is approximately 60°C/W, based on JEDEC 51-5 profile. Therefore, the junction temperature rise above ambient is approximately equal to:

0.974 W × 60°C/W = 58.44°C

The maximum junction temperature is then equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$T_J$ max = 50°C + 58.44°C = 108.44°C

## Protection Features

The TPS798xx incorporates several protection features that make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse-input voltages, and reverse currents from output to input.

Current-limit protection and thermal-overload protection are intended to protect the device against current overload conditions at the output of the device. The junction temperature should not exceed 125°C.

The input of the device withstands reverse voltages of –60 V. Current flow into the device is limited to less than 6 mA (typically, less than 100 µA), and no negative voltage appears at the output. The device protects both itself and the load. This architecture also provides protection against batteries that may be plugged in backwards.

The FB pin of the adjustable device can be pulled above or below ground by as much as 7 V without damaging the device. If the input is left open or grounded, the FB pin behaves as an open circuit when pulled below ground, or as a large resistor (typically, 100 kΩ) in series with a diode when pulled above ground. If the input is powered by a voltage source, pulling the FB pin below the reference voltage increases the output voltage. This configuration causes the output to go to a unregulated high voltage. Pulling the FB pin above the reference voltage turns off all output current.

In situations where the FB pin is connected to a resistor divider that would pull the FB pin above its 7 V clamp voltage if the output is pulled high, the FB pin input current must be limited to less than 5 mA. For example, a resistor divider provides a regulated 1.5 V output from the 1.275-V reference when the output is forced to 28 V. The top resistor of the resistor divider must be chosen to limit the current into the FB pin to less than 5 mA when the FB pin is at 7 V. The 21-V difference between the OUT and FB pins divided by the 5-mA maximum current into the FB pin yields a minimum top resistor value of 5.8 kΩ.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open. The rise in reverse output current above 7 V occurs from the breakdown of the 7 V clamp on the FB pin. With a resistor divider on the regulator output, this current is reduced, depending on the size of the resistor divider.

When the IN pin of the TPS798xx is forced below the OUT pin, or the OUT pin is pulled above the IN pin, input current typically drops to less than 0.6 mA. This scenario can occur if the input of the TPS798xx is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the EN pin has no effect on the reverse output current when the output is pulled above the input.

## Thermal Information

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J$ max) above which normal operation is not assured. The operating environment must be designed so that the operating junction temperature ($T_J$) does not exceed the maximum junction temperature ($T_J$ max). The two primary environmental variables that can be used to improve thermal performance are air flow and external heatsinks. The purpose of this section is to help the designer to determine the proper operating environment for a linear regulator that operates at a specific power level.

In general, the maximum expected power ($P_D$ max) consumed by a linear regulator is computed as shown in Equation 1:

$$P_D max = (V_{IN(avg)} – V_{OUT(avg)}) × I_{OUT(avg)} + V_{I(avg)} × I_Q \quad (1)$$

Where:

$V_{IN(avg)}$ is the average input voltage.
$V_{OUT(avg)}$ is the average output voltage.
$I_{OUT(avg)}$ is the average output current.
$I_Q$ is the quiescent current.

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{IN(avg)} × I_Q$ can be ignored. The operating junction temperature is computed by adding the ambient temperature ($T_A$) and the increase in temperature as a result of the regulator power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{θJC}$), the case to heatsink ($R_{θCS}$), and the heatsink to ambient ($R_{θSA}$). Thermal resistances are measurements of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the device thermal resistance.

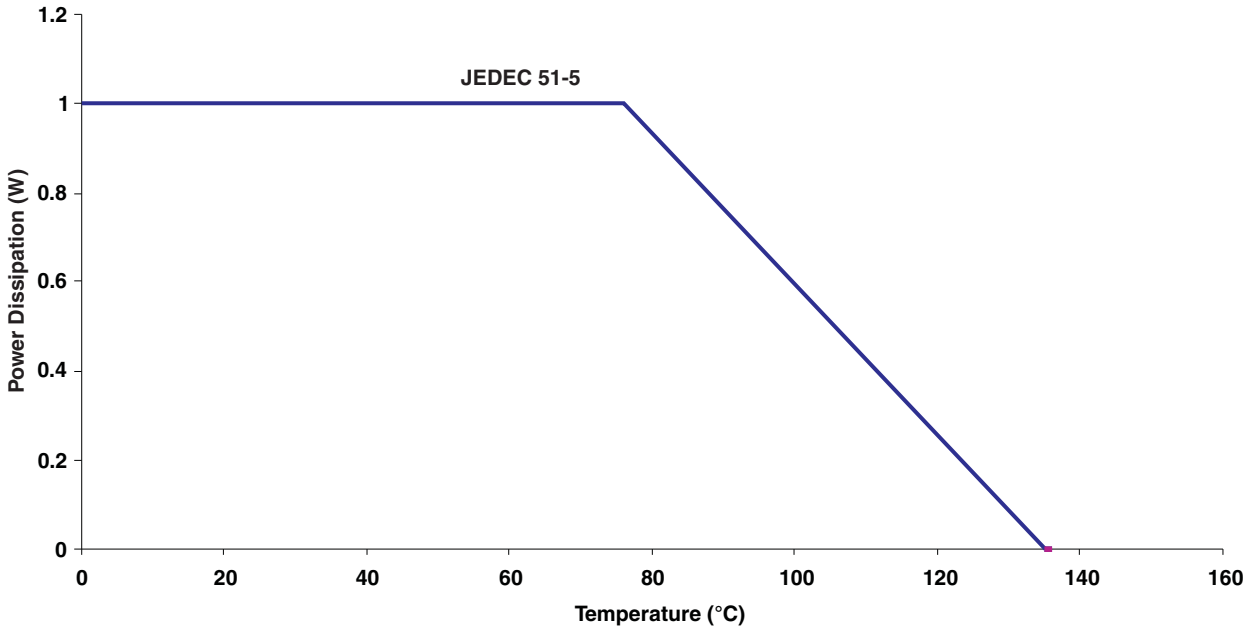



**Figure 19. Power Dissipation vs Temperature**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS79801QDGNRQ1 | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PMRQ | Samples |
| TPS79850QDGNRQ1 | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OOLQ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

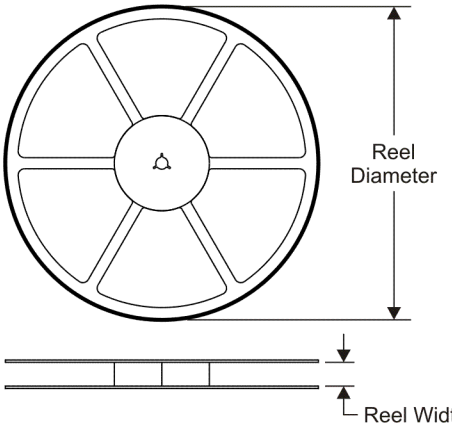
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

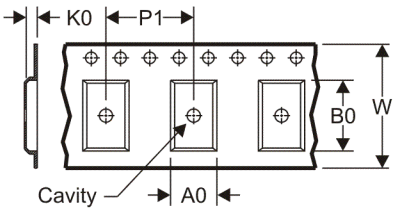
(4) Only one of markings shown within the brackets will appear on the physical device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

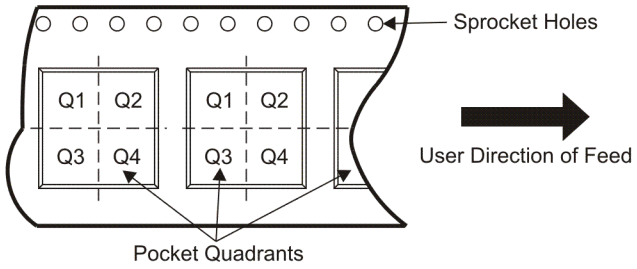



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

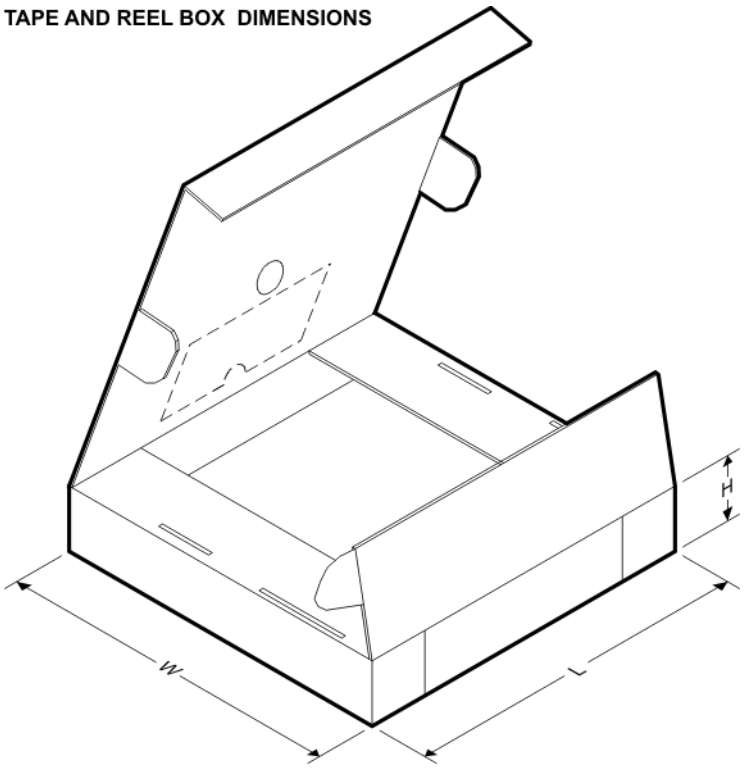
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS79801QDGNRQ1 | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| TPS79850QDGNRQ1 | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |

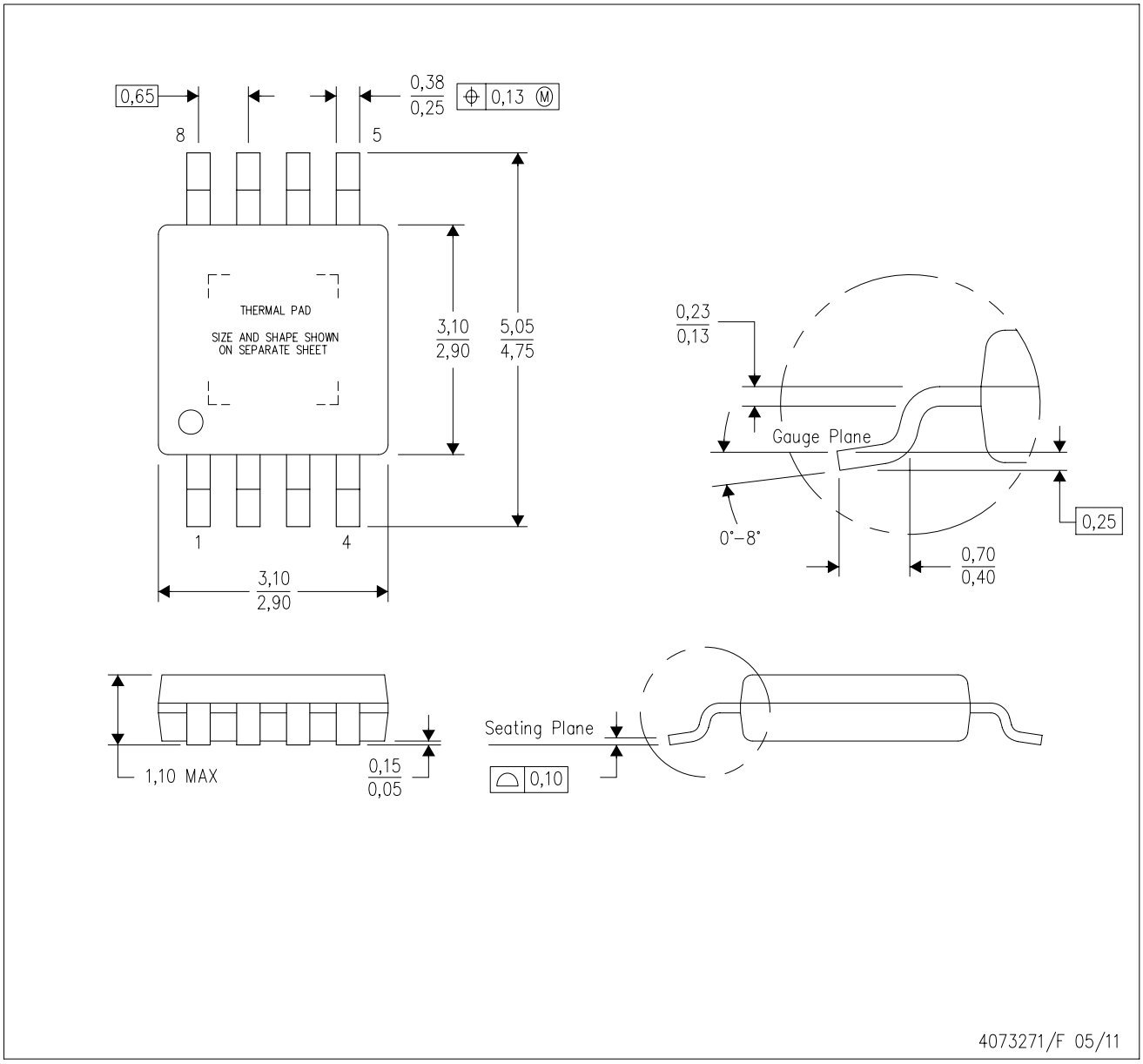
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS79801QDGNRQ1 | MSOP-PowerPAD | DGN | 8 | 2500 | 370.0 | 355.0 | 55.0 |
| TPS79850QDGNRQ1 | MSOP-PowerPAD | DGN | 8 | 2500 | 370.0 | 355.0 | 55.0 |

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

**PowerPAD is a trademark of Texas Instruments.**

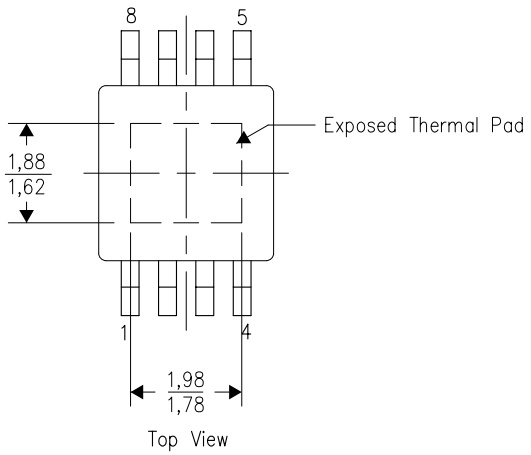
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



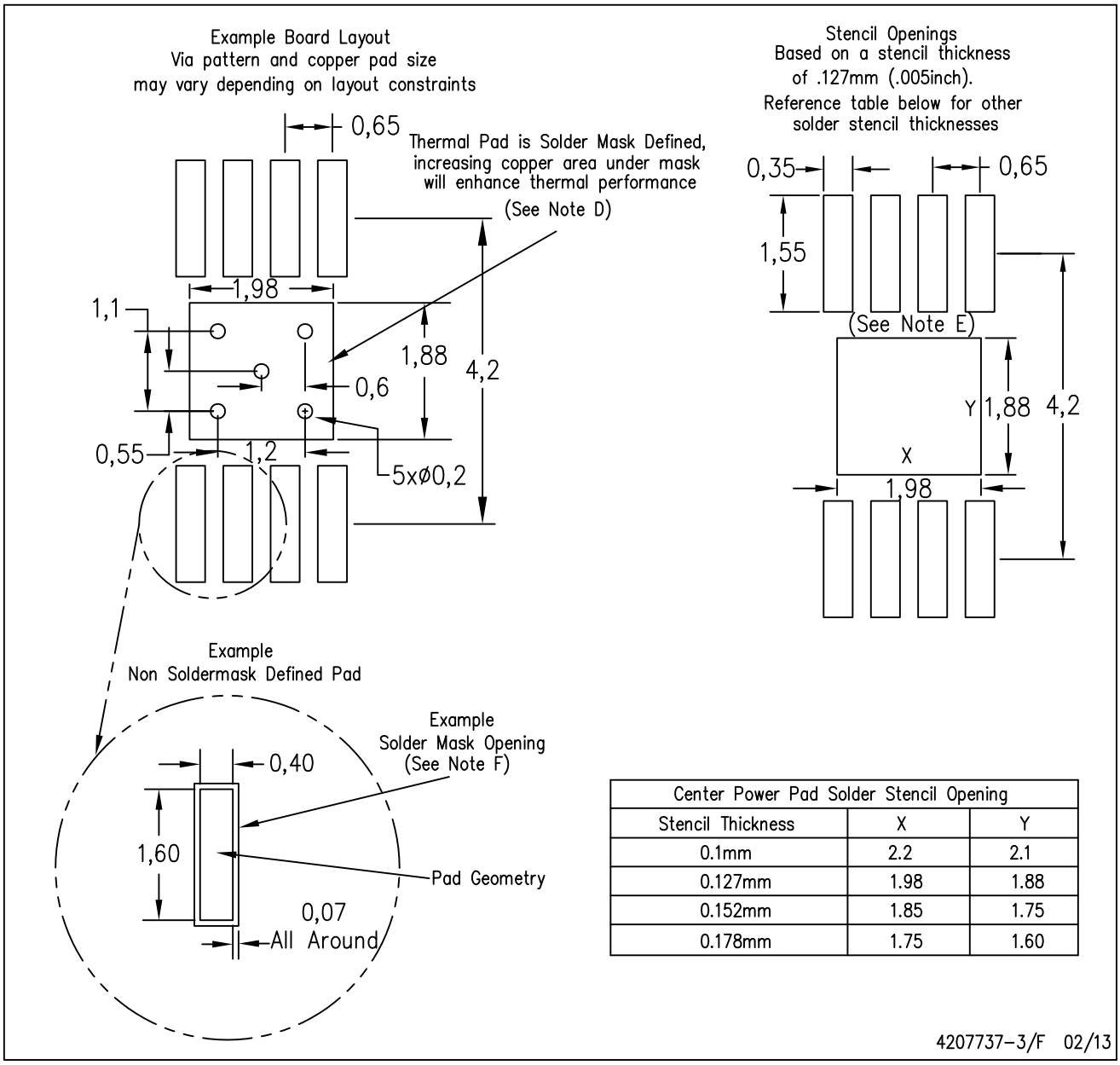

Exposed Thermal Pad Dimensions

4206323–3/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

# DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.2 | 2.1 |
| 0.127mm | 1.98 | 1.88 |
| 0.152mm | 1.85 | 1.75 |
| 0.178mm | 1.75 | 1.60 |

4207737–3/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

# AMEYA360
Components Supply Platform

## Authorized Distribution Brand :

## Website :

Welcome to visit www.ameya360.com

## Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com