PI7C9X20505GP

PCI EXPRESS PACKET SWITCH

DATASHEET

REVISION 1.5

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REVISION HISTORY

Date	Revision Number	Description
12/28/06	0.1	Initial Preliminary Datasheet
01/02/07	0.2	Add Chapter 3, 4 , 6 and 7
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1 Features

- 5-lane PCI Express Switch with 5 PCI Express ports
- Non-blocking full-wired switching capability at 20 Gbps when all 5 ports are enabled
- Supports "Cut-through"(Default) as well as "Store and Forward" mode for packet switching
- Peer-to-peer switching between any two downstream ports
- 150 ns typical latency for packet routed through Switch without blocking
- Strapped pins configurable with optional EEPROM or SMBus
- SMBus interface support
- Compliant with System Management (SM) Bus, Version 1.0
- Compliant with *PCI Express Base Specification Revision 1.1*
- Compliant with *PCI Express CEM Specification Revision 1.1*
- Compliant with *PCI-to-PCI Bridge Architecture Specification Revision 1.2*
- Compliant with *Advanced Configuration Power Interface (ACPI) Specification*
- Compliant with *PCI Standard Hot-Plug Controller (SHPC) and Subsystem Specification Revision 1.0*
- Reliability, Availability and Serviceability
  - Supports Data Poisoning and End-to-End CRC
  - Advanced Error Reporting and Logging
  - Hot Plug support
  - IEEE 1149.6 JTAG interface support
- Advanced Power Saving
  - Empty downstream ports are set to idle state to minimize power consumption
- Link Power Management
  - Supports L0, L0s, L1, L2, $L2/L3_{Ready}$ and L3 link power states
  - Active state power management for L0s and L1 states
  - Beacon or Wake# support in L2 state
- Device State Power Management
  - Supports D0, $D3_{Hot}$ and $D3_{Cold}$ device power states
  - 3.3V Aux Power support in $D3_{Cold}$ power state
- Port Arbitration: Round Robin (RR), Weighted RR and Time-based Weighted RR
- Extended Virtual Channel capability
  - Two Virtual Channels (VC) and Eight Traffic Class (TC) support
  - Disabled VCs' buffer is assigned to enabled VCs for resource sharing
  - Independent TC/VC mapping for each port
  - Provides VC arbitration selections: Strict Priority, Round Robin (RR) and Programmable Weighted RR
- Supports Isochronous Traffic
  - Isochronous traffic class mapped to VC1 only
  - Strict time based credit policing
- Supports up to 256-byte maximum payload size
- Programmable driver current and de-emphasis level at each individual port
- Low Power Dissipation at 1.0W in L0 normal mode
- Industrial Temperature Range -40° to 85°C
- 256-pin PBGA 17mm x 17mm package, 1.0 mm Ball Pitch

2 GENERAL DESCRIPTION

Similar to the role of PCI/PCIX Bridge in PCI/PCIX bus architecture, the function of PCI Express (PCIE) Switch is to expand the connectivity to allow more end devices to be reached by host controllers in PCIE serial interconnect architecture. The 5-lane PCIE Switch can be configured as 5-port type combinations. It provides users the flexibility to expand or fan-out the PCI Express lanes based on their application needs. For some systems that do not need all the 5 lanes, the unused lanes can be disabled to reduce power consumption.

In the PCI Express Architecture, the PCIE Switch forwards posted and non-posted requests and completion packets in either downstream or upstream direction concurrently as if a virtual PCI Bridge is in operation on each port. By visualizing the port as a virtual Bridge, the Switch can be logically viewed as two-level cascaded multiple virtual PCI-to-PCI Bridges, where one upstream-port Bridge sits on all downstream-port Bridges. Similar to a PCI Bridge during enumeration, each port is given a unique bus number, device number, and function number by the initiating software. The bus number, device number, and function number are combined to form a destination ID for each specific port. In addition to that, the memory-map and IO address ranges are exclusively allocated to each port as well. After the software enumeration is finished, the packets are routed to the dedicated port based on the embedded address or destination ID. To ensure the packet integrity during forwarding, the Switch is not allowed to split the packets to multiple small packets or merge the received packets into a large transmit packet. Also, the IDs of the requesters and completers are kept unchanged along the path between ingress and egress port.

The Switch employs the architecture of Combined Input and Output Queue (CIOQ) in implementation. The main reason for choosing CIOQ is that the required memory bandwidth of input queue equals to the bandwidth of ingress port rather than increasing proportionally with port numbers as an output queue Switch does. The CIOQ at each ingress port contains separate dedicated queues to store packets. The packets are arbitrated to the egress port based on the PCIe transaction-ordering rule. For the packets without ordering information, they are permitted to pass over each other in case that the addressed egress port is available to accept them. As to the packets required to follow the ordering rule, the Head-Of-Line (HOL) issue becomes unavoidable for packets destined to different egress ports since the operation of producer-consumer model has to be retained; otherwise the system might occur hang-up problem. On the other hand, the Switch places replay buffer at each egress port to defer the packets before sending it out. This can assure the maximum throughput being achieved and therefore the Switch works efficiently. Another advantage of implementing CIOQ in PCIe Switch is that the credit announcement to the counterpart is simplified and streamlined because of the credit-based flow control protocol. The protocol requires that each ingress port maintains the credits independently without checking other ports' credit availability, which is otherwise required by pure output queue architecture.

The Switch supports two virtual channels (VC0, VC1) and eight traffic classes (TC0 ~ TC7) at each port. The ingress port independently assigns packets into the preferred virtual channel while the egress port outputs the packet based on the predefined port and VC arbitration algorithm. For instance, the isochronous packet is given a special traffic class number other than TC0 and mapped into VC1 accordingly. By employing the strict time based credit policy for port arbitration and assigning higher priority to VC1 than VC0, the Switch can therefore guarantee the time-sensitive packet is not blocked by regular traffic to assure the quality of service. In addition, some data-centric applications only carry TC0/VC0 traffic. As a result, there are no packets that would consume VC1 bandwidth. In order to improve the efficiency of buffer usage, the unused VC1 queues can be reassigned to VC0 and enable each of the ingress ports to handle more data traffic bursts. This virtual channel resource relocation feature enhances the performance of the PCIe Switch further.

3 PIN DESCRIPTION

3.1 PCI EXPRESS INTERFACE SIGNALS

NAME	PIN	TYPE	DESCRIPTION
REFCLKP REFCLKN	A16 A15	I	**Reference Clock Input Pairs:** Connects to external 100MHz differential clock. The input clock signals must be delivered to the clock buffer cell through an AC-coupled interface so that only the AC information of the clock is received, converted, and buffered. It is recommended that a 0.1uF be used in the AC-coupling.
PERP [4:0]	D16, K16, M15, T13, A13	I	**PCI Express Data Serial Input Pairs:** Differential data receive signals in five ports. Port 0 (Upstream Port) is PERP[0] and PERN[0] Port 1 (Downstream Port) is PERP[1] and PERN[1] Port 2 (Downstream Port) is PERP[2] and PERN[2] Port 3 (Downstream Port) is PERP[3] and PERN[3] Port 4 (Downstream Port) is PERP[4] and PERN[4]
PERN [4:0]	D15, K15, M16, T12, B13	I	
PETP [4:0]	F15, H15, P16, T15, A11	O	**PCI Express Data Serial Output Pairs:** Differential data transmit signals in five ports. Port 0 (Upstream Port) is PETP[0] and PETN[0] Port 1 (Downstream Port) is PETP[1] and PETN[1] Port 2 (Downstream Port) is PETP[2] and PETN[2] Port 3 (Downstream Port) is PETP[3] and PETN[3] Port 4 (Downstream Port) is PETP[4] and PETN[4]
PETN [4:0]	F16, H16, P15, T16, B11	O	
WAKEUP_L	F2	I	**Wakeup Signal (Active LOW):** When WAKEUP_L is asserted, the upstream port has to generate a Beacon that is propagated to the Root Complex/Power Management Controller. Pin has an internal pull-up.
RESET_L	E4	I	**System Reset (Active LOW):** When RESET_L is asserted, the internal states of whole chip except sticky logics are initialized.
DWNRST_L [4:1]	E5, D5, E6, D6	O	**Downstream Device Reset (Active LOW):** It provides a reset signal to the devices connected to the downstream ports of Switch. The signal is active when either RESET_L is asserted or the device is just plugged into the Switch. DWNRST_L [x] corresponds to Portx, where x= 1,2,3,4.

3.2 PORT CONFIGURATION SIGNALS

NAME	PIN	TYPE	DESCRIPTION
VC1_EN	F4	I	**Virtual Channel 1 Enable:** The chip provides the capability to support virtual channel 1 (VC1), in addition to the standard virtual channel 0. When this pin is asserted high, Virtual Channel 1 is enabled, and virtual channel resource sharing is not available. When it is asserted low, the chip would allocate the additional VC1 resource to VC0, and VC1 capability is disabled. The pin has internal pull-down.
SLOT_IMP [4:1]	*T6, G4, G2, G1	I	**Slot Implemented:** It decides if the downstream port is connected to slot. SLOT_IMP [x] is correspondent to Portx, where x= 1,2,3,4. When SLOT_IMP [x] is high, the Portx is connected to slot. The strapping pin SLOT_IMP[4] is shared with PWR_IND[1]. By default, downstream Port1, Port2, Port3, and Port4 are implemented with slots. SLOT_IMP[4] has internal pull-down, and SLOT_IMP[3:1] have internal pull-up.

NAME	PIN	TYPE	DESCRIPTION
HOTPLUG [4:1]	*R6, H2, H1, H4	I	**Hot Plug Capability:** It determines if the downstream port is able to support hot plug capability. HOTPLUG [x] is correspondent to Portx, where x=1,2,3,4. When HOTPLUG [x] is high, Portx supports hot plug operation. The strapping pin HOTPLUG[4] is shared with PWR_IND[2]. By default, downstream Port1, Port2, Port 3, and Port4 are equipped with hot plug function. HOTPLUG[4] has internal pull-down, and HOTPLUG[3:1] have internal pull-up.
SLOTCLK [4:0]	*P6, J3, J1, H5, H3	I	**Slot Clock Configuration:** It determines if the downstream component uses the same physical reference clock that the platform provides on the connector. When SLOTCLK is high, the platform reference clock is employed. The strapping pin SLOTCLK[4] is shared with PWR_IND[3]. By default, downstream Port1, Port2, Port 3, and Port4 use the same physical reference clock provided by platform. SLOTCLK[4] has internal pull-down, and SLOTCLK[3:0] have internal pull-up.

3.3 HOT PLUG SIGNALS

NAME	PIN	TYPE	DESCRIPTION
PWR_IND [4:1]	T7, *P6, *R6, *T6	O	**Power Indicator:** Indicates the power status for each slot at downstream port. PWR_IND [x] is correspondent to Port x, where x=1,2,3,4. They are active-high signals. The pins have internal pull-down.
ATT_IND [4:1]	L7, N7, P7, R7	O	**Attention Indicator:** Indicates the attention status for each slot at downstream port. ATT_IND [x] is correspondent to Port x, where x=1,2,3,4. They are active-high signals. Pins are set to "0000" by default. ATT_IND [4] should be tied to ground through a 47K pull-down resistor to disable the internal test function. ATT_IND[4:2] have internal pull-down.
ATT_BTN [4:1]	L8, M8, P8, R8	I	**Attention Button:** When asserted high, it represents the attention button has been pressed for the slot at the downstream port. ATT_BTN [x] is correspondent to Port x, where x=1,2,3,4.
MRL_PDC [4:1]	L9, N9, P9, R9	I	**Presence Detected Change:** When asserted low, it represents the device is present in the slot of downstream ports. Otherwise, it represents the absence of the device. MRL_PDC [x] is correspondent to Port x, where x=1,2,3,4.
PWR_ENA_L [4:1]	M10, N10, R10, T10	O	**SLOT Power Enable (Active LOW):** Indicates the enable status of the power connecting to the associated slot. PWR_ENA [x] is correspondent to Portx, where x=1,2,3,4. They are active-low signals. Pins are set to "0000" by default.
PWR_FLT [4:1]	M11, N11, P11, R11	I	**SLOT Power Fault:** When asserted high, it indicates a power fault on one or more supply rails. PWR_FLT [x] is correspondent to Port x, where x=1,2,3,4.

3.4 MISCELLANEOUS SIGNALS

NAME	PIN	TYPE	DESCRIPTION
EECLK	R14	O	**EEPROM Clock:** Clock signal to the EEPROM interface.
EEPD	P14	I/O	**EEPROM Data: Bi-directional** serial data interface to and from the EEPROM. The pin has internal pull-up.
SMBCLK	T4	I	**SMBus Clock:** System management Bus Clock. Pin has an internal pull-down.
SMBDATA	T5	I/O	**SMBus Data: Bi-Directional** System Management Bus Data.
SCAN_EN	N14	I/O	**Full-Scan Enable Control:** For normal operation, SCAN_EN is an output with a value of "0". SCAN_EN becomes an input during manufacturing testing.
PORTERR [4:0]	N13, P13, M12, N12, P12	O	**Port PHY Error Status:** These pins are used to display the PHY Error status of the ports. When PORTERR is flashing (alternating high and low signals), it indicates that a PHY error is detected. When it is low, no PHY error is detected. PORTERR [x] is correspondent to Port x, where x=0,1,2,3,4.

NAME	PIN	TYPE	DESCRIPTION
GPIO [7:0]	L2, L1, K5, K4, K3, K2, J6, J5	I/O	**General Purpose Input and Output:** These eight general-purpose pins are programmed as either input-only or bi-directional pins by writing the GPIO output enable control register. When SMBus is implemented, GPIO[7:5] act as the SMBus address pins, which set Bit 2 to 0 of the SMBus address.
HIDRV	L6	I	**High Driver Control:** This mode bit is for increasing the nominal value of the lane's driver current level. (See Sec. 5.1 for more detailed descriptions) By default, it is set to '0' without pin strapped.
LODRV	M2	I	**Low Driver Control:** This mode bit is for decreasing the nominal value of the lane's driver current level. (See Sec. 5.1 for more detailed descriptions) By default, it is set to '0' without pin strapped.
DTX [3:0]	N1, M6, M5, M3	I	**Driver Current Level Control:** This 4-bit digital word is to control the driver current level. (See Sec. 5.1 for more detailed descriptions) By default, they are set to "0000" without pin strapped.
DEQ [3:0]	P1, N5, N4, N2	I	**Driver Equalization Level Control:** This 4-bit digital word is to control the driver equalization level. (See Sec. 5.1 for more detailed descriptions) By default, they are set to "1000" without pin strapped.
RXEQCTL [1:0]	P4, P3	I	**Receiver Equalization Level Control:** This 2-bit digital word is to control the receiver equalization level. By default, they are set to "00" without pin strapped.
RXTERMADJ [1:0]	T3, R2	I	**Receive Termination Adjustment:** A control bus to adjust the receive termination resistor value. By default, they are set to "00" without pin strapped.
TXTERMADJ [1:0]	T2, R1	I	**Transmit Termination Adjustment:** A control bus to adjust the transmit termination resistor value. By default, they are set to "00" without pin strapped.
TEST1	L4	I	**Test1:** This pin is for internal test purpose. Test1 should be tied to ground through a pull-down resistor.
TEST2 TEST3 TEST4 TEST5	D4 D8 E8 E7	I	**Test2/3/4/5:** These pins are for internal test purpose. Test2, Test3, Test4 and Test5 should be tied to 3.3V through a pull-up resistor.
TEST6	E14	I	**Test6:** This pin is for internal test purpose. Test6 should be connected to an (475 ohm +/- 1%) external resistor to Vss.
NC	A3, A5, A7, A9, B1, B3, B5, B7, B9, C1, D12, D13, E1, E2, F3, F12, F13, H12, H13, R3, R5,		**Not Connected:** These pins can be just left open.

3.5 JTAG BOUNDARY SCAN SIGNALS

NAME	PIN	TYPE	DESCRIPTION
TCK	L12	I	**Test Clock:** Used to clock state information and data into and out of the chip during boundary scan. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TMS	L13	I	**Test Mode Select:** Used to control the state of the Test Access Port controller. The pin has internal pull-up. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 5.1K pull-down resistor.
TDO	M13	O	**Test Data Output:** When SCAN_EN is high, it is used (in conjunction with TCK) to shift data out of the Test Access Port (TAP) in a serial bit stream. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TDI	L14	I	**Test Data Input:** When SCAN_EN is high, it is used (in conjunction with TCK) to shift data and instructions into the TAP in a serial bit stream. The pin has internal pull-up. When JTAG boundary scan function is not implemented, this pin should be left open (NC).

NAME	PIN	TYPE	DESCRIPTION
TRST_L	K11	I	**Test Reset (Active LOW):** Active LOW signal to reset the TAP controller into an initialized state. The pin has internal pull-up. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 5.1K pull-down resistor.

3.6 POWER PINS

NAME	PIN	TYPE	DESCRIPTION
VDDC	D7, D10, E9, E10, F6, F7, F8, F9, F10, G5, G7, G12, G13, H6, H7, J7, J12, K6, K8, K10, K12, L5, L10, L11, M7, M9, N6, N8	P	**VDDC Supply (1.0V):** Used as digital core power pins.
VDDR	C6, D14, E12, G3, G14, J4, K13, L3, M4, P5, R13, T1, T8	P	**VDDR Supply (3.3V):** Used as digital I/O power pins.
VDDA	D9, D11, E11, F11, G10, G11, H11, J11, J13	P	**VDDA Supply (1.0V):** Used as analog power pins.
VDDCAUX	A8, D3, E3, N15	P	**VDDCAUX Supply (1.0V):** Used as auxiliary core power pins.
VAUX	F1	P	**VAUX Supply (3.3V):** Used as auxiliary I/O power pins.
VTT	A1, A2, A10, B10, G15, G16, R15, R16	P	**Termination Voltage (1.5V):** Provides driver termination voltage at transmitter. Should be given the same consideration as VDDCAUX.
VSS	A4, A6, A12, A14, B2, B4, B6, B8, B12, B14, B15, B16, C2, C3, C4, C5, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, D1, D2, E13, E15, E16, F5, F14, G6, G8, G9, H8, H9, H10, H14, J2, J8, J9, J10, J14, J15, J16, K1, K7, K9, K14, L15, L16, M1, M14, N3, N16, P2, P10, R4, R12, T9, T11, T14	P	**VSS Ground:** Used as ground pins**.**

4 PIN ASSIGNMENTS

4.1 PIN LIST of 256-PIN PBGA

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	VTT	E1	NC	J1	SLOTCLK[2]	N1	DTX[3]
A2	VTT	E2	NC	J2	VSS	N2	DEQ[0]
A3	NC	E3	VDDCAUX	J3	SLOTCLK[3]	N3	VSS
A4	VSS	E4	RESET_L	J4	VDDR	N4	DEQ[1]
A5	NC	E5	DWNRST_L[4]	J5	GPIO[0]	N5	DEQ[2]
A6	VSS	E6	DWNRST_L[2]	J6	GPIO[1]	N6	VDDC
A7	NC	E7	TEST5	J7	VDDC	N7	ATT_IND[3]
A8	VDDCAUX	E8	TEST4	J8	VSS	N8	VDDC
A9	NC	E9	VDDC	J9	VSS	N9	MRL_PDC[3]
A10	VTT	E10	VDDC	J10	VSS	N10	PWR_ENA_L[3]
A11	PETP[0]	E11	VDDA	J11	VDDA	N11	PWR_FLT[3]
A12	VSS	E12	VDDR	J12	VDDC	N12	PORTERR[1]
A13	PERP[0]	E13	VSS	J13	VDDA	N13	PORTERR[4]
A14	VSS	E14	TEST6	J14	VSS	N14	SCAN_EN
A15	REFCLKN	E15	VSS	J15	VSS	N15	VDDCAUX
A16	REFCLKP	E16	VSS	J16	VSS	N16	VSS
B1	NC	F1	VAUX	K1	VSS	P1	DEQ[3]
B2	VSS	F2	WAKEUP_L	K2	GPIO[2]	P2	VSS
B3	NC	F3	NC	K3	GPIO[3]	P3	RXEQCTL[0]
B4	VSS	F4	VC1_EN	K4	GPIO[4]	P4	RXEQCTL[1]
B5	NC	F5	VSS	K5	GPIO[5]	P5	VDDR
B6	VSS	F6	VDDC	K6	VDDC	P6	PWR_IND[3] / SLOTCLK[4]
B7	NC	F7	VDDC	K7	VSS	P7	ATT_IND[2]
B8	VSS	F8	VDDC	K8	VDDC	P8	ATT_BTN[2]
B9	NC	F9	VDDC	K9	VSS	P9	MRL_PDC[2]
B10	VTT	F10	VDDC	K10	VDDC	P10	VSS
B11	PETN[0]	F11	VDDA	K11	TRST_L	P11	PWR_FLT[2]
B12	VSS	F12	NC	K12	VDDC	P12	PORTERR[0]
B13	PERN[0]	F13	NC	K13	VDDR	P13	PORTERR[3]
B14	VSS	F14	VSS	K14	VSS	P14	EEPD
B15	VSS	F15	PETP[4]	K15	PERN[3]	P15	PETN[2]
B16	VSS	F16	PETN[4]	K16	PERP[3]	P16	PETP[2]
C1	NC	G1	SLOT_IMP[1]	L1	GPIO[6]	R1	TXTERMADJ[0]
C2	VSS	G2	SLOT_IMP[2]	L2	GPIO[7]	R2	RXTERMADJ[0]
C3	VSS	G3	VDDR	L3	VDDR	R3	NC
C4	VSS	G4	SLOT_IMP[3]	L4	TEST1	R4	VSS
C5	VSS	G5	VDDC	L5	VDDC	R5	NC
C6	VDDR	G6	VSS	L6	HIDRV	R6	PWR_IND[2] / HOTPLUG[4]
C7	VSS	G7	VDDC	L7	ATT_IND[4]	R7	ATT_IND[1]
C8	VSS	G8	VSS	L8	ATT_BTN[4]	R8	ATT_BTN[1]
C9	VSS	G9	VSS	L9	MRL_PDC[4]	R9	MRL_PDC[1]
C10	VSS	G10	VDDA	L10	VDDC	R10	PWR_ENA_L[2]
C11	VSS	G11	VDDA	L11	VDDC	R11	PWR_FLT[1]
C12	VSS	G12	VDDC	L12	TCK	R12	VSS
C13	VSS	G13	VDDC	L13	TMS	R13	VDDR
C14	VSS	G14	VDDR	L14	TDI	R14	EECLK
C15	VSS	G15	VTT	L15	VSS	R15	VTT
C16	VSS	G16	VTT	L16	VSS	R16	VTT
D1	VSS	H1	HOTPLUG[2]	M1	VSS	T1	VDDR
D2	VSS	H2	HOTPLUG[3]	M2	LODRV	T2	TXTERMADJ[1]
D3	VDDCAUX	H3	SLOTCLK[0]	M3	DTX[0]	T3	RXTERMADJ[1]
D4	TEST2	H4	HOTPLUG[1]	M4	VDDR	T4	SMBCLK
D5	DWNRST_L[3]	H5	SLOTCLK[1]	M5	DTX[1]	T5	SMBDATA

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
D6	DWNRST_L[1]	H6	VDDC	M6	DTX[2]	T6	PWR_IND[1] / SLOT_IMP[4]
D7	VDDC	H7	VDDC	M7	VDDC	T7	PWR_IND[4]
D8	TEST3	H8	VSS	M8	ATT_BTN[3]	T8	VDDR
D9	VDDA	H9	VSS	M9	VDDC	T9	VSS
D10	VDDC	H10	VSS	M10	PWR_ENA_L[4]	T10	PWR_ENA_L[1]
D11	VDDA	H11	VDDA	M11	PWR_FLT[4]	T11	VSS
D12	NC	H12	NC	M12	PORTERR[2]	T12	PERN[1]
D13	NC	H13	NC	M13	TDO	T13	PERP[1]
D14	VDDR	H14	VSS	M14	VSS	T14	VSS
D15	PERN[4]	H15	PETP[3]	M15	PERP[2]	T15	PETP[1]
D16	PERP[4]	H16	PETN[3]	M16	PERN[2]	T16	PETN[1]

5 FUNCTIONAL DESCRIPTION

Multiple virtual PCI-to-PCI Bridges (VPPB), connected by a virtual PCI bus, reside in the Switch. Each VPPB contains the complete PCIe architecture layers that consist of the physical, data link, and transaction layer. The packets entering the Switch via one of VPPBs are first converted from serial bit-stream into parallel bus signals in physical layer, stripped off the link-related header by data link layer, and then relayed up to the transaction layer to extract out the transaction header. According to the address or ID embedded in the transaction header, the entire transaction packets are forwarded to the destination VPPB for formatting as a serial-type PCIe packet through the transmit circuits in the data link layer and physical layer. The following sections describe these function elements for processing PCIe packets within the Switch.

5.1 PHYSICAL LAYER CIRCUIT

The physical layer circuit design is based on the **P**HY **I**nterface for **P**CI **E**xpress Architecture (PIPE). It contains Physical Media Attachment (PMA) and Physical Coding Sub-layer (PCS) blocks. PMA includes Serializer/ Deserializer (SERDES), PLL[1], Clock Recovery module, receiver detection circuits, beacon transmitter, electrical idle detector, and input/output buffers. PCS consists of framer, 8B/10B encoder/decoder, receiver elastic buffer, and PIPE PHY control/status circuitries. To provide the flexibility for port configuration, each lane has its own control and status signals for MAC to access individually. In addition, a pair of PRBS generator and checker is included for PHY built-in self test. The main functions of physical layer circuits include the conversion between serial-link and parallel bus, provision of clock source for the Switch, resolving clock difference in receiver end, and detection of physical layer errors.

In order to meet the different application needs, the driving current and equalization of each transmitting channels can be adjusted using strapped pins individually (refer to section 3.4 for pin descriptions). The driver current of each channel is set to 20mA in default mode without pins being strapped. To change the current value, the user can strap the pins either for nominal value (HIDRV, LODRV) or actual value (DTX [3:0]), which is a scaled multiple of Inom. The following tables illustrate the possible transmitted current values the chip provides.

Table 5-1 Nominal Driver Current Values (Inom)

HIDRV	LODRV	NOMINAL DRIVER CURENT
0	0	20 mA
0	1	10 mA
1	0	28 mA
1	1	Reserved

Table 5-2 Ratio of Actual Current and Nominal Current

DTX [3:0]	ACTUAL CURRENT / NOMINAL CURRENT
0000	1.00
0001	1.05
0010	1.10
0011	1.15
0100	1.20
0101	1.25
0110	1.30

[1] Multiple lanes could share the PLL.

DTX [3:0]	ACTUAL CURRENT / NOMINAL CURRENT
0111	1.35
1000	0.60
1001	0.65
1010	0.70
1011	0.75
1100	0.80
1101	0.85
1110	0.90
1111	0.95

The equalization function of transmitting channels can optimize the driver current for different back-plane lengths and materials. The table shown below lists the combinations of de-emphasized driver current ($I_{TX} - I_{EQ}$) to non-de-emphasized driver current (I_{TX}) for different values of DEQ [3:0].

Table 5-3 De-emphasis Level versus DEQ [3:0]

DEQ [3:0]	$(I_{TX} - I_{EQ}) / I_{TX}$	De-emphasis (dB)
0000	1.00	0.00
0001	0.96	-0.35
0010	0.92	-0.72
0011	0.88	-1.11
0100	0.84	-1.51
0101	0.80	-1.94
0110	0.76	-2.38
0111	0.72	-2.85
1000	0.68	-3.35
1001	0.64	-3.88
1010	0.60	-4.44
1011	0.56	-5.04
1100	0.52	-5.68
1101	0.48	-6.38
1110	0.44	-7.13
1111	0.40	-7.96

By default, the DEQ is set to “1000” to conform to the PCI Express 1.0a specification, which calls for a de-emphasis level of between –3 dB and –4 dB.

In order to improve the data stream integrity across the channels, the receiver of each port of the Switch includes a reception equalizer to mitigate the effects of ISI. The reception equalizer is implemented as a selectable high-pass filter at the input node, and it is capable of removing as much as 0.4UI of ISI related jitter. The following table shows a simple guideline for selecting the appropriate value to adapt with different lengths or connector numbers in various applications.

Table 5-4 Rx Equalizer Settings (RXEQCTL)

RXEQCTL [1]	RXEQCTL [0]	Rx Eq Setting	Input Jitter	Channel Length
0	0	Max Rx Eq	> 0.25 UI	> 20" and two or more connectors
0	1	Min Rx Eq	Between 0.1 UI and 0.25 UI	Between 8" and 20" and up to two connectors
1	X		< 0.1 UI	8" or less, up to one connector

5.2 DATA LINK LAYER (DLL)

The Data Link Layer (DLL) provides a reliable data transmission between two PCI Express points. An ACK/NACK protocol is employed to guarantee the integrity of the packets delivered. Each Transaction Layer Packet (TLP) is protected by a 32-bit LCRC for error detection. The DLL receiver performs LCRC calculation to determine if the incoming packet is corrupted in the serial link. If an LCRC error is found, the DLL transmitter would issue a NACK data link layer packet (DLLP) to the opposite end to request a re-transmission, otherwise an ACK DLLP would be sent out to acknowledge on reception of a good TLP.

In the transmitter, a retry buffer is implemented to store the transmitted TLPs whose corresponding ACK/NACK DLLP have not been received yet. When an ACK is received, the TLPs with sequence number equals to and smaller than that carried in the ACK would be flushed out from the buffer. If a NACK is received or no ACK/NACK is returned from the link partner after the replay timer expires, then a replay mechanism built in DLL transmitter is triggered to re-transmit the corresponding packet that receives NACK or time-out and any other TLP transmitted after that packet.

Meanwhile, the DLL is also responsible for the initialization, updating, and monitoring of the flow-control credit. All of the flow control information is carried by DLLP to the other end of the link. Unlike TLP, DLLP is guarded by 16-bit CRC to detect if data corruption occurs.

In addition, the Media Access Control (MAC) block, which is consisted of LTSSM, multiple lanes deskew, scrambler/de-scrambler, clock correction from inserting skip order-set, and PIPE-related control/status circuits, is implemented to interface physical layer with data link layer.

5.3 TRANSACTION LAYER RECEIVE BLOCK (TLP DECAPSULATION)

The receiving end of the transaction layer performs header information retrieval and TC/VC mapping (see section 5.5), and it validates the correctness of the transaction type and format. If the TLP is found to contain illegal header or the indicated packet length mismatches with the actual packet length, then a Malformed TLP is reported as an error associated with the receiving port. To ensure end-to-end data integrity, a 32-bit ECRC is checked against the TLP at the receiver if the digest bit is set in header.

5.4 ROUTING

The transaction layer implements three types of routing protocols: ID-based, address-based, and implicit routing. For configuration reads, configuration writes, transaction completion, and user-defined messages, the packets are routed by their destination ID constituted of bus number, device number, and function number. Address routing is employed to forward I/O or memory transactions to the destination port, which is located within the address range indicated by the address field carried in the packet header. The packet header indicates the packet types including memory read, memory write, IO read, IO write, Message Signaling Interrupt (MSI) and user-defined message. Implicit routing is mainly used to forward system message transactions such as virtual interrupt line, power management, and so on. The message type embedded in the packet header determines the routing mechanism.

If the incoming packet can not be forwarded to any other port due to a miss to hit the defined address range or targeted ID, this is considered as Unsupported Request (UR) packet, which is similar to a master abort event in PCI protocol.

5.5 TC/VC MAPPING

The 3-bit TC field defined in the header identifies the traffic class of the incoming packets. To enable the differential service, a TC/VC mapping table at destination port that is pre-programmed by system software or EEPROM pre-load is utilized to cast the TC labeled packets into the desired virtual channel. Note that TC0 traffic is mapped into VC0 channel by default. After the TC/VC mapping, the receive block dispatches the incoming request, completion, or data into the appropriate VC0 and VC1 queues.

5.6 QUEUE

In PCI Express, it defines six different packet types to represent request, completion, and data. They are respectively Posted Request Header (PH), Posted Request Data payload (PD), Non-Posted Request Header (NPH), Non-Posted Data Payload (NPD), Completion Header (CPLH) and Completion Data payload (CPLD). Each packet with different type would be put into a separate queue in order to facilitate the following ordering processor. Since NPD usually contains one DW, it can be merged with the corresponding NPH into a common queue named NPHD. Except NPHD, each virtual channel (VC0 or VC1) has its own corresponding packet header and data queue. When only VC0 is needed in some applications, VC1 can be disabled and its resources assigned to VC0 by asserting VC1_EN (Virtual Channel 1 Enable) to low.

5.6.1 PH

PH queue provides TLP header spaces for posted memory writes and various message request headers. Each header space occupies sixteen bytes to accommodate 3 DW or 4 DW headers. There are two PH queues for VC0 and VC1 respectively.

5.6.2 PD

PD queue is used for storing posted request data. If the received TLP is of the posted request type and is determined to have payload coming with the header, the payload data would be put into PD queue. There are two PD queues for VC0 and VC1 respectively.

5.6.3 NPHD

NPHD queue provides TLP header spaces for non-posted request packets, which include memory read, IO read, IO write, configuration read, and configuration write. Each header space takes twenty bytes to accommodate a 3-DW header, s 4-DW header, s 3-WD header with 1-DW data, and a 4-DW header with 1-DW data. There is only one NPHD queue for VC0, since non-posted request cannot be mapped into VC1.

5.6.4 CPLH

CPLH queue provides TLP header space for completion packets. Each header space takes twelve bytes to accommodate a 3-DW header. Please note that there is no 4-DW completion headers. There are two CPLH queues for VC0 and VC1 respectively.

5.6.5 CPLD

CPLD queue is used for storing completion data. If the received TLP is of the completion type and is determined to have payload coming with the header, the payload data would be put into CPLD queue. There are two CPLD queues for VC0 and VC1 respectively.

5.7 TRANSACTION ORDERING

Within a VPPB, a set of ordering rules is defined to regulate the transactions on the PCI Express Switch including Memory, IO, Configuration and Messages, in order to avoid deadlocks and to support the Producer-Consumer model. The ordering rules defined in table 5-4 apply within a single Traffic Class (TC). There is no ordering requirement among transactions within different TC labels. Since the transactions with the same TC label are not allowed to map into different virtual channels, it implies no ordering relationship between the traffic in VC0 and VC1.

Table 5-4 Summary of PCI Express Ordering Rules

Row Pass Column	Posted Request	Read Request	Non-posted Write Request	Read Completion	Non-posted Write Completion
Posted Request	Yes/No[1]	Yes[5]	Yes[5]	Yes[5]	Yes[5]
Read Request	No[2]	Yes	Yes	Yes	Yes
Non-posted Write Request	No[2]	Yes	Yes	Yes	Yes
Read Completion	Yes/No[3]	Yes	Yes	Yes	Yes
Non-Posted Write Completion	Yes[4]	Yes	Yes	Yes	Yes

1. When the Relaxed Ordering Attribute bit is cleared, the Posted Request transactions including memory write and message request must complete on the egress bus of VPPB in the order in which they are received on the ingress bus of VPPB. If the Relaxed Ordering Attribute bit is set, the Posted Request is permitted to pass over other Posted Requests occurring before it.

2. A Read Request transmitting in the same direction as a previously queued Posted Request transaction must push the posted write data ahead of it. The Posted Request transaction must complete on the egress bus before the Read Request can be attempted on the egress bus. The Read transaction can go to the same location as the Posted data. Therefore, if the Read transaction were to pass the Posted transaction, it would return stale data.

3. When the Relaxed Ordering Attribute bit is cleared, a Read completion must ‘‘pull’’ ahead of previously queued posted data transmitting in the same direction. In this case, the read data transmits in the same direction as the posted data, and the requestor of the read transaction is on the same side of the VPPB as the completer of the posted transaction. The posted transaction must deliver to the completer before the read data is returned to the requestor. If the Relaxed Ordering Attribute bit is set, then a read completion is permitted to pass a previously queued Memory Write or Message Request.

4. Non-Posted Write Completions are permitted to pass a previous Memory Write or Message Request transaction. Such transactions are actually transmitting in the opposite directions and hence have no ordering relationship.

5. Posted Request transactions must be given opportunities to pass Non-posted Read and Write Requests as well as Completions. Otherwise, deadlocks may occur when some older Bridges that do not support delayed transactions are mixed with PCIe Switch in the same system. A fairness algorithm is used to arbitrate between the Posted Write queue and the Non-posted transaction queue.

5.8 PORT ARBITRATION

Among multiple ingress ports, the port arbitration built in the egress port determines which input traffic to be forwarded to the output port. The arbitration algorithm contains hardware fixed Round Robin, 128-phase Weighted Round-Robin and programmable 128-phase time-based WRR. The port arbitration is held within the same VC channel. It means that each port has two port arbitration circuitries for VC0 and VC1 respectively. At upstream port, in addition to the traffic from inter-port, the intra-port packet such as configurations completion would also join the arbitration loop to get the service in Virtual Channel 0.

5.9 VC ARBITRATION

After port arbitration, VC arbitration is executed among different VC channels within the same source. Three arbitration algorithms are provided to choose the appropriate VC. They are respectively Strict Priority, Round Robin or Weighted Round Robin.

5.10 FLOW CONTROL

PCI Express employs Credit-Based Flow Control mechanism to make buffer utilization more efficient. The transaction layer transmitter ensures that it does not transmit a TLP to an opposite receiver unless the receiver has enough buffer space to accept the TLP. The transaction layer receiver has the responsibility to advertise the free buffer space to an opposite transmitter to avoid packet stale. In this switch, each port has separate queues for different traffic types and the credits are on the fly sent to data link layer, which compares the current available credits with the monitored one and reports the updated credit to the counterpart. If no new credit is acquired, the credit reported is scheduled for every 30 us to prevent from link entering retrain. On the other hand, the receiver at each egress port gets the usable credits from the opposite end in a link. It would broadcast them to all the other ingress ports for gating the packet transmission.

5.11 TRANSATION LAYER TRANSMIT BLOCK (TLP ENCAPSULATION)

The transmit portion of transaction layer performs the following functions. They are to construct the all types of forwarded TLP generated from VC arbiter, respond with the completion packet when the local resource (i.e. configuration register) is accessed and regenerate the message that terminated at receiver to RC if acts as an upstream port.

6 EEPROM INTERFACE AND SYSTEM MANAGEMENT BUS

The EEPROM interface consists of two pins: EECLK (EEPROM clock output) and EEPD (EEPROM bi-directional serial data). The Switch may control an ISSI IS24C04 or compatible parts using into 512x8 bits. The EEPROM is used to initialize a number of registers before enumeration. This is accomplished after PRST# is de-asserted, at which time the data from the EEPROM is loaded. The EEPROM interface is organized into a 16-bit base, and the Switch supplies a 7-bit EEPROM word address. The Switch does not control the EEPROM address input. It can only access the EEPROM with address input set to 0.

The System Management Bus interface consists of two pins: SMBCLK (System Management Bus Clock input) and SMBDATA (System Management Bus Data input/ output).

6.1 EEPROM INTERFACE

6.1.1 AUTO MODE EERPOM ACCESS

The Switch may access the EEPROM in a WORD format by utilizing the auto mode through a hardware sequencer. The EEPROM start-control, address, and read/write commands can be accessed through the configuration register. Before each access, the software should check the Autoload Status bit before issuing the next start.

6.1.2 EEPROM MODE AT RESET

During a reset, the Switch will automatically load the information/data from the EEPROM if the automatic load condition is met. The first offset in the EEPROM contains a signature. If the signature is recognized, the autoload initiates right after the reset.

During the autoload, the Bridge will read sequential words from the EEPROM and write to the appropriate registers. Before the Bridge registers can be accessed through the host, the autoload condition should be verified by reading bit [3] offset DCh (EEPROM Autoload Status). The host access is allowed only after the status of this bit is set to '0' which indicates that the autoload initialization sequence is complete.

6.1.3 EEPROM SPACE ADDRESS MAP

15 – 8	7 – 0	BYTE OFFSET
EEPROM Signature (1516h)		00h
Vendor ID		02h
Device ID		04h
Extended VC Count / Link Capability / Switch Mode Operation / Interrupt pin for Port 1 ~ 4		06h
Subsystem Vender ID		08h
Subsystem ID		0Ah
Max_Payload_Size Support / ASPM Support / Role_Base Error Reporting / RefClk ppm Difference		0Ch
Reserved		0Eh
PM Data for Port 0	PM Capability for Port 0	10h
PM Data for Port 1	PM Capability for Port 1	12h
PM Data for Port 2	PM Capability for Port 2	14h
PM Data for Port 3	PM Capability for Port 3	16h
PM Data for Port 4	PM Capability for Port 4	18h
Reserved		1Ah

15 – 8	7 – 0	BYTE OFFSET
Reserved		1Ch
Reserved		1Eh
TC/VC Map for Port 0 (VC0)	Slot Clock / LPVC Count / Port Num, Port 0	20h
TC/VC Map for Port 1(VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 1	22h
TC/VC Map for Port 2 (VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 2	24h
TC/VC Map for Port 3 (VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 3	26h
TC/VC Map for Port 4 (VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 4	28h
Reserved		2Ah
Reserved		2Ch
Reserved		2Eh
Reserved		30h
Slot Capability 0 for Port 1		32h
Slot Capability 0 for Port 2		34h
Slot Capability 0 for Port 3		36h
Slot Capability 0 for Port 4		38h
Reserved		3Ah
Reserved		3Ch
Reserved		3Eh
Reserved		40h
Slot Capability 1 for Port 1		42h
Slot Capability 1 for Port 2		44h
Slot Capability 1 for Port 3		46h
Slot Capability 1 for Port 4		48h
Reserved		4Ah
Reserved		4Ch
Reserved		4Eh
TC/VC Map for Port 0 (VC1)	Maximum Time Slot for Port 0	50h
TC/VC Map for Port 1 (VC1)	Maximum Time Slot for Port 1	52h
TC/VC Map for Port 2 (VC1)	Maximum Time Slot for Port 2	54h
TC/VC Map for Port 3 (VC1)	Maximum Time Slot for Port 3	56h
TC/VC Map for Port 4 (VC1)	Maximum Time Slot for Port 4	58h
Reserved		5Ah
Reserved		5Ch
Reserved		5Eh
Power Budgeting Capability Register for Port 0		60h
Power Budgeting Capability Register for Port 1		62h
Power Budgeting Capability Register for Port 2		64h
Power Budgeting Capability Register for Port 3		66h
Power Budgeting Capability Register for Port 4		68h
Reserved		6Ah
Reserved		6Ch
Reserved		6Eh
Replay Time-out Counter for Port 0		70h
Replay Time-out Counter for Port 1		72h
Replay Time-out Counter for Port 2		74h
Replay Time-out Counter for Port 3		76h
Replay Time-out Counter for Port 4		78h
Reserved		7Ah
Reserved		7Ch
Reserved		7Eh
Acknowledge Latency Timer for Port 0		80h
Acknowledge Latency Timer for Port 1		82h
Acknowledge Latency Timer for Port 2		84h
Acknowledge Latency Timer for Port 3		86h
Acknowledge Latency Timer for Port 4		88h
Reserved		8Ah
Reserved		8Ch
Reserved		8Eh

15 – 8	7 – 0	BYTE OFFSET
PHY Parameter for Port 0		90h
PHY Parameter for Port 1		92h
PHY Parameter for Port 2		94h
PHY Parameter for Port 3		96h
PHY Parameter for Port 4		98h
Reserved		9Ah
Reserved		9Ch
Reserved		9Eh
Reserved	PM Control Para/Rx Polarity for Port 0	A0h
Reserved	PM Control Para/Rx Polarity for Port 1	A2h
Reserved	PM Control Para/Rx Polarity for Port 2	A4h
Reserved	PM Control Para/Rx Polarity for Port 3	A6h
Reserved	PM Control Para/Rx Polarity for Port 4	A8h

6.1.4 MAPPING EEPROM CONTENTS TO CONFIGURATION REGISTERS

ADDRESS	PCI CFG OFFSET	DESCRIPTION
00h		**EEPROM signature** – 1516h
02h	00h ~ 01h	**Vendor ID**
04h	02h ~ 03h	**Device ID**
06h	144h (Port 0~4) 144h: Bit [0] ECh (Port 0~4) ECh: Bit [14:12] ECh: Bit [17:15] B4h (Port 0~4) B4h:Bit [5] Bit [6] Bit [0] Bit [2:1] Bit [3] Bit [4] 3Ch (Port 1~4) 3Ch: Bit [8]	**Extended VC Count for Port 0 ~ 4** ▪ Bit [0]: It represents the supported VC count other than the default VC **Link Capability for Port 0 ~ 4** ▪ Bit [3:1]: It represents L0s Exit Latency for all ports ▪ Bit [6:4]: It represents L1 Exit Latency for all ports **Switch Mode Operation for Port 0** ▪ Bit [8]: no ordering on packets for different egress port mode ▪ Bit [9]: no ordering on different tag of completion mode ▪ Bit [10]: Store and Forward ▪ Bit [12:11]: Cut-through Threshold ▪ Bit [13] : Port arbitrator Mode ▪ Bit [14]: Credit Update Mode **Interrupt pin for Port 1 ~ 4** ▪ Bit [15]: Set when INTA is requested for interrupt resource
08h	BCh: Bit [15:0]	**Subsystem Vender ID**
0Ah	BCh: Bit [31:16]	**Subsystem ID**
0Ch	E4h(Port 0~4) E4h: Bit 0 ECh(Port 0~4) ECh: Bit[11:10] E4h(Port 0~4) E4h: Bit[15] B0h(port 0~4) B0h : Bit [14] B0h(port 0~4) B0h : Bit [15] B4h(port 0~4) B4h : Bit [15]	**Max_Payload_Size Support for Port 0 ~ 4** ▪ Bit [0]: Indicated the maximum payload size that the device can support for the TLP **ASPM Support for Port 0 ~ 4** ▪ Bit [2:1] : Indicate the level of ASPM supported on the PCIe link **Role_Base Error Reporting for Port 0 ~ 4** ▪ Bit [3] : Indicate implement the role-base error reporting **MSI Capability Disable for Port 0~4** ▪ Bit [4] : Disable MSI capability **AER Capability Disable for Port 0~4** ▪ Bit [5] : Disable AER capability **Compliance Pattern Parity Control Disable for Port 0~4** ▪ Bit [6] : Disable compliance pattern parity

ADDRESS	PCI CFG OFFSET	DESCRIPTION
	B0h(port 0~4) B0h : Bit [13] A8h(Port 0~4) A8h: Bit [14:13]	**Power Management Capability Disable for Port 0~4** ▪ Bit [7] : Disable Power Management Capability **RefClk ppm Difference for Port 0 ~ 4** ▪ Bit [9:8]: It represents RefClk ppm difference between the two ends in one link; 00: 0 ppm, 01: 100 ppm, 10: 200 ppm, 11: 300 ppm
10h	84h (Port 0) 84h: Bit [3] 80h (Port 0) 80h: Bit [24:22] 80h: Bit [25] 80h: Bit [26] 80h: Bit [29:28]	**No_Soft_Reset for Port 0** ▪ Bit [0]: No_Soft_Reset. **Power Management Capability for Port 0** ▪ Bit [3:1]: AUX Current. ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states
11h	84h (Port 0) 84h: Bit [31:24]	**Power Management Data for Port 0** ▪ Bit [15:8]: read only as Data register
12h	84h (Port 1) 84h: Bit [3] 80h (Port 1) 80h: Bit [24:22] 80h: Bit [25] 80h: Bit [26] 80h: Bit [29:28]	**No_Soft_Reset for Port 1** ▪ Bit [0]: No_Soft_Reset. **Power Management Capability for Port 1** ▪ Bit [3:1]: AUX Current. ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states
13h	84h (Port 1) 84h: Bit [31:24]	**Power Management Data for Port 1** ▪ Bit [15:8] – read only as Data register
14h	84h (Port 2) 84h: Bit [3] 80h (Port 2) 80h: Bit [24:22] 80h: Bit [25] 80h: Bit [26] 80h: Bit [29:28]	**No_Soft_Reset for Port 2** ▪ Bit [0]: No_Soft_Reset **Power Management Capability for Port 2** ▪ Bit [3:1]: AUX Current ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states
15h	84h (Port 2) 84h: Bit [31:24]	**Power Management Data for Port 2** ▪ Bit [15:8] – read only as Data register
16h	84h (Port 3) 84h: Bit [3] 80h (Port 3) 80h: Bit [24:22] 80h: Bit [25] 80h: Bit [26] 80h: Bit [29:28]	**No_Soft_Reset for Port 3** ▪ Bit [0]: No_Soft_Reset **Power Management Capability for Port 3** ▪ Bit [3:1]: AUX Current ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states
17h	84h (Port 3) 84h: Bit [31:24]	**Power Management Data for Port 3** ▪ Bit [15:8] – read only as Data register
18h	84h (Port 4) 84h: Bit [3] 80h (Port 4) 80h: Bit [24:22] 80h: Bit [25] 80h: Bit [26]	**No_Soft_Reset for Port 4** ▪ Bit [0]: No_Soft_Reset **Power Management Capability for Port 4** ▪ Bit [3:1]: AUX Current ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state

ADDRESS	PCI CFG OFFSET	DESCRIPTION
	80h: Bit [29:28]	▪ Bit [7:6]: PME Support for D2 and D1 states
19h	84h (Port 4) 84h: Bit [31:24]	**Power Management Data for Port 4** ▪ Bit [15:8] – read only as Data register
20h	F0h (Port 0) F0h: Bit [28] 80h (Port 0) 80h: Bit[21] 144h (Port 0) 144h: Bit [4] ECh (Port 0) ECh: Bit [26:24]	**Slot Clock Configuration for Port 0** ▪ Bit [1]: When set, the component uses the clock provided on the connector **Device specific Initialization for Port 0** ▪ Bit [2]: When set, the DSI is required **LPVC Count for Port 0** ▪ Bit [3]: When set, the VC1 is allocated to LPVC of Egress Port 0 **Port Number for Port 0** ▪ Bit [6:4]: It represents the logic port numbering for physical port 0
	154h (Port 0) 154h: Bit [7:1]	**VC0 TC/VC Map for Port 0** ▪ Bit [15:9]: When set, it indicates the corresponding TC is mapped into VC0
22h	E0h (Port1) E0h: Bit [24] F0h (Port 1) F0h: Bit [28] 80h (Port 1) 80h: Bit[21] 144h (Port 1) 144h: Bit [4] ECh (Port 1) ECh: Bit [26:24]	**PCIe Capability Slot Implemented for Port 1** ▪ Bit [0]: When set, the slot is implemented for Port 1 **Slot Clock Configuration for Port 1** ▪ Bit [1]: When set, the component uses the clock provided on the Connector **Device specific Initialization for Port 1** ▪ Bit [2]: When set, the DSI is required **LPVC Count for Port 1** ▪ Bit [3]: When set, the VC1 is allocated to LPVC of Egress Port 1 **Port Number for Port 1** ▪ Bit [6:4]: It represents the logic port numbering for physical port 1
	154h (Port 1) 154h: Bit [7:1]	**VC0 TC/VC Map for Port 1** ▪ Bit [15:9]: When set, it indicates the corresponding TC is mapped into VC0
24h	E0h (Port 2) E0h: Bit [24] F0h (Port 2) F0h: Bit [28] 80h (Port 2) 80h: Bit[21] 144h (Port 2) 144h: Bit [4] ECh (Port 2) ECh: Bit [26:24]	**PCIe Capability Slot Implemented for Port 2** ▪ Bit [0]: When set, the slot is implemented for Port 2 **Slot Clock Configuration for Port 2** ▪ Bit [1]: When set, the component uses the clock provided on the Connector **Device specific Initialization for Port 2** ▪ Bit [2]: When set, the DSI is required **LPVC Count for Port 2** ▪ Bit [3]: When set, the VC1 is allocated to LPVC of Egress Port 2 **Port Number for Port 2** ▪ Bit [6:4]: It represents the logic port numbering for physical port 2
	154h (Port 2) 154h: Bit [7:1]	**VC0 TC/VC Map for Port 2** ▪ Bit [15:9]: When set, it indicates the corresponding TC is mapped into VC0

ADDRESS	PCI CFG OFFSET	DESCRIPTION
26h	E0h (Port 3) E0h: Bit [24] F0h (Port 3) F0h: Bit [28] 80h (Port 3) 80h: Bit[21] 144h (Port 3) 144h: Bit [4] ECh (Port 3) ECh: Bit [26:24]	**PCIe Capability Slot Implemented for Port 3** ▪ Bit [0]: When set, the slot is implemented for Port 3 **Slot Clock Configuration for Port 3** ▪ Bit [1]: When set, the component uses the clock provided on the Connector **Device specific Initialization for Port 3** ▪ Bit [2]: When set, the DSI is required **LPVC Count for Port 3** ▪ Bit [3]: When set, the VC1 is allocated to LPVC of Egress Port 3 **Port Number for Port 3** ▪ Bit [6:4]: It represents the logic port numbering for physical port 3
	154h (Port 3) 154h: Bit [7:1]	**VC0 TC/VC Map for Port 3** ▪ Bit [15:9]: When set, it indicates the corresponding TC is mapped into VC0
28h	E0h (Port 4) E0h: Bit [24] F0h (Port 4) F0h: Bit [28] 80h (Port 4) 80h: Bit[21] 144h (Port 4) 144h: Bit [4] ECh (Port 4) ECh: Bit [26:24]	**PCIe Capability Slot Implemented for Port 4** ▪ Bit [0]: When set, the slot is implemented for Port 4 **Slot Clock Configuration for Port 4** ▪ Bit [1]: When set, the component uses the clock provided on the Connector **Device specific Initialization for Port 4** ▪ Bit [2]: When set, the DSI is required **LPVC Count for Port 4** ▪ Bit [3]: When set, the VC1 is allocated to LPVC of Egress Port 4 **Port Number for Port 4** ▪ Bit [6:4]: It represents the logic port numbering for physical port 4
	154h (Port 4) 154h: Bit [7:1]	**VC0 TC/VC Map for Port 4** ▪ Bit [15:9]: When set, it indicates the corresponding TC is mapped into VC0
32h	F4h (Port 1) F4h: Bit [15:0]	**Slot Capability 0 of Port 1** ▪ Bit [15:0]: Mapping to the low word of slot capability register
34h	F4h (Port 2) F4h: Bit [15:0]	**Slot Capability 0 of Port 2** ▪ Bit [15:0]: Mapping to the low word of slot capability register
36h	F4h (Port 3) F4h: Bit [15:0]	**Slot Capability 0 of Port 3** ▪ Bit [15:0]: Mapping to the low word of slot capability register
38h	F4h (Port 4) F4h: Bit [15:0]	**Slot Capability 0 of Port 4** ▪ Bit [15:0]: Mapping to the low word of slot capability register
42h	F4h (Port 1) F4h: Bit [31:16]	**Slot Capability 1 of Port 1** ▪ Bit [15:0]: Mapping to the high word of slot capability register
44h	F4h (Port 2) F4h: Bit [31:16]	**Slot Capability 1 of Port 2** ▪ Bit [15:0]: Mapping to the high word of slot capability register
46h	F4h (Port 3) F4h: Bit [31:16]	**Slot Capability 1 of Port 3** ▪ Bit [15:0]: Mapping to the high word of slot capability register
48h	F4h (Port 4) F4h: Bit [31:16]	**Slot Capability 1 of Port 4** ▪ Bit [15:0]: Mapping to the high word of slot capability register
50h	15Ch (Port 0) 15Ch: Bit [22:16] 160h: Bit [7:0]	**VC1 MAX Time Slot and TC/VC Map for Port 0** ▪ Bit [6:0]: The maximum time slot supported by VC1 ▪ Bit [15:8]: When set, it indicates the corresponding TC is mapped into VC1
52h	15Ch (Port 1) 15Ch: Bit [22:16] 160h: Bit [7:0]	**VC1 MAX Time Slot and TC/VC Map for Port 1** ▪ Bit [6:0]: The maximum time slot supported by VC1 ▪ Bit [15:8]: When set, it indicates the corresponding TC is mapped into VC1

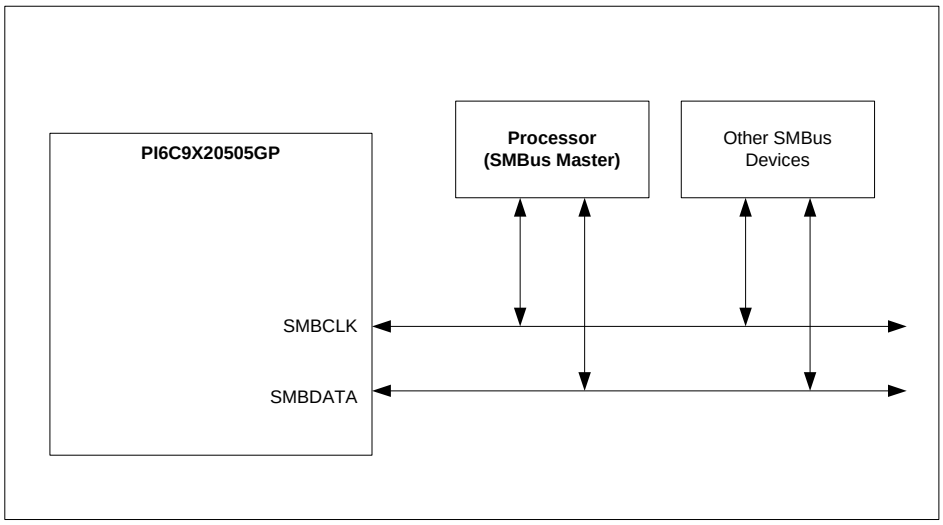
ADDRESS	PCI CFG OFFSET	DESCRIPTION
54h	15Ch (Port 2) 15Ch: Bit [22:16] 160h: Bit [7:0]	**VC1 MAX Time Slot and TC/VC Map for Port 2** ▪ Bit [6:0]: The maximum time slot supported by VC1 ▪ Bit [15:8]: When set, it indicates the corresponding TC is mapped into VC1
56h	15Ch (Port 3) 15Ch: Bit [22:16] 160h: Bit [7:0]	**VC1 MAX Time Slot and TC/VC Map for Port 3** ▪ Bit [6:0]: The maximum time slot supported by VC1 ▪ Bit [15:8]: When set, it indicates the corresponding TC mapped into VC1
58h	15Ch (Port 4) 15Ch: Bit [22:16] 160h: Bit [7:0]	**VC1 MAX Time Slot and TC/VC Map for Port 4** ▪ Bit [6:0]: The maximum time slot supported by VC1 ▪ Bit [15:8]: When set, it indicates the corresponding TC is mapped into VC1
60h	214h (Port 0) 214h: Bit [7:0] 214h: Bit [9:8] 214h: Bit [14:13] 218h: Bit [0]	**Power Budget Register for Port 0** ▪ Bit [7:0]: Base Power ▪ Bit [9:8]: Data Scale ▪ Bit [11:10]: PM State ▪ Bit [15]: System Allocated
62h	214h (Port 1) 214h: Bit [7:0] 214h: Bit [9:8] 214h: Bit [14:13] 218h: Bit [0]	**Power Budget Register for Port 1** ▪ Bit [7:0]: Base Power ▪ Bit [9:8]: Data Scale ▪ Bit [11:10]: PM State ▪ Bit [15]: System Allocated
64h	214h (Port 2) 214h: Bit [7:0] 214h: Bit [9:8] 214h: Bit [14:13] 218h: Bit [0]	**Power Budget Register for Port 2** ▪ Bit [7:0]: Base Power ▪ Bit [9:8]: Data Scale ▪ Bit [11:10]: PM State ▪ Bit [15]: System Allocated
66h	214h (Port 3) 214h: Bit [7:0] 214h: Bit [9:8] 214h: Bit [14:13] 218h: Bit [0]	**Power Budget Register for Port 3** ▪ Bit [7:0]: Base Power ▪ Bit [9:8]: Data Scale ▪ Bit [11:10]: PM State ▪ Bit [15]: System Allocated
68h	214h (Port 4) 214h: Bit [7:0] 214h: Bit [9:8] 214h: Bit [14:13] 218h: Bit [0]	**Power Budget Register for Port 4** ▪ Bit [7:0]: Base Power ▪ Bit [9:8]: Data Scale ▪ Bit [11:10]: PM State ▪ Bit [15]: System Allocated
70h	B0h (Port 0) B0h: Bit [15:0]	**Replay Time-out Counter for Port 0** ▪ Bit [15:0]: Relay Time-out Counter
72h	B0h (Port 1) B0h: Bit [15:0]	**Replay Time-out Counter for Port 1** ▪ Bit [15:0]: Relay Time-out Counter
74h	B0h (Port 2) B0h: Bit [15:0]	**Replay Time-out Counter for Port 2** ▪ Bit [15:0]: Relay Time-out Counter
76h	B0h (Port 3) B0h: Bit [15:0]	**Replay Time-out Counter for Port 3** ▪ Bit [15:0]: Relay Time-out Counter
78h	B0h (Port 4) B0h: Bit [15:0]	**Replay Time-out Counter for Port 4** ▪ Bit [15:0]: Relay Time-out Counter
80h	B0h (Port 0) B0h: Bit [31:16]	**Acknowledge Latency Timer for Port 0** ▪ Bit [31:16]: Acknowledge Latency Timer
82h	B0h (Port 1) B0h: Bit [31:16]	**Acknowledge Latency Timer for Port 1** ▪ Bit [31:16]: Acknowledge Latency Timer
84h	B0h (Port 2) B0h: Bit [31:16]	**Acknowledge Latency Timer for Port 2** ▪ Bit [31:16]: Acknowledge Latency Timer
86h	B0h (Port 3) B0h: Bit [31:16]	**Acknowledge Latency Timer for Port 3** ▪ Bit [31:16]: Acknowledge Latency Timer
88h	B0h (Port 4) B0h: Bit [31:16]	**Acknowledge Latency Timer for Port 4** ▪ Bit [31:16]: Acknowledge Latency Timer
90h	B4h (Port 0) B4h: Bit [31:16]	**PHY Parameter for Port 0** ▪ Bit [31:16]: PHY Parameter
92h	B4h (Port 1) B4h: Bit [31:16]	**PHY Parameter for Port 1** ▪ Bit [31:16]: PHY Parameter
94h	B4h (Port 2) B4h: Bit [31:16]	**PHY Parameter for Port 2** ▪ Bit [31:16]: PHY Parameter

ADDRESS	PCI CFG OFFSET	DESCRIPTION
96h	B4h (Port 3) B4h: Bit [31:16]	**PHY Parameter for Port 3** ▪ Bit [31:16]: PHY Parameter
98h	B4h (Port 4) B4h: Bit [31:16]	**PHY Parameter for Port 4** ▪ Bit [31:16]: PHY Parameter
A0h	B4h (Port 0) B4h: Bit [13:8] B4h (Port 0) B4h: Bit [14]	**PM Control Parameter for Port 0** ▪ Bit [5:4] : L0s enable ▪ Bit [3:2] : L1 delay count select ▪ Bit [1:0] : D3 enters L1 **Rx Polarity Inversion Disable for port 0** ▪ Bit [6] : Disable Rx polarity capability
A2h	B4h (Port 1) B4h: Bit [13:8] B4h (Port 1) B4h: Bit [14]	**PM Control Parameter for Port 1** ▪ Bit [5:4] : L0s enable ▪ Bit [3:2] : L1 delay count select ▪ Bit [1:0] : D3 enters L1 **Rx Polarity Inversion Disable for port 1** ▪ Bit [6] : Disable Rx polarity capability
A4h	B4h (Port 2) B4h: Bit [13:8] B4h (Port 2) B4h: Bit [14]	**PM Control Parameter for Port 2** ▪ Bit [5:4] : L0s enable ▪ Bit [3:2] : L1 delay count select ▪ Bit [1:0] : D3 enters L1 **Rx Polarity Inversion Disable for port 2** ▪ Bit [6] : Disable Rx polarity capability
A6h	B4h (Port 3) B4h: Bit [13:8] B4h (Port 3) B4h: Bit [14]	**PM Control Parameter for Port 3** ▪ Bit [5:4] : L0s enable ▪ Bit [3:2] : L1 delay count select ▪ Bit [1:0] : D3 enters L1 **Rx Polarity Inversion Disable for port 3** ▪ Bit [6] : Disable Rx polarity capability
A8h	B4h (Port 4) B4h: Bit [13:8] B4h (Port 4) B4h: Bit [14]	**PM Control Parameter for Port 4** ▪ Bit [5:4] : L0s enable ▪ Bit [3:2] : L1 delay count select ▪ Bit [1:0] : D3 enters L1 **Rx Polarity Inversion Disable for port 4** Bit [6] : Disable Rx polarity capability

6.2 SMBus INTERFACE

The PI7C9X20505GP provides the System Management Bus (SMBus), a two-wire interface through which a simple device can communicate with the rest of the system. The SMBus interface on the PI7C9X20505GP is a bi-directional slave interface. It can receive data from the SMBus master or send data to the master. The interface allows full access to the configuration registers. A SMBus master, such as the processor or other SMBus devices, can read or write to every RW configuration register (read/write register). In addition, the RO and HwInt registers (read-only and hardware initialized registers) that can be auto-loaded by the EEPROM interface can also be read and written by the SMBus interface. This feature allows increases in the system expandability and flexibility in system implementation.

Figure 6-1 SMBus Architecture Implementation on PI7C9X20505GP



The SMBus interface on the PI7C9X20505GP consists of one SMBus clock pin (SMBCLK), a SMBus data pin (SMBDATA), and 3 SMBus address pins (GPIO[5:7]). The SMBus clock pin provides or receives the clock signal. The SMBus data pin facilitates the data transmission and reception. Both of the clock and data pins are bi-directional. The SMBus address pins determine the address to which the PI7C9X20505GP responds to. The SMBus address pins generate addresses according to the following table:

Table 6-1 SMBus Address Pin Configuration

BIT	SMBus Address
0	GPIO[5]
1	GPIO[6]
2	GPIO[7]
3	1
4	0
5	1
6	1

7 REGISTER DESCRIPTION

7.1 REGISTER TYPES

REGISTER TYPE	DEFINITION
HwInt	Hardware Initialization
RO	Read Only
RW	Read / Write
RWC	Read / Write 1 to Clear
RWCS	Sticky - Read Only / Write 1 to Clear
RWS	Sticky - Read / Write
ROS	Sticky – Read Only

7.2 TRANSPARENT MODE CONFIGURATION REGISTERS

When the port of the Switch is set to operate at the transparent mode, it is represented by a logical PCI-to-PCI Bridge that implements type 1 configuration space header. The following table details the allocation of the register fields of the PCI 2.3 compatible type 1 configuration space header.

31 –24	23 – 16	15 - 8	7 –0	BYTE OFFSET
Device ID		Vendor ID		00h
Primary Status		Command		04h
Class Code			Revision ID	08h
Reserved	Header Type	Primary Latency Timer	Cache Line Size	0Ch
Reserved				10h – 17h
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status		I/O Limit Address	I/O Base Address	1Ch
Memory Limit Address		Memory Base Address		20h
Prefetchable Memory Limit Address		Prefetchable Memory Base Address		24h
Prefetchable Memory Base Address Upper 32-bit				28h
Prefetchable Memory Limit Address Upper 32-bit				2Ch
I/O Limit Address Upper 16-bit		I/O Base Address Upper 16-bit		30h
Reserved			Capability Pointer to 80h	34h
Reserved				38h
Bridge Control		Interrupt Pin	Interrupt Line	3Ch
Reserved				40h – 7Fh
Power Management Capabilities		Next Item Pointer=8C	Capability ID=01	80h
PM Data	PPB Support Extensions	Power Management Data		84h
Message Control		Next Item Pointer=9C	Capability ID=05	8Ch
Message Address				90h
Message Upper Address				94h
Reserved		Message Data		98h
VPD Register		Next Item Pointer=A4	Capability ID=03	9Ch
VPD Data Register				A0h
Length in Bytes (14h)		Next Item Pointer=B8	Capability ID=09	A4h
XPIP_CSR0				A8h
XPIP_CSR1				ACh
ACK Latency Timer		Replay Time-out Counter		B0h
Reserved			Forwarding Modes	B4h
Reserved		Next Item Pointer=E0	SSID/SSVID Capability ID=0D	B8h
SSID		SSVID		BCh
Reserved				C0h – D7h

31 –24	23 – 16	15 - 8	7 –0	BYTE OFFSET
GPIO Data and Control				D8h
EEPROM Data		EEPROM Address	EEPROM Control	DCh
PCI Express Capabilities Register		Next Item Pointer=00	Capability ID=10	E0h
Device Capabilities				E4h
Device Status		Device Control		E8h
Link Capabilities				ECh
Link Status		Link Control		F0h
Slot Capabilities				F4h
Slot Status		Slot Control		F8h
Reserved				FCh

Other than the PCI 2.3 compatible configuration space header, the Switch also implements PCI express extended configuration space header, which includes advanced error reporting, virtual channel, and power budgeting capability registers. The following table details the allocation of the register fields of PCI express extended capability space header. The first extended capability always begins at offset 100h with a PCI Express Enhanced Capability header and the rest of capabilities are located at an offset greater than 0FFh relative to the beginning of PCI compatible configuration space.

31 –24	23 – 16	15 - 8	7 –0	BYTE OFFSET
Next Capability Offset=140h	Cap. Version	PCI Express Extended Capability ID=0001h		100h
Uncorrectable Error Status Register				104h
Uncorrectable Error Mask Register				108h
Uncorrectable Error Severity Register				10Ch
Correctable Error Status Register				110h
Correctable Error Mask Register				114h
Advanced Error Capabilities and Control Register				118h
Header Log Register				11Ch – 128h
Reserved				12Ch – 13Fh
Next Capability Offset=20Ch	Cap. Version	PCI Express Extended Capability ID=0002h		140h
Port VC Capability Register 1				144h
VC Arbitration Table Offset=3	Port VC Capability Register 2			148h
Port VC Status Register		Port VC Control Register		14Ch
Port Arbitration Table Offset=4	VC Resource Capability Register (0)			150h
VC Resource Control Register (0)				154h
VC Resource Status Register (0)		Reserved		158h
Port Arbitration Table Offset=6	VC Resource Capability Register (1)			15Ch
VC Resource Control Register (1)				160h
VC Resource Status Register (1)		Reserved		164h
Reserved				16Ch – 168h
VC Arbitration Table with 32 Phases				170h – 17Ch
Port Arbitration Table with 128 Phases for VC0				180h – 1BCh
Port Arbitration Table with 128 Phases for VC1				1C0h – 1FCh
Reserved				200h – 20Bh
Next Capability Offset=000h	Cap. Version	PCI Express Extended Capability ID=0004h		20Ch
Reserved			Data Select Register	210h
Data Register				214h
Reserved			Power Budget Capability Register	218h

7.2.1 VENDOR ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Vendor ID	RO	Identifies Pericom as the vendor of this device. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 12D8h.

7.2.2 DEVICE ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Device ID	RO	Identifies this device as the PI7C9X20505GP. The default value may be changed by SMBus or auto-loading from EEPROM. Resets to 0505h.

7.2.3 COMMAND REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	I/O Space Enable	RW	0b: Ignores I/O transactions on the primary interface 1b: Enables responses to I/O transactions on the primary interface Resets to 0b.
1	Memory Space Enable	RW	0b: Ignores memory transactions on the primary interface 1b: Enables responses to memory transactions on the primary interface Reset to 0b.
2	Bus Master Enable	RW	0b: Does not initiate memory or I/O transactions on the upstream port and handles as an Unsupported Request (UR) to memory and I/O transactions on the downstream port. For Non-Posted Requests, a completion with UR completion status must be returned 1b: Enables the Switch Port to forward memory and I/O Read/Write transactions in the upstream direction Reset to 0b.
3	Special Cycle Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
4	Memory Write And Invalidate Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
5	VGA Palette Snoop Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
6	Parity Error Response Enable	RW	0b: Switch may ignore any parity errors that it detects and continue normal operation 1b: Switch must take its normal action when a parity error is detected Reset to 0b.
7	Wait Cycle Control	RO	Does not apply to PCI Express. Must be hardwired to 0.
8	SERR# enable	RW	0b: Disables the reporting of Non-fatal and Fatal errors detected by the Switch to the Root Complex b1: Enables the Non-fatal and Fatal error reporting to Root Complex Reset to 0b.
9	Fast Back-to-Back Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
10	Interrupt Disable	RW	Controls the ability of a PCI Express device to generate INTx Interrupt Messages. In the Switch, this bit does not affect the forwarding of INTx messages from the downstream ports. Reset to 0b.
15:11	Reserved	RO	Reset to 0b.

7.2.4 PRIMARY STATUS REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Reserved	RO	Reset to 000b.
19	Interrupt Status	RO	Indicates that an INTx Interrupt Message is pending internally to the device. In the Switch, the forwarding of INTx messages from the downstream device of the Switch port is not reflected in this bit. Must be hardwired to 0b.
20	Capabilities List	RO	Set to 1 to enable support for the capability list (offset 34h is the pointer to the data structure). Reset to 1b.
21	66MHz Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
22	Reserved	RO	Reset to 0b.
23	Fast Back-to-Back Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
24	Master Data Parity Error	RWC	Set to 1 (by a requester) whenever a Parity error is detected or forwarded on the primary side of the port in a Switch. If the Parity Error Response Enable bit is cleared, this bit is never set. Reset to 0b.
26:25	DEVSEL# timing	RO	Does not apply to PCI Express. Must be hardwired to 0b.
27	Signaled Target Abort	RO	Set to 1 (by a completer) whenever completing a request on the primary side using the Completer Abort Completion Status. Reset to 0b.
28	Received Target Abort	RO	Set to 1 (by a requestor) whenever receiving a Completion with Completer Abort Completion Status on the primary side. Reset to 0b.
29	Received Master Abort	RO	Set to 1 (by a requestor) whenever receiving a Completion with Unsupported Request Completion Status on primary side. Reset to 0b.
30	Signaled System Error	RWC	Set to 1 when the Switch sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. Reset to 0b.
31	Detected Parity Error	RWC	Set to 1 whenever the primary side of the port in a Switch receives a Poisoned TLP. Reset to 0b.

7.2.5 REVISION ID REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Revision	RO	Indicates revision number of device. Hardwired to 01h.

7.2.6 CLASS CODE REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Programming Interface	RO	Read as 00h to indicate no programming interfaces have been defined for PCI-to-PCI Bridges.
23:16	Sub-Class Code	RO	Read as 04h to indicate device is a PCI-to-PCI Bridge.
31:24	Base Class Code	RO	Read as 06h to indicate device is a Bridge device.

7.2.7 CACHE LINE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Cache Line Size	RW	The cache line size register is set by the system firmware and the operating system cache line size. This field is implemented by PCI Express devices as a RW field for legacy compatibility, but it has no impact on any PCI Express device functionality. Reset to 0b.

7.2.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Primary Latency timer	RO	Does not apply to PCI Express. Must be hardwired to 00h.

7.2.9 HEADER TYPE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
23:16	Header Type	RO	Read as 01h to indicate that the register layout conforms to the standard PCI-to-PCI Bridge layout.

7.2.10 PRIMARY BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Primary Bus Number	RW	Indicates the number of the PCI bus to which the primary interface is connected. The value is set in software during configuration. Reset to 00h.

7.2.11 SECONDARY BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Secondary Bus Number	RW	Indicates the number of the PCI bus to which the secondary interface is connected. The value is set in software during configuration. Reset to 00h.

7.2.12 SUBORDINATE BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
23:16	Subordinate Bus Number	RW	Indicates the number of the PCI bus with the highest number that is subordinate to the Bridge. The value is set in software during configuration. Reset to 00h.

7.2.13 SECONDARY LATENCY TIMER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	Secondary Latency Timer	RO	Does not apply to PCI Express. Must be hardwired to 00h.

7.2.14 I/O BASE ADDRESS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	32-bit Indicator	RO	Read as 01h to indicate 32-bit I/O addressing.
7:4	I/O Base Address [15:12]	RW	Defines the bottom address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be 0. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O base address upper 16 bits address register. Reset to 0h.

7.2.15 I/O LIMIT ADDRESS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
11:8	32-bit Indicator	RO	Read as 01h to indicate 32-bit I/O addressing.
15:12	I/O Limit Address [15:12]	RW	Defines the top address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be FFFh. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O limit address upper 16 bits address register. Reset to 0h.

7.2.16 SECONDARY STATUS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
20:16	Reserved	RO	Reset to 00000b.
21	66MHz Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
22	Reserved	RO	Reset to 0b.
23	Fast Back-to-Back Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
24	Master Data Parity Error	RWC	Set to 1 (by a requester) whenever a Parity error is detected or forwarded on the secondary side of the port in a Switch. If the Parity Error Response Enable bit is cleared, this bit is never set. Reset to 0b.
26:25	DEVSEL_L timing	RO	Does not apply to PCI Express. Must be hardwired to 0b.
27	Signaled Target Abort	RO	Set to 1 (by a completer) whenever completing a request in the secondary side using Completer Abort Completion Status. Reset to 0b.
28	Received Target Abort	RO	Set to 1 (by a requestor) whenever receiving a Completion with Completer Abort Completion Status in the secondary side. Reset to 0b.
29	Received Master Abort	RO	Set to 1 (by a requestor) whenever receiving a Completion with Unsupported Request Completion Status in secondary side. Reset to 0b.
30	Received System	RWC	Set to 1 when the Switch sends an ERR_FATAL or ERR_NONFATAL

BIT	FUNCTION	TYPE	DESCRIPTION
	Error		Message, and the SERR Enable bit in the Bridge Control register is 1. Reset to 0b.
31	Detected Parity Error	RWC	Set to 1 whenever the secondary side of the port in a Switch receives a Poisoned TLP. Reset to 0b.

7.2.17 MEMORY BASE ADDRESS REGISTER – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Reserved	RO	Reset to 0h.
15:4	Memory Base Address [15:4]	RW	Defines the bottom address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are able to be written to. The lower 20 bits corresponding to address bits [19:0] are assumed to be 0. Reset to 000h.

7.2.18 MEMORY LIMIT ADDRESS REGISTER – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Reserved	RO	Reset to 0h.
31:20	Memory Limit Address [31:20]	RW	Defines the top address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits corresponding to address bits [19:0] are assumed to be FFFFFh. Reset to 000h.

7.2.19 PREFETCHABLE MEMORY BASE ADDRESS REGISTER – OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	64-bit addressing	RO	Read as 0001b to indicate 64-bit addressing.
15:4	Prefetchable Memory Base Address [31:20]	RW	Defines the bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits are assumed to be 0. The memory base register upper 32 bits contain the upper half of the base address. Reset to 000h.

7.2.20 PREFETCHABLE MEMORY LIMIT ADDRESS REGISTER – OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	64-bit addressing	RO	Read as 0001b to indicate 64-bit addressing.
31:20	Prefetchable Memory Limit Address [31:20]	RW	Defines the top address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits are assumed to be FFFFFh. The memory limit upper 32 bits register contains the upper half of the limit address. Reset to 000h.

7.2.21 PREFETCHABLE MEMORY BASE ADDRESS UPPER 32-BITS REGISTER – OFFSET 28h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Prefetchable Memory Base Address, Upper 32-bits [63:32]	RW	Defines the upper 32-bits of a 64-bit bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. Reset to 00000000h.

7.2.22 PREFETCHABLE MEMORY LIMIT ADDRESS UPPER 32-BITS REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Prefetchable Memory Limit Address, Upper 32-bits [63:32]	RW	Defines the upper 32-bits of a 64-bit top address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. Reset to 00000000h.

7.2.23 I/O BASE ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	I/O Base Address, Upper 16-bits [31:16]	RW	Defines the upper 16-bits of a 32-bit bottom address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other. Reset to 0000h.

7.2.24 I/O LIMIT ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	I/O Limit Address, Upper 16-bits [31:16]	RW	Defines the upper 16-bits of a 32-bit top address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other. Reset to 0000h.

7.2.25 CAPABILITY POINTER REGISTER – OFFSET 34h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capability Pointer	RO	Pointer points to the PCI power management registers (80h). Reset to 80h.

7.2.26 INTERRUPT LINE REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Line	RW	Reset to 00h.

7.2.27 INTERRUPT PIN REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Interrupt Pin	RO	The Switch implements INTA virtual wire interrupt signals to represent hot-plug events at downstream ports. The default value on the downstream ports may be changed by SMBus or auto-loading from EEPROM. Reset to 00h.

7.2.28 BRIDGE CONTROL REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	Parity Error Response	RW	0b: Ignore Poisoned TLPs on the secondary interface 1b: Enable the Poisoned TLPs reporting and detection on the secondary interface Reset to 0b.
17	S_SERR# enable	RW	0b: Disables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary interface 1b: Enables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary interface Reset to 0b.
18	ISA Enable	RW	0b: Forwards downstream all I/O addresses in the address range defined by the I/O Base, I/O Base, and Limit registers 1b: Forwards upstream all I/O addresses in the address range defined by the I/O Base and Limit registers that are in the first 64KB of PCI I/O address space (top 768 bytes of each 1KB block) Reset to 0b.
19	VGA Enable	RW	0: Ignores access to the VGA memory or IO address range 1: Forwards transactions targeted at the VGA memory or IO address range VGA memory range starts from 000A 0000h to 000B FFFFh VGA IO addresses are in the first 64KB of IO address space. AD [9:0] is in the ranges 3B0 to 3BBh and 3C0h to 3DFh. Reset to 0b. Please note that this bit is reserved in Port 2, Port 3 and Port 4.
20	VGA 16-bit decode	RW	0b: Executes 10-bit address decoding on VGA I/O accesses 1b: Executes 16-bit address decoding on VGA I/O accesses Reset to 0b. Please note that this bit is reserved in Port 2, Port 3 and Port 4.
21	Master Abort Mode	RO	Does not apply to PCI Express. Must be hardwired to 0b.
22	Secondary Bus Reset	RW	0b: Does not trigger a hot reset on the corresponding PCI Express Port 1b: Triggers a hot reset on the corresponding PCI Express Port At the downstream port, it asserts PORT_RST# to the attached downstream device. At the upstream port, it asserts the PORT_RST# at all the downstream ports. Reset to 0b.
23	Fast Back-to-Back Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
24	Primary Master Timeout	RO	Does not apply to PCI Express. Must be hardwired to 0b.
25	Secondary Master Timeout	RO	Does not apply to PCI Express. Must be hardwired to 0b.
26	Master Timeout Status	RO	Does not apply to PCI Express. Must be hardwired to 0b.
27	Discard Timer SERR# enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
31:28	Reserved	RO	Reset to 0h.

7.2.29 POWER MANAGEMENT CAPABILITY ID REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 01h to indicate that these are power management enhanced capability registers.

7.2.30 NEXT ITEM POINTER REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	At upstream ports, the pointer points to the Vital Protocol Data (VPD) capability register (9Ch). At downstream ports, the pointer points to the Message capability register (8Ch). Reset to 9Ch (Upstream port). Reset to 8Ch (Downstream port).

7.2.31 POWER MANAGEMENT CAPABILITIES REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Power Management Revision	RO	Read as 011b to indicate the device is compliant to Revision 1.2 of *PCI Power Management Interface Specifications.*
19	PME# Clock	RO	Does not apply to PCI Express. Must be hardwired to 0b.
20	Reserved	RO	Reset to 0b.
21	Device Specific Initialization	RO	Read as 0b to indicate Switch does not have device specific initialization requirements. The default value may be changed by SMBus or auto-loading from EEPROM.
24:22	AUX Current	RO	Reset as 111b to indicate the Switch needs 375 mA in D3 state. The default value may be changed by SMBus or auto-loading from EEPROM.
25	D1 Power State Support	RO	Read as 1b to indicate Switch supports the D1 power management state. The default value may be changed by SMBus or auto-loading from EEPROM.
26	D2 Power State Support	RO	Read as 1b to indicate Switch supports the D2 power management state. The default value may be changed by SMBus or auto-loading from EEPROM.
31:27	PME# Support	RO	Read as 11111b to indicate Switch supports the forwarding of PME# message in all power states. The default value may be changed by SMBus or auto-loading from EEPROM.

7.2.32 POWER MANAGEMENT DATA REGISTER – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Power State	RW	Indicates the current power state of the Switch. Writing a value of D0 when the previous state was D3 cause a hot reset without asserting DWNRST_L. 00b: D0 state 01b: D1 state 10b: D2 state 11b: D3 hot state Reset to 00b.
2	Reserved	RO	Reset to 0b.
3	No_Soft_Reset	RO	When set, this bit indicates that device transitioning from D3hot to D0 does not perform an internal reset. When clear, an internal reset is performed when power state transits from D3hot to D0. This bit can be rewritten with EEPROM programming. The default value may be changed by SMBus or auto-loading from EEPROM.

BIT	FUNCTION	TYPE	DESCRIPTION
			Reset to 1b.
7:4	Reserved	RO	Reset to 0b.
8	PME# Enable	RWS	When asserted, the Switch will generate the PME# message. Reset to 0b.
12:9	Data Select	RW	Select data registers. Reset to 0h.
14:13	Data Scale	RO	Reset to 00b.
15	PME status	ROS	Read as 0b as the PME# message is not implemented.

7.2.33 PPB SUPPORT EXTENSIONS – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
21:16	Reserved	RO	Reset to 000000b.
22	B2_B3 Support for $D3_{HOT}$	RO	Does not apply to PCI Express. Must be hardwired to 0b.
23	Bus Power / Clock Control Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.

7.2.34 DATA REGISTER – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	Data Register	RO	Data Register. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.

7.2.35 MSI CAPABILITY ID REGISTER – OFFSET 8Ch (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 05h to indicate that this is message signal interrupt capability register.

7.2.36 NEXT ITEM POINTER REGISTER – OFFSET 8Ch (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Pointer points to the Vendor specific capability register (A4h). Reset to A4h.

7.2.37 MESSAGE CONTROL REGISTER – OFFSET 8Ch (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
16	MSI Enable	RW	0b: The function is prohibited from using MSI to request service 1b: The function is permitted to use MSI to request service and is prohibited from using its INTx # pin Reset to 0b.
19:17	Multiple Message Capable	RO	Read as 000b.
22:20	Multiple Message	RW	Reset to 000b.

BIT	FUNCTION	TYPE	DESCRIPTION
	Enable		
23	64-bit address capable	RO	0b: The function is not capable of generating a 64-bit message address 1b: The function is capable of generating a 64-bit message address Reset to 1b.
31:24	Reserved	RO	Reset to 00h.

7.2.38 MESSAGE ADDRESS REGISTER – OFFSET 90h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Reserved	RO	Reset to 00b.
31:2	Message Address	RW	If the message enable bit is set, the contents of this register specify the DWORD aligned address for MSI memory write transaction. Reset to 0.

7.2.39 MESSAGE UPPER ADDRESS REGISTER – OFFSET 94h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Message Upper Address	RW	This register is only effective if the device supports a 64-bit message address is set. Reset to 00000000h.

7.2.40 MESSAGE DATA REGISTER – OFFSET 98h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Message Data	RW	Reset to 0000h.

7.2.41 VPD CAPABILITY ID REGISTER – OFFSET 9Ch (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 03h to indicate that these are VPD enhanced capability registers. Reset to 03h.

7.2.42 NEXT ITEM POINTER REGISTER – OFFSET 9Ch (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Pointer points to the Vendor specific capability register (A4h). Reset to A4h.

7.2.43 VPD REGISTER – OFFSET 9Ch (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
17:16	Reserved	RO	Reset to 00b.

BIT	FUNCTION	TYPE	DESCRIPTION
23:18	VPD Address	RW	Contains DWORD address that is used to generate read or write cycle to the VPD table stored in EEPROM. Reset to 000000b.
30:24	Reserved	RO	Reset to 0000000b.
31	VPD operation	RW	0b: Performs VPD read command to VPD table at the location as specified in VPD address. This bit is kept '0' and then set to '1' automatically after EEPROM cycle is finished 1b: Performs VPD write command to VPD table at the location as specified in VPD address. This bit is kept '1' and then set to '0' automatically after EEPROM cycle is finished. Reset to 0b.

7.2.44 VPD DATA REGISTER – OFFSET A0h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	VPD Data	RW	When read, it returns the last data read from VPD table at the location as specified in VPD Address. When written, it places the current data into VPD table at the location as specified in VPD Address.

7.2.45 VENDOR SPECIFIC CAPABILITY ID REGISTER – OFFSET A4h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 09h to indicate that these are vendor specific capability registers. Reset to 09h.

7.2.46 NEXT ITEM POINTER REGISTER – OFFSET A4h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Pointer points to the SSID/SSVID capability register (B8h). Reset to B8h.

7.2.47 LENGTH REGISTER – OFFSET A4h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Length Information	RO	The length field provides the information for number of bytes in the capability structure (including the ID and Next pointer bytes). Reset to 000Ch.

7.2.48 XPIP CSR0 – OFFSET A8h (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Reserved	RW	Reset to 04001060h.

7.2.49 XPIP CSR1 – OFFSET ACh (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Reserved	RW	Reset to 04000800h.

7.2.50 REPLAY TIME-OUT COUNTER – OFFSET B0h

BIT	FUNCTION	TYPE	DESCRIPTION
11:0	User Replay Timer	RW	A 12-bit register contains a user-defined value. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000h.
12	Enable User Replay Timer	RW	When asserted, the user-defined replay time-out value is be employed. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
13	Power Management Capability Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
14	MSI Capability Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
15	AER Capability Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.

7.2.51 ACKNOWLEDGE LATENCY TIMER – OFFSET B0h

BIT	FUNCTION	TYPE	DESCRIPTION
29:16	User ACK Latency Timer	RW	A 14-bit register contains a user-defined value. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0.
30	Enable User ACK Latency	RW	When asserted, the user-defined ACK latency value is be employed. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
31	Reserved	RO	Reset to 0b.

7.2.52 SWITCH OPERATION MODE – OFFSET B4h (Upstream Port)

BIT	FUNCTION	TYPE	DESCRIPTION
0	Store-Forward	RW	When set, a store-forward mode is used. Otherwise, the chip is working under cut-through mode. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
2:1	Cut-through Threshold	RW	Cut-through Threshold. When forwarding a packet from low-speed port to high-speed mode, the chip provides the capability to adjust the forwarding threshold. The default value may be changed by SMBus or auto-loading from EEPROM. 00b: the threshold is set at the middle of forwarding packet 01b: the threshold is set ahead 1-cycle of middle point 10b: the threshold is set ahead 2-cycle of middle point. 11b: the threshold is set ahead 3-cycle of middle point. Reset to 01b.
3	Port Arbitration Mode	RW	When set, the round-robin arbitration will stay in the arbitrated port even if the credit is not enough but request is pending. When clear, the round-robin arbitration will always go to the requesting port, which the outgoing credit is enough for the packet queued in the port. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
4	Credit Update Mode	RW	When set, the frequency of releasing new credit to the link partner will be one credit per update. When clear, the frequency of releasing new credit to the link partner will be two credits per update. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
5	Ordering on Different Egress Port Mode	RW	When set, there has ordering rule on packets for different egress port. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
6	Ordering on Different Tag of Completion Mode	RW	When set, there has ordering rule between completion packet with different tag. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
7	Reserved	RO	Reset to 0.
13:8	Power management Control parameter	RW	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000001b.
14	RX Polarity Inversion Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
15	Compliance pattern Parity Control Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
16	Low Driver Current	HwInt	It indicates the status of the strapping pin LODRV. The default value may be changed by SMBus or auto-loading from EEPROM.
17	High Driver Current	HwInt	It indicates the status of the strapping pin HIDRV. The default value may be changed by SMBus or auto-loading from EEPROM.
21:18	Driver Transmit Current	HwInt	It indicates the status of the strapping pins DTX[3:0]. The default value may be changed by SMBus or auto-loading from EEPROM.
25:22	De-emphasis Transmit Equalization	HwInt	It indicates the status of the strapping pins DEQ[3:0]. The default value may be changed by SMBus or auto-loading from EEPROM.
27:26	Receive Termination Adjustment	HwInt	It indicates the status of the strapping pins RXTRMADJ[1:0]. The default value may be changed by SMBus or auto-loading from EEPROM.
29:28	Transmit Termination Adjustment	HwInt	It indicates the status of the strapping pins TXTRMADJ[1:0]. The default value may be changed by SMBus or auto-loading from EEPROM.

BIT	FUNCTION	TYPE	DESCRIPTION
31:30	Receiver Equalization Level Control	HwInt	It indicates the status of the strapping pins RXEQCTL[1:0]. The default value may be changed by SMBus or auto-loading from EEPROM.

7.2.53 SWITCH OPERATION MODE – OFFSET B4h (Downstream Port)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Reserved	RO	Reset to 0.
13:8	Power management Control parameter	RW	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000001b.
14	RX Polarity Inversion Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
15	Compliance pattern Parity Control Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
16	Low Driver Current	HwInt	It indicates the status of the strapping pin LODRV. The default value may be changed by SMBus or auto-loading from EEPROM.
17	High Driver Current	HwInt	It indicates the status of the strapping pin HIDRV. The default value may be changed by SMBus or auto-loading from EEPROM.
21:18	Driver Transmit Current	HwInt	It indicates the status of the strapping pins DTX[3:0]. The default value may be changed by SMBus or auto-loading from EEPROM.
25:22	De-emphasis Transmit Equalization	HwInt	It indicates the status of the strapping pins DEQ[3:0]. The default value may be changed by SMBus or auto-loading from EEPROM.
27:26	Receive Termination Adjustment	HwInt	It indicates the status of the strapping pins RXTRMADJ[1:0]. The default value may be changed by SMBus or auto-loading from EEPROM.
29:28	Transmit Termination Adjustment	HwInt	It indicates the status of the strapping pins TXTRMADJ[1:0]. The default value may be changed by SMBus or auto-loading from EEPROM.
31:30	Receiver Equalization Level Control	HwInt	It indicates the status of the strapping pins RXEQCTL[1:0]. The default value may be changed by SMBus or auto-loading from EEPROM.

7.2.54 SSID/SSVID CAPABILITY ID REGISTER – OFFSET B8h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	SSID/SSVID Capabilities ID	RO	Read as 0Dh to indicate that these are SSID/SSVID capability registers.

7.2.55 NEXT ITEM POINTER REGISTER – OFFSET B8h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Pointer points to the PCI Express capability register (E0h). Reset to E0h.

7.2.56 SUBSYSTEM VENDOR ID REGISTER – OFFSET BCh

BIT	FUNCTION	TYPE	DESCRIPTION

15:0	SSVID	RO	It indicates the sub-system vendor id. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0000h.

7.2.57 SUBSYSTEM ID REGISTER – OFFSET BCh

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	SSID	RO	It indicates the sub-system device id. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0000h.

7.2.58 GPIO CONTROL REGISTER – OFFSET D8h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	GPIO [0] Input	RO	State of GPIO [0] pin
1	GPIO [0] Output Enable	RW	0b: GPIO [0] is an input pin 1b: GPIO [0] is an output pin Reset to 0b.
2	GPIO [0] Output Register	RW	Value of this bit will be output to GPIO [0] pin if GPIO [0] is configured as an output pin. Reset to 0b.
3	Reserved	RO	Reset to 0b.
4	GPIO [1] Input	RO	State of GPIO [1] pin.
5	GPIO [1] Output Enable	RW	0b: GPIO [1] is an input pin 1b: GPIO [1] is an output pin Reset to 0b.
6	GPIO [1] Output Register	RW	Value of this bit will be output to GPIO [1] pin if GPIO [1] is configured as an output pin. Reset to 0b.
7	Reserved	RO	Reset to 0b.
8	GPIO [2] Input	RO	State of GPIO [2] pin
9	GPIO [2] Output Enable	RW	0b: GPIO [2] is an input pin 1b: GPIO [2] is an output pin Reset to 0b.
10	GPIO [2] Output Register	RW	Value of this bit will be output to GPIO [2] pin if GPIO [2] is configured as an output pin. Reset to 0b.
11	Reserved	RO	Reset to 0b.
12	GPIO [3] Input	RO	State of GPIO [3] pin.
13	GPIO [3] Output Enable	RW	0b: GPIO [3] is an input pin 1b: GPIO [3] is an output pin Reset to 0b.
14	GPIO [3] Output Register	RW	Value of this bit will be output to GPIO [3] pin if GPIO [3] is configured as an output pin. Reset to 0b.
15	Reserved	RO	Reset to 0b.
16	GPIO [4] Input	RO	State of GPIO [4] pin.

BIT	FUNCTION	TYPE	DESCRIPTION
17	GPIO [4] Output Enable	RW	0b: GPIO [4] is an input pin 1b: GPIO [4] is an output pin Reset to 0b.
18	GPIO [4] Output Register	RW	Value of this bit will be output to GPIO [4] pin if GPIO [4] is configured as an output pin. Reset to 0b.
19	Reserved	RO	Reset to 0b.
20	GPIO [5] Input	RO	State of GPIO [5] pin.
21	GPIO [5] Output Enable	RW	0b: GPIO [5] is an input pin 1b: GPIO [5] is an output pin Reset to 0b.
22	GPIO [5] Output Register	RW	Value of this bit will be output to GPIO [5] pin if GPIO [5] is configured as an output pin. Reset to 0b.
23	Reserved	RO	Reset to 0b.
24	GPIO [6] Input	RO	State of GPIO [6] pin.
25	GPIO [6] Output Enable	RW	0b: GPIO [6] is an input pin 1b: GPIO [6] is an output pin Reset to 0b.
26	GPIO [6] Output Register	RW	Value of this bit will be output to GPIO [6] pin if GPIO [6] is configured as an output pin. Reset to 0b.
27	Reserved	RO	Reset to 0b.
28	GPIO [7] Input	RO	State of GPIO [7] pin.
29	GPIO [7] Output Enable	RW	0b: GPIO [7] is an input pin 1b: GPIO [7] is an output pin Reset to 0b.
30	GPIO [7] Output Register	RW	Value of this bit will be output to GPIO [7] pin if GPIO [7] is configured as an output pin. Reset to 0b.
31	Reserved	RO	Reset to 0b.

7.2.59 EEPROM CONTROL REGISTER – OFFSET DCh (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	EEPROM Start	RW	Starts the EEPROM read or write cycle. Reset to 0b.
1	EEPROM Command	RW	Sends the command to the EEPROM. 0b: EEPROM read 1b: EEPROM write Reset to 0b.
2	EEPROM Error Status	RO	1b: EEPROM acknowledge was not received during the EEPROM cycle. Reset to 0b.
3	EEPROM Autoload Success	RO	0b: EEPROM autoload was unsuccessful or is disabled 1b: EEPROM autolad occurred successfully after RESET. Configuration registers were loaded with values in the EEPROM It will be cleared when read at this bit.

BIT	FUNCTION	TYPE	DESCRIPTION
4	EEPROM Autoload Status	RO	0b: EEPROM autoload was unsuccessful or is disabled 1b: EEPROM autoload occurred successfully after PREST. Configuration registers were loaded with values stored in the EEPROM Reset to 0b.
5	EEPROM Autoload Disable	RW	0b: EEPROM autoload enabled 1b: EEPROM autoload disabled Reset to 1b.
7:6	EEPROM Clock Rate	RW	Determines the frequency of the EEPROM clock, which is derived from the primary clock. 00b: Reserved 01b: PEXCLK / 1024 (PEXCLK is 125MHz) 10b: Reserved 11b: Test Mode Reset to 01b.

7.2.60 EEPROM ADDRESS REGISTER – OFFSET DCh (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
8	Reserved	RO	Reset to 0b.
15:9	EEPROM Address	RW	Contains the EEPROM address. Reset to 0.

7.2.61 EEPROM DATA REGISTER – OFFSET DCh (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	EEPROM Data	RW	Contains the data to be written to the EEPROM. After completion of a read cycle, this register will contain the data from the EEPROM. Reset to 0000h.

7.2.62 PCI EXPRESS CAPABILITY ID REGISTER – OFFSET E0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 10h to indicate that these are PCI express enhanced capability registers.

7.2.63 NEXT ITEM POINTER REGISTER – OFFSET E0h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Read as 00h. No other ECP registers.

7.2.64 PCI EXPRESS CAPABILITIES REGISTER – OFFSET E0h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Capability Version	RO	Read as 0001b to indicate the device is compliant to Revision 1.0a of *PCI Express Base Specifications.*

BIT	FUNCTION	TYPE	DESCRIPTION
23:20	Device/Port Type	RO	Indicates the type of PCI Express logical device. Reset to 0101b (Upstream port). Reset to 0110b (Downstream port).
24	Slot Implemented	HwInt	When set, indicates that the PCIe Link associated with this Port is connected to a slot. This field is valid for downstream port of the switch. The default value may be changed by the status of strapped pin, SMBus, or auto-loading from EEPROM.
29:25	Interrupt Message Number	RO	Read as 0b. No MSI messages are generated in the transparent mode.
31:30	Reserved	RO	Reset to 00b.

7.2.65 DEVICE CAPABILITIES REGISTER – OFFSET E4h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Max_Payload_Size Supported	RO	Indicates the maximum payload size that the device can support for TLPs. Each port of the Switch supports 256 bytes max payload size. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 001b.
4:3	Phantom Functions Supported	RO	Indicates the support for use of unclaimed function numbers as Phantom functions. Read as 00b, since the Switch does not act as a requester. Reset to 00b.
5	Extended Tag Field Supported	RO	Indicates the maximum supported size of Tag field as a Requester. Read as 0, since the Switch does not act as a requester. Reset to 0b.
8:6	Endpoint L0s Acceptable Latency	RO	Acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. For Switch, the ASPM software would not check this value. Reset to 000b.
11:9	Endpoint L1 Acceptable Latency	RO	Acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. For Switch, the ASPM software would not check this value. Reset to 000b.
14:12	Reserved	RO	Reset to 000b.
15	Role_Based Error Reporting	RO	When set, indicates that the device implements the functionality originally defined in the Error Reporting ECN. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 1b.
17:16	Reserved	RO	Reset to 00b.
25:18	Captured Slot Power Limit Value	RO	It applies to Upstream Port only. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. This value is set by the Set_Slot_Power_Limit message or hardwired to 00h. Reset to 00h.
27:26	Captured Slot Power Limit Scale	RO	It applies to Upstream Port only. Specifies the scale used for the Slot Power Limit Value. This value is set by the Set_Slot_Power_Limit message or hardwired to 00b. Reset to 00b.
31:28	Reserved	RO	Reset to 0h.

7.2.66 DEVICE CONTROL REGISTER – OFFSET E8h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Correctable Error Reporting Enable	RW	0b: Disable Correctable Error Reporting 1b: Enable Correctable Error Reporting Reset to 0b.
1	Non-Fatal Error Reporting Enable	RW	0b: Disable Non-Fatal Error Reporting 1b: Enable Non-Fatal Error Reporting Reset to 0b.
2	Fatal Error Reporting Enable	RW	0b: Disable Fatal Error Reporting 1b: Enable Fatal Error Reporting Reset to 0b.
3	Unsupported Request Reporting Enable	RW	0b: Disable Unsupported Request Reporting 1b: Enable Unsupported Request Reporting Reset to 0b.
4	Enable Relaxed Ordering	RO	When set, it permits the device to set the Relaxed Ordering bit in the attribute field of transaction. Since the Switch can not either act as a requester or alter the content of packet it forwards, this bit always returns '0' when read. Reset to 0b.
7:5	Max_Payload_Size	RW	This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value. Reset to 000b.
8	Extended Tag Field Enable	RW	Does not apply to PCI Express Switch. Returns '0' when read. Reset to 0.
9	Phantom Function Enable	RW	Does not apply to PCI Express Switch. Returns '0' when read. Reset to 0b.
10	Auxiliary (AUX) Power PM Enable	RWS	When set, indicates that a device is enabled to draw AUX power independent of PME AUX power. Reset to 0b.
11	Enable No Snoop	RO	When set, it permits to set the No Snoop bit in the attribute field of transaction. Since the Switch can not either act as a requester or alter the content of packet it forwards, this bit always returns '0' when read. Reset to 0b.
14:12	Max_Read_ Request_Size	RO	This field sets the maximum Read Request size for the device as a Requester. Since the Switch does not generate read request by itself, these bits are hardwired to 000b. Reset to 000b.
15	Reserved	RO	Reset to 0b.

7.2.67 DEVICE STATUS REGISTER – OFFSET E8h

BIT	FUNCTION	TYPE	DESCRIPTION
16	Correctable Error Detected	RW1C	Asserted when correctable error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
17	Non-Fatal Error Detected	RW1C	Asserted when non-fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
18	Fatal Error Detected	RW1C	Asserted when fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
19	Unsupported Request Detected	RW1C	Asserted when unsupported request is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
20	AUX Power Detected	RO	Asserted when the AUX power is detected by the Switch Reset to 1b.
21	Transactions Pending	RO	Each port of Switch does not issue Non-posted Requests on its own behalf, so this bit is hardwired to 0b. Reset to 0b.
31:22	Reserved	RO	Reset to 0.

7.2.68 LINK CAPABILITIES REGISTER – OFFSET ECh

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Maximum Link Speed	RO	Read as 0001b to indicate the maximum speed of the Express link is 2.5 Gb/s.
9:4	Maximum Link Width	RO	Indicates the maximum width of the given PCIe Link. The width of each port is determined by strapped pin or EEPROM pre-loaded value. Reset to 000001b (x1) for Port 0. Reset to 000001b (x1) for Port 1. Reset to 000001b (x1) for Port 2. Reset to 000001b (x1) for Port 3. Reset to 000001b (x1) for Port 4.
11:10	Active State Power Management (ASPM) Support	RO	Indicates the level of ASPM supported on the given PCIe Link. Each port of Switch supports L0s and L1 entry. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 11b. Reset to 01b.
14:12	L0s Exit Latency	RO	Indicates the L0s exit latency for the given PCIe Link. The length of time this port requires to complete transition from L0s to L0 is in the range of 256ns to less than 512ns. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 011b.
17:15	L1 Exit Latency	RO	Indicates the L1 exit latency for the given PCIe Link. The length of time this port requires to complete transition from L1 to L0 is in the range of 16us to less than 32us. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000b.
19:18	Reserved	RO	Reset to 00b.

BIT	FUNCTION	TYPE	DESCRIPTION
20	Data Link Layer Active Reporting Capable	RO	For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port, this bit must be set to 1b. For Upstream Port, this bit must be hardwired to 0b. Reset to 0b for upstream port. Reset to 1b for downstream ports.
23:21	Reserved	R0	Reset to 000b
31:24	Port Number	RO	Indicates the PCIe Port Number for the given PCIe Link. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00h for Port 0. Reset to 01h for Port 1. Reset to 02h for Port 2. Reset to 03h for Port 3. Reset to 04h for Port 4.

7.2.69 LINK CONTROL REGISTER – OFFSET F0h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Active State Power Management (ASPM) Control	RW	00b: ASPM is Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled Note that the receiver must be capable of entering L0s even when the field is disabled. Reset to 00b.
2	Reserved	RO	Reset to 0b.
3	Read Completion Boundary (RCB)	RO	Does not apply to PCI Express Switch. Returns ‘0’ when read. Reset to 0b.
4	Link Disable	RW	At upstream port, it is not allowed to disable the link, so this bit is hardwired to ‘0’. For downstream ports, it disables the link when this bit is set. Reset to 0b.
5	Retrain Link	RW	At upstream port, it is not allowed to retrain the link, so this bit is hardwired to 0b. For downstream ports, it initiates Link Retraining when this bit is set. This bit always returns 0b when read.
6	Common Clock Configuration	RW	0b: The components at both ends of a link are operating with asynchronous reference clock 1b: The components at both ends of a link are operating with a distributed common reference clock Reset to 0b.
7	Extended Synch	RW	When set, it transmits 4096 FTS ordered sets in the L0s state for entering L0 state and transmits 1024 TS1 ordered sets in the L1 state for entering L0 state. Reset to 0b.
15:8	Reserved	RO	Reset to 00h.

7.2.70 LINK STATUS REGISTER – OFFSET F0h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Link Speed	RO	Read as 0001b to indicate the negotiated speed of the Express link is 2.5 Gb/s.

BIT	FUNCTION	TYPE	DESCRIPTION
25:20	Negotiated Link Width	RO	Indicates the negotiated width of the given PCIe link. Reset to 000001b (x1).
26	Training Error	RO	When set, indicates a Link training error occurred. This bit is cleared by hardware upon successful training of the link to the L0 link state. Reset to 0b.
27	Link Training	RO	When set, indicates the link training is in progress. Hardware clears this bit once link training is complete. Reset to 0b.
28	Slot Clock Configuration	HwInt	0b: the switch uses an independent clock irrespective of the presence of a reference on the connector 1b: the switch uses the same reference clock that the platform provides on the connector The default value may be changed by the status of strapped pin, SMBus, or auto-loading from EEPROM. Reset to 0b.
29	Data Link Layer Link Active	RO	Indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. Reset to 0b.
31:30	Reserved	RO	Reset to 00b.

7.2.71 SLOT CAPABILITIES REGISTER (Downstream Port Only) – OFFSET F4h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Attention Button Present	RO	When set, it indicates that an Attention Button is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
1	Power Controller Present	RO	When set, it indicates that a Power Controller is implemented for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
2	Reserved	RO	Reset to 0b.
3	Attention Indicator Present	RO	When set, it indicates that an Attention Indicator is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
4	Power Indicator Present	RO	When set, it indicates that a Power Indicator is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
5	Hot-Plug Surprise	RO	When set, it indicates that a device present in this slot might be removed from the system without any prior notification. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
6	Hot-Plug Capable	HwInt	When set, it indicates that this slot is capable of supporting Hot-Plug operation. The default value may be changed by the status of strapped pin or auto-loading from EEPROM.

BIT	FUNCTION	TYPE	DESCRIPTION
14:7	Slot Power Limit Value	RW	It applies to Downstream Port only. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Writes to this register also cause the Port to send the Set_Slot_Power_Limit message. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00h.
16:15	Slot Power Limit Scale	RW	It applies to Downstream Port only. Specifies the scale used for the Slot Power Limit Value. Writes to this register also cause the Port to send the Set_Slot_Power_Limit message. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00b.
18:17	Reserved	RO	Reset to 00b.
31:19	Physical Slot Number	RO	It indicates the physical slot number attached to this Port. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0.

7.2.72 SLOT CONTROL REGISTER (Downstream Port Only) – OFFSET F8h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Attention Button Pressed Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on an attention button pressed event. Reset to 0b.
1	Power Fault Detected Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on a power fault event. Reset to 0b.
2	Reserved	RO	Reset to 0b.
3	Presence Detect Changed Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on a presence detect changed event. Reset to 0b.
4	Command Completed Interrupt Enable	RW	When set, it enables the generation of Hot-Plug interrupt when the Hot-Plug Controller completes a command. Reset to 0b.
5	Hot-Plug Interrupt Enable	RW	When set, it enables generation of Hot-Plug interrupt on enabled Hot-Plug events. Reset to 0b.
7:6	Attention Indicator Control	RW	Controls the display of Attention Indicator. 00b: Reserved 01b: On 10b: Blink 11b: Off Writes to this register also cause the Port to send the ATTENTION_INDICATOR_* Messages. Reset to 11b.

BIT	FUNCTION	TYPE	DESCRIPTION
9:8	Power Indicator Control	RW	Controls the display of Power Indicator. 00b: Reserved 01b: On 10b: Blink 11b: Off Writes to this register also cause the Port to send the POWER_INDICATOR_* Messages. Reset to 11b.
10	Power Controller Control	RW	0b: reset the power state of the slot (Power On) 1b: set the power state of the slot (Power Off) Reset to 0b.
11	Reserved	RO	Reset to 0b.
12	Data Link Layer State Changed Enable	RW	If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Link Active field is changed. Reset to 0b.
15:13	Reserved	RO	Reset to 000b

7.2.73 SLOT STATUS REGISTER (Downstream Port Only) – OFFSET F8h

BIT	FUNCTION	TYPE	DESCRIPTION
16	Attention Button Pressed	RW1C	When set, it indicates the Attention Button is pressed. Reset to 0b.
17	Power Fault Detected	RW1C	When set, it indicates a Power Fault is detected. Reset to 0b.
18	MRL Sensor Changed	RO	When set, it indicates a MRL Sensor Changed is detected. Reset to 0b.
19	Presence Detect Changed	RW1C	When set, it indicates a Presence Detect Changed is detected. Reset to 0b.
20	Command Completed	RW1C	When set, it indicates the Hot-Plug Controller completes an issued command. Reset to 0b.
21	MRL Sensor State	RO	Reflects the status of MRL Sensor. 0b: MRL Closed 1b: MRL Opened Reset to 0b.
22	Presence Detect State	RO	Indicates the presence of a card in the slot. 0b: Slot Empty 1b: Card Present in slot This register is implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities register is 0b), this bit returns 1b. Reset to 1b.
23	Reserved	RO	Reset to 0.
24	Data Link Layer State Changed	RW1C	This bit is set when the value reported in the Data Link Layer Link Active field of the Link Status register is changed.
31:25	Reserved	RO	Reset to 0

7.2.74 PCI EXPRESS ADVANCED ERROR REPORTING CAPABILITY ID REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Extended Capabilities ID	RO	Read as 0001h to indicate that these are PCI express extended capability registers for advance error reporting.

7.2.75 CAPABILITY VERSION – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Capability Version	RO	Read as 1h. Indicates PCI-SIG defined PCI Express capability structure version number. Reset to 1h.

7.2.76 NEXT ITEM POINTER REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
31:20	Next Capability Offset	RO	Pointer points to the PCI Express Extended VC capability register (140h). Reset to 140h.

7.2.77 UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 104h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Status	RW1CS	When set, indicates that the Training Error event has occurred. Reset to 0b.
3:1	Reserved	RO	Reset to 000b.
4	Data Link Protocol Error Status	RW1CS	When set, indicates that the Data Link Protocol Error event has occurred. Reset to 0b.
11:5	Reserved	RO	Reset to 0.
12	Poisoned TLP Status	RW1CS	When set, indicates that a Poisoned TLP has been received or generated. Reset to 0b.
13	Flow Control Protocol Error Status	RW1CS	When set, indicates that the Flow Control Protocol Error event has occurred. Reset to 0b.
14	Completion Timeout Status	RW1CS	When set, indicates that the Completion Timeout event has occurred. Reset to 0b.
15	Completer Abort Status	RW1CS	When set, indicates that the Completer Abort event has occurred. Reset to 0b.
16	Unexpected Completion Status	RW1CS	When set, indicates that the Unexpected Completion event has occurred. Reset to 0b.
17	Receiver Overflow Status	RW1CS	When set, indicates that the Receiver Overflow event has occurred. Reset to 0b.
18	Malformed TLP Status	RW1CS	When set, indicates that a Malformed TLP has been received. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
19	ECRC Error Status	RW1CS	When set, indicates that an ECRC Error has been detected. Reset to 0b.
20	Unsupported Request Error Status	RW1CS	When set, indicates that an Unsupported Request event has occurred. Reset to 0b.
31:21	Reserved	RO	Reset to 0.

7.2.78 UNCORRECTABLE ERROR MASK REGISTER – OFFSET 108h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Mask	RWS	When set, the Training Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
3:1	Reserved	RO	Reset to 000b.
4	Data Link Protocol Error Mask	RWS	When set, the Data Link Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
11:5	Reserved	RO	Reset to 0.
12	Poisoned TLP Mask	RWS	When set, an event of Poisoned TLP has been received or generated is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
13	Flow Control Protocol Error Mask	RWS	When set, the Flow Control Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
14	Completion Timeout Mask	RWS	When set, the Completion Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
15	Completer Abort Mask	RWS	When set, the Completer Abort event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
16	Unexpected Completion Mask	RWS	When set, the Unexpected Completion event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
17	Receiver Overflow Mask	RWS	When set, the Receiver Overflow event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
18	Malformed TLP Mask	RWS	When set, an event of Malformed TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
19	ECRC Error Mask	RWS	When set, an event of ECRC Error has been detected is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
20	Unsupported Request Error Mask	RWS	When set, the Unsupported Request event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
31:21	Reserved	RO	Reset to 0.

7.2.79 UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 10Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
3:1	Reserved	RO	Reset to 000b.
4	Data Link Protocol Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
11:5	Reserved	RO	Reset to 0.
12	Poisoned TLP Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
13	Flow Control Protocol Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
14	Completion Timeout Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
15	Completer Abort Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
16	Unexpected Completion Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
17	Receiver Overflow Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
18	Malformed TLP Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
19	ECRC Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0.
20	Unsupported Request Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
31:21	Reserved	RO	Reset to 0.

7.2.80 CORRECTABLE ERROR STATUS REGISTER – OFFSET 110 h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Receiver Error Status	RW1CS	When set, the Receiver Error event is detected. Reset to 0b.
5:1	Reserved	RO	Reset to 00000b.
6	Bad TLP Status	RW1CS	When set, the event of Bad TLP has been received is detected. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
7	Bad DLLP Status	RW1CS	When set, the event of Bad DLLP has been received is detected. Reset to 0b.
8	REPLAY_NUM Rollover status	RW1CS	When set, the REPLAY_NUM Rollover event is detected. Reset to 0b.
11:9	Reserved	RO	Reset to 000b.
12	Replay Timer Timeout status	RW1CS	When set, the Replay Timer Timeout event is detected. Reset to 0b.
13	Advisory Non-Fatal Error status	RW1CS	When set, the Advisory Non-Fatal Error event is detected. Reset to 0b.
31:14	Reserved	RO	Reset to 0b.

7.2.81 CORRECTABLE ERROR MASK REGISTER – OFFSET 114 h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Receiver Error Mask	RWS	When set, the Receiver Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
5:1	Reserved	RO	Reset to 00000b.
6	Bad TLP Mask	RWS	When set, the event of Bad TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
7	Bad DLLP Mask	RWS	When set, the event of Bad DLLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
8	REPLAY_NUM Rollover Mask	RWS	When set, the REPLAY_NUM Rollover event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
11:9	Reserved	RO	Reset to 000b.
12	Replay Timer Timeout Mask	RWS	When set, the Replay Timer Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
13	Advisory Non-Fatal Error Mask	RWS	When set, the Advisory Non-Fatal Error event is not logged in the Header Long register and not issued as an Error Message to RC either. Reset to 1b.
31:14	Reserved	RO	Reset to 0.

7.2.82 ADVANCE ERROR CAPABILITIES AND CONTROL REGISTER – OFFSET 118h

BIT	FUNCTION	TYPE	DESCRIPTION
4:0	First Error Pointer	ROS	It indicates the bit position of the first error reported in the Uncorrectable Error Status register. Reset to 00000b.
5	ECRC Generation Capable	RO	When set, it indicates the Switch has the capability to generate ECRC. Reset to 1b.

BIT	FUNCTION	TYPE	DESCRIPTION
6	ECRC Generation Enable	RWS	When set, it enables the generation of ECRC when needed. Reset to 0b.
7	ECRC Check Capable	RO	When set, it indicates the Switch has the capability to check ECRC. Reset to 1b.
8	ECRC Check Enable	RWS	When set, the function of checking ECRC is enabled. Reset to 0b.
31:9	Reserved	RO	Reset to 0.

7.2.83 HEADER LOG REGISTER – OFFSET From 11Ch to 128h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	1st DWORD	ROS	Hold the 1st DWORD of TLP Header. The Head byte is in big endian.
63:32	2nd DWORD	ROS	Hold the 2nd DWORD of TLP Header. The Head byte is in big endian.
95:64	3rd DWORD	ROS	Hold the 3rd DWORD of TLP Header. The Head byte is in big endian.
127:96	4th DWORD	ROS	Hold the 4th DWORD of TLP Header. The Head byte is in big endian.

7.2.84 PCI EXPRESS VIRTUAL CHANNEL CAPABILITY ID REGISTER – OFFSET 140h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Extended Capabilities ID	RO	Read as 0002h to indicate that these are PCI express extended capability registers for virtual channel.

7.2.85 CAPABILITY VERSION – OFFSET 140h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Capability Version	RO	Read as 1h. Indicates PCIe Base Specification REV. 1.0a. Reset to 1h.

7.2.86 NEXT ITEM POINTER REGISTER – OFFSET 140h

BIT	FUNCTION	TYPE	DESCRIPTION
31:20	Next Capability Offset	RO	Pointer points to the PCI Express Power Budgeting Capability register (20Ch). Reset to 20Ch.

7.2.87 PORT VC CAPABILITY REGISTER 1 – OFFSET 144h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Extended VC Count	HwInt	It indicates the number of extended Virtual Channels in addition to the default VC supported by the Switch. The default value may be changed by the status of strapped pin or auto-loading from EEPROM. Reset to 001b.
3	Reserved	RO	Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
6:4	Low Priority Extended VC Count	RO	It indicates the number of extended Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000b.
7	Reserved	RO	Reset to 0b.
9:8	Reference Clock	RO	It indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration. Defined encoding is 00b for 100 ns reference clock. Reset to 00b.
11:10	Port Arbitration Table Entry Size	RO	Read as 10b to indicate the size of Port Arbitration table entry in the device is 4 bits. Reset to 10b.
31:12	Reserved	RO	Reset to 0.

7.2.88 PORT VC CAPABILITY REGISTER 2 – OFFSET 148h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	VC Arbitration Capability	RO	It indicates the types of VC Arbitration supported by the device for the LPVC group. This field is valid when LPVC is greater than 0. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin and Weight Round Robin arbitration with 32 phases in LPVC. Reset to 00000011b.
23:8	Reserved	RO	Reset to 0.
31:24	VC Arbitration Table Offset	RO	It indicates the location of the VC Arbitration Table as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). Reset to 03h.

7.2.89 PORT VC CONTROL REGISTER – OFFSET 14Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Load VC Arbitration Table	RW	When set, the programmed VC Arbitration Table is applied to the hardware. This bit always returns 0b when read. Reset to 0b.
3:1	VC Arbitration Select	RW	This field is used to configure the VC Arbitration by selecting one of the supported VC Arbitration schemes. The valid values for the schemes supported by Switch are 0b and 1b. Other value than these written into this register will be treated as default. Reset to 0b.
15:4	Reserved	RO	Reset to 0.

7.2.90 PORT VC STATUS REGISTER – OFFSET 14Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	VC Arbitration Table Status	RO	When set, it indicates that any entry of the VC Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the VC Arbitration Table after the bit of "Load VC Arbitration Table" is set. Reset to 0b.
31:17	Reserved	RO	Reset to 0.

7.2.91 VC RESOURCE CAPABILITY REGISTER (0) – OFFSET 150h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Port Arbitration Capability	RO	It indicates the types of Port Arbitration supported by the VC resource. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Note that the Time-based WRR is only valid in VC1. Reset to 00001001b.
13:8	Reserved	RO	Reset to 000000b.
14	Advanced Packet Switching	RO	When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS). Reset to 0b.
15	Reject Snoop Transactions	RO	This bit is not applied to PCIe Switch. Reset to 0b.
22:16	Maximum Time Slots	RO	It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 7Fh.
23	Reserved	RO	Reset to 0b.
31:24	Port Arbitration Table Offset	RO	It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). Reset to 04h for Port Arbitration Table (0).

7.2.92 VC RESOURCE CONTROL REGISTER (0) – OFFSET 154h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	TC/VC Map	RW	This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to FFh.
15:8	Reserved	RO	Reset to 00h.
16	Load Port Arbitration Table	RW	When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns 0b when read. Reset to 0b.
19:17	Port Arbitration Select	RW	This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Switch are 000b and 011b at VC0, other value than these written into this register will be treated as default. Reset to 000b.
23:20	Reserved	RO	Reset to 0h.
26:24	VC ID	RW	This field assigns a VC ID to the VC resource. Reset to 000b.
30:27	Reserved	RO	Reset to 0h.
31	VC Enable	RW	0b: it disables this Virtual Channel 1b: it enables this Virtual Channel Reset to 1b.

7.2.93 VC RESOURCE STATUS REGISTER (0) – OFFSET 158h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Reserved	RO	Reset to 0000h.
16	Port Arbitration Table Status	RO	When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of "Load Port Arbitration Table" is set. Reset to 0b.
17	VC Negotiation Pending	RO	When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete. Reset to 0b.
31:18	Reserved	RO	Reset to 0.

7.2.94 VC RESOURCE CAPABILITY REGISTER (1) – OFFSET 15Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Port Arbitration Capability	RO	It indicates the types of Port Arbitration supported by the VC resource. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Note that the Time-based WRR is only valid in VC1. Reset to 00011001b.
13:8	Reserved	RO	Reset to 000000b.
14	Advanced Packet Switching	RO	When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS). Reset to 0b.
15	Reject Snoop Transactions	RO	This bit is not applied to PCIe Switch. Reset to 0b.
22:16	Maximum Time Slots	RO	It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 7Fh.
23	Reserved	RO	Reset to 0b.
31:24	Port Arbitration Table Offset	RO	It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). Reset to 08h for Port Arbitration Table (1)

7.2.95 VC RESOURCE CONTROL REGISTER (1) – OFFSET 160h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	TC/VC Map	RW (Exception for bit0)	This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. Bit 0 of this filed is read-only and must be set to "0" for the VC1. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00h.
15:8	Reserved	RO	Reset to 00h.

BIT	FUNCTION	TYPE	DESCRIPTION
16	Load Port Arbitration Table	RW	When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns 0b when read. Reset to 0b.
19:17	Port Arbitration Select	RW	This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Switch are 000b, 011b and 100b at VC1, other value than these written into this register will be treated as default. Reset to 000b.
23:20	Reserved	RO	Reset to 0h.
26:24	VC ID	RW	This field assigns a VC ID to the VC resource. Reset to 001b.
30:27	Reserved	RO	Reset to 0h.
31	VC Enable	RW	0b: it disables this Virtual Channel 1b: it enables this Virtual Channel Reset to 0b.

7.2.96 VC RESOURCE STATUS REGISTER (1) – OFFSET 164h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Reserved	RO	Reset to 0000h.
16	Port Arbitration Table Status	RO	When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of "Load Port Arbitration Table" is set. Reset to 0b.
17	VC Negotiation Pending	RO	When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete. Reset to 0b.
31:18	Reserved	RO	Reset to 0.

7.2.97 VC ARBITRATION TABLE REGISTER – OFFSET 170h

The VC arbitration table is a read-write register array that contains a table for VC arbitration. Each table entry allocates four bits, of which three bits are used to represent VC ID and one bit is reserved. A total of 32 entries are used to construct the VC arbitration table. The layout for this register array is shown below.

Table 7-1 Register Array Layout for VC Arbitration

31 - 28	27 - 24	23 - 20	19 - 16	15 - 12	11 - 8	7 - 4	3 - 0	Byte Location
Phase [7]	Phase [6]	Phase [5]	Phase [4]	Phase [3]	Phase [2]	Phase [1]	Phase [0]	00h
Phase [15]	Phase [14]	Phase [13]	Phase [12]	Phase [11]	Phase [10]	Phase [9]	Phase [8]	04h
Phase [23]	Phase [22]	Phase [21]	Phase [20]	Phase [19]	Phase [18]	Phase [17]	Phase [16]	08h
Phase [31]	Phase [30]	Phase [29]	Phase [28]	Phase [27]	Phase [26]	Phase [25]	Phase [24]	0Ch

7.2.98 PORT ARBITRATION TABLE REGISTER (0) and (1) – OFFSET 180h and 1C0h

The Port arbitration table is a read-write register array that contains a table for Port arbitration. Each table entry allocates two bits to represent Port Number. The table entry size is dependent on the number of enabled ports (refer to bit 10 and 11 of Port VC capability register 1). The arbitration table contains 128 entries if three or four ports are to be enabled. The following table shows the register array layout for the size of entry equal to two.

Table 7-2 Table Entry Size in 4 Bits

63 - 56	55 - 48	47 - 40	39 - 32	31 - 24	23 - 16	15 - 8	7 - 0	Byte Location
Phase [15:14]	Phase [13:12]	Phase [11:10]	Phase [9:8]	Phase [7:6]	Phase [5:4]	Phase [3:2]	Phase [1:0]	00h
Phase [31:30]	Phase [29:28]	Phase [27:26]	Phase [25:24]	Phase [23:22]	Phase [21:20]	Phase [19:18]	Phase [17:16]	08h
Phase [47:46]	Phase [45:44]	Phase [43:42]	Phase [41:40]	Phase [39:38]	Phase [37:36]	Phase [35:34]	Phase [33:32]	10h
Phase [63:62]	Phase [61:60]	Phase [59:58]	Phase [57:56]	Phase [55:54]	Phase [53:52]	Phase [51:50]	Phase [49:48]	18h
Phase [79:78]	Phase [77:76]	Phase [75:74]	Phase [73:72]	Phase [71:70]	Phase [69:68]	Phase [67:66]	Phase [65:64]	20h
Phase [95:94]	Phase [93:92]	Phase [91:90]	Phase [89:88]	Phase [87:86]	Phase [85:84]	Phase [83:82]	Phase [81:80]	28h
Phase [111:110]	Phase [109:108]	Phase [107:106]	Phase [105:104]	Phase [103:102]	Phase [101:100]	Phase [99:98]	Phase [97:96]	30h
Phase [127:126]	Phase [125:124]	Phase [123:122]	Phase [121:120]	Phase [119:118]	Phase [117:116]	Phase [115:114]	Phase [113:112]	38h

7.2.99 PCI EXPRESS POWER BUDGETING CAPABILITY ID REGISTER – OFFSET 20Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Extended Capabilities ID	RO	Read as 0004h to indicate that these are PCI express extended capability registers for power budgeting.

7.2.100 CAPABILITY VERSION – OFFSET 20Ch

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Capability Version	RO	Read as 1h. Indicates PCIe Base Specification REV. 1.0a. Reset to 1h.

7.2.101 NEXT ITEM POINTER REGISTER – OFFSET 20Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:20	Next Capability Offset	RO	Read as 000h. No other ECP registers. Reset to 000h.

7.2.102 DATA SELECT REGISTER – OFFSET 210h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Data Selection	RW	It indexes the power budgeting data reported through the data register. When 00h, it selects D0 Max power budget When 01h, it selects D0 Sustained power budget Other values would return zero power budgets, which means not supported Reset to 00h.
31:8	Reserved	RO	Reset to 000000h.

7.2.103 POWER BUDGETING DATA REGISTER – OFFSET 214h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Base Power	RO	It specifies the base power value in watts. This value represents the required power budget in the given operation condition. The default value may be changed by auto-loading from EEPROM. Reset to 04h.
9:8	Data Scale	RO	It specifies the scale to apply to the base power value. The default value may be changed by auto-loading from EEPROM. Reset to 00b.
12:10	PM Sub State	RO	It specifies the power management sub state of the given operation condition. It is initialized to the default sub state. Reset to 000b.
14:13	PM State	RO	It specifies the power management state of the given operation condition. It defaults to the D0 power state. The default value may be changed by auto-loading from EEPROM. Reset to 00b.
17:15	Type	RO	It specifies the type of the given operation condition. It defaults to the Maximum power state. The default value may be changed by auto-loading from EEPROM. Reset to 111b.
20:18	Power Rail	RO	It specifies the power rail of the given operation condition. Reset to 010b.
31:21	Reserved	RO	Reset to 0.

7.2.104 POWER BUDGET CAPABILITY REGISTER – OFFSET 218h

BIT	FUNCTION	TYPE	DESCRIPTION
0	System Allocated	RO	When set, it indicates that the power budget for the device is included within the system power budget. The default value may be changed by auto-loading from EEPROM. Reset to 0b.
31:1	Reserved	RO	Reset to 0.

8 CLOCK SCHEME

The PI7C9X20505GP requires 100MHz differential clock inputs through REFCLKP and REFCLKN Pins as shown in the following table.

Table 8-1 Input Clock Requirements

Symbol	Description		Min	Typical	Max.	Unit
$ClkIn_{FREQ}$	Reference input clock range		-	100	-	MHz
$ClkIn_{DC}$	Duty cycle of input clock		40	50	60	%
T_R, T_F	Rise/Fall time of input clock		-	-	0.2	RCUI[a]
V_{SW}	Differential input voltage swing	(peak-to-peak)	800	-	2000	mV
		(zero-to-peak)	400	-	1000	mV

a. RCUI (Reference Clock Unit Interval) refers to the reference clock period

9 HOT PLUG OPERATION

The PI7C9X20505GP is compliant with the *PCI Standard Hot-Plug Controller (SHPC) and Subsystem Specification Revision 1.0*.

Systems with the Hot Plug capability allow the attachment and removal of components from the running system without severely affecting the normal operation of the system. This feature prevents down-time of the system when faulty components need to be replaced or the re-configuration of the system needs to be performed. This feature also allows the system to isolate a faulty component and maintain the stability of the rest of the system upon the detection of such event. Each downstream port of the device has its own Hot Plug Controller, which operates independently from the others. The Hot Plug Controller of the device provides the parallel interface bus to the slot, and, therefore, no extra logic is required to convert the signals from the serial interface bus into parallel.

The Hot Plug operation of the PI7C9X20505GP is implemented by the Hot Plug Signal Pins (Section 3.3) and Hot Plug Capability related register sets (Section 7.2.71 to 7.2.73). The Hot Plug Signal Pins of the device consist of "PWR_IND", "ATT_IND", "ATT_BTN", "MRL_PDC", "PWR_ENA_L" and "PWR_FLT" pins. The Hot Plug Capability register sets provide Hot Plug related status reporting. Additionally, the register sets provide interrupt messaging, which signal the occurrences of various Hot Plug events that take place on the slots. Upon receiving of the interrupt events, the system software can use the Hot Plug Capability registers to respond to these events.

10 IEEE 1149.1 COMPATIBLE JTAG CONTROLLER

An IEEE 1149.1 compatible Test Access Port (TAP) controller and associated TAP pins are provided to support boundary scan in PI7C9X20505GP for board-level continuity test and diagnostics. The TAP pins assigned are TCK, TDI, TDO, TMS and TRST_L. All digital input, output, input/output pins are tested except TAP pins.

10.1 INSTRUCTION REGISTER

The IEEE 1149.1 Test Logic consists of a TAP controller, an instruction register, and a group of test data registers including Bypass and Boundary Scan registers. The TAP controller is a synchronous 16-state machine driven by the Test Clock (TCK) and the Test Mode Select (TMS) pins. An independent power on reset circuit is provided to ensure the machine is in TEST_LOGIC_RESET state at power-up.
PI7C9X20505GP implements a 5-bit Instruction register to control the operation of the JTAG logic. The defined instruction codes are shown in Table 10-1. Those bit combinations that are not listed are equivalent to the BYPASS (11111) instruction:

Table 10-1 Instruction register codes

Instruction	Operation Code (binary)	Register Selected	Operation
EXTEST	00000	Boundary Scan	Drives / receives off-chip test data
SAMPLE	00001	Boundary Scan	Samples inputs / pre-loads outputs
HIGHZ	00101	Bypass	Tri-states output and I/O pins except TDO pin
CLAMP	00100	Bypass	Drives pins from boundary-scan register and selects Bypass register for shifts
IDCODE	01100	Device ID	Accesses the Device ID register, to read manufacturer ID, part number, and version number
BYPASS	11111	Bypass	Selected Bypass Register
INT_SCAN	00010	Internal Scan	Scan test
MEM_BIST	01010	Memory BIST	Memory BIST test

10.2 BYPASS REGISTER

The required bypass register (one-bit shift register) provides the shortest path between TDI and TDO when a bypass instruction is in effect. This allows rapid movement of test data to and from other components on the board. This path can be selected when no test operation is being performed on the PI7C9X20505GP.

10.3 DEVICE ID REGISTER

This register identifies Pericom as the manufacturer of the device and details the part number and revision number for the device.

Table 10-2 JTAG device ID register

Bit	Type	Value	Description
31-28	RO	0001	Version number
27-12	RO	1001001000000100	Last 4 digits (hex) of the die part number
11-1	RO	01000111111	Pericom identifier assigned by JEDEC
0	RO	1	Fixed bit equal to 1'b1

10.4 BOUNDARY SCAN REGISTER

The boundary scan register has a set of serial shift-register cells. A chain of boundary scan cells is formed by connected the internal signal of the PI7C9X20505GP package pins. The VDD, VSS, and JTAG pins are not in the boundary scan chain. The input to the shift register is TDI and the output from the shift register is TDO. There are 4 different types of boundary scan cells, based on the function of each signal pin.

The boundary scan register cells are dedicated logic and do not have any system function. Data may be loaded into the boundary scan register master cells from the device input pins and output pin-drivers in parallel by the mandatory SAMPLE and EXTEST instructions. Parallel loading takes place on the rising edge of TCK.

10.5 JTAG BOUNDARY SCAN REGISTER ORDER

Table 10-3 JTAG boundary scar register definition

Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
0	CLKREQ1_L	H15	Input	
1	DWNRST_L[1]	P11	Output2	
2	CLKREQ2_L	P12	Input	
3	DWNRST_L[2]	P13	Output2	
4	CLKREQ3_L	N14	Input	
5	DWNRST_L[3]	L14	Output2	
6	PERST_L	K14	Input	
7	WAKE_L	H14	Input	
8	DEBUG_OUT[0]	G14	Bidir	14
9	DEBUG_OUT[1]	D16	Bidir	14
10	DEBUG_OUT[2]	D15	Bidir	14
11	DEBUG_OUT[3]	C16	Bidir	14
12	DEBUG_OUT[4]	C15	Bidir	14
13	DEBUG_OUT[5]	C14	Bidir	14
14			Control	
15	DEBUG_OUT[6]	B16	Bidir	14
16	DEBUG_OUT[7]	B15	Bidir	14
17	DEBUG_OUT[8]	B14	Bidir	14
18	DEBUG_OUT[9]	A16	Bidir	14
19	DEBUG_OUT[10]	A15	Bidir	14
20	DEBUG_OUT[11]	A14	Bidir	14
21	GPIO[0]	A13	Bidir	22
22			Control	
23	GPIO[1]	B13	Bidir	24
24			Control	
25	GPIO[2]	A12	Bidir	26
26			Control	
27	GPIO[3]	B12	Bidir	28
28			Control	
29	GPIO[4]	A11	Bidir	30
30			Control	
31	GPIO[5]	B11	Bidir	32
32			Control	
33	GPIO[6]	A10	Bidir	34
34			Control	
35	GPIO[7]	B10	Bidir	36
36			Control	
37	PWR_IND[1]	D2	Output2	
38	PWR_IND[2]	E1	Output2	
39	PWR_IND[3]	F1	Output2	
40	ATT_IND[1]	G3	Output2	

Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
41	ATT_IND[2]	G1	Output2	
42	ATT_IND[3]	H1	Output2	
43	ATT_BTN[1]	F2	Input	
44	ATT_BTN[2]	F3	Input	
45	ATT_BTN[3]	G2	Input	
46	MRL_PDC[1]	H3	Input	
47	MRL_PDC[2]	J3	Input	
48	MRL_PDC[3]	K3	Input	
49	PWR_ENA[1]	L3	Output2	
50	PWR_ENA[2]	M3	Output2	
51	PWR_ENA[3]	P3	Output2	
52	PWR_FLT[1]	P4	Input	
53	PWR_FLT[2]	P5	Input	
54	PWR_FLT[3]	P6	Input	
55	LANEACT[0]	J1	Output2	
56	LANEACT[1]	K1	Output2	
57	LANEACT[2]	L1	Output2	
58	LANEACT[3]	M1	Output2	
59	EECLK	N1	Output2	
60	EEPD	N2	Bidir	61
61			Control	

11 POWER MANAGEMENT

The PI7C9X20505GP supports D0, D1, D2, D3-hot, and D3-cold Power States. The PCI Express Physical Link Layer of the PI7C9X20505GP device supports the PCI Express Link Power Management with L0, L0s, L1, L2/L3 ready and L3 Power States.

During the transition from D3-hot to D3-cold state, the main power supplies of VDDC and VDDR are turned off to save power while keeping the VDDCAUX and VAUX with the auxiliary power supplies to maintain all necessary information to be restored to the full power D0 state. PI7C9X20505GP has been designed to have sticky registers that are powered by auxiliary power supplies. PI7C9X20505GP forwards power management messages to the upstream Switches or root complex.

PI7C9X20505GP also supports ASPM (Active State Power Management) to facilitate the link power saving.

PI7C9X20505GP supports beacon generation and WAKEUP_L signal.

12 ELECTRICAL AND TIMING SPECIFICATIONS

12.1 ABSOLUTE MAXIMUM RATINGS

Table 12-1 Absolute maximum ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to 150°C
Ambient Temperature with power applied	-40°C to 85°C
PCI Express supply voltage to ground potential (VDDA, VDDC, and VDDCAUX)	-0.3v to 3.0v
DC input voltage for PCI Express signals	-0.3v to 3.0v

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

12.2 DC SPECIFICATIONS

Table 12-2 DC electrical characteristics

Power Pins	Min.	Typ.	Max.
VDDA	0.9v	1.0v	1.1v
VDDR	3.0v	3.3v	3.6v
VDDC	0.9v	1.0v	1.1v
VAUX	3.0v	3.3v	3.6v
VDDCAUX	0.9v	1.0v	1.1v
VTT	VDDC	1.5v	1.8v

VDDA: analog power supply for PCI Express Interface
VDDR: digital power supply for 3.3v I/O Interface
VDDC: digital power supply for the core
VAUX: digital auxiliary power supply for 3.3v I/O Interface
VDDCAUX: auxiliary power supply for the core
VTT: termination power supply for PCI Express Interface

In order to support auxiliary power management fully, it is recommended to have VDDC and VDDCAUX separated.
The typical power consumption of PI7C9X20505GP is about 1.0 watt.

12.3 AC SPECIFICATIONS

Table 12-3 Transmitter Characteristics

Symbol	Description	Min	Typical	Max.	Unit
Voltage Parameters					
$V_{TX-DIFF}$[a]	Output voltage compliance @ typical swing				
	$V_{TX-DIFFp}$ (peak-to-peak, single ended)	400	500	600	mV
	$V_{TX-DIFFpp}$ (peak-to-peak, differential)	800	1000	1200	mV
V_{SW}	Supported TX output voltage range (pp, differential)	400[b]		1500[c]	mV
V_{OL}	Low-level output voltage		V_{TT} - 1.5 *$V_{TX-DIFFp}$		V
V_{OH}	High-level output voltage		V_{TT} - 0.5$V_{TX-DIFFp}$		V
$V_{TX-CM-AC}$	Transmit common-mode voltage in L0	0.50	V_{TT} - $V_{TX-DIFFp}$	1.45	V
$V_{TX-CM-HiZ}$	Transmit common-mode voltage in L0s (TX) & L1		$V_{TX-CM-AC}$		V
$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	0		-7.96	dB
$V_{TX-IDLE-DIFFp}$	Electric Idle differential peak voltage			20	mV
$V_{TX-RCV-DETECT}$	Voltage change during Receive Detection		$V_{TX-DIFFp}$		mV
$RL_{TX-DIFF}$	Transmitter Differential Return loss	10			dB
RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB
Z_{OSE}	Single-ended output impedance	40	50	60	Ω
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω
$T_{TX-RISE, TTX-FALL}$	Rise / Fall time of TxP, TxN outputs	80		110[d]	ps
Jitter Parameters					
UI	Unit Interval	399.88	400	400.12	ps
$T_{TX-MAX-JITTER}$	Transmitter total jitter (peak-to-peak)			0.25[e]	UI
T_{TX-EYE}	Minimum TX Eye Width (1 - $T_{TX-MAX-JITTER}$)	0.75			UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.125	UI
Timing Parameters					
$L_{TLAT-10}$	Transmitter data latency (for n=10)	9		11	UI
$L_{TLAT-20}$	Transmitter data latency (for n=20)	9		11	UI
$L_{TX-SKEW}$	Transmitter data skew between any 2 lanes	0		2 + 200ps	UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an Electrical Idle ordered set		4	6	ns
T_{EIExit}	Time to exit Electrical Idle (L0s) state into L0		12	16	ns
T_{BTEn}	Time from asserting BeaconTxEn to beacon being transmitted on the lane		30	80	ns
$T_{RxDetectEn}$	Pulse width of RxDetectEn input	9.8	10	10.2	us
$T_{RxDetect}$	RxDetectEn falling edge to RxDetect delay		1	2	ns

a. Measured with Vtt = 1.2V, HiDrv=’0’,LowDrv=’0’ and Dtx=’0000’.
b. Minimum swing assumes LoDrv = 1, HiDrv = 0 and Dtx =1100
c. Max swing assumes LoDrv = 0, HiDrv = 1, Dtx = 0010, VTT = 1.8V
d. As measured between 20% and 80% points. Will depend on package characteristics.
e. Measured using PCI Express Compliance Pattern

Table 12-4 Receiver Characteristics

Symbol	Description	Min	Typical	Max.	Unit
Voltage Parameters					
$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	170		1200	mV
$V_{RX-IDLE-DET-DIFFp-p}$	Differential input threshold voltage (peak-to-peak) to assert TxIdleDetect output	65		175	mV
$V_{RX-CM-AC}$	Receiver common-mode voltage for AC-coupling		0	150	mV
$T_{RX-RISE, TRX-FALL}$	Rise time / Fall time of RxP, RxN inputs			160	Ps
$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω
$Z_{RX-COM-DC}$	Single-ended input impedance	40	50	60	Ω
$Z_{RX-COM-INITIAL-DC}$	Initial input common mode impedance (DC)	5	50	60	Ω
$Z_{RX-COM-HIGH-IMP-DC}$	Powered down input common mode impedance (DC)	200k			Ω
$RL_{RX-DIFF}$	Receiver Differential Return Loss[a]	10			dB
RL_{RX-CM}	Receiver Common Mode Return Loss[b]	6			dB
Jitter Parameters					
$T_{RX-MAX-JITTER}$	Receiver total jitter tolerance			0.65	UI
T_{RX-EYE}	Minimum Receiver Eye Width	0.35			UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between jitter median and max deviation from median			0.325	UI
Timing Parameters					
LRLAT-10	Receiver data latency for n=10	28		29	bits
LRLAT-20	Receiver data latency for n=20	49		60	bits
TRX-SKEW	Receiver data skew between any 2 lanes	0		1[c]	bits
TBDDly	Beacon-Activity on channel to detection of Beacon[d]			200	us
TRX-IDLE_ENTER	Delay from detection of Electrical Idle condition on the channel to assertion of TxIdleDetect output		10	20	ns
TRX-IDLE_EXIT	Delay from detection of L0s to L0 transition to deassertion of TxIdleDetect output		5	10	ns

a. Over a frequency range of 50 MHz to 1.25 GHz.
b. Over a frequency range of 50 MHz to 1.25 GHz.
c. Assuming synchronized bit streams at the respective receiver inputs.
d. This is a function of beacon frequency

13 PACKAGE INFORMATION

The package of PI7C9X20505GP is a 17mm x 17mm PBGA (256 Pin) package. The ball pitch is 1.0mm and the ball size is 0.5mm. The following are the package information and mechanical dimension:

Figure 13-1 Bottom view drawing

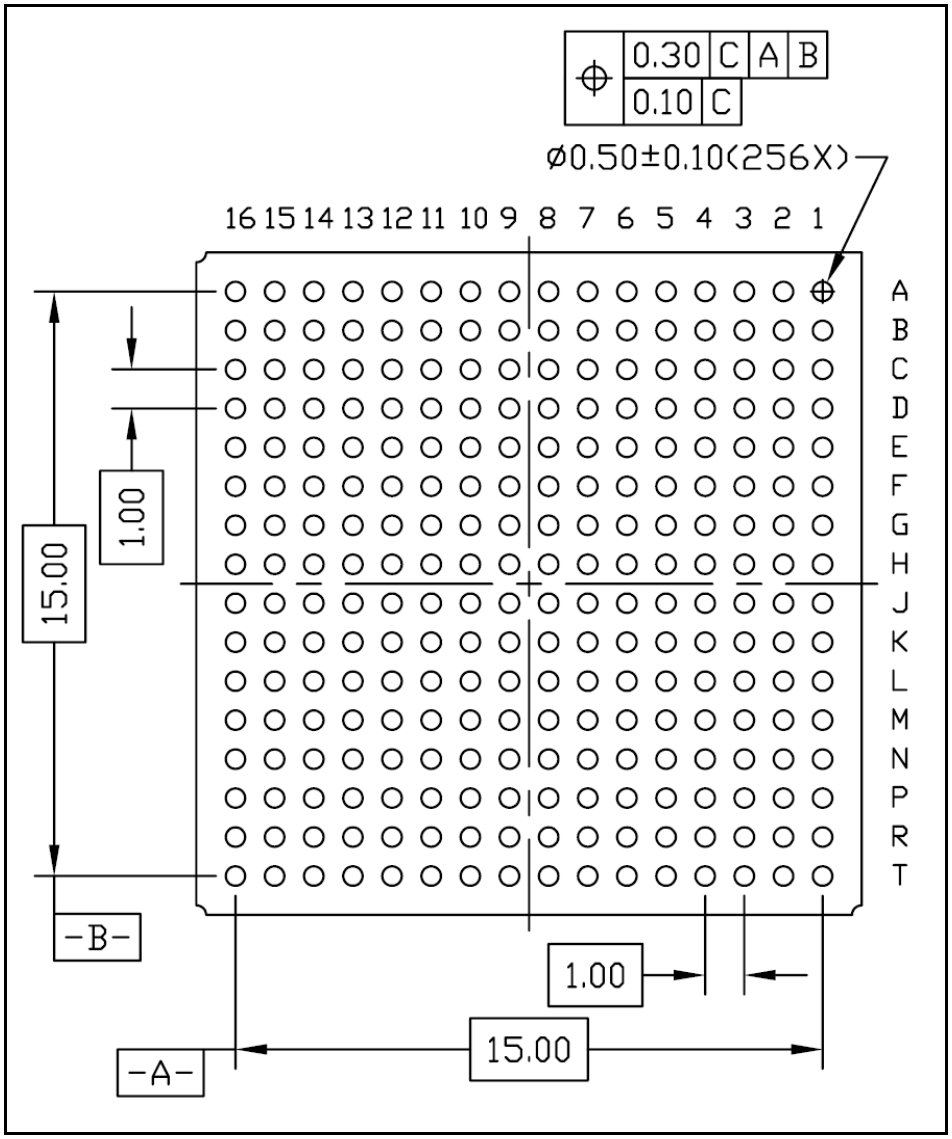
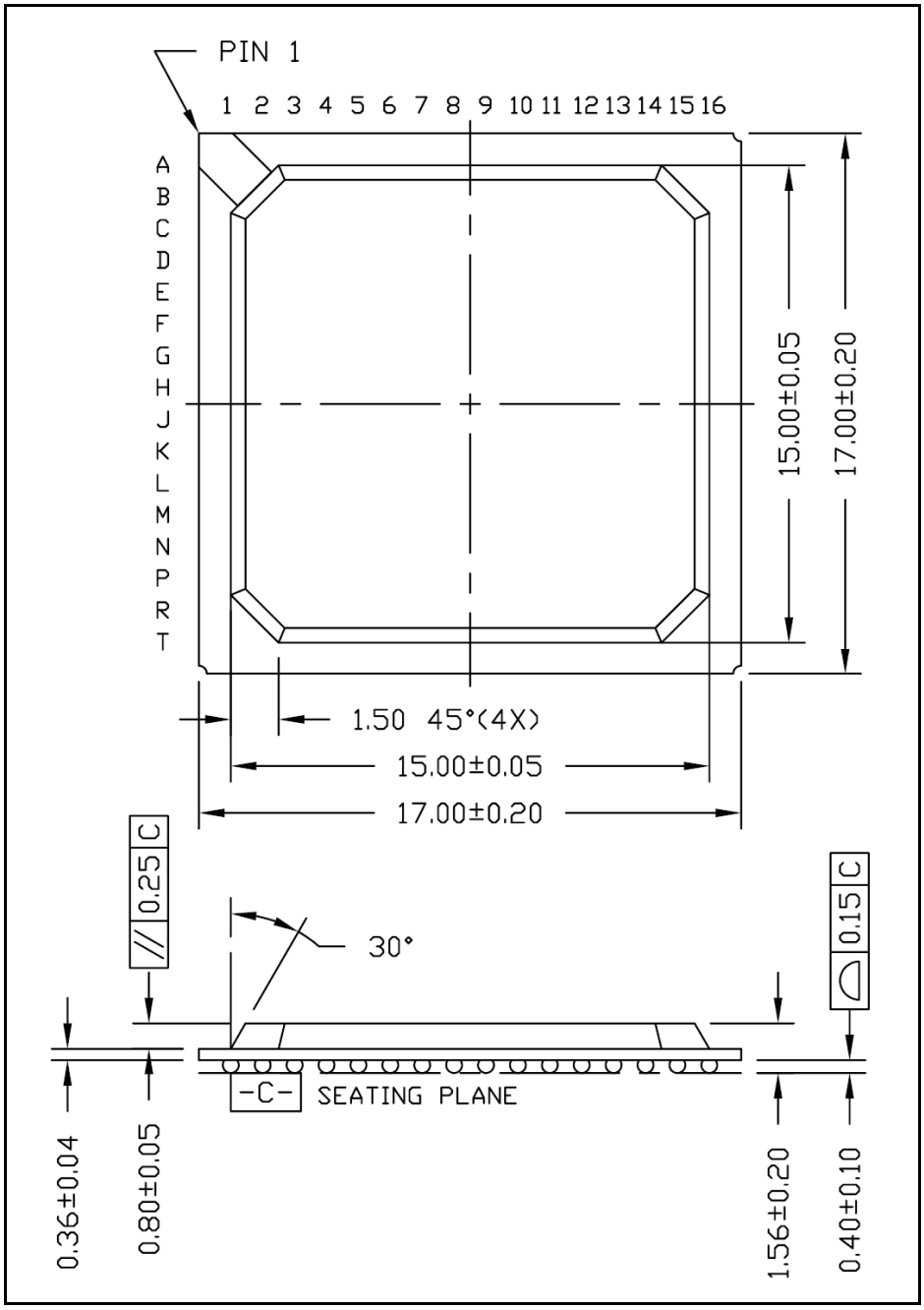
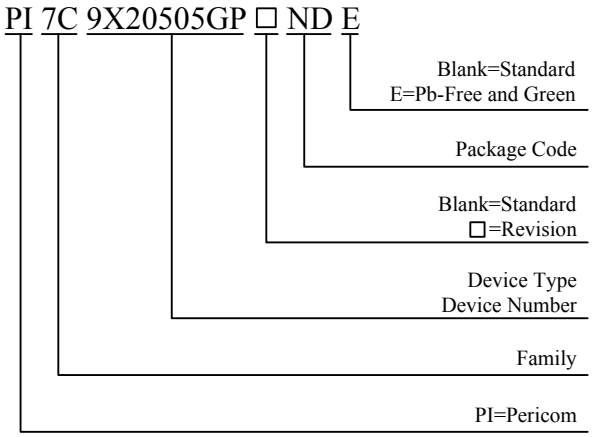


Figure 13-2 Package outline drawing



14 ORDERING INFORMATION

Part Number	Temperature Range	Package	Pb-Free & Green
PI7C9X20505GP□NDE	-40° to 85°C (Industrial Temperature)	256-pin PBGA 17mm x 17mm	Yes



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