



# FDD86110

## N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET

100 V, 50 A, 10.2 mΩ

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 10.2 mΩ at  $V_{GS} = 10$  V,  $I_D = 12.5$  A
- Max  $r_{DS(on)}$  = 16 mΩ at  $V_{GS} = 6$  V,  $I_D = 9.8$  A
- 100% UIL tested
- RoHS Compliant

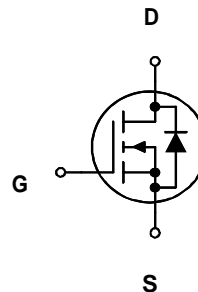
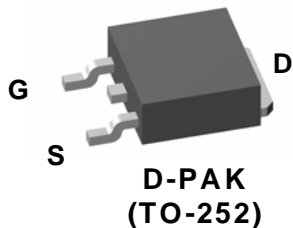


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

### Application

- DC - DC Conversion



### MOSFET Maximum Ratings $T_C = 25$ °C unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous $T_C = 25$ °C	50	A
	-Continuous $T_A = 25$ °C (Note 1a)	12.5	
	-Pulsed (Note 4)	150	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	135	mJ
$P_D$	Power Dissipation $T_C = 25$ °C	127	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	3.1	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.98	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD86110	FDD86110	D-PAK(TO-252)	13 "	12 mm	2500 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		72		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	2	2.8	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-10		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 12.5\text{ A}$		8.5	10.2	m $\Omega$
		$V_{GS} = 6\text{ V}$ , $I_D = 9.8\text{ A}$		11.3	16	
		$V_{GS} = 10\text{ V}$ , $I_D = 12.5\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		15	18	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 12.5\text{ A}$		38		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		1702	2265	pF
$C_{oss}$	Output Capacitance			379	505	pF
$C_{rss}$	Reverse Transfer Capacitance			17	30	pF
$R_g$	Gate Resistance		0.1	0.5	1.5	$\Omega$

### Switching Characteristics

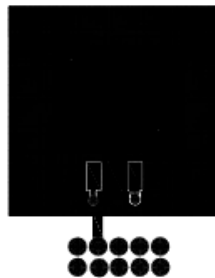
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$ , $I_D = 12.5\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		12	20	ns
$t_r$	Rise Time			5.4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			19	35	ns
$t_f$	Fall Time			3.9	10	ns
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		25	35
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 50\text{ V}$ , $I_D = 12.5\text{ A}$		7.1		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			5.2		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 12.5\text{ A}$ (Note 2)		0.80	1.3	V
		$V_{GS} = 0\text{ V}$ , $I_S = 2.6\text{ A}$ (Note 2)		0.72	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 12.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		52	83	ns
$Q_{rr}$	Reverse Recovery Charge			60	96	nC

#### Notes:

- 1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a) 40  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



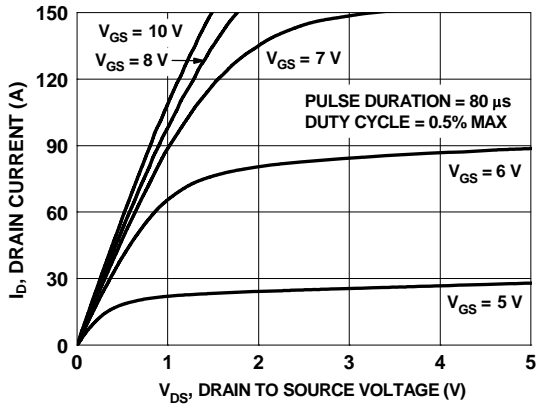
b) 96  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad

2: Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

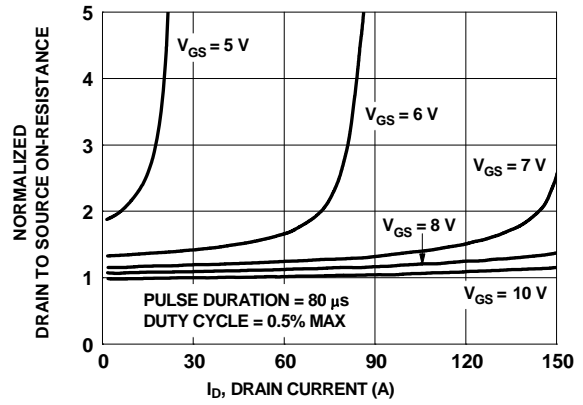
3: Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 0.3\text{ mH}$ ,  $I_{AS} = 30\text{ A}$ ,  $V_{DD} = 90\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 48\text{ A}$ .

4: Pulsed Drain current is tested at 300  $\mu\text{s}$  with 2% duty cycle. For repetitive pulses, the pulse width is limited by the maximum junction temperature.

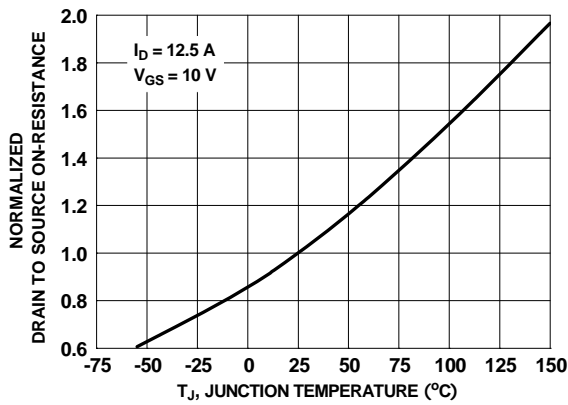
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



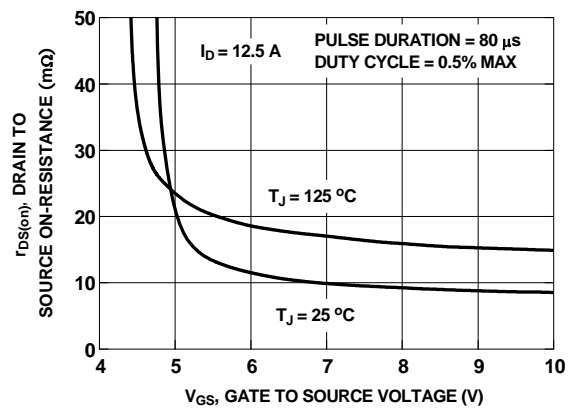
**Figure 1. On Region Characteristics**



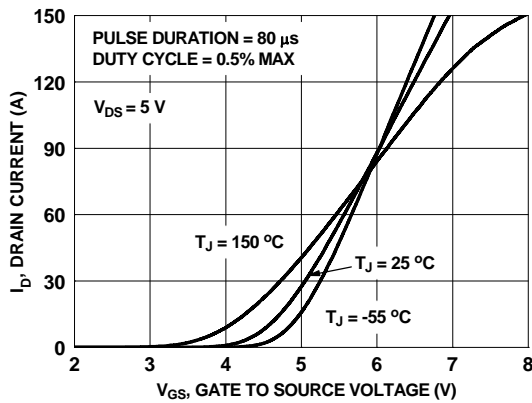
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



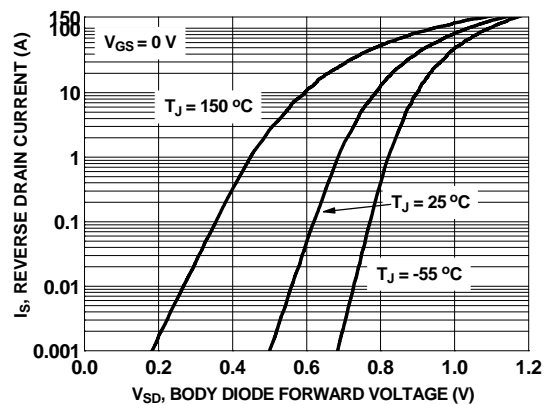
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

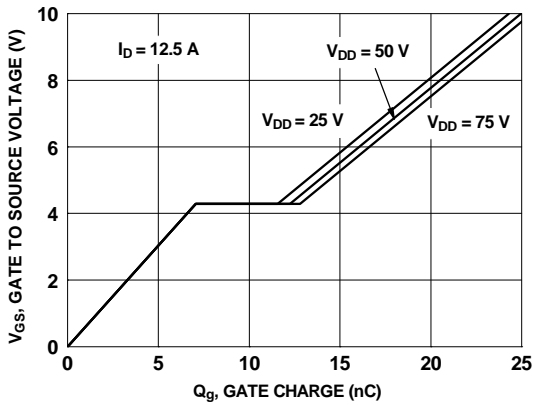


**Figure 5. Transfer Characteristics**

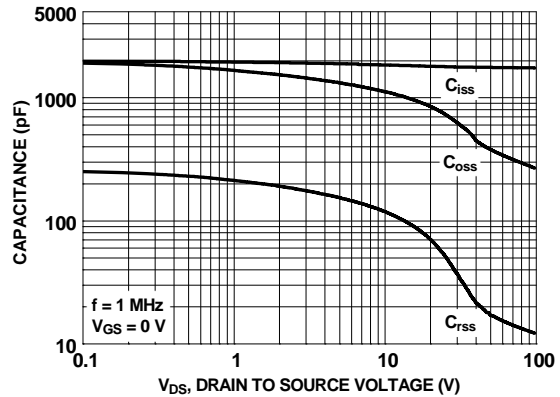


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

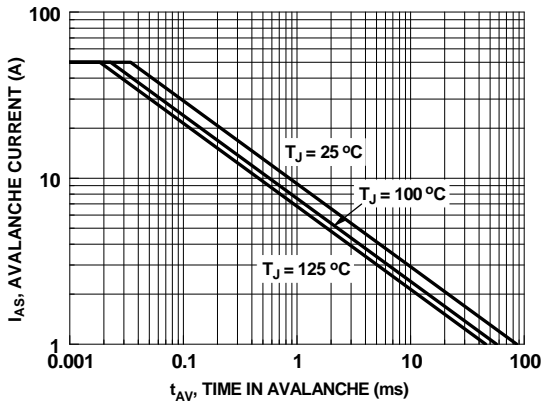
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



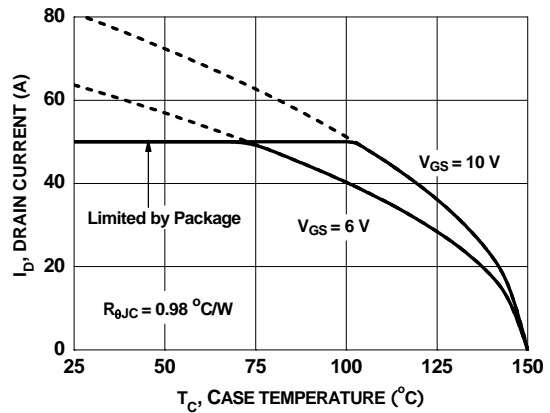
**Figure 7. Gate Charge Characteristics**



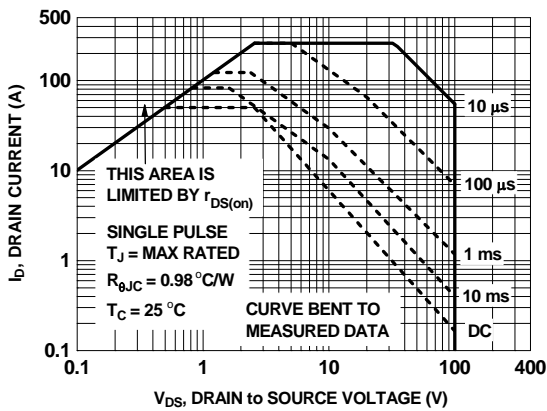
**Figure 8. Capacitance vs Drain to Source Voltage**



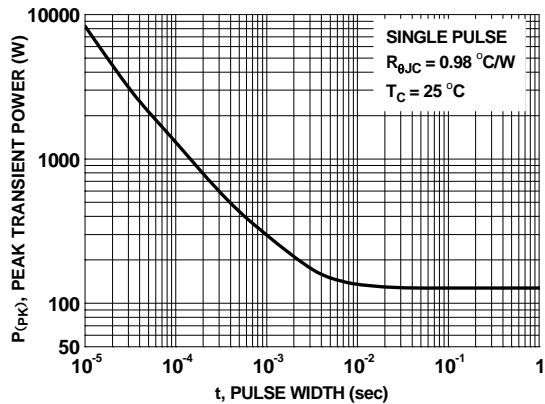
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

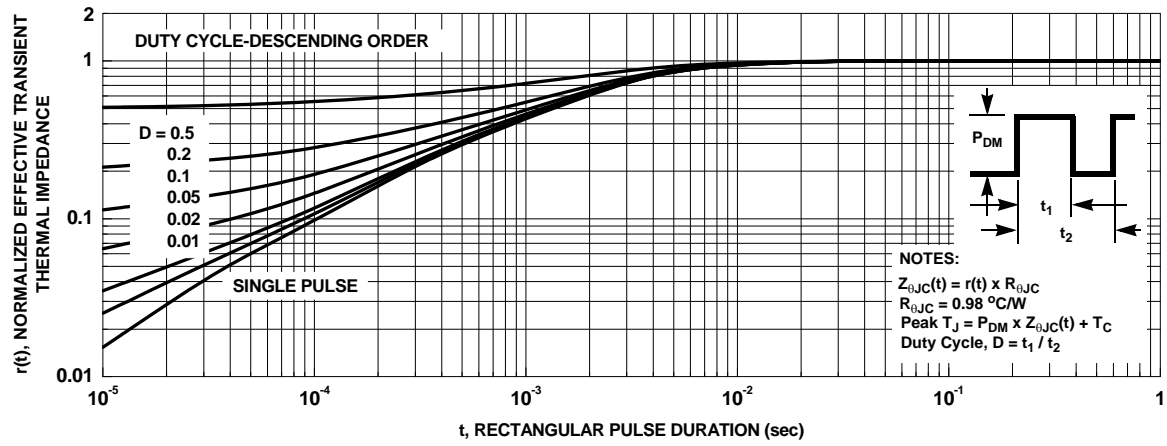


**Figure 11. Forward Bias Safe Operating Area**

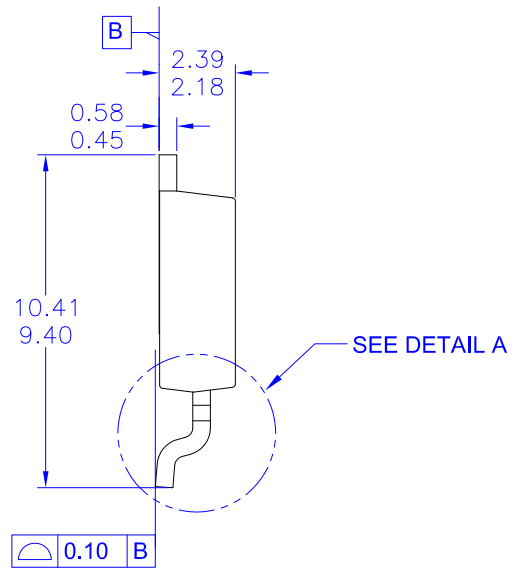
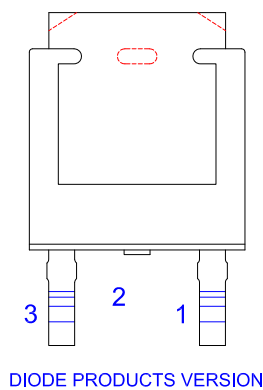
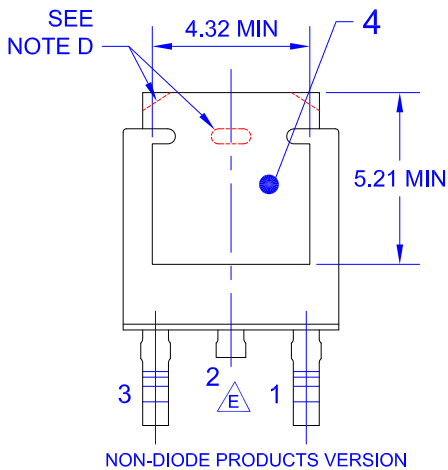
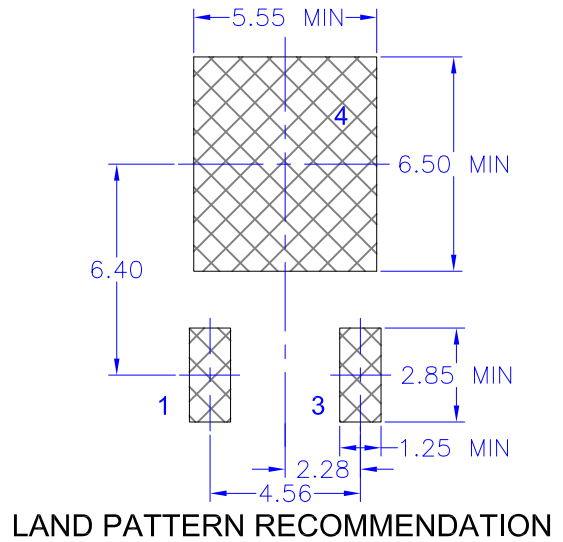
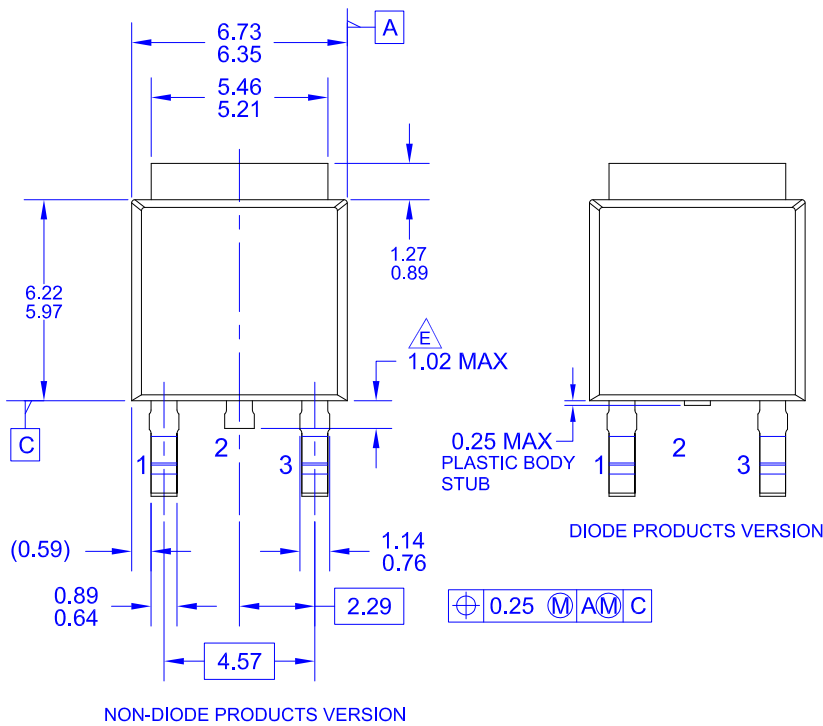


**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

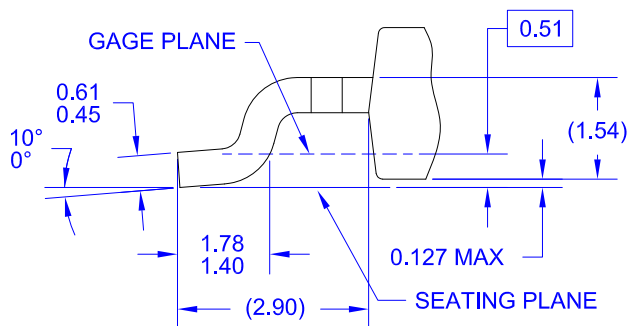


**Figure 13. Junction-to-Case Transient Thermal Response Curve**



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV10








DETAIL A  
(ROTATED -90°)  
SCALE: 12X





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| EfficientMax™   | MicroPak™                                      | Solutions for Your Success™   | UHC®  |
| ESBC™   | MicroPak2™                                     | SPM®  | Ultra FRFET™  |
|  | MillerDrive™                                   | STEALTH™  | UniFET™   |
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| Fairchild Semiconductor®  | MotionGrid®                                    | SuperSOT™-3   | VisualMax™  |
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| FETBench™   | OptoHiT™                                       | Sync-Lock™  |   |
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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