

NL17SZ125

Non-Inverting 3-State Buffer

The NL17SZ125 is a high performance non-inverting buffer operating from a 1.65 V to 5.5 V supply.

Features

- Extremely High Speed: t_{PD} 2.6 ns (typical) at $V_{CC} = 5.0$ V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Overvoltage Tolerant Inputs and Outputs
- LVTTL Compatible – Interface Capability With 5.0 V TTL Logic with $V_{CC} = 3.0$ V
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- 3-State OE Input is Active-Low
- Replacement for NC7SZ125
- Chip Complexity = 36 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

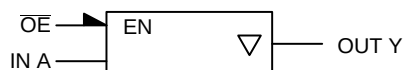


Figure 1. Logic Symbol

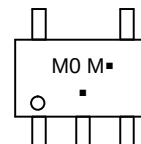


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MARKING DIAGRAMS

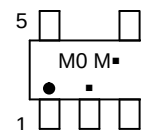

SC-88A (SOT-353)
DF SUFFIX
CASE 419A



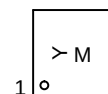

SOT-553
XV5 SUFFIX
CASE 463B



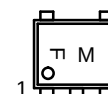

TSOP-5
DT SUFFIX
CASE 483




UDFN6
1.0 x 1.0
CASE 517BX




SOT-953
CASE 527AE



M0 or F = Specific Device Code
(F with 90 degree clockwise rotation)
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NL17SZ125

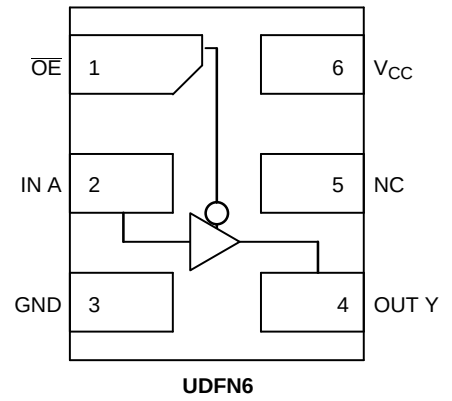
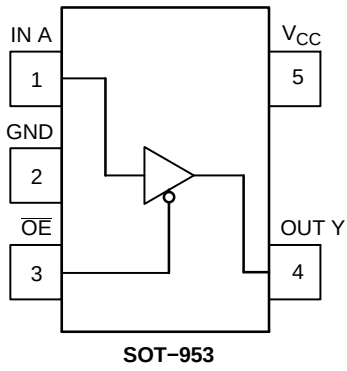
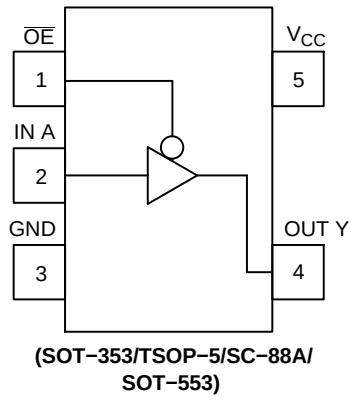


Figure 2. Pinout (Top View)

PIN ASSIGNMENT (SOT-353/ TSOP-5/SC-88A/SOT-553)

Pin	Function
1	$\overline{OE}$
2	IN A
3	GND
4	OUT Y
5	V _{CC}

PIN ASSIGNMENT (SOT-953)

Pin	Function
1	IN A
2	GND
3	$\overline{OE}$
4	OUT Y
5	V _{CC}

PIN ASSIGNMENT (UDFN)

Pin	Function
1	$\overline{OE}$
2	IN A
3	GND
4	OUT Y
5	NC
6	V _{CC}

FUNCTION TABLE

Input		Output
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

X = Don't Care

MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_{IN}	DC Input Voltage	-0.5 to +7.0	V
V_{OUT}	DC Output Voltage (SOT-353/TSOP-5/SC-88A/SOT-553/UDFN Packages) Power-Down Mode	-0.5 to +7.0	V
V_{OUT}	DC Output Voltage (SOT-953 Package)	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	-50	mA
I_{OK}	DC Output Diode Current (SOT-953 Package) $V_{OUT} < GND, V_{OUT} > V_{CC}$	± 50	mA
I_{OK}	DC Output Diode Current (SOT-353/SC70-5/SC-88A/SOT-553 Packages) $V_{OUT} < GND$	-50	mA
I_{OUT}	DC Output Sink Current	± 50	mA
I_{CC}	DC Supply Current per Supply Pin	± 100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 1) SC-88A/SOT-553 TSOP-5	350 230	°C/W
P_D	Power Dissipation in Still Air at 85°C	150	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 5)	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	DC Supply Voltage	1.65	5.5	V
V_{IN}	DC Input Voltage	0	5.5	V
V_{OUT}	DC Output Voltage (SOT-353/TSOP-5/SC-88A/SOT-553/UDFN Packages)	0	5.5	V
V_{OUT}	DC Output Voltage (SOT-953 Package)	0	V_{CC}	V
T_A	Operating Temperature Range	-55	+125	°C
t_r, t_f	Input Rise and Fall Time $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$ $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ $V_{CC} = 3.0 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0 0 0 0	20 20 10 5.0	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

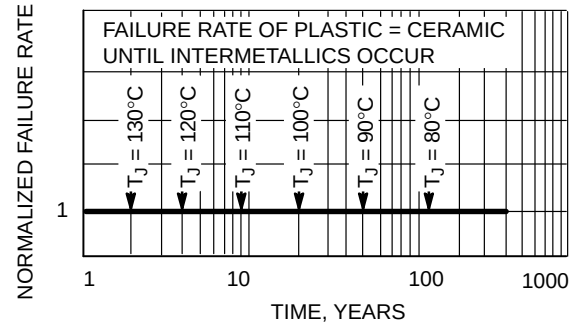


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	$T_A = 25^\circ\text{C}$			$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Units	Condition
			Min	Typ	Max	Min	Max		
V_{IH}	High-Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.75 V_{CC} 0.7 V_{CC}			0.75 V_{CC} 0.7 V_{CC}		V	
V_{IL}	Low-Level Input Voltage	1.65 to 1.95 2.3 to 5.5			0.25 V_{CC} 0.3 V_{CC}		0.25 V_{CC} 0.3 V_{CC}	V	
V_{OH}	High-Level Output Voltage $V_{IN} = V_{IH}$	1.65 1.8 2.3 3.0 4.5	1.55 1.7 2.2 2.9 4.4	1.65 1.8 2.3 3.0 4.5		1.55 1.7 2.2 2.9 4.4		V	$I_{OH} = -100 \mu\text{A}$
		1.65 2.3 3.0 3.0 4.5	1.29 1.9 2.4 2.3 3.8	1.52 2.15 2.80 2.68 4.20		1.29 1.9 2.4 2.3 3.8		V	$I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$ $I_{OH} = -16 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -32 \text{ mA}$
V_{OL}	Low-Level Output Voltage $V_{IN} = V_{IL}$	1.65 1.8 2.3 3.0 4.5		0.0 0.0 0.0 0.0 0.0	0.1 0.1 0.1 0.1 0.1		0.1 0.1 0.1 0.1 0.1	V	$I_{OL} = 100 \mu\text{A}$
		1.65 2.3 3.0 3.0 4.5		0.08 0.10 0.15 0.22 0.22	0.24 0.30 0.40 0.55 0.55		0.24 0.30 0.40 0.55 0.55	V	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$ $I_{OL} = 16 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 32 \text{ mA}$

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	T _A = 25°C			-55°C ≤ T _A ≤ 125°C		Units	Condition
			Min	Typ	Max	Min	Max		
I _{IN}	Input Leakage Current	0 to 5.5			±0.1		±1.0	μA	V _{IN} = 5.5 V or GND
I _{OZ}	3-State Output Leakage	1.65 to 5.5			±0.5		±5.0	μA	V _{IN} = V _{IH} or V _{IL} 0 V ≤ V _{OUT} ≤ 5.5 V
I _{OFF}	Power Off Leakage Current (SOT-353/ TSOP-5/SC-88A/ SOT-553/ UDFN Packages)	0			1.0		10	μA	V _{IN} = 5.5 V or V _{OUT} = 5.5 V
I _{CC}	Quiescent Supply Current	5.5			1.0		10	μA	V _{IN} = 5.5 V or GND

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (t_R = t_F = 3.0 ns)

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-55°C ≤ T _A ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay AN to YN (Figures 4 and 5, Table 1)	R _L = 1 MΩ C _L = 15 pF	1.8 ± 0.15	2.0	9.0	10	2.0	10.5	ns
		R _L = 1 MΩ C _L = 15 pF	2.5 ± 0.2	1.0		7.5	1.0	8.0	
		R _L = 1 MΩ C _L = 15 pF	3.3 ± 0.3	0.8		5.2	0.8	5.5	
		R _L = 500 Ω C _L = 50 pF		1.2		5.7	1.2	6.0	
t _{PZH} t _{PZL}	Output Enable Time (Figures 6, 7 and 8, Table 1)	R _L = 1 MΩ C _L = 15 pF	5.0 ± 0.5	0.5		4.5	0.5	4.8	ns
		R _L = 500 Ω C _L = 50 pF		0.8		5.0	0.8	5.3	
		R _L = 250 Ω C _L = 50 pF	1.8 ± 0.15	2.0	7.6	9.5	2.0	10	
			2.5 ± 0.2	1.8		8.5	1.8	9.0	
t _{PHZ} t _{PLZ}	Output Disable Time (Figures 6, 7 and 8, Table 1)		3.3 ± 0.3	1.2		6.2	1.2	6.5	ns
			5.0 ± 0.5	0.8		5.5	0.8	5.8	
		R _L and R ₁ = 500 Ω C _L = 50 pF	1.8 ± 0.15	2.0	8.0	10	2.0	10.5	
			2.5 ± 0.2	1.5		8.0	1.5	8.5	
			3.3 ± 0.3	0.8		5.7	0.8	6.0	ns
			5.0 ± 0.5	0.3		4.7	0.3	5.0	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	2.5	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	2.5	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC} 10 MHz, V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	9 11	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

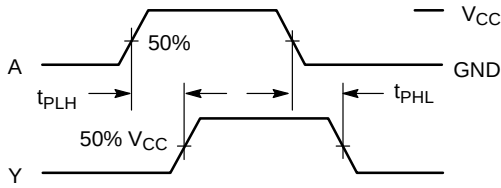
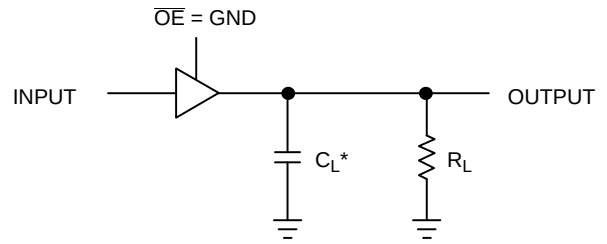
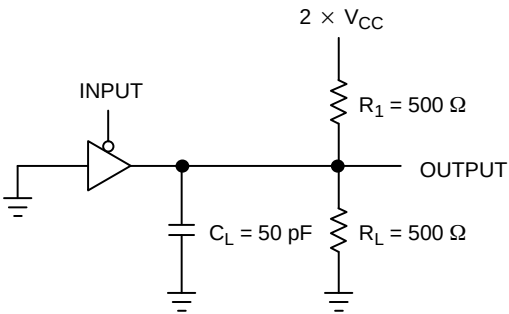


Figure 4. Switching Waveform



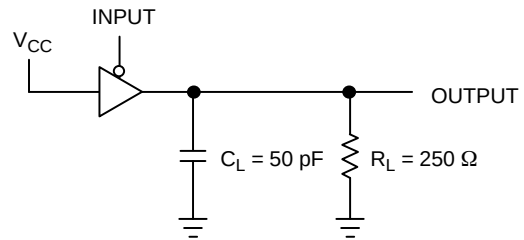
*Includes all probe and jig capacitance.
A 1 MHz square input wave is recommended for propagation delay tests.

Figure 5. t_{PLH} or t_{PHL}



A 1 MHz square input wave is recommended for propagation delay tests.

Figure 6. t_{PZL} or t_{PLZ}



A 1 MHz square input wave is recommended for propagation delay tests.

Figure 7. t_{PZH} or t_{PHZ}

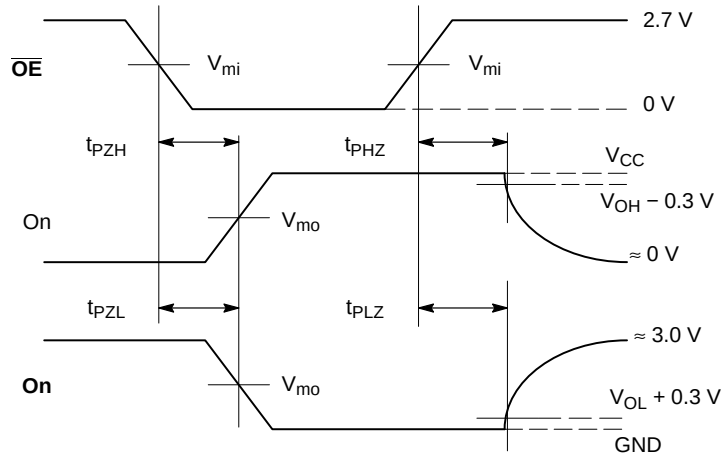


Figure 8. AC Output Enable and Disable Waveform

Table 1. OUTPUT ENABLE AND DISABLE TIMES

$t_R = t_F = 2.5$ ns, 10% to 90%; $f = 1$ MHz; $t_W = 500$ ns

Symbol	V_{CC}		
	$3.3 \text{ V} \pm 0.3 \text{ V}$	2.7 V	$2.5 \text{ V} \pm 0.2 \text{ V}$
V_{mi}	1.5 V	1.5 V	$V_{CC}/2$
V_{mo}	1.5 V	1.5 V	$V_{CC}/2$

NL17SZ125

DEVICE ORDERING INFORMATION

Device	Package	Shipping†
NL17SZ125DFT2G	SC-88A (SOT-353) (Pb-Free)	3000 / Tape & Reel
NLV17SZ125DFT1G*	SC-88A (SOT-353) (Pb-Free)	3000 / Tape & Reel
NLV17SZ125DFT2G*	SC-88A (SOT-353) (Pb-Free)	3000 / Tape & Reel
NL17SZ125XV5T2G	SOT-553 (Pb-Free)	4000 / Tape & Reel
NL17SZ125DTT1G	TSOP-5 (Pb-Free)	3000 / Tape & Reel
NL17SZ125CMUTCG	UDFN6, 1.0 x 1.0 x 0.35P (Pb-Free)	3000 / Tape & Reel
NL17SZ125P5T5G	SOT-953 (Pb-Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

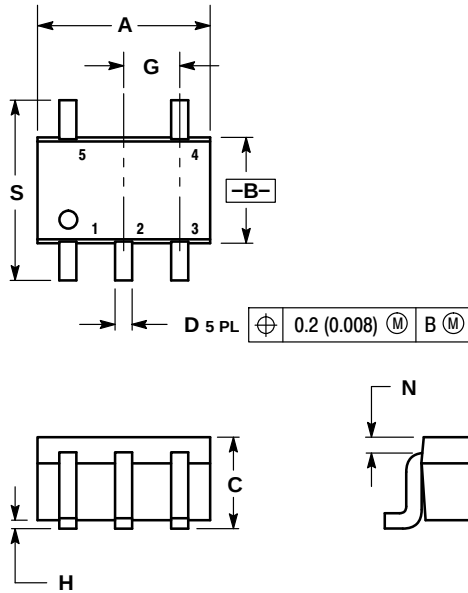
NL17SZ125

PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353)

CASE 419A-02

ISSUE L

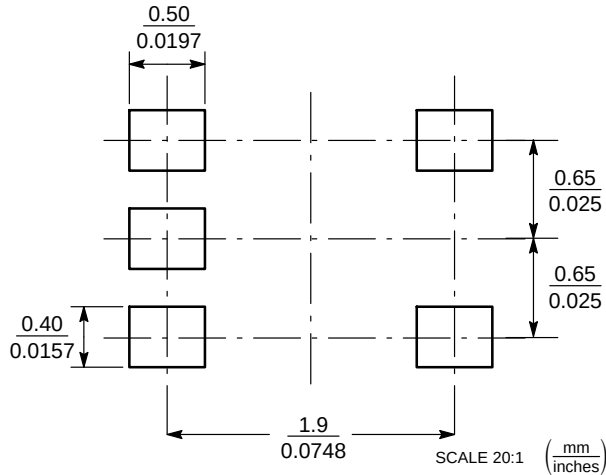


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT*

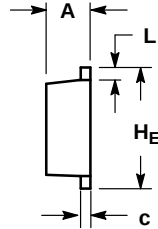
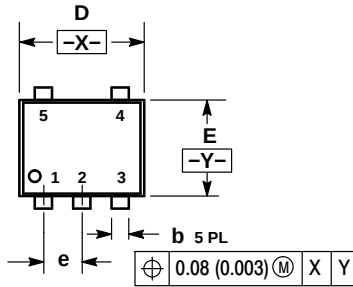


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NL17SZ125

PACKAGE DIMENSIONS

SOT-553, 5 LEAD CASE 463B ISSUE C

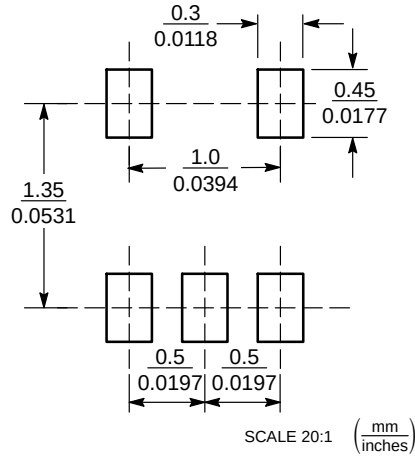


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.15	1.20	1.25	0.045	0.047	0.049
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H _E	1.55	1.60	1.65	0.061	0.063	0.065

SOLDERING FOOTPRINT*

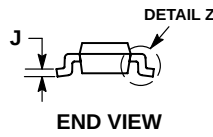
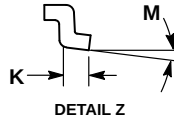
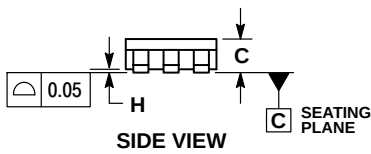
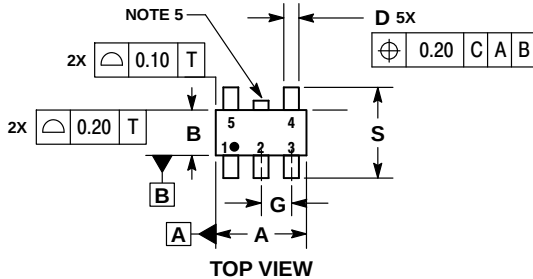


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NL17SZ125

PACKAGE DIMENSIONS

TSOP-5 CASE 483-02 ISSUE K

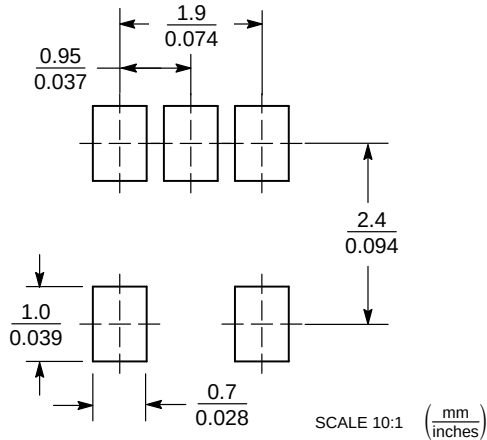


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

MILLIMETERS		
DIM	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

SOLDERING FOOTPRINT*

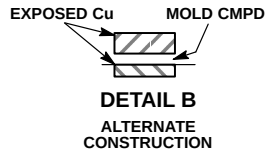
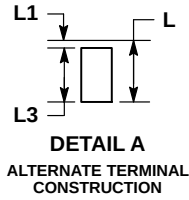
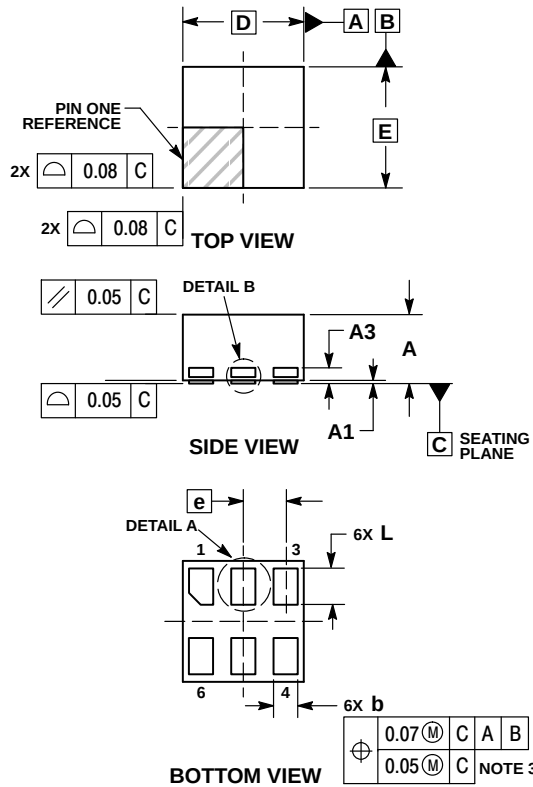


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NL17SZ125

PACKAGE DIMENSIONS

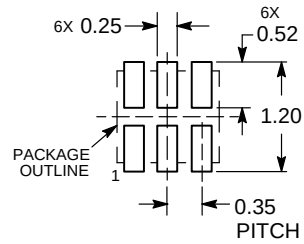
UDFN6, 1x1, 0.35P
CASE 517BX
ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
 4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	0.50	0.65
A1	0.00	0.05
A3	0.13	REF
b	0.17	0.23
D	1.00	BSC
E	1.00	BSC
e	0.35	
L	0.20	0.40
L1	---	0.15
L3	0.26	0.33

RECOMMENDED SOLDERING FOOTPRINT*



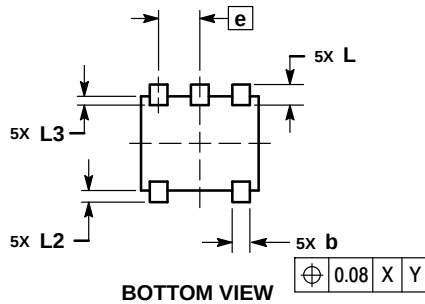
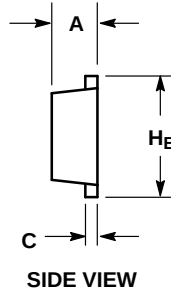
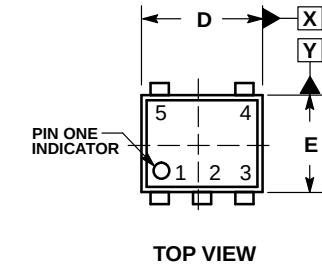
DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NL17SZ125

PACKAGE DIMENSIONS

SOT-953 CASE 527AE ISSUE E

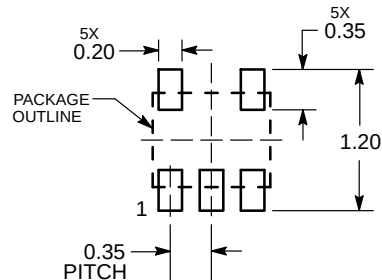


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H _E	0.95	1.00	1.05
L	0.175 REF		
L2	0.05	0.10	0.15
L3	---	---	0.15

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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