TPS6213xA-Q1 3V to 17-V 3A Step-Down Converter with DCS-Control™

1 Features

- DCS-Control™ Topology
- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade: –40°C to 125°C Operating Junction Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Input Voltage Range: 3 to 17V
- Adjustable Output Voltage from 0.9 to 6V
- Pin-Selectable Output Voltage (nominal, + 5%)
- Programmable Soft Start and Tracking
- Seamless Power Save Mode Transition
- Quiescent Current of 17µA (typ.)
- Power Good Output
- 100% Duty Cycle Mode
- Short Circuit Protection
- Over Temperature Protection
- Available in a 3 × 3 mm, VQFN-16 Package

2 Applications

- Automotive POL supply
- Standard 12-V Rail Supplies
- Embedded Systems
- LDO Replacement

3 Description

The TPS62130A-Q1 device is an easy-to-use synchronous step-down DC-DC converter optimized for applications with high power density. A high switching frequency of typically 2.5 MHz allows the use of small inductors and provides fast transient response as well as high output-voltage accuracy through the use of the DCS-Control™ topology.

With a wide operating input-voltage range of 3 to 17 V, the device is ideally suited for systems powered from intermediate bus power rails. The device supports up to 3-A continuous output current at output voltages between 0.9 V and 6 V (with 100% duty cycle mode).

The output-voltage startup ramp is controlled by the soft-start pin, which allows operation as either a standalone power supply or in tracking configurations. Power sequencing is also possible by configuring the enable and open-drain power-good pins.

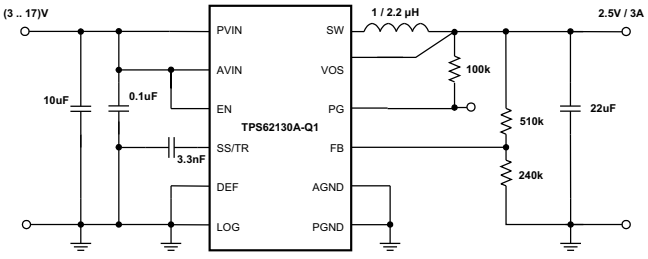
In power save mode, the device shows quiescent current of about 17 µA from V_{IN}. Power save mode which is entered automatically and seamlessly if the load is small, maintains high efficiency over the entire load range. In shutdown mode, the device is turned off and shutdown current consumption is less than 2 µA. The device is packaged in a 16-pin VQFN package measuring 3 × 3 mm (RGT).

Device Information(1)

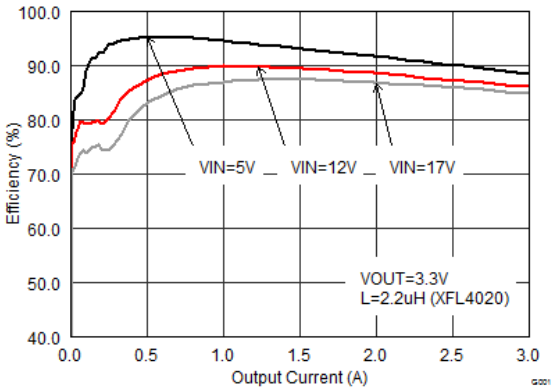
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62130A-Q1	VQFN (16)	3.00 mm x 3.00 mm
TPS62133A-Q1		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Efficiency vs Output Current



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5 Revision History

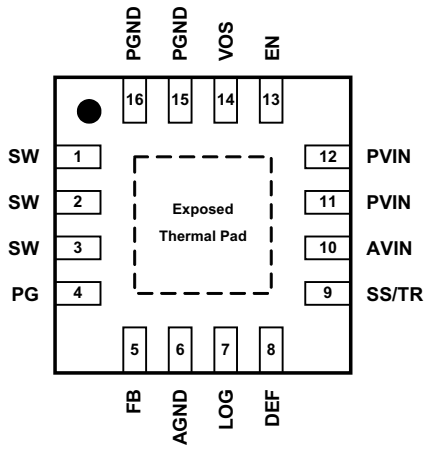
DATE	REVISION	NOTES
May 2014	*	Initial release.

6 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	T_J	PACKAGE MARKING
TPS62130A-Q1	adjustable	–40°C to 125°C	PA6IQ
TPS62133A-Q1	5V	–40°C to 125°C	PA6JQ

7 Pin Configuration and Functions

VQFN Package
16-Pin
Top View



Pin Functions

PIN[1]		I/O	DESCRIPTION
NAME	NO.		
SW	1,2,3	O	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
PG	4	O	Output power good (High = VOUT ready, Low = VOUT below nominal regulation) ; open drain (requires pull-up resistor)
FB	5	I	Voltage feedback pin. Connect resistive voltage divider to this pin.
AGND	6		Analog Ground. Must be connected directly to the Exposed Thermal Pad and common ground plane.
LOG	7	I	This pin is used for internal logic and must be connected to GND.
DEF	8	I	Output Voltage Scaling (Low = nominal, High = nominal + 5%)[2]
SS/TR	9	I	Soft-Start / Tracking Pin. An external capacitor connected to this pin sets the internal voltage reference rise time. It can be used for tracking and sequencing.
AVIN	10	I	Supply voltage for control circuitry. Connect to same source as PVIN.
PVIN	11,12	I	Supply voltage for power stage. Connect to same source as AVIN.
EN	13	I	Enable input (High = enabled, Low = disabled)[2]
VOS	14	I	Output voltage sense pin and connection for the control loop circuitry.
PGND	15,16		Power Ground. Must be connected directly to the Exposed Thermal Pad and common ground plane.
Exposed Thermal Pad			Must be connected to AGND (pin 6), PGND (pin 15,16) and common ground plane[3]. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see *Detailed Description* and *Application and Implementation* sections.
(2) An internal pull-down resistor keeps logic level low, if pin is floating.
(3) See Figure 39.

8 Specifications

8.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Pin voltage (2)	AVIN, PVIN	–0.3	20	V
	EN, SS/TR, SW	–0.3	V_{IN}+0.3	
	DEF, LOG, FB, PG, VOS	–0.3	7	V
Power Good sink current	PG		10	mA
Temperature	Operating junction temperature, T_J	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (2)	–2000	2000	V
		Charged device model (CDM), per AEC Q100-011	–500	500	

(1) Electrostatic discharge (ESD) measures device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{IN}	Supply Voltage	at AVIN and PVIN	3		17	V
V_{OUT}	Output Voltage Range	TPS62130A-Q1	0.9		6	V
T_J	Operating junction temperature		–40		125	°C

8.4 Thermal Information

THERMAL METRIC(1)		TPS6213xA-Q1 RGT 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15	
$R_{\theta JB}$	Junction-to-board thermal resistance	11	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	10	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

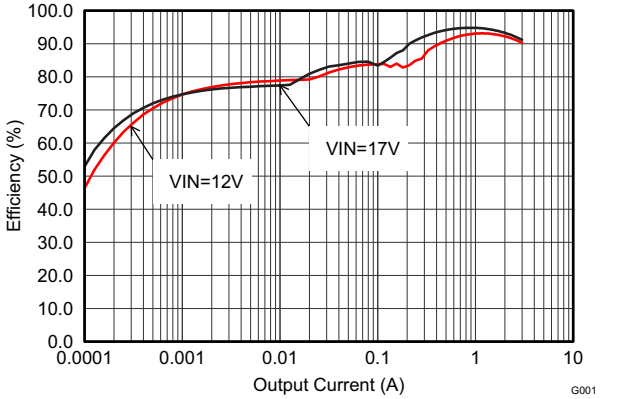
over junction temperature range (T_J = –40°C to +125°C), typical values at V_{IN} = 12V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		3		17	V
I_Q	Operating quiescent current	EN=High, I_{OUT}=0mA, device not switching		17	30	µA
I_{SD}	Shutdown current(1)	EN=Low		1.5	25	µA
V_{UVLO}	Undervoltage lockout threshold	Falling Input Voltage (PWM mode operation)	2.6	2.7	2.8	V
		Hysteresis		200		mV
T_{SD}	Thermal shutdown temperature			160		°C
	Thermal shutdown hysteresis			20		
CONTROL (EN, DEF, LOG, SS/TR, PG)						
V_H	High level input threshold voltage (EN, DEF)		0.9			V
V_L	Low level input threshold voltage (EN, DEF)				0.3	V
I_{LKG}	Input leakage current (EN, DEF, LOG)	EN=V_{IN} or GND; DEF=V_{OUT} or GND; LOG=GND		0.01	1	µA
V_{TH_PG}	Power good threshold voltage	Rising (%V_{OUT})	92%	95%	98%	
		Falling (%V_{OUT})	87%	90%	94%	
V_{OL_PG}	Power good output low	I_{PG}=–2mA		0.07	0.3	V
I_{LKG_PG}	Input leakage current (PG)	V_{PG}=1.8V		1	400	nA
$I_{SS/TR}$	SS/TR pin source current		2.3	2.5	2.7	µA
POWER SWITCH						
$R_{DS(ON)}$	High-side MOSFET ON-resistance	V_{IN}≥6V		90	170	mΩ
		V_{IN}=3V		120		
	Low-side MOSFET ON-resistance	V_{IN}≥6V		40	70	mΩ
		V_{IN}=3V		50		
I_{LIMF}	High-side MOSFET forward current limit	V_{IN} =12V, T_A= 25°C	3.6	4.2	4.9	A
OUTPUT						
VREF	Internal reference voltage			0.8		V
I_{LKG_FB}	Input leakage current (FB)	V_{FB}=0.8V		1	100	nA
V_{OUT}	Output voltage range (TPS62130A-Q1)	V_{IN} ≥ V_{OUT}	0.9		6.0	V
	DEF (Output voltage programming)	DEF=0 (GND)		VOUT		
		DEF=1 (V_{OUT})		VOUT+5%		
	Output voltage accuracy(2)	PWM mode operation, V_{IN} ≥ V_{OUT} +1V	–1.8 %		1.8%	
		Power Save Mode operation, C_{OUT}=22µF	–2.3 %		2.8%	
	Load regulation	V_{IN}=12V, V_{OUT}=3.3V, PWM mode operation		0.05		%/A
	Line regulation	3V ≤ V_{IN} ≤ 17V, V_{OUT}=3.3V, I_{OUT}= 1A, PWM mode operation		0.02		%/V

(1) Current into AVIN+PVIN pin.
(2) This is the regulation accuracy of the voltage at the FB pin (adjustable version).

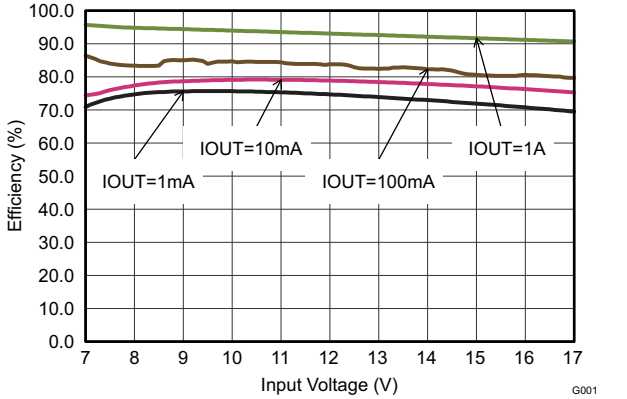
8.6 Typical Characteristics

At V_{IN}=12V, V_{OUT}=3.3V and T_A=25°C, (unless otherwise noted)



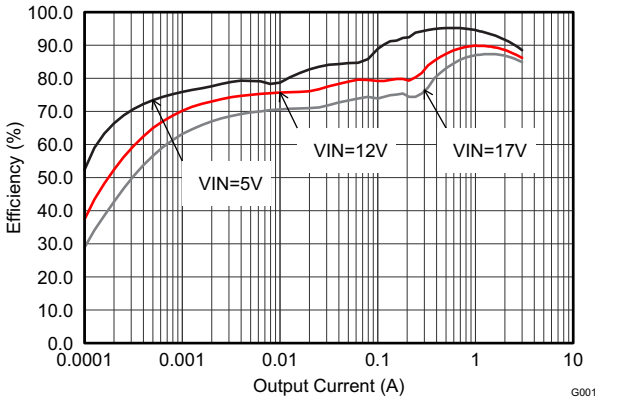
V_{OUT} = 5.0 V L = 2.2 µH (XFL4020) C_{OUT} = 22 µH

Figure 1. Efficiency vs. Output Current



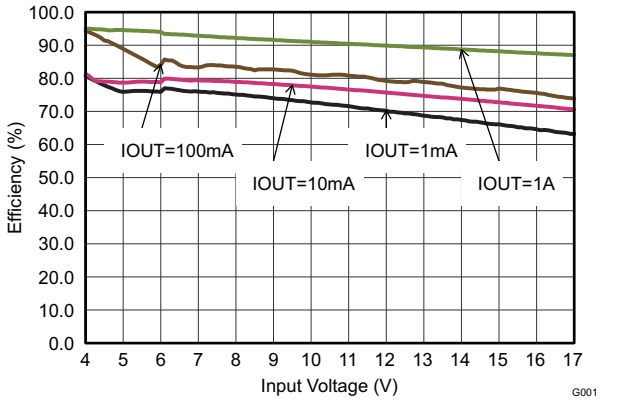
V_{OUT} = 5.0 V L = 2.2 µH (XFL4020) C_{OUT} = 22 µH

Figure 2. Efficiency vs. Input Voltage



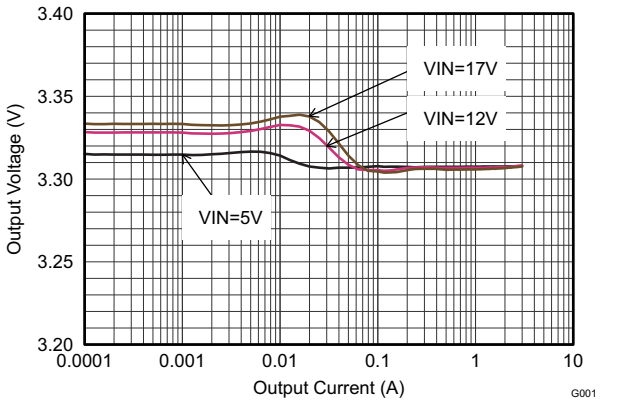
V_{OUT} = 3.3 V L = 2.2 µH (XFL4020) C_{OUT} = 22 µH

Figure 3. Efficiency vs. Output Current



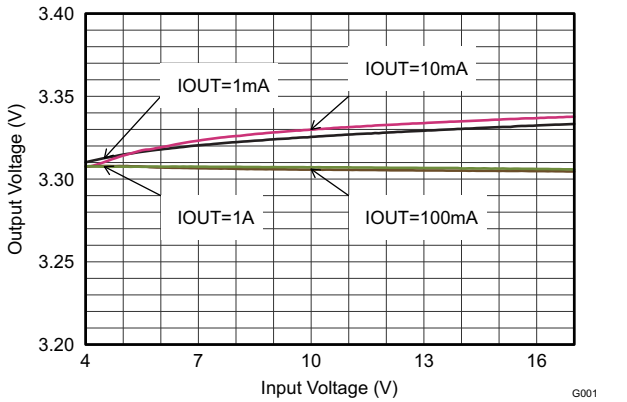
V_{OUT} = 3.3 V L = 2.2 µH (XFL4020) C_{OUT} = 22 µH

Figure 4. Efficiency vs. Input Voltage



V_{OUT} = 3.3 V L = 2.2 µH (XFL4020) C_{OUT} = 22 µH

Figure 5. Output Voltage Accuracy (Load Regulation)



V_{OUT} = 3.3 V L = 2.2 µH (XFL4020) C_{OUT} = 22 µH

Figure 6. Output Voltage Accuracy (Line Regulation)

Typical Characteristics (continued)

At V_{IN}=12V, V_{OUT}=3.3V and T_A=25°C, (unless otherwise noted)

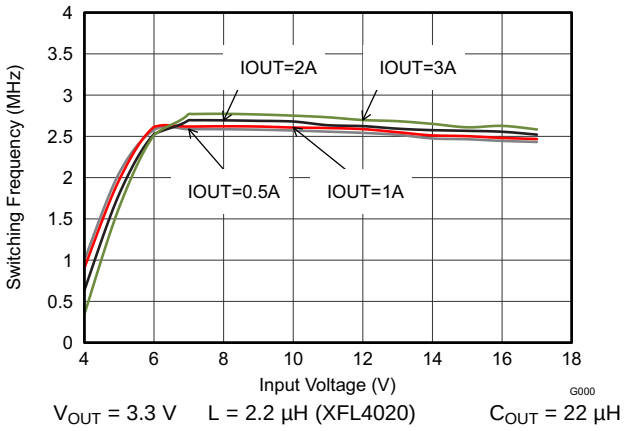


Figure 7. Switching Frequency vs. Input Voltage

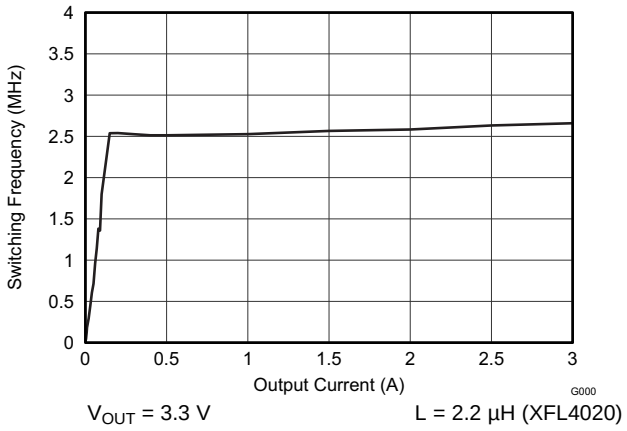


Figure 8. Switching Frequency vs. Output Current

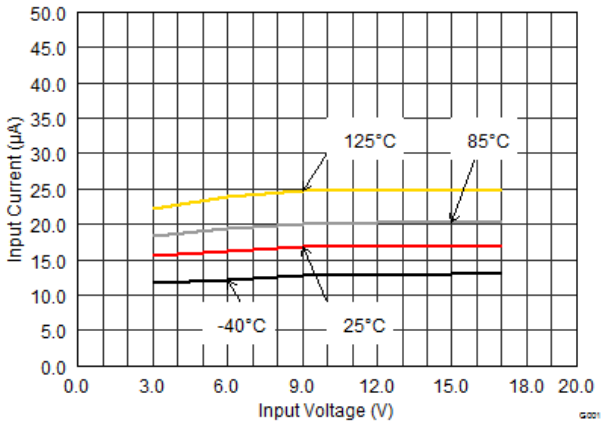


Figure 9. Quiescent Current

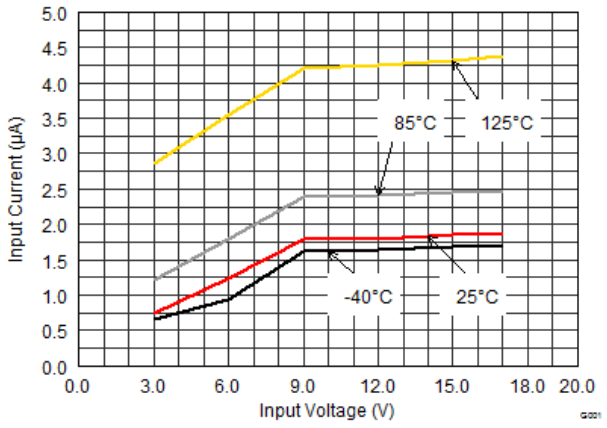


Figure 10. Shutdown Current

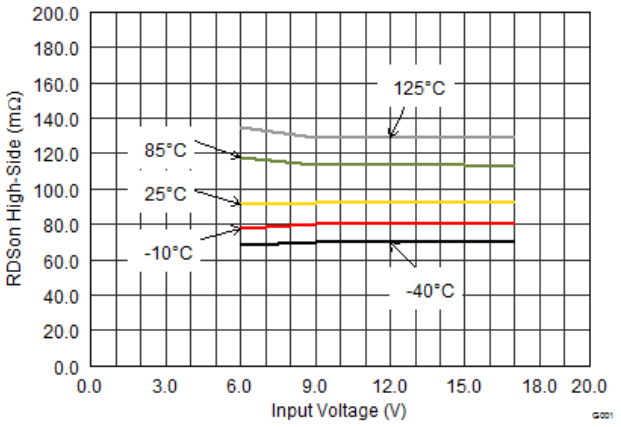


Figure 11. High-side Switch Resistance

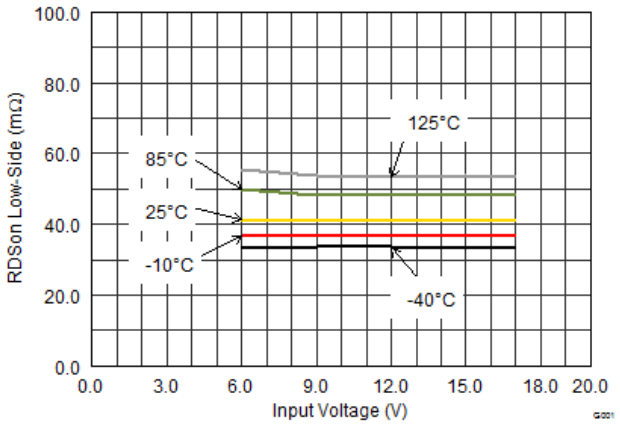


Figure 12. Low-Side Switch Resistance

Typical Characteristics (continued)

At V_{IN}=12V, V_{OUT}=3.3V and T_A=25°C, (unless otherwise noted)

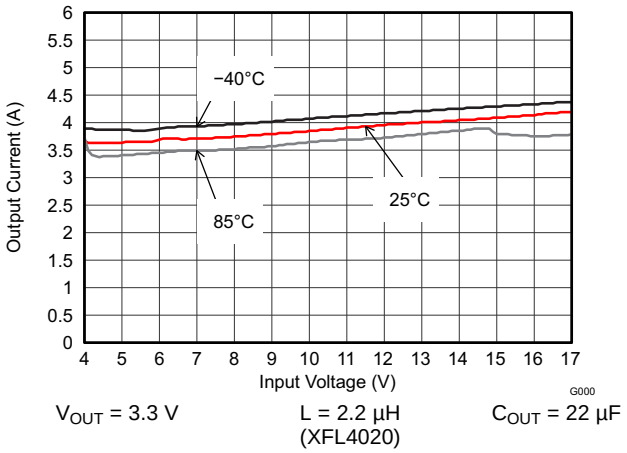


Figure 13. Maximum Output Current

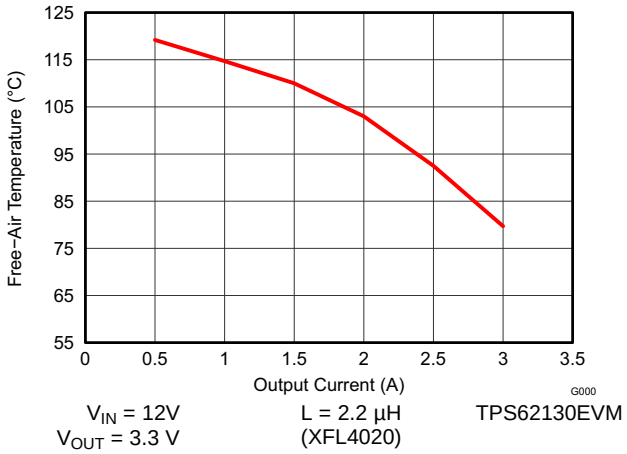


Figure 14. Maximum Ambient Temperature

9 Parameter Measurement Information

Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
IC	17V, 3A Step-Down Converter, QFN	TPS62130A-QRGT, Texas Instruments
L1	2.2µH, 0.165 x 0.165 in	XFL4020-222MEB, Coilcraft
Cin	10µF, 25V, Ceramic	Standard
Cout	22µF, 6.3V, Ceramic	Standard
Css	3300pF, 25V, Ceramic	
R1	depending on Vout	
R2	depending on Vout	
R3	100kΩ, Chip, 0603, 1/16W, 1%	Standard

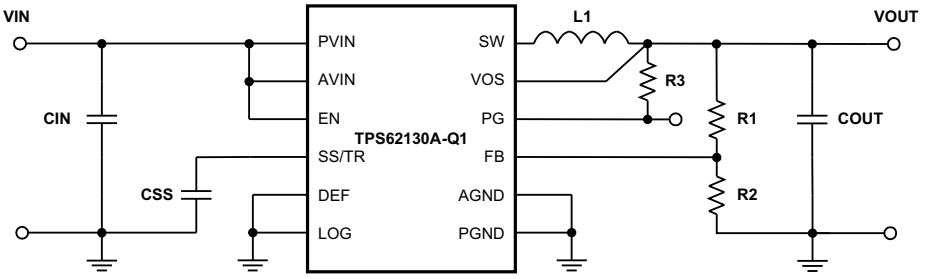


Figure 15. Measurement Setup

10 Detailed Description

10.1 Overview

The TPS6213xA-Q1 synchronous switched mode power converter is based on DCS-Control™ (**D**irect **C**ontrol with **S**eamless Transition into Power Save Mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-ControlTM topology supports PWM (Pulse Width Modulation) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.5MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Mode the switching frequency decreases linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage.

10.2 Functional Block Diagram

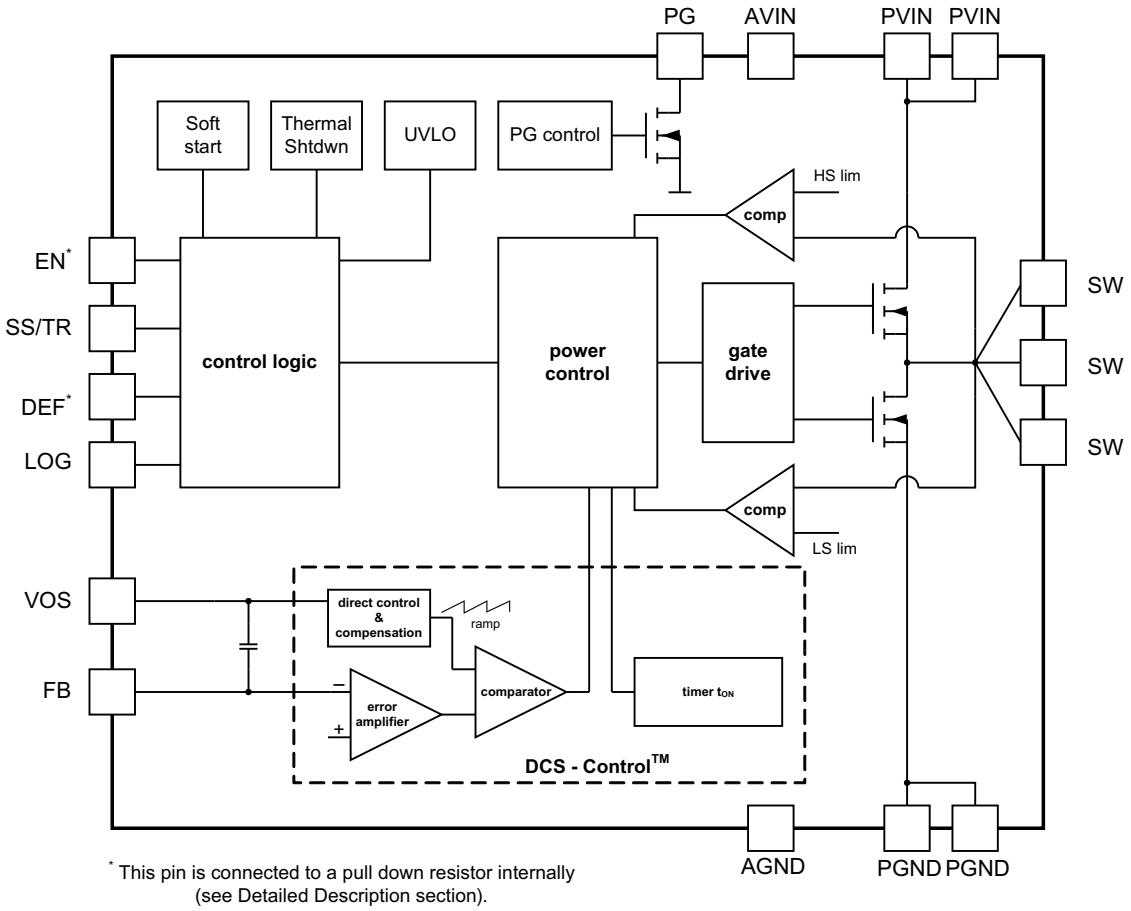


Figure 16. TPS62130A-Q1 (Adjustable Output Voltage)

Functional Block Diagram (continued)

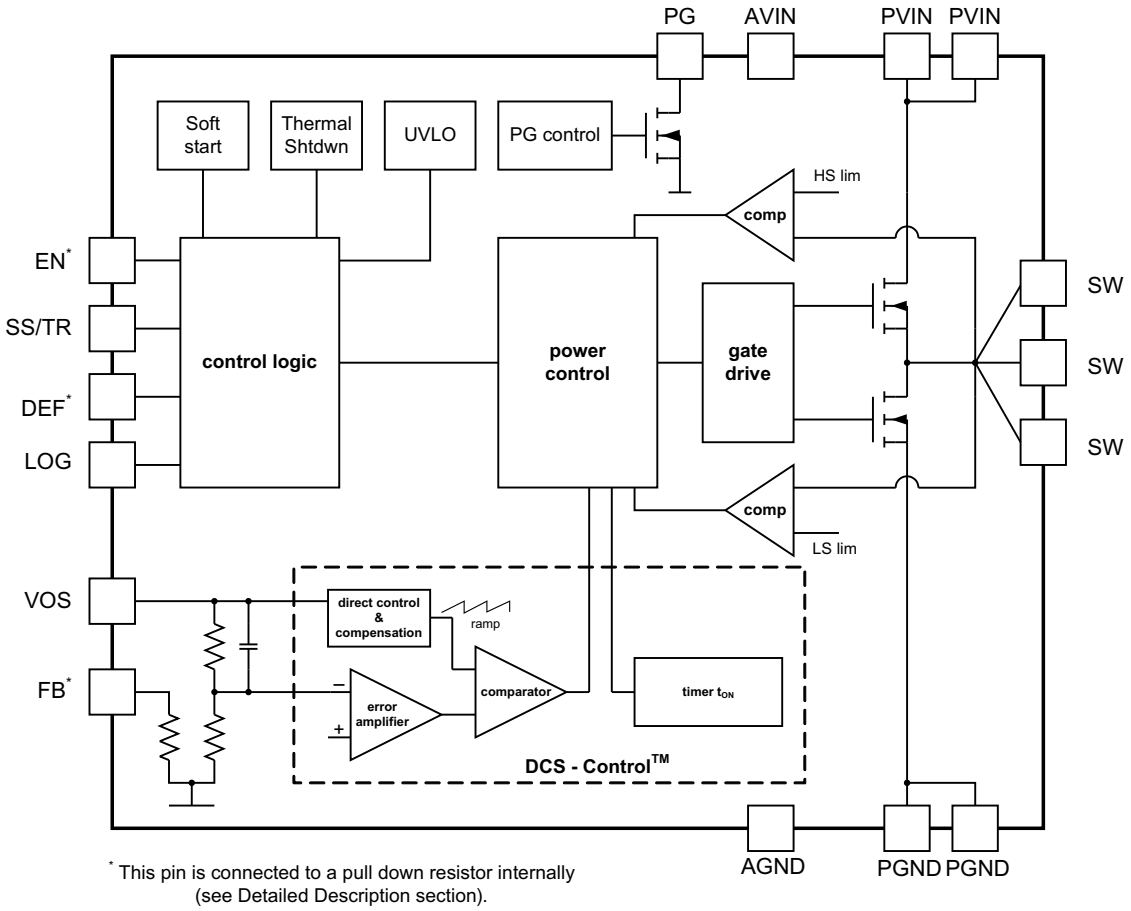


Figure 17. TPS62133A-Q1 (5V Fixed Output Voltage)

10.3 Feature Description

10.3.1 Pulse Width Modulation (PWM) Operation

The TPS6213xA-Q1 operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of 2.5 MHz. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT} and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM). PSM operation occurs if the output current becomes smaller than half the inductor's ripple current.

10.3.2 Power Save Mode Operation

The built in Power Save Mode of the TPS6213xA-Q1 is entered seamlessly, if the load current decreases. This secures a high efficiency in light load operation. The device remains in Power Save Mode as long as the inductor current is discontinuous.

In Power Save Mode, the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

TPS6213xA-Q1 includes a fixed on-time circuitry. This on-time, in steady-state operation, can be estimated as:

Feature Description (continued)

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 400ns \quad (1)$$

For very small output voltages, an absolute minimum on-time of about 80ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, keeping efficiency high. Using t_{ON}, the typical peak inductor current in Power Save Mode can be approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{ON} \quad (2)$$

When V_{IN} decreases to typically 15% above VOUT, the TPS6213xA-Q1 does not enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

10.3.3 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by D=Vout/Vin and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences, e.g. for longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left(R_{DS(on)} + R_L\right) \quad (3)$$

where

I_{OUT} is the output current,
$R_{DS(on)}$ is the $R_{DS(on)}$ of the high-side FET and
R_L is the DC resistance of the inductor used.

10.3.4 Enable / Shutdown (EN)

When Enable (EN) is set High, the device starts operation. Shutdown is forced if EN is pulled Low with a shutdown current of typically 1.5µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. The EN signal must be set externally to High or Low. An internal pull-down resistor of about 400kΩ is connected and keeps EN logic low, if Low is set initially and then the pin gets floating. It is disconnected if the pin is set High.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

10.3.5 Soft Start / Tracking (SS/TR)

The internal soft start circuitry controls the output voltage slope during startup, avoiding excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50µs and VOUT rises with a slope controlled by an external capacitor connected to the SS/TR pin. See Figure 27 and Figure 28 for typical startup operation.

Using very small capacitor (or leaving SS/TR pin un-connected) provides fastest startup behavior. The TPS6213xA-Q1 can start into a pre-biased output. During monotonic pre-biased startup, both of the power MOSFETs are not allowed to turn on until the device's internal ramp sets an output voltage above the pre-bias voltage. As long as the output is below about 0.5V, a reduced current limit of typically 1.6A is set internally. If the device is set to shutdown (EN=GND), undervoltage lockout or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those states causes a new startup sequence as set by the SS/TR connection.

Feature Description (continued)

A voltage supplied to SS/TR can be used for tracking a master voltage. The output voltage will follow this voltage in both directions up and down (see *Application and Implementation*).

10.3.6 Current Limit And Short Circuit Protection

The TPS6213xA-Q1 is protected against heavy load and short circuit events. If a short circuit is detected (VOUT drops below 0.5V), the current limit is reduced to 1.6A typically. If the output voltage rises above 0.5V, the device runs in normal operation again. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET turns off. Avoiding shoot through current, the low-side FET will be switched on to sink the inductor current. The high-side FET will turn on again, only if the current in the low-side FET has decreased below the low side current limit threshold.

The output current of the device is limited by the current limit (see *Electrical Characteristics*). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD} \quad (4)$$

where

I_{LIMF} is the static current limit, specified in the *Electrical Characteristics*,
L is the inductor value,
V_L is the voltage across the inductor (V_{IN} - V_{OUT}) and
t_{PD} is the internal propagation delay.

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{(V_{IN} - V_{OUT})}{L} \cdot 30ns \quad (5)$$

10.3.7 Power Good (PG)

The TPS6213xA-Q1 has a built in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor (to any voltage below 7V). It can sink 2mA of current and maintain its specified logic low level. TPS6213xA-Q1 features PG=Low when the device is turned off due to EN, UVLO or thermal shutdown and can be used to actively discharge Vout (see Figure 31). VIN must remain present for the PG pin to stay Low.

10.3.8 Pin-Selectable Output Voltage (DEF)

The output voltage of the TPS6213xA-Q1 can be increased by 5% above the nominal voltage by setting the DEF pin to High (1). When DEF is Low, the device regulates to the nominal output voltage. Increasing the nominal voltage allows adapting the power supply voltage to the variations of the application hardware. More detailed information on voltage margining using TPS6213xA-Q1 can be found in SLVA489. A pull down resistor of about 400kOhm is internally connected to the pin, to ensure a proper logic level if the pin is high impedance or floating after initially set to Low. The resistor is disconnected if the pin is set High.

10.3.9 Under Voltage Lockout (UVLO)

If the input voltage drops, the under voltage lockout prevents misoperation of the device by switching off both the power FETs. The under voltage lockout threshold is set typically to 2.7V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 200mV.

(1) Maximum allowed voltage is 7V. Therefore it's recommended to connect it to VOUT, not VIN.

Feature Description (continued)

10.3.10 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 160°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes Low. When T_J decreases below the hysteresis amount, the converter resumes normal operation, beginning with Soft Start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shutdown temperature.

10.4 Device Functional Modes

10.4.1 Operation Above T_J=125°C

The operating junction temperature of the device is specified up to 125°C. In power supplying circuits, the self heating effect causes, that the junction temperature, T_J, is even higher than the ambient temperature T_A (see Figure 14). Depending on T_A and the load current, the maximum operating T_J can be exceeded. However, the electrical characteristics are specified up to a T_J of 125°C only. The device operates as long as thermal shutdown threshold is not triggered.

10.4.2 Operation with V_{IN} < 3V

The device is functional for supply voltages below 3V and above the UVLO threshold. Parameters may differ from specified values. The minimum V_{IN} value of 3V is not violated by UVLO threshold and hysteresis variations.

10.4.3 Operation with Separate EN Control

The EN pin can be connected to V_{IN} or be controlled separately. While the EN control voltage level can be lower than the actual V_{IN} value, it must not exceed V_{IN} to avoid damage of the device. This might happen at low V_{IN}, during startup or power sequencing.

11 Application and Implementation

11.1 Application Information

TPS62130xA-Q1 are synchronous switch mode step-down converters, able to convert a 3V to 17V input voltage into a lower, 0.9V to 6V, output voltage, providing up to 3A load current. The following section gives guidance on choosing external components to complete the power supply design. *Application Curves* are included for the typical application shown here.

11.2 Typical Application

11.2.1 TPS62130A-Q1 Point-Of-Load Step Down Converter

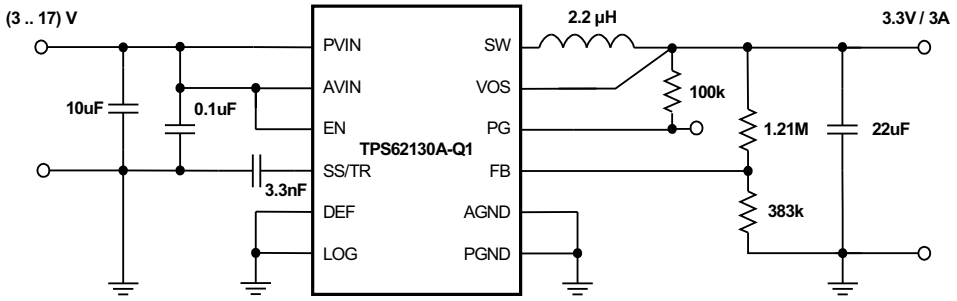


Figure 18. Typical Schematic for 3.3V Step-Down Converter

11.2.1.1 Design Requirements

The step-down converter design can be adapted to different output voltage and load current needs by choosing external components appropriate. The following design procedure is adequate for whole VIN, VOUT and load current range of TPS62130A-Q1. Using Table 2, the design procedure needs minimum effort.

11.2.1.2 Detailed Design Procedure

11.2.1.2.1 Programming The Output Voltage

The TPS6213xA-Q1 can be programmed for output voltages from 0.9V to 6V by using a resistive divider from VOUT to AGND. The voltage at the FB pin is regulated to 800mV. The value of the output voltage is set by the selection of the resistive divider from Equation 6 (see Figure 15). It is recommended to choose resistor values which allow a current of at least 2uA, meaning the value of R2 shouldn't exceed 400kΩ. Lower resistor values are recommended for highest accuracy and most robust design. For applications requiring lowest current consumption, the use of fixed output voltage versions is recommended.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (6)$$

In case the FB pin gets opened, the device clamps the output voltage at the VOS pin internally to about 7.4V.

11.2.1.2.2 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the device's control loop. The TPS6213xA-Q1 is optimized to work within a range of external components. The LC output filter's inductance and capacitance must be considered together, creating a double pole, responsible for the corner frequency of the converter (see *Output Filter And Loop Stability*). Table 2 can be used to simplify the output filter component selection.

Typical Application (continued)

Table 2. Recommended LC Output Filter Combinations(1)

	4.7µF	10µF	22µF	47µF	100µF	200µF	400µF
0.47µH							
1µH			√	√	√	√	
2.2µH		√	√(2)	√	√	√	
3.3µH		√	√	√	√		
4.7µH							

(1) The values in the table are nominal values.
(2) This LC combination is the standard value and recommended for most applications.

More detailed information on further LC combinations can be found in SLVA463.

11.2.1.2.3 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \tag{7}$$

$$\Delta I_{L(\max)} = V_{OUT} \cdot \left(\frac{1 - \frac{V_{OUT}}{V_{IN(\max)}}}{L_{(\min)} \cdot f_{SW}} \right) \tag{8}$$

where

I_L(max) is the maximum inductor current,
ΔI_L is the Peak to Peak Inductor Ripple Current,
L(min) is the minimum effective inductor value and
f_{SW} is the actual PWM Switching Frequency.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and solution size as well. The following inductors have been used with the TPS6213xA-Q1 and are recommended for use:

Table 3. List of Inductors(1)

Type	Inductance [µH]	Current [A](2)	Dimensions [LxBxH] mm	MANUFACTURER
XFL4020-102ME_	1.0 µH, ±20%	4.7	4 x 4 x 2.1	Coilcraft
XFL4020-152ME_	1.5 µH, ±20%	4.2	4 x 4 x 2.1	Coilcraft
XFL4020-222ME_	2.2 µH, ±20%	3.8	4 x 4 x 2.1	Coilcraft
IHLP1212BZ-11	1.0 µH, ±20%	4.5	3 x 3.6 x 2	Vishay
IHLP1212BZ-11	2.2 µH, ±20%	3.0	3 x 3.6 x 2	Vishay

(1) See *Third-Party Products Disclaimer*
(2) Lower of I_{RMS} at 40°C rise or I_{SAT} at 30% drop.

Table 3. List of Inductors(1) (continued)

Type	Inductance [µH]	Current [A](2)	Dimensions [LxBxH] mm	MANUFACTURER
SRP4020-3R3M	3.3µH, ±20%	3.3	4.8 x 4 x 2	Bourns
VLC5045T-3R3N	3.3µH, ±30%	4.0	5 x 5 x 4.5	TDK

The inductor value also determines the load current at which Power Save Mode is entered:

$$I_{load(PSM)} = \frac{1}{2}\Delta I_L \quad (9)$$

Using Equation 8, this current level can be adjusted by changing the inductor value.

11.2.1.2.4 Output Capacitor

The recommended value for the output capacitor is 22uF. The architecture of the TPS6213xA-Q1 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it's recommended to use an X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in Power Save Mode (see SLVA463).

Note: In power save mode, the output voltage ripple depends on the output capacitance, its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

11.2.1.2.5 Input Capacitor

For most applications, 10µF is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage during transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between PVIN and PGND as close as possible to those pins. Even though AVIN and PVIN must be supplied from the same input source, it's required to place a capacitance of 0.1uF from AVIN to AGND, to avoid potential noise coupling. An RC, low-pass filter from PVIN to AVIN may be used but is not required.

11.2.1.2.6 Soft Start Capacitor

A capacitance connected between SS/TR pin and AGND allows a user programmable start-up slope of the output voltage. A constant current source supports 2.5µA to charge the external capacitance. The capacitor required for a given soft-start ramp time for the output voltage is given by:

$$C_{SS} = t_{SS} \cdot \frac{2.5\mu A}{1.25V} \quad [F] \quad (10)$$

where

C_{SS} is the capacitance (F) required at the SS/TR pin and
t_{SS} is the desired soft-start ramp time (s).

NOTE

DC Bias effect: High capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

11.2.1.2.7 Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage. If the tracking voltage is between 50mV and 1.2V, the FB pin tracks the SS/TR pin voltage as described in Equation 11 and shown in Figure 19.

$$V_{FB} \approx 0.64 \cdot V_{SS/TR} \tag{11}$$

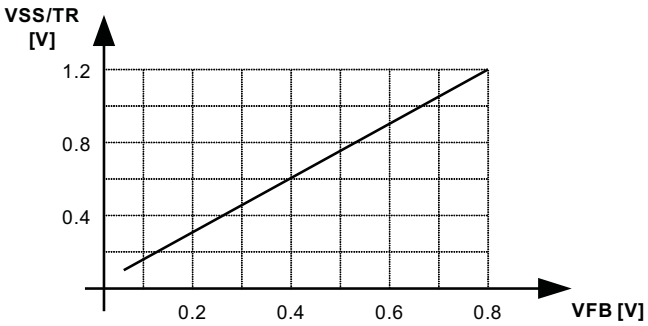


Figure 19. Voltage Tracking Relationship

Once the SS/TR pin voltage reaches about 1.2V, the internal voltage is clamped to the internal feedback voltage and device goes to normal regulation. This works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. For decreasing SS/TR pin voltage, the device doesn't sink current from the output. So, the resulting decrease of the output voltage may be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is V_{IN}+0.3V.

If the input voltage drops into undervoltage lockout or even down to zero, the output voltage will go to zero, independent of the tracking voltage. Figure 20 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function.

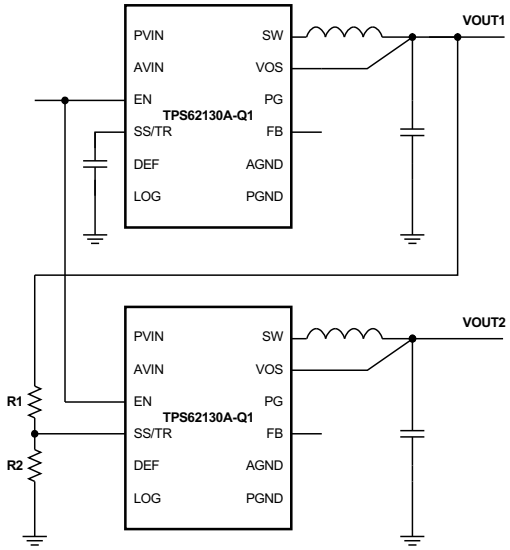


Figure 20. Sequence for Ratiometric and Simultaneous Startup

The resistive divider of R1 and R2 can be used to change the ramp rate of VOUT2 faster, slower or the same as VOUT1.

A sequential startup is achieved by connecting the PG pin of VOUT1 to the EN pin of VOUT2. Ratiometric start up sequence happens if both supplies are sharing the same soft start capacitor. Equation 10 calculates the soft start time, though the SS/TR current has to be doubled. Details about these and other tracking and sequencing circuits are found in SLVA470.

Note: If the voltage at the FB pin is below its typical value of 0.8V, the output voltage accuracy may have a wider tolerance than specified.

11.2.1.2.8 Output Filter And Loop Stability

The devices of the TPS6213xA-Q1 family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with Equation 12:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \tag{12}$$

Proven nominal values for inductance and ceramic capacitance are given in Table 2 and are recommended for use. Different values may work, but care has to be taken on the loop stability which is affected. More information including a detailed LC stability matrix can be found in SLVA463.

The TPS6213xA-Q1 includes an internal 25pF feedforward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per equation Equation 13 and Equation 14:

$$f_{zero} = \frac{1}{2\pi \cdot R_1 \cdot 25pF} \tag{13}$$

$$f_{pole} = \frac{1}{2\pi \cdot 25pF} \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \tag{14}$$

Though the TPS6213xA-Q1 is stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in Power Save mode and/or improved transient response. An external feedforward capacitor can also be added. A more detailed discussion on the optimization for stability vs. transient response can be found in SLVA289 and SLVA466.

11.2.1.3 Application Curves

At V_{IN}=12V, V_{OUT}=3.3V and T_A=25°C, (unless otherwise noted)

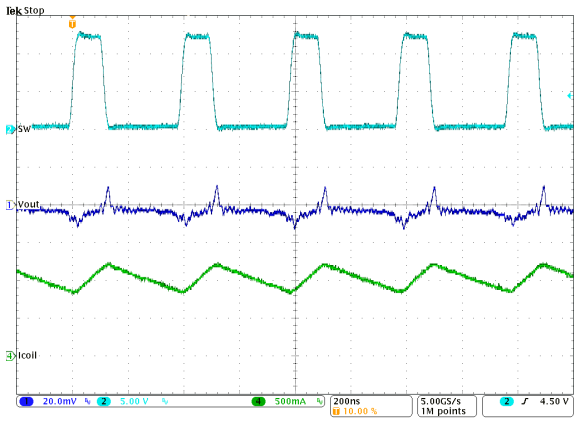


Figure 21. Typical Operation in PWM Mode (I_{OUT}=1A)

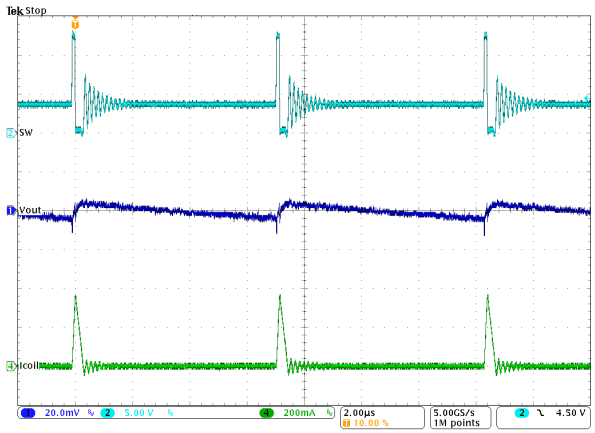


Figure 22. Typical Operation in Power Save Mode (I_{OUT}=10mA)

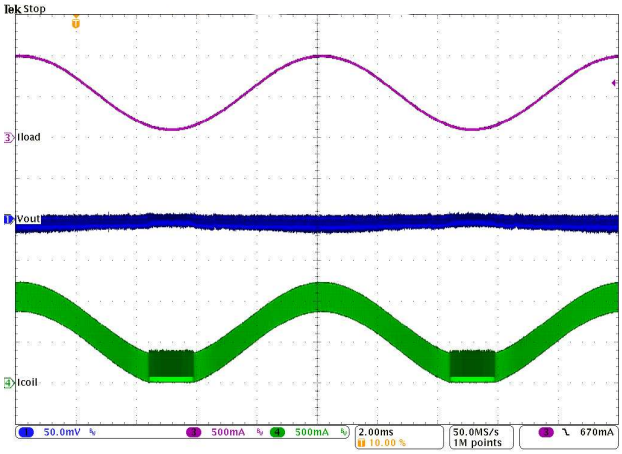


Figure 23. PWM-PSM-Transition

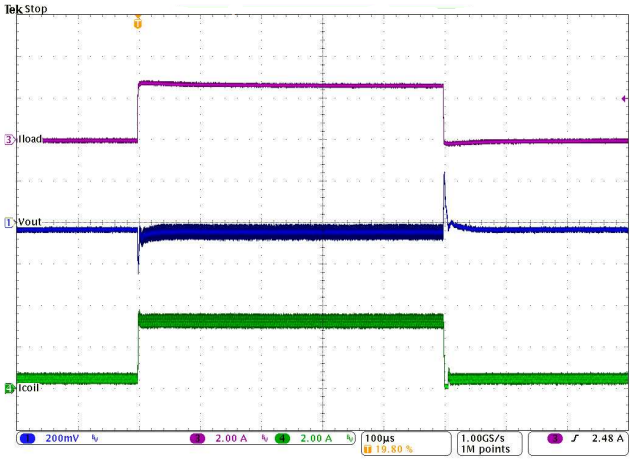


Figure 24. Load Transient Response (0.5 to 3 to 0.5 A)

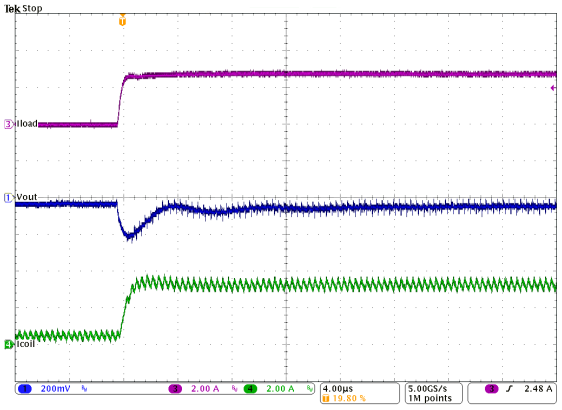


Figure 25. Load Transient Response of Figure 24, Rising Edge

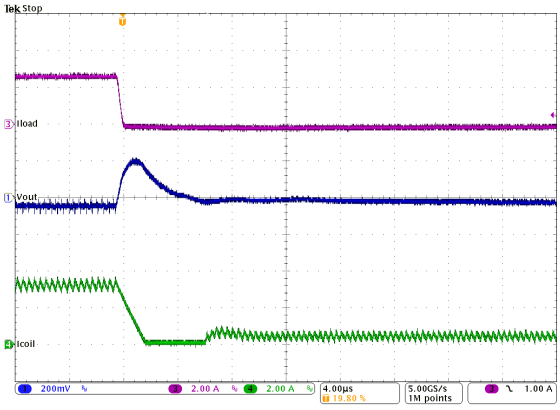


Figure 26. Load Transient Response of Figure 24, Falling Edge

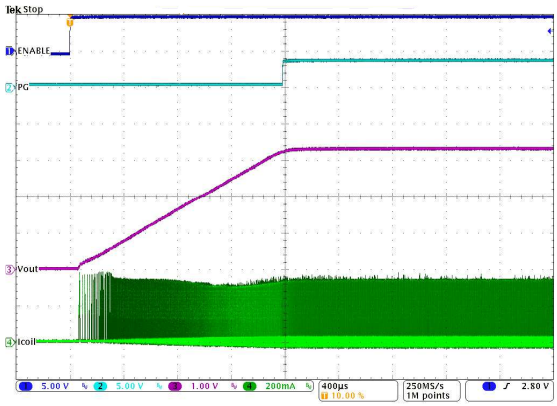


Figure 27. Start Up into 100mA

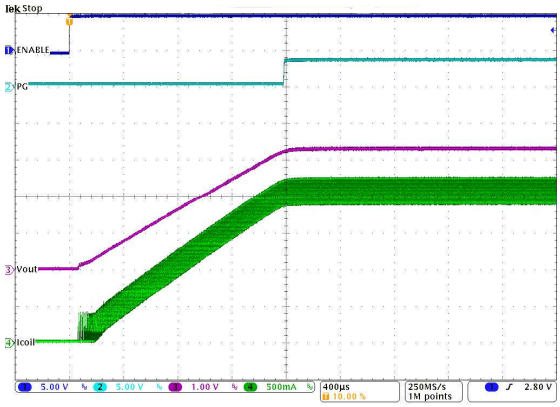


Figure 28. Start Up into 3A

11.2.2 Regulated Power LED Supply

The TPS62130A-Q1 can be used as a power supply for power LEDs. The FB pin can be easily set down to lower values than nominal by using the SS/TR pin. With that, the voltage drop on the sense resistor is low, avoiding excessive power loss. Since this pin provides 2.5µA, the feedback pin voltage can be adjusted by an external resistor per Equation 15. This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TPS62130A-Q1. Figure 29 shows an application circuit, tested with analog dimming:

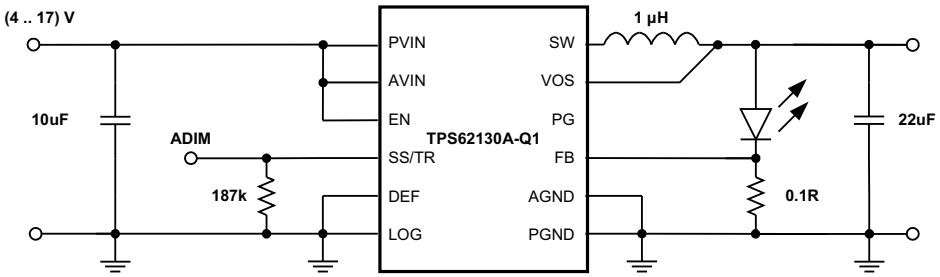


Figure 29. Single Power LED Supply

11.2.2.1 Design Requirements

The TPS62130A-Q1 is connected to drive a power LED. The power losses of current detection have to be small and analog dimming is required.

11.2.2.2 Detailed Design Procedure

The resistor at SS/TR sets the FB voltage to a level of about 300mV and is calculated from Equation 15.

$$V_{FB} = 0.64 \cdot 2.5\mu A \cdot R_{SS/TR} \quad (15)$$

The device now supplies a constant current, set by the resistor at the FB pin, by regulating the output voltage accordingly. The minimum input voltage has to be rated according the forward voltage needed by the LED used. More information is available in the Application Note SLVA451.

11.2.3 Inverting Power Supply

The TPS62130A-Q1 can be used as inverting power supply by rearranging external circuitry as shown in Figure 30.

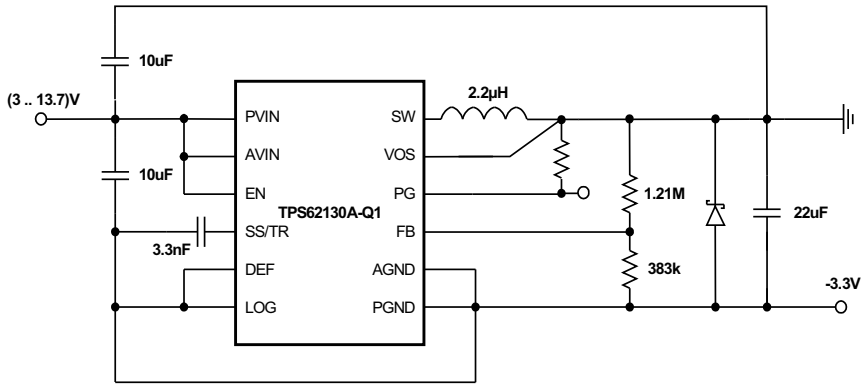


Figure 30. -3.3V Inverting Power Supply

11.2.3.1 Design Requirements

The TPS62130A-Q1 is connected to build an inverting power supply, providing a negative output voltage.

11.2.3.2 Detailed Design Procedure

As the former GND node now represents a voltage level below system ground, the voltage difference between V_{IN} and V_{OUT} has to be limited for operation to the maximum supply voltage of 17V (see Equation 16).

$$V_{IN} + V_{OUT} \leq V_{IN\,max} \tag{16}$$

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a Right Half Plane Zero additionally. The loop stability has to be adapted and an output capacitance of at least 22µF is recommended. A detailed design example is given in SLVA469.

11.2.4 Active Output Discharge

The TPS6213xA-Q1 pulls the PG pin Low, when the device is shut down by EN, UVLO or thermal shutdown. Connecting PG to Vout through a resistor can be used to discharge Vout in those cases (see Figure 31). The discharge rate can be adjusted by R3, which is also used to pull up the PG pin in normal operation. For reliability, keep the maximum current into the PG pin less than 10mA.

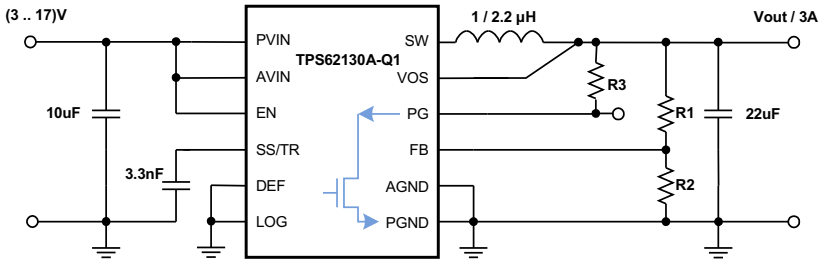


Figure 31. Output Discharge using PG Pin

11.2.4.1 Design Requirements

The output of TPS62130A-Q1 power supply needs to be discharged actively, when device is switched off.

11.2.4.2 Detailed Design Procedure

The discharge rate can be adjusted by R3, which is also used to pull up the PG pin in normal operation. For reliability, keep the maximum current into the PG pin less than 10mA.

11.2.5 Various Output Voltages

The TPS62130A-Q1 can be set for different output voltages between 0.9V and 6V. Some examples are shown below.

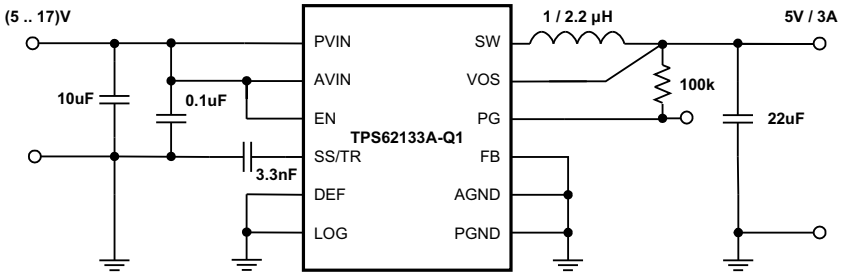


Figure 32. 5V Power Supply using TPS62133A-Q1 fixed V_{OUT} version

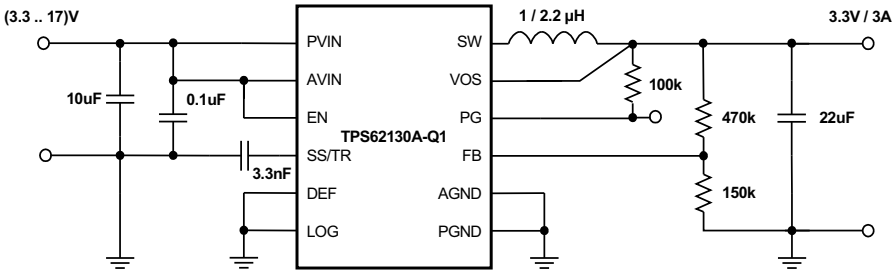


Figure 33. 3.3V/3A Power Supply

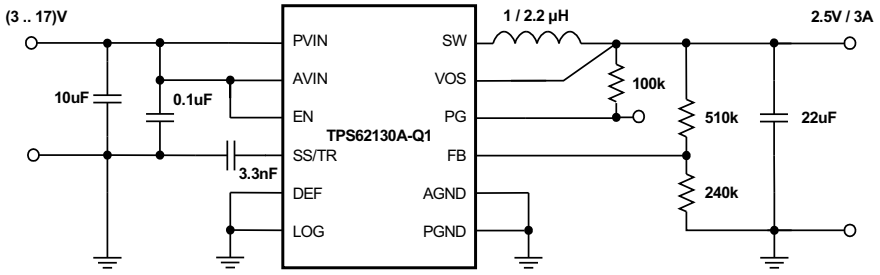


Figure 34. 2.5V/3A Power Supply

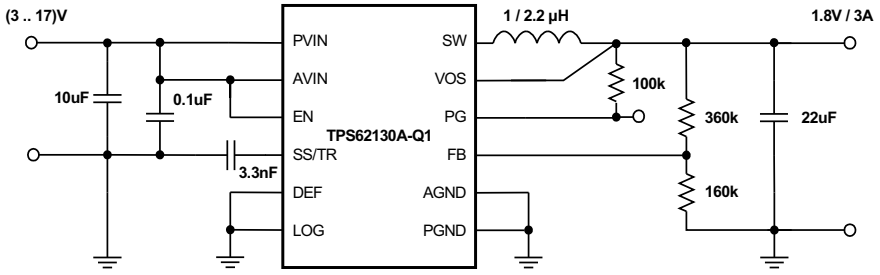


Figure 35. 1.8V/3A Power Supply

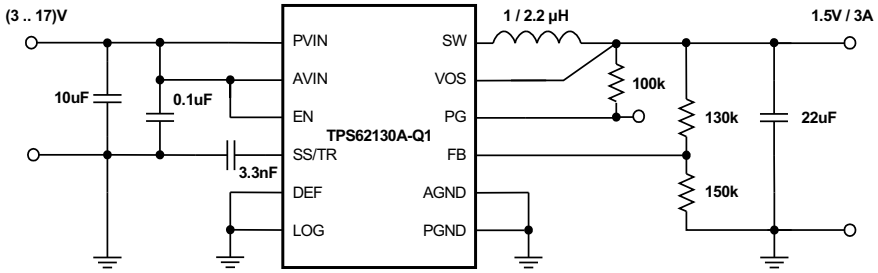


Figure 36. 1.5V/3A Power Supply

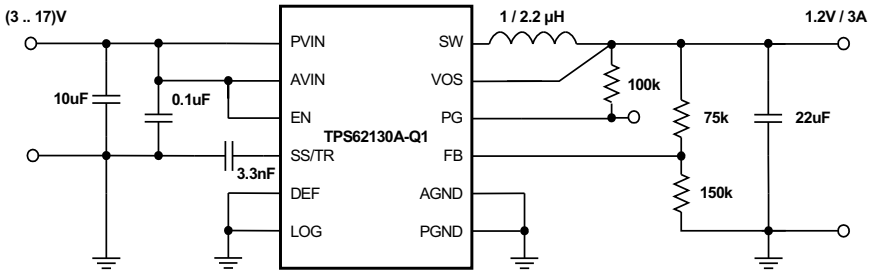


Figure 37. 1.2V/3A Power Supply

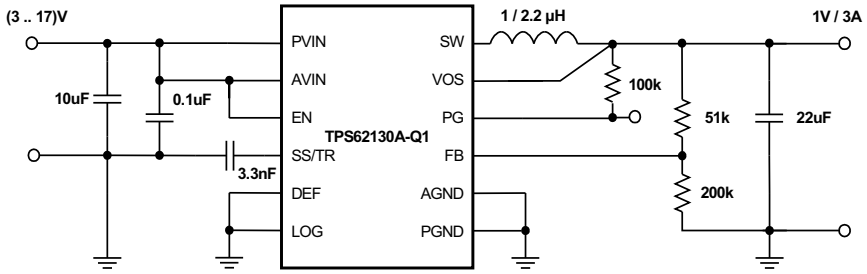


Figure 38. 1V/3A Power Supply

11.2.5.1 Design Requirements

The TPS62150A-Q1 power supply is set to different output voltages.

11.2.5.2 Detailed Design Procedure

See TPS62130A-Q1 Point-Of-Load Step Down Converter. The output voltage is set as described in *Programming The Output Voltage*.

12 Power Supply Recommendations

The TPS6213xA-Q1 devices are designed to operate from a 3 to 17V input voltage supply. To avoid insufficient supply current due to line drop, ringing due to trace inductance at the VIN terminal or supply peak current limitations, additional bulk capacitance may be required. In the case ringing that is caused by the interaction with the ceramic input capacitors, an electrolytic or tantalum type capacitor may be needed for damping.

13 Layout

13.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TPS6213xA-Q1 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation and noise sensitivity. The layout also influences the thermal performance of the solution by its power dissipation capabilities.

See Figure 39 for the recommended layout of the TPS62130A-Q1, which is designed for common external ground connections. Therefore both AGND and PGND pins are directly connected to the Exposed Thermal Pad. On the PCB, the direct common ground connection of AGND and PGND to the Exposed Thermal Pad and the system ground (ground plane) is mandatory. Also connect the VOS pin in the shortest way to the VOUT potential at the output capacitor.

Provide low inductive and resistive paths for loops with high di/dt. Therefore paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and VOS need to be connected with short wires and not nearby high dv/dt signals (e.g. SW). As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin and on AVIN as well as the FB resistors, R1 and R2, should be kept close to the IC and connect directly to those pins and the AGND pin.

The Exposed Thermal Pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.

The recommended layout is implemented on the EVM and shown in its Users Guide, SLVU437. Additionally, the EVM Gerber data are available for download here, SLVC394.

13.2 Layout Example

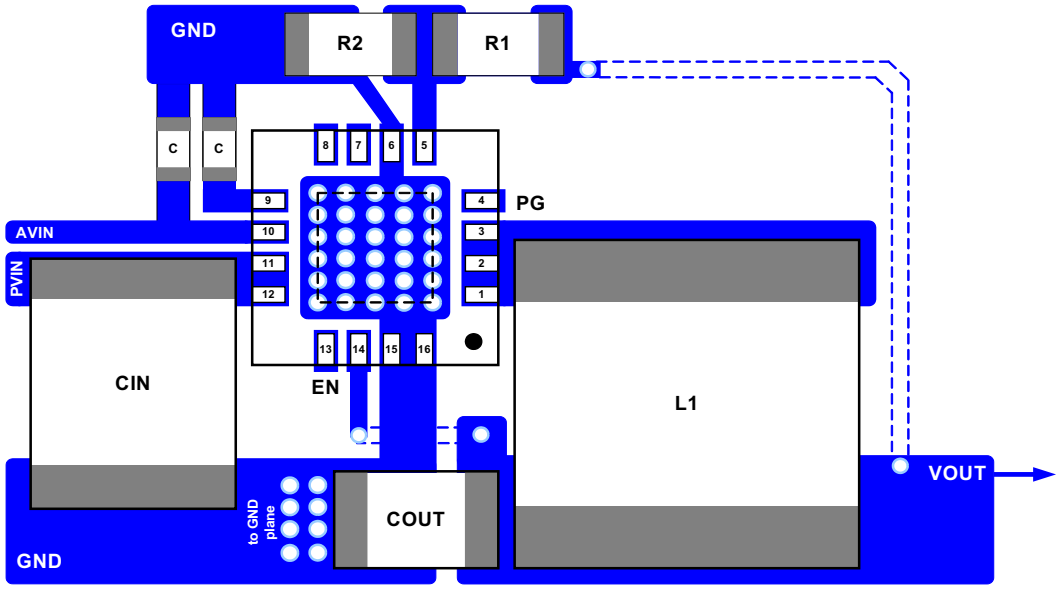


Figure 39. Layout Example with TPS62130A-Q1

14 Device and Documentation Support

14.1 Device Support

14.1.1 Third-Party Products Disclaimer

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14.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62130A-Q1	Click here	Click here	Click here	Click here	Click here
TPS62133A-Q1	Click here	Click here	Click here	Click here	Click here

14.3 Trademarks

DCS-Control is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

14.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62130AQRGTRQ1	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA6IQ	Samples
TPS62130AQRGTTQ1	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA6IQ	Samples
TPS62133AQRGTRQ1	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA6JQ	Samples
TPS62133AQRGTTQ1	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA6JQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS62130A-Q1 :

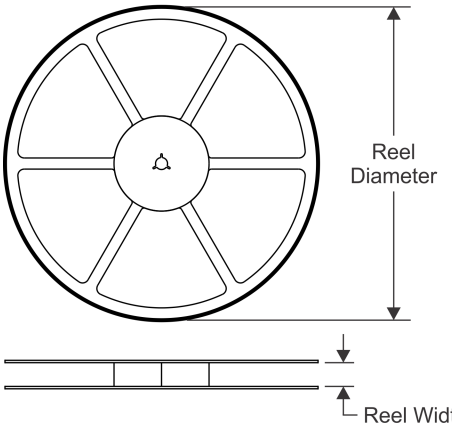
- Catalog: TPS62130A

NOTE: Qualified Version Definitions:

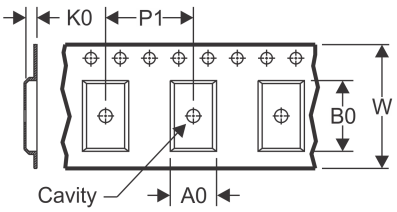
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

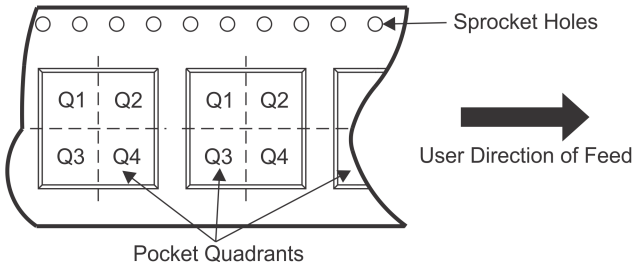


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

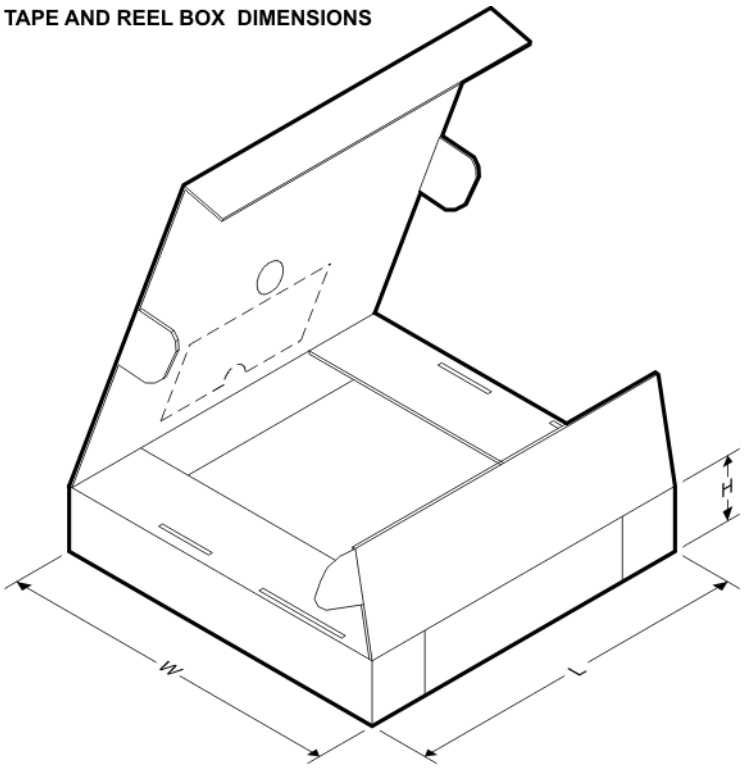
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62130AQRGTRQ1	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62130AQRGTTQ1	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62133AQRGTRQ1	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62133AQRGTTQ1	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

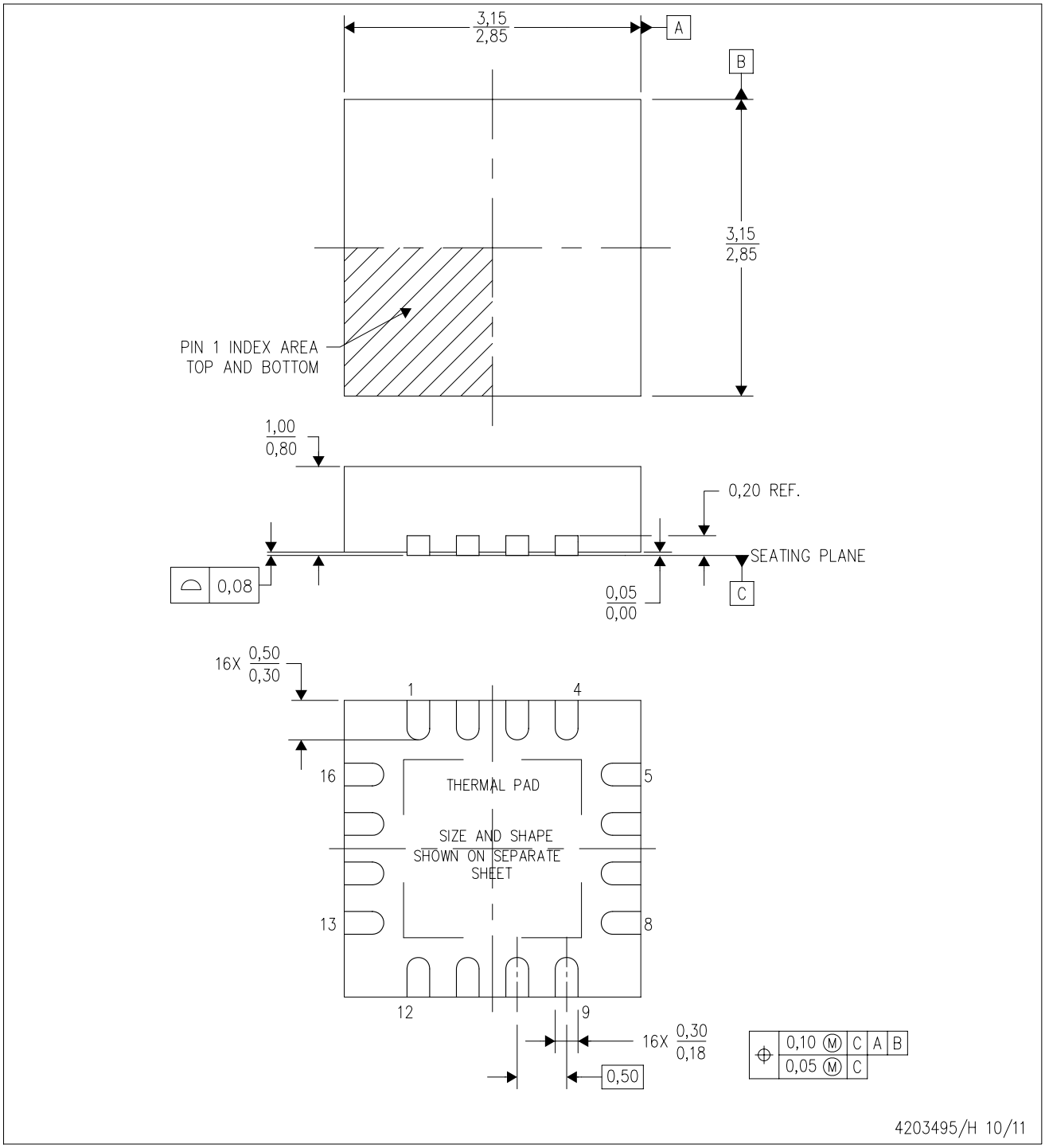
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62130AQRGTRQ1	QFN	RGT	16	3000	552.0	367.0	36.0
TPS62130AQRGTTQ1	QFN	RGT	16	250	552.0	185.0	36.0
TPS62133AQRGTRQ1	QFN	RGT	16	3000	552.0	367.0	36.0
TPS62133AQRGTTQ1	QFN	RGT	16	250	552.0	185.0	36.0

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

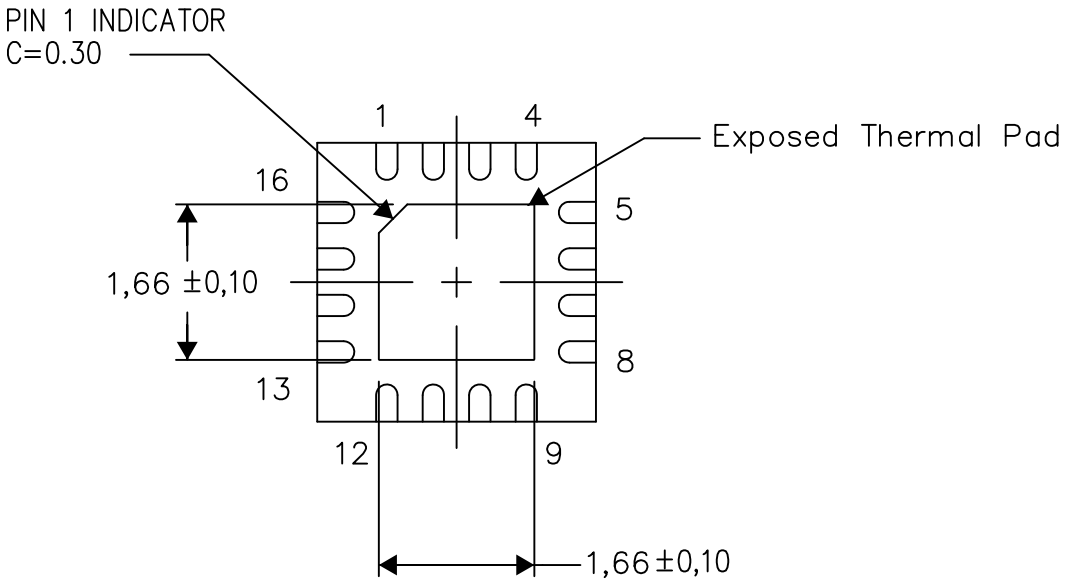
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206349–10/W 10/14

NOTE: All linear dimensions are in millimeters

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