



# Octal, 13-Bit Voltage-Output DAC with Parallel Interface

MAX547

## General Description

The MAX547 contains eight 13-bit, voltage-output digital-to-analog converters (DACs). On-chip precision output amplifiers provide the voltage outputs. The MAX547 operates from a  $\pm 5V$  supply. Bipolar output voltages with up to  $\pm 4.5V$  voltage swing can be achieved with no external components. The MAX547 has four separate reference inputs; each is connected to two DACs, providing different full-scale output voltages for every DAC pair.

The MAX547 features double-buffered interface logic with a 13-bit parallel data bus. Each DAC has an input latch and a DAC latch. Data in the DAC latch sets the output voltage. The eight input latches are addressed with three address lines. Data is loaded to the input latch with a single write instruction. An asynchronous load ( $\overline{LD}$ ) input transfers data from the input latch to the DAC latch. The four  $\overline{LD}$  inputs each control two DACs, and all DAC latches can be updated simultaneously by asserting all  $\overline{LD}$  pins. An asynchronous clear ( $\overline{CLR}$ ) input resets the output of all eight DACs to AGND. Asserting  $\overline{CLR}$  resets both the DAC and the input latch to bipolar zero (1000hex). On power-up, reset circuitry performs the same function as  $\overline{CLR}$ . All logic inputs are TTL/CMOS compatible.

The MAX547 is available in 44-pin plastic quad flat pack and 44-pin PLCC packages.

## Applications

Automatic Test Equipment  
Minimum Component-Count Analog Systems  
Digital Offset/Gain Adjustment  
Arbitrary Function Generators  
Industrial Process Controls  
Avionics Equipment

## Features

- ♦ Full 13-Bit Performance without Adjustments
- ♦ 8 DACs in One Package
- ♦ Buffered Voltage Outputs
- ♦ Calibrated Linearity
- ♦ Guaranteed Monotonic to 13 Bits
- ♦  $\pm 5V$  Supply Operation
- ♦ Unipolar or Bipolar Outputs Swing to  $\pm 4.5V$
- ♦ Fast Output Settling ( $5\mu s$  to  $\pm 1/2$ LSB)
- ♦ Double-Buffered Digital Inputs
- ♦ Asynchronous Load Inputs Load Pairs of DAC Latches
- ♦ Asynchronous  $\overline{CLR}$  Input Resets DACs to Analog Ground
- ♦ Power-On Reset Circuit Resets DACs to Analog Ground
- ♦ Microprocessor and TTL/CMOS Compatible

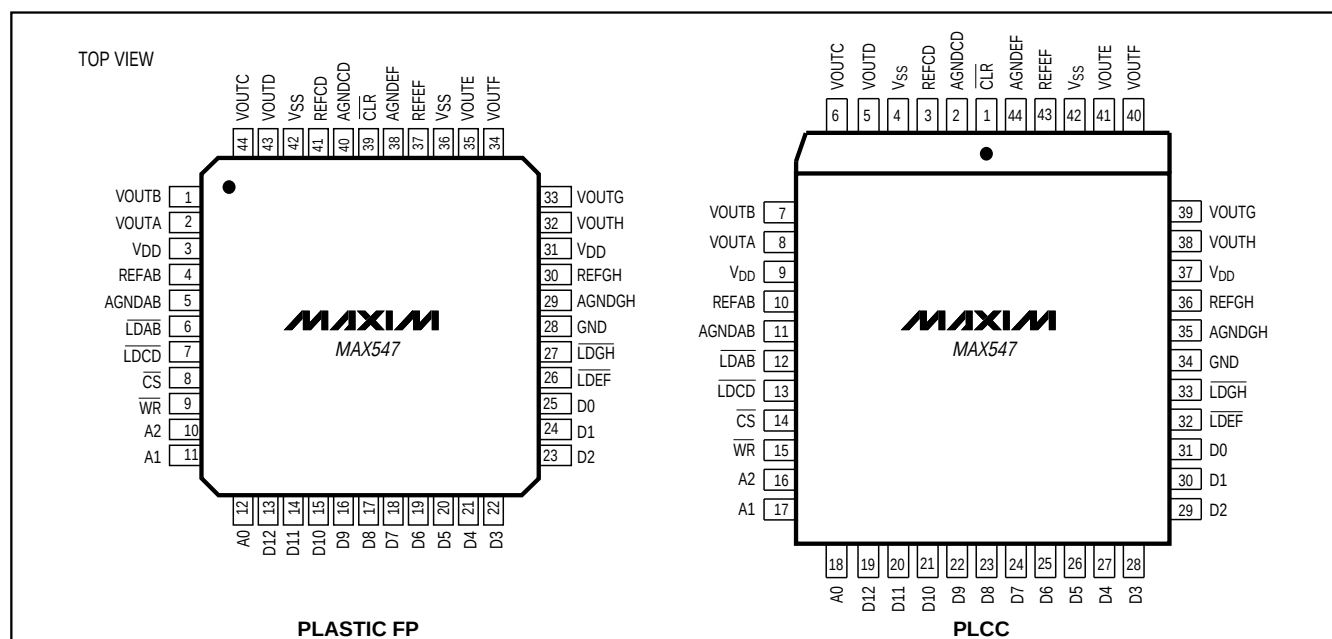
## Ordering Information

| PART       | TEMP. RANGE  | PIN-PACKAGE   | INL (LSBs) |
|------------|--------------|---------------|------------|
| MAX547ACQH | 0°C to +70°C | 44 PLCC       | $\pm 2$    |
| MAX547BCQH | 0°C to +70°C | 44 PLCC       | $\pm 4$    |
| MAX547ACMH | 0°C to +70°C | 44 Plastic FP | $\pm 2$    |
| MAX547BCMH | 0°C to +70°C | 44 Plastic FP | $\pm 4$    |
| MAX547BC/D | 0°C to +70°C | Dice*         | $\pm 4$    |

Ordering Information continued at end of data sheet.

\*Contact factory for dice specifications.

## Pin Configurations



# Octal, 13-Bit Voltage-Output DAC with Parallel Interface

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$  to GND .....-0.3V to +6V  
 $V_{SS}$  to GND .....-6V to +0.3V  
 Digital Input Voltage to GND .....-0.3V to ( $V_{DD} + 0.3$ )V  
 $REF_-$  .....( $AGND_- - 0.3$ )V to ( $V_{DD} + 0.3$ )V  
 $AGND_-$  .....( $V_{SS} - 0.3$ )V to ( $V_{DD} + 0.3$ )V  
 $V_{OUT_-}$  ..... $V_{DD}$  to  $V_{SS}$   
 Maximum Current into  $REF_-$  Pin .....±10mA  
 Maximum Current into Any Other Signal Pin .....±50mA

Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )  
     PLCC (derate 13.33mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) .....1067mW  
     Plastic FP (derate 11.11mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) .....889mW  
 Operating Temperature Ranges  
     MAX547\_C\_H ..... $0^\circ\text{C}$  to  $+70^\circ\text{C}$   
     MAX547\_E\_H ..... $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 Storage Temperature Range ..... $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Lead Temperature (soldering, 10sec) ..... $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{DD} = +5\text{V}$ ,  $V_{SS} = -5\text{V}$ ,  $REF_- = 4.096\text{V}$ ,  $AGND_- = \text{GND} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $C_L = 50\text{pF}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .)

| PARAMETER                                                       | SYMBOL   | CONDITIONS                                 | MIN      | TYP            | MAX      | UNITS            |
|-----------------------------------------------------------------|----------|--------------------------------------------|----------|----------------|----------|------------------|
| <b>STATIC PERFORMANCE—ANALOG SECTION</b>                        |          |                                            |          |                |          |                  |
| Resolution                                                      | N        |                                            | 13       |                |          | Bits             |
| Relative Accuracy                                               | INL      | MAX547A                                    |          | ±0.5           | ±2       | LSB              |
|                                                                 |          | MAX547B                                    |          | ±0.5           | ±4       |                  |
| Differential Nonlinearity                                       | DNL      | Guaranteed monotonic                       |          |                | ±1       | LSB              |
| Bipolar Zero-Code Error                                         |          |                                            |          | ±5             | ±20      | LSB              |
| Gain Error                                                      |          |                                            |          | ±1             | ±8       | LSB              |
| Power-Supply Rejection Ratio                                    | PSRR     | $\Delta\text{Gain}/\Delta V_{DD}$ (Note 1) |          |                | ±0.0025  | %/%              |
|                                                                 |          | $\Delta\text{Gain}/\Delta V_{SS}$ (Note 1) |          |                | ±0.0025  |                  |
| Load Regulation                                                 |          | $R_L = \infty$ to $10\text{k}\Omega$       |          | 0.3            |          | LSB              |
| <b>REFERENCE INPUT (Note 2)</b>                                 |          |                                            |          |                |          |                  |
| Reference Input Range                                           | REF      | (Notes 2, 3)                               | $AGND_-$ |                | $V_{DD}$ | V                |
| Reference Input Resistance                                      | RREF     | Each $REF_-$ pin (Note 3)                  | 5        |                |          | k $\Omega$       |
| <b>ANALOG OUTPUT</b>                                            |          |                                            |          |                |          |                  |
| Maximum Output Voltage                                          |          |                                            |          | $V_{DD} - 0.5$ |          | V                |
| Minimum Output Voltage                                          |          |                                            |          | $V_{SS} + 0.5$ |          | V                |
| <b>DYNAMIC PERFORMANCE—ANALOG SECTION</b>                       |          |                                            |          |                |          |                  |
| Voltage-Output Slew Rate                                        |          |                                            |          | 3              |          | V/ $\mu\text{s}$ |
| Output Settling Time                                            |          | To $\pm 1/2$ LSB of full scale (Note 4)    |          | 5              |          | $\mu\text{s}$    |
| Digital Feedthrough                                             |          |                                            |          | 5              |          | nV-s             |
| Digital Crosstalk                                               |          |                                            |          | 5              |          | nV-s             |
| <b>DIGITAL INPUTS (<math>V_{DD} = 5\text{V} \pm 5\%</math>)</b> |          |                                            |          |                |          |                  |
| Input Voltage High                                              | $V_{IH}$ |                                            | 2.4      |                |          | V                |
| Input Voltage Low                                               | $V_{IL}$ |                                            |          |                | 0.8      | V                |
| Input Current                                                   | $I_{IN}$ | $V_{IN} = 0\text{V}$ or $V_{DD}$           |          |                | 1.0      | $\mu\text{A}$    |
| Input Capacitance                                               | $C_{IN}$ | (Note 5)                                   |          |                | 10       | pF               |

# Octal, 13-Bit Voltage-Output DAC with Parallel Interface

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +5V$ ,  $V_{SS} = -5V$ ,  $REF_- = 4.096V$ ,  $AGND_- = GND = 0V$ ,  $R_L = 10k\Omega$ ,  $C_L = 50pF$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

| PARAMETER               | SYMBOL   | CONDITIONS                   | MIN   | TYP | MAX   | UNITS |
|-------------------------|----------|------------------------------|-------|-----|-------|-------|
| <b>POWER SUPPLIES</b>   |          |                              |       |     |       |       |
| Positive Supply Range   | $V_{DD}$ | (Note 6)                     | 4.75  |     | 5.25  | V     |
| Negative Supply Range   | $V_{SS}$ | (Note 6)                     | -5.25 |     | -4.75 | V     |
| Positive Supply Current | $I_{DD}$ | $T_A = T_{MIN}$ to $T_{MAX}$ |       | 14  | 44    | mA    |
| Negative Supply Current | $I_{SS}$ | $T_A = T_{MIN}$ to $T_{MAX}$ |       | 11  | 40    | mA    |

**Note 1:** PSRR is tested by changing the respective supply voltage by  $\pm 5\%$ .

**Note 2:** For best performance,  $REF_-$  should be greater than  $AGND_- + 2V$  and less than  $V_{DD} - 0.6V$ . The device operates with reference inputs outside this range, but performance may degrade. For further information on the reference, see the *Reference and Analog-Ground Inputs* section in the *Detailed Description*.

**Note 3:** Reference input resistance is code dependent. See *Reference and Analog-Ground Inputs* section in the *Detailed Description*.

**Note 4:** Typical settling time with 1000pF capacitive load is 10 $\mu s$ .

**Note 5:** Guaranteed by design. Not production tested.

**Note 6:** Guaranteed by supply-rejection test.

## TIMING CHARACTERISTICS

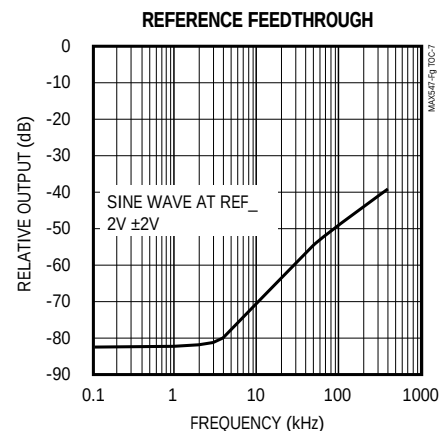
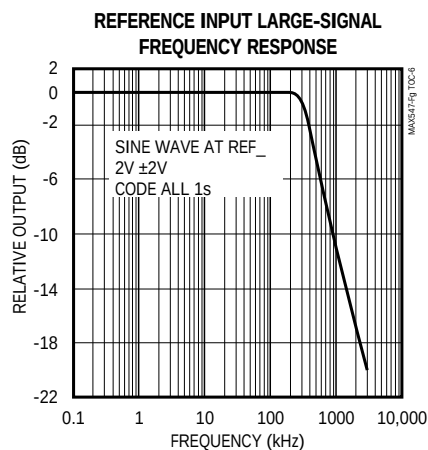
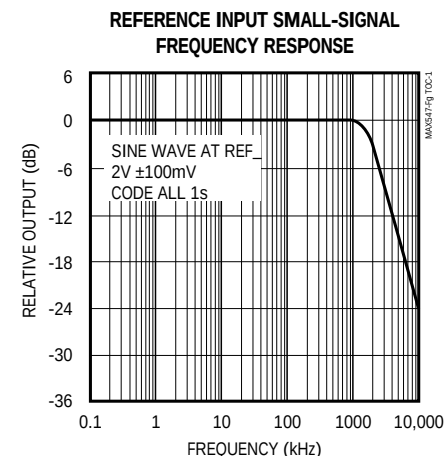
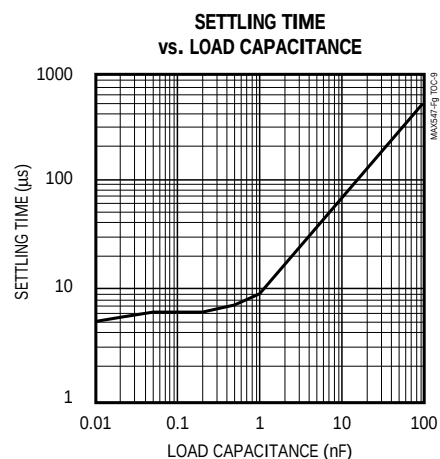
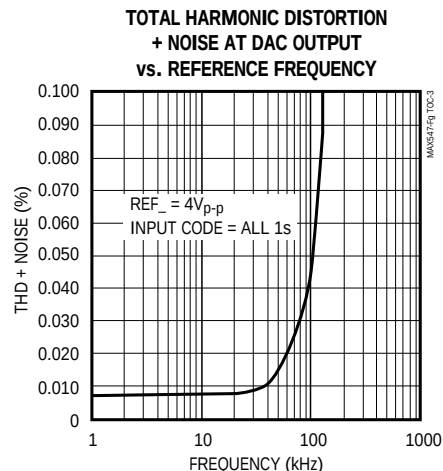
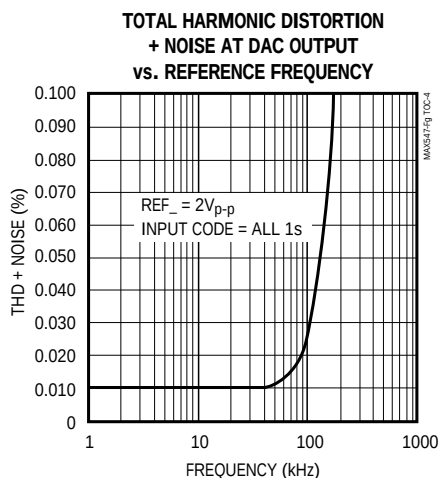
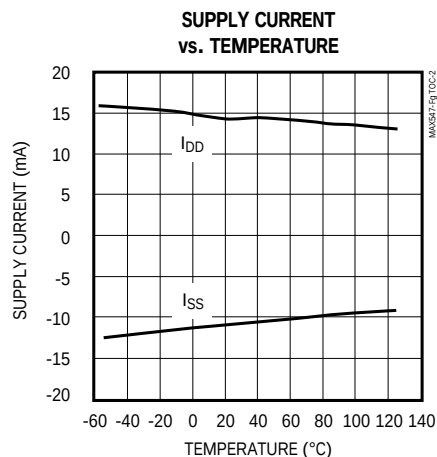
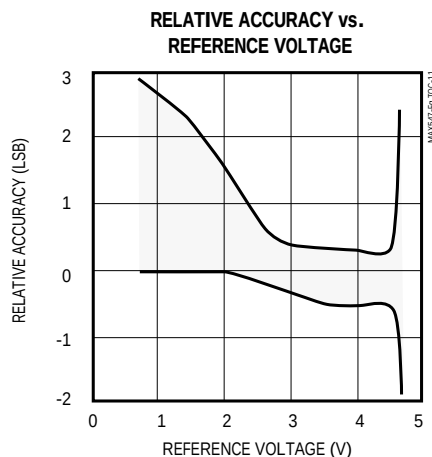
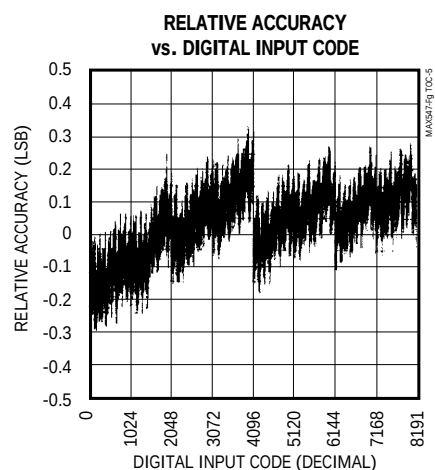
( $V_{DD} = +5V$ ,  $V_{SS} = -5V$ ,  $REF_- = 4.096V$ ,  $AGND_- = GND = 0V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

| PARAMETER                                    | SYMBOL   | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------------------------|----------|------------|-----|-----|-----|-------|
| $\overline{CS}$ Pulse Width Low              | $t_1$    |            | 50  |     |     | ns    |
| $\overline{WR}$ Pulse Width Low              | $t_2$    |            | 50  |     |     | ns    |
| $\overline{LD_-}$ Pulse Width Low            | $t_3$    |            | 50  |     |     | ns    |
| $\overline{CLR}$ Pulse Width Low             | $t_4$    |            | 100 |     |     | ns    |
| $\overline{CS}$ Low to $\overline{WR}$ Low   | $t_5$    |            | 0   |     |     | ns    |
| $\overline{CS}$ High to $\overline{WR}$ High | $t_6$    |            | 0   |     |     | ns    |
| Data Valid to $\overline{WR}$ Setup          | $t_7$    |            | 50  |     |     | ns    |
| Data Valid to $\overline{WR}$ Hold           | $t_8$    |            | 0   |     |     | ns    |
| Address Valid to $\overline{WR}$ Setup       | $t_9$    |            | 10  |     |     | ns    |
| Address Valid to $\overline{WR}$ Hold        | $t_{10}$ |            | 0   |     |     | ns    |

# Octal, 13-Bit Voltage-Output DAC with Parallel Interface

## Typical Operating Characteristics

( $V_{DD} = 5V$ ,  $V_{SS} = -5V$ ,  $REF_- = 4.096V$ ,  $AGND_- = GND = 0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

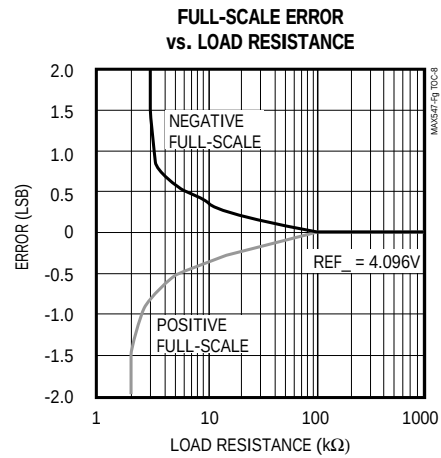
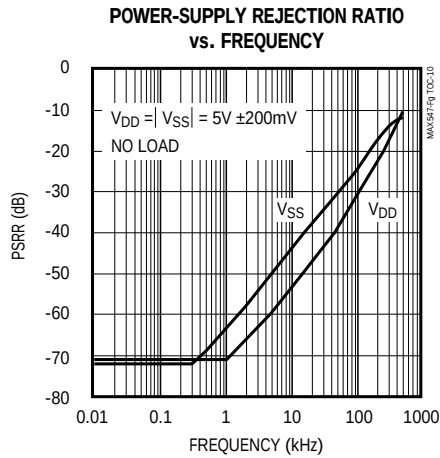


# Octal, 13-Bit Voltage-Output DAC with Parallel Interface

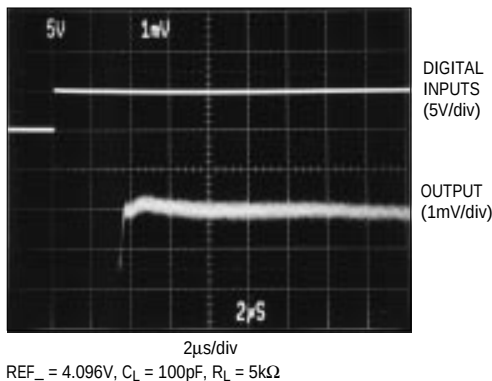
MAX547

## Typical Operating Characteristics (continued)

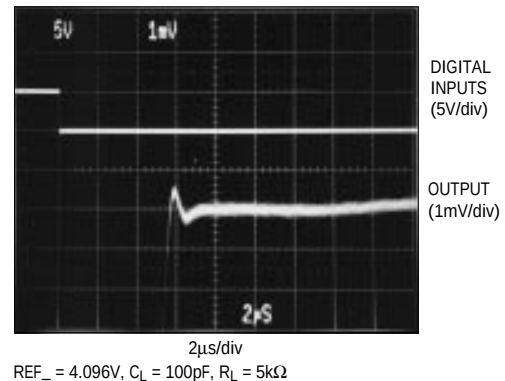
( $V_{DD} = 5V$ ,  $V_{SS} = -5V$ ,  $REF_- = 4.096V$ ,  $AGND_- = GND = 0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



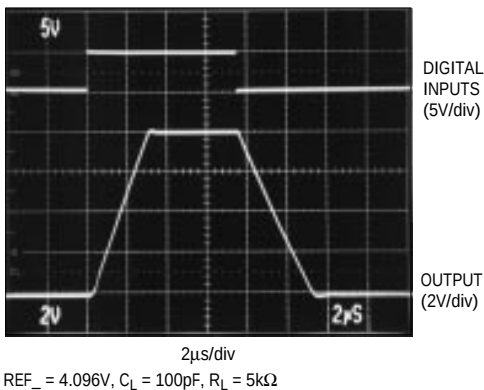
**POSITIVE SETTLING TIME TO FULL-SCALE STEP  
(ALL BITS OFF TO ALL BITS ON)**



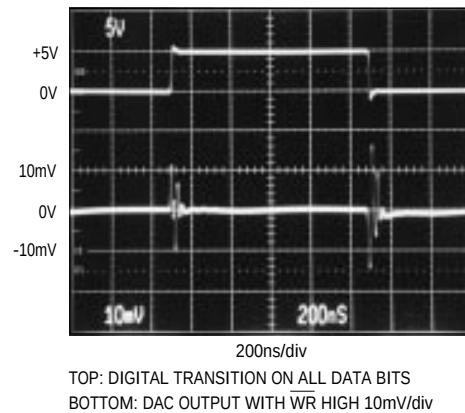
**NEGATIVE SETTLING TIME TO FULL-SCALE STEP  
(ALL BITS ON TO ALL BITS OFF)**



**DYNAMIC RESPONSE  
(ALL BITS OFF, ON, OFF)**



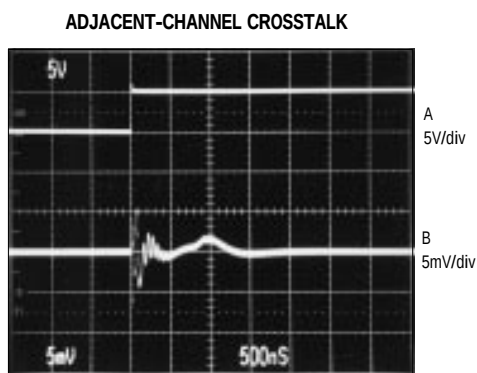
**DIGITAL FEEDTHROUGH  
(GLITCH IMPULSE)**



# Octal, 13-Bit Voltage-Output DAC with Parallel Interface

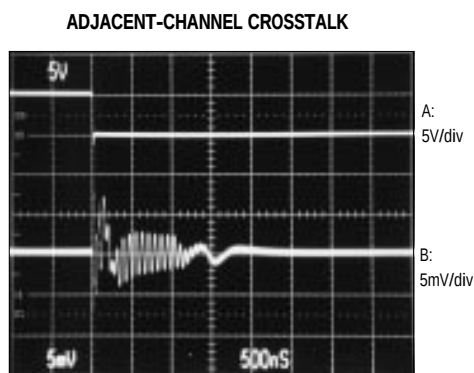
## Typical Operating Characteristics (continued)

( $V_{DD} = 5V$ ,  $V_{SS} = -5V$ ,  $REF_- = 4.096V$ ,  $AGND_- = GND = 0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



$REF_- = 4.096V$ ,  $C_L = 50pF$ ,  $R_L = 10k\Omega$

A: DIGITAL INPUTS, DAC A, DATA BITS from ALL 0s to OAAAhex  
B: OUTPUT, DAC B



$REF_- = 4.096V$ ,  $C_L = 50pF$ ,  $R_L = 10k\Omega$

A: DIGITAL INPUTS, DAC A, DATA BITS from OAAAhex to ALL 0s  
B: OUTPUT, DAC B

## Pin Description

| PIN   |           | NAME              | FUNCTION                                                                                                                                                             |
|-------|-----------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PLCC  | FLAT PACK |                   |                                                                                                                                                                      |
| 1     | 39        | $\overline{CLR}$  | Clear Input (active low). Driving this asynchronous input low sets the content of all latches to 1000hex. All DAC outputs are reset to AGND <sub>-</sub> .           |
| 2     | 40        | AGNDCD            | Analog Ground for DAC C and DAC D                                                                                                                                    |
| 3     | 41        | REFCD             | Reference Voltage Input for DAC C and DAC D. Bypass to AGNDCD with a 0.1 $\mu F$ to 1 $\mu F$ capacitor.                                                             |
| 4, 42 | 42, 36    | $V_{SS}$          | Negative Power Supply, -5V (2 pins). Connect both pins to the supply voltage. Bypass each pin to the system analog ground with a 0.1 $\mu F$ to 1 $\mu F$ capacitor. |
| 5     | 43        | VOUTD             | DAC D Output Voltage                                                                                                                                                 |
| 6     | 44        | VOUTC             | DAC C Output Voltage                                                                                                                                                 |
| 7     | 1         | VOUTB             | DAC B Output Voltage                                                                                                                                                 |
| 8     | 2         | VOUTA             | DAC A Output Voltage                                                                                                                                                 |
| 9, 37 | 3, 31     | $V_{DD}$          | Positive Power Supply, 5V (2 pins). Connect both pins to the supply voltage. Bypass each pin to the system analog ground with a 0.1 $\mu F$ to 1 $\mu F$ capacitor.  |
| 10    | 4         | REFAB             | Reference Voltage Input for DAC A and DAC B. Bypass to AGNDAB with a 0.1 $\mu F$ to 1 $\mu F$ capacitor.                                                             |
| 11    | 5         | AGNDAB            | Analog Ground for DAC A and DAC B                                                                                                                                    |
| 12    | 6         | $\overline{LDAB}$ | Load Input (active low). Driving this asynchronous input low transfers the contents of input latches A and B to the respective DAC latches.                          |
| 13    | 7         | $\overline{LDCD}$ | Load Input (active low). Driving this asynchronous input low transfers the contents of input latches C and D to the respective DAC latches.                          |
| 14    | 8         | $\overline{CS}$   | Chip Select (active low)                                                                                                                                             |
| 15    | 9         | $\overline{WR}$   | Write Input (active low). $\overline{WR}$ , along with $\overline{CS}$ , loads data into the DAC input latch selected by A0–A2.                                      |

# Octal, 13-Bit Voltage-Output DAC with Parallel Interface

## Pin Description (continued)

| PIN   |           | NAME                     | FUNCTION                                                                                                                                    |
|-------|-----------|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| PLCC  | FLAT PACK |                          |                                                                                                                                             |
| 16    | 10        | A2                       | Address Bit 2                                                                                                                               |
| 17    | 11        | A1                       | Address Bit 1                                                                                                                               |
| 18    | 12        | A0                       | Address Bit 0                                                                                                                               |
| 19–31 | 13–25     | D12–D0                   | Data Bits 12–0                                                                                                                              |
| 32    | 26        | $\overline{\text{LDEF}}$ | Load Input (active low). Driving this asynchronous input low transfers the contents of input latches E and F to the respective DAC latches. |
| 33    | 27        | $\overline{\text{LDGH}}$ | Load Input (active low). Driving this asynchronous input low transfers the contents of input latches G and H to the respective DAC latches. |
| 34    | 28        | GND                      | Digital Ground                                                                                                                              |
| 35    | 29        | AGNDGH                   | Analog Ground for DAC G and DAC H                                                                                                           |
| 36    | 30        | REFGH                    | Reference Voltage Input for DAC G and DAC H. Bypass to AGNDGH with a 0.1 $\mu$ F to 1 $\mu$ F capacitor.                                    |
| 38    | 32        | VOUTH                    | DAC H Output Voltage                                                                                                                        |
| 39    | 33        | VOUTG                    | DAC G Output Voltage                                                                                                                        |
| 40    | 34        | VOUTF                    | DAC F Output Voltage                                                                                                                        |
| 41    | 35        | VOUTE                    | DAC E Output Voltage                                                                                                                        |
| 43    | 37        | REFEF                    | Reference Voltage Input for DAC E and DAC F. Bypass to AGNDEF with a 0.1 $\mu$ F to 1 $\mu$ F capacitor.                                    |
| 44    | 38        | AGNDEF                   | Analog Ground for DAC E and DAC F                                                                                                           |

## Detailed Description

### Analog Section

The MAX547 contains eight 13-bit, voltage-output DACs. These DACs are “inverted” R-2R ladder networks that convert 13-bit digital inputs into equivalent analog output voltages, in proportion to the applied reference voltages. The MAX547 has one reference input (REF<sub>-</sub>) and one analog-ground input (AGND<sub>-</sub>) for each pair of DACs. The four REF<sub>-</sub> inputs allow different full-scale output voltages for each DAC pair, and the four AGND<sub>-</sub> inputs allow different offset voltages for each DAC pair.

The DAC ladder outputs are buffered with op amps that operate with a gain of two. The inverting node of the amplifier is connected to the respective reference input, resulting in bipolar output voltages from -REF<sub>-</sub> to 4095/4096 REF<sub>-</sub>. Figure 1 shows the simplified DAC circuit.

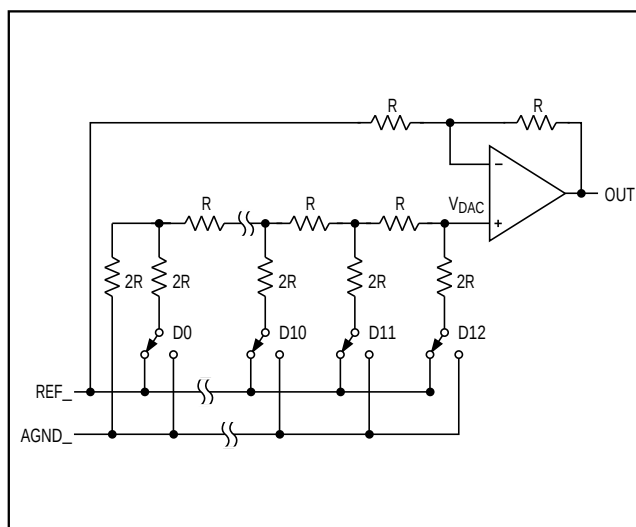


Figure 1. DAC Simplified Circuit Diagram

# Octal, 13-Bit Voltage-Output DAC with Parallel Interface

## Reference and Analog-Ground Inputs

The REF<sub>-</sub> inputs can range between AGND<sub>-</sub> and V<sub>DD</sub>. However, the DAC outputs will operate to V<sub>DD</sub> - 0.6V and V<sub>SS</sub> + 0.6V, due to the output amplifiers' voltage-swing limitations. The AGND<sub>-</sub> inputs can be offset by any voltage within the supply rails. The offset-voltage potential must be lower than the reference-voltage potential. For more information, refer to the *Digital Code and Analog Output Voltage* section in the *Applications Information*.

The input impedance of the REF<sub>-</sub> inputs is code dependent. It is at its lowest value (5k $\Omega$  min) when the input code of the referring DAC pair is 0 1010 1010 (0AAAhex). Its maximum value, typically 50k $\Omega$ , occurs when the code is 0000hex. When all reference inputs are driven from the same source, the minimum load impedance is 1.25k $\Omega$ . Since the input impedance at REF<sub>-</sub> is code dependent, load regulation of the reference used is important. For more information, see *Reference Selection* in the *Applications Information* section.

The input capacitance at REF<sub>-</sub> is also code dependent, and typically varies from 125pF to 300pF. Its minimum value occurs when the code of the referring DAC pair is set to all 0s. It is at its maximum value with all 1s on both DACs.

## Output Buffer Amplifiers

The MAX547's voltage outputs are internally buffered by precision gain-of-two amplifiers with a typical slew rate of 3V/ $\mu$ s. With a full-scale transition at its output, the typical settling time to  $\pm 1/2$ LSB is 5 $\mu$ s when loaded with 10k $\Omega$  in parallel with 50pF, or 6 $\mu$ s when loaded with 10k $\Omega$  in parallel with 100pF.

## Digital Inputs and Interface Logic

All digital inputs are compatible with both TTL and CMOS logic. The MAX547 interfaces with microprocessors using a data bus at least 13 bits wide. The interface is double buffered, allowing simultaneous update of all DACs. There are two latches for each DAC (see *Functional Diagram*): an input latch that receives data from the data bus, and a DAC latch that receives data from the input latch. Address lines A0, A1, and A2 select which DAC's input latch receives data from the data bus, as shown in Table 1. Transfer data from the input latches to the DAC latches by asserting the asynchronous  $\overline{\text{LD}}$  signal. Each DAC's analog output reflects the data held in its DAC latch. All control inputs are level triggered.

Data can be latched or transferred directly to the DAC.  $\overline{\text{CS}}$  and  $\overline{\text{WR}}$  control the input latch and  $\overline{\text{LD}}$  transfers information from the input latch to the DAC latch. The input latch is transparent when  $\overline{\text{CS}}$  and  $\overline{\text{WR}}$  are low, and

Table 1. MAX547 DAC Addressing

| A2 | A1 | A0 | FUNCTION          |
|----|----|----|-------------------|
| 0  | 0  | 0  | DAC A input latch |
| 0  | 0  | 1  | DAC B input latch |
| 0  | 1  | 0  | DAC C input latch |
| 0  | 1  | 1  | DAC D input latch |
| 1  | 0  | 0  | DAC E input latch |
| 1  | 0  | 1  | DAC F input latch |
| 1  | 1  | 0  | DAC G input latch |
| 1  | 1  | 1  | DAC H input latch |

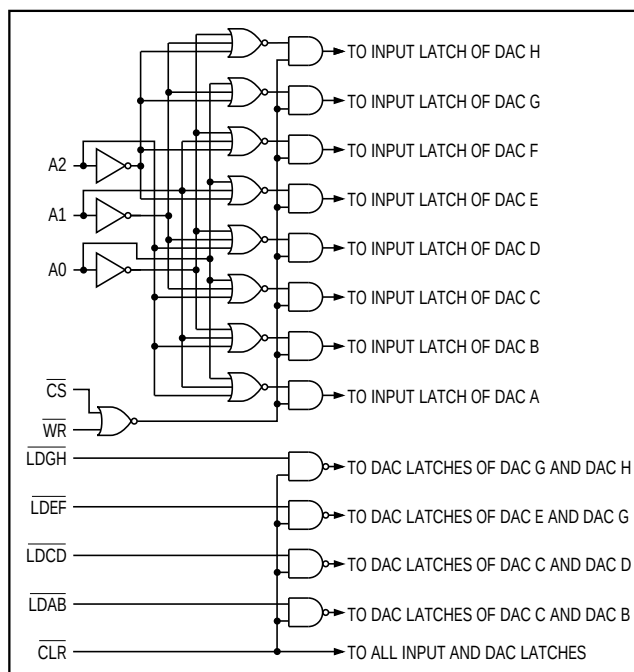


Figure 2. Input Control Logic

the DAC latch is transparent when  $\overline{\text{LD}}$  is low. The address lines (A0, A1, A2) must be valid throughout the time  $\overline{\text{CS}}$  and  $\overline{\text{WR}}$  are low (Figure 3). Otherwise, the data can be inadvertently written to the wrong DAC. Data is latched within the input latch when either  $\overline{\text{CS}}$  or  $\overline{\text{WR}}$  is high. Taking  $\overline{\text{LD}}$  high latches data into the DAC latches. If  $\overline{\text{LD}}$  is brought low when  $\overline{\text{WR}}$  and  $\overline{\text{CS}}$  are low, it must be held low for  $t_3$  or longer after  $\overline{\text{WR}}$  and  $\overline{\text{CS}}$  are high (Figure 3).

Pulling the asynchronous  $\overline{\text{CLR}}$  input low sets all DAC outputs to a nominal 0V, regardless of the state of  $\overline{\text{CS}}$ ,  $\overline{\text{WR}}$ , and  $\overline{\text{LD}}$ . Taking  $\overline{\text{CLR}}$  high latches 1000hex into all input latches and DAC latches.



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**Table 2. Interface Truth Table**

| $\overline{\text{CLR}}$ | $\overline{\text{LD}}_{-}$ | $\overline{\text{WR}}$ | $\overline{\text{CS}}$ | FUNCTION                                                           |
|-------------------------|----------------------------|------------------------|------------------------|--------------------------------------------------------------------|
| 1                       | 0                          | 0                      | 0                      | Both latches transparent                                           |
| 1                       | 1                          | 1                      | X                      | Both latches latched                                               |
| 1                       | 1                          | X                      | 1                      | Both latches latched                                               |
| 1                       | X                          | 0                      | 0                      | Input latch transparent                                            |
| 1                       | X                          | 1                      | X                      | Input latch latched                                                |
| 1                       | X                          | X                      | 1                      | Input latch latched                                                |
| 1                       | 0                          | X                      | X                      | DAC latch transparent                                              |
| 0                       | X                          | X                      | X                      | All input and DAC latches at 1000hex, outputs at AGND <sub>-</sub> |

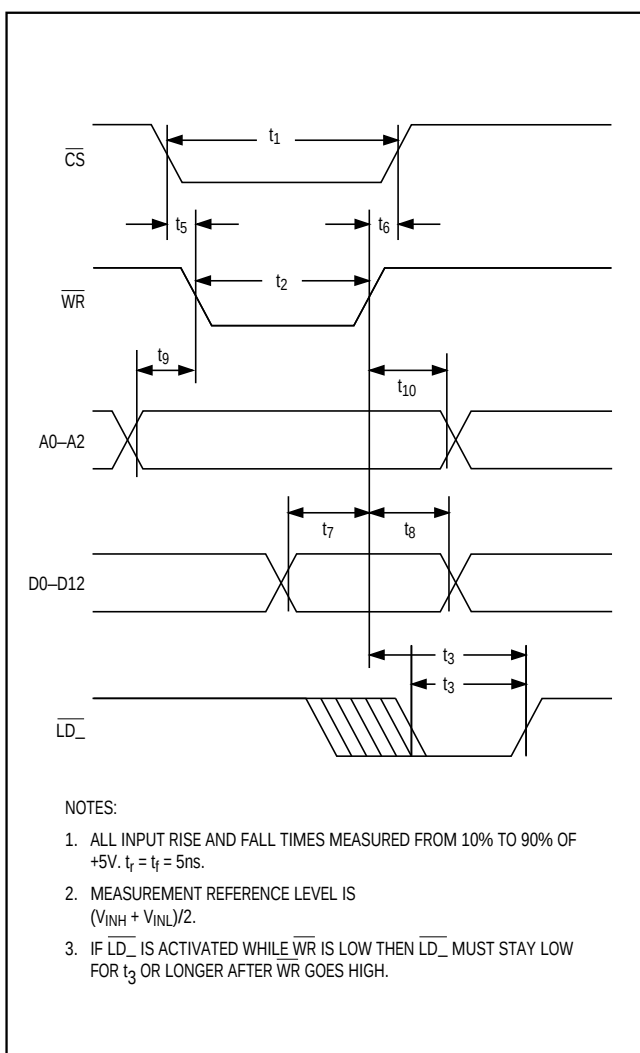


Figure 3. Write-Cycle Timing

## Applications Information

### Multiplying Operation

The MAX547 can be used for multiplying applications. Its reference accepts both DC and AC signals. The voltage at each REF<sub>-</sub> input sets the full-scale output voltage for its respective DACs. Since the reference inputs accept only positive voltages, multiplying operation is limited to two quadrants. Do not bypass the reference inputs when applying AC signals to them. Refer to the graphs in the *Typical Operating Characteristics* for dynamic performance of the DACs and output buffers.

### Digital Code and Analog Output Voltage

The MAX547 uses offset binary coding. A 13-bit twos-complement code can be converted to a 13-bit offset binary code by adding  $2^{12} = 4096$ .

### Bipolar Output Voltage Range (AGND<sub>-</sub> = 0V)

For symmetrical bipolar operation, tie AGND<sub>-</sub> to the system ground. Table 3 shows the relationship between digital code and output voltage. The following paragraphs give a detailed explanation of this mode.

The DAC ladder output voltage ( $V_{\text{DAC}}$ ) is multiplied by 2 and level shifted by the reference voltage, which is internally connected to the output amplifiers (Figure 1). Since the feedback resistors are the same size, the amplifier's output voltage is 2 times the voltage at its noninverting input, minus the reference voltage.

$$V_{\text{OUT}} = 2(V_{\text{DAC}}) - \text{REF}_{-}$$

where  $V_{\text{DAC}}$  is the voltage at the amplifier's noninverting input (DAC ladder output voltage), and  $\text{REF}_{-}$  is the voltage applied to the reference input of the DAC.

With AGND<sub>-</sub> connected to the system ground, the DAC ladder output voltage is:

$$V_{\text{DAC}} = \frac{D}{2^n} (\text{REF}_{-}) = \frac{D}{2^{13}} (\text{REF}_{-})$$

where  $D$  is the numeric value of the DAC's binary input code and  $n$  is the DAC's resolution (13 bits). Replace  $V_{\text{DAC}}$  in the equation and calculate the output voltage.

$$\begin{aligned} V_{\text{OUT}} &= 2 \left( \frac{D}{2^{13}} \right) (\text{REF}_{-}) - \text{REF}_{-} \\ &= \text{REF}_{-} \left( \frac{D}{2^{12}} - 1 \right) = \text{REF}_{-} \left( \frac{D}{4096} - 1 \right) \end{aligned}$$

$D$  ranges from 0 ( $2^0$ ) to 8191 ( $2^{13} - 1$ ).

$$1\text{LSB} = \text{REF}_{-} \left( \frac{1}{4096} \right)$$

# Octal, 13-Bit Voltage-Output DAC with Parallel Interface

**Table 3. MAX547 Bipolar Code Table**  
(AGND<sub>-</sub> = 0V)

| INPUT            | OUTPUT                                    |
|------------------|-------------------------------------------|
| 1 1111 1111 1111 | $+REF_- \left( \frac{4095}{4096} \right)$ |
| 1 0000 0000 0001 | $+REF_- \left( \frac{1}{4096} \right)$    |
| 1 0000 0000 0000 | 0V                                        |
| 0 1111 1111 1111 | $-REF_- \left( \frac{1}{4096} \right)$    |
| 0 0000 0000 0001 | $-REF_- \left( \frac{4095}{4096} \right)$ |
| 0 0000 0000 0000 | $-REF_-$                                  |

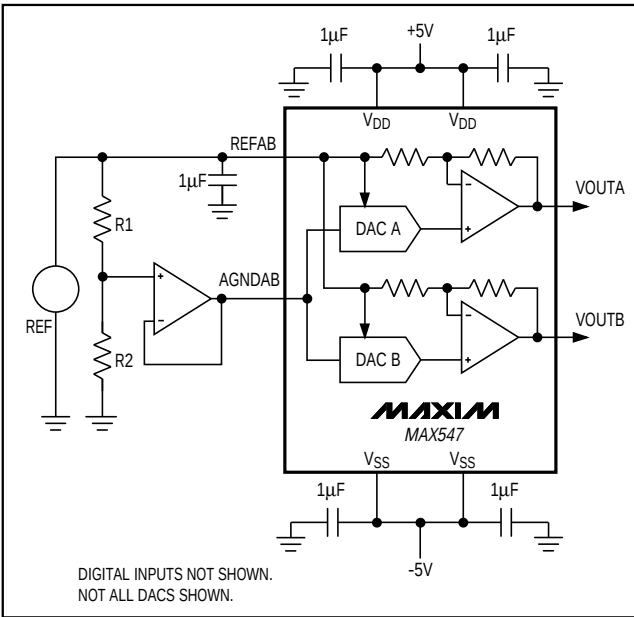


Figure 4. Offsetting AGND<sub>-</sub>

## Positive Unipolar Output Voltage Range (AGND<sub>-</sub> = REF<sub>-</sub>/2)

For positive unipolar output operation, set AGND<sub>-</sub> to (REF<sub>-</sub>/2). For example, if you use Figure 4's circuit with, a 4.096V reference and offset AGND<sub>-</sub> by 2.048V with matched resistors (R1 = R2) and an op amp, it results in a 0V to 4.0955V (nominal) unipolar output voltage, where 1LSB = 500μV. In general, the maximum current flowing out of any AGND<sub>-</sub> pin is given by:

$$I_{AGND_-} = \left( \frac{REF_- - AGND_-}{5k\Omega} \right)$$

**Table 4. MAX547 Positive Unipolar Code Table**  
(AGND<sub>-</sub> =  $\frac{REF_-}{2}$ )

| INPUT            | OUTPUT                                    |
|------------------|-------------------------------------------|
| 1 1111 1111 1111 | $+REF_- \left( \frac{8191}{8192} \right)$ |
| 1 0000 0000 0000 | $+REF_- / 2$                              |
| 0 0000 0000 0000 | 0V                                        |

## Customizing the Output Voltage Range

The AGND<sub>-</sub> inputs can be offset by any voltage within the supply rails if the voltage at the referring REF<sub>-</sub> input is higher than the voltage at the AGND<sub>-</sub> input. Select the reference voltage and the voltage at AGND<sub>-</sub> so the resulting output voltages do not come within ±0.6V of the supply rails. Figure 4's circuit shows one way to add positive offset to AGND<sub>-</sub>; make sure that the op amp used has sufficient current-sink capability to take up the remaining AGND<sub>-</sub> current:

$$I_{AGND_-} = \left( \frac{REF_- - AGND_-}{5k\Omega} \right)$$

Another way is to digitally offset AGND<sub>-</sub> by connecting the output of one DAC to one or more AGND<sub>-</sub> inputs. Do not connect a DAC output to its own AGND<sub>-</sub> input.

Table 5 summarizes the relationship between the reference and AGND<sub>-</sub> potentials and the output voltage in the different modes of operation.

## Power-Supply Sequencing

The sequence in which the supply voltages come up is not critical. However, we recommend that on power-up, V<sub>SS</sub> comes up first, V<sub>DD</sub> next, followed by the reference voltages. If you use other sequences, limit the current into any reference pin to 10mA. Also, make sure that V<sub>SS</sub> is never more than 300mV above ground. If there is a risk that this can occur at power-up, connect a Schottky diode between V<sub>SS</sub> and GND, as shown in Figure 5. We recommend that you not power up the logic input pins before establishing the supply voltages. If this is not possible and the digital lines can drive more than 10mA, you should place current-limiting resistors (e.g., 470Ω) in series with the logic pins.

## Reference Selection

If you want a ±2.5V full-scale output voltage swing, you can use the MAX873 reference. It operates from a single 5V supply and is specified to drive up to 10mA. Therefore, it can drive all four reference inputs simultaneously. Because the maximum load impedance can vary from 1.25kΩ to 12.5kΩ (four reference inputs in parallel), the reference load current ranges from 2mA to 0.2mA (1.8mA maximum load step). The MAX873's

# Octal, 13-Bit Voltage-Output DAC with Parallel Interface

**Table 5. Reference, AGND<sub>-</sub> and Output Relationships**

| PARAMETER                                                               | BIPOLAR OPERATION<br>(AGND <sub>-</sub> = 0V) | POSITIVE UNIPOLAR<br>OPERATION<br>(AGND <sub>-</sub> = REF <sub>-</sub> /2) | CUSTOM OPERATION                                        |
|-------------------------------------------------------------------------|-----------------------------------------------|-----------------------------------------------------------------------------|---------------------------------------------------------|
| Bipolar Zero Level, or<br>Unipolar Mid-scale,<br>(Code = 1000000000000) | AGND <sub>-</sub> (=0V)                       | $AGND_{-} \left( = \frac{REF_{-}}{2} \right)$                               | AGND <sub>-</sub>                                       |
| Differential Reference Voltage<br>(V <sub>DR</sub> )                    | REF <sub>-</sub>                              | REF <sub>-</sub> /2                                                         | REF <sub>-</sub> - AGND <sub>-</sub>                    |
| Negative Full-scale Output<br>(Code = All 0s)                           | -REF <sub>-</sub>                             | 0V                                                                          | AGND <sub>-</sub> - V <sub>DR</sub>                     |
| Positive Full-Scale Output<br>(Code = All 1s)                           | $\left( \frac{4095}{4096} \right) (REF_{-})$  | $\left( \frac{8191}{8192} \right) (REF_{-})$                                | $AGND_{-} + \left( \frac{4095}{4096} \right) (V_{DR})$  |
| LSB Weight                                                              | $\frac{REF_{-}}{4096}$                        | $\left( \frac{REF_{-}}{8192} \right)$                                       | $\frac{V_{DR}}{4096}$                                   |
| VOUT <sub>-</sub> as a Function of<br>Digital Code (D, 0 to 8191)       | $\left( \frac{D}{4096} - 1 \right) (REF_{-})$ | $\left( \frac{D}{8192} \right) (REF_{-})$                                   | $AGND_{-} + \left( \frac{D}{4096} - 1 \right) (V_{DR})$ |

load regulation is specified to 20ppm/mA max over temperature, resulting in a maximum error of 36ppm (90μV). This corresponds to a maximum error caused by reference load regulation of only 0.147LSB [0.147LSB = 90μV/(5V/8192)LSB] over temperature.

If you want a ±4.096V full-scale output swing (1LSB = 1mV), you can use the calibrated, low-drift, low-dropout MAX676. Operating from a 5V supply, it is fully specified to drive two REF<sub>-</sub> inputs with less than 60.4μV error (0.0604LSB) over temperature, caused by the maximum load step.

## Reference Buffering

Another way to obtain high accuracy is to buffer a reference with an op amp. When driving all reference inputs simultaneously, keep the closed-loop output impedance of the op amp below 0.03Ω to ensure an error of less than 0.1LSB. The op amp must also drive the capacitive load (typically 500pF to 1200pF).

Each reference input can also be buffered separately by using the circuit in Figure 6. A reference load step caused by a digital transition only affects the DAC pair where the code transition occurs. It also allows the use of references with little drive capability. Keep the closed-loop output impedance of each op amp below 0.12Ω, to ensure an error of less than 0.1LSB. Figure 6 shows the op amp's inverting input directly connected to the MAX547's reference terminal. This eliminates the

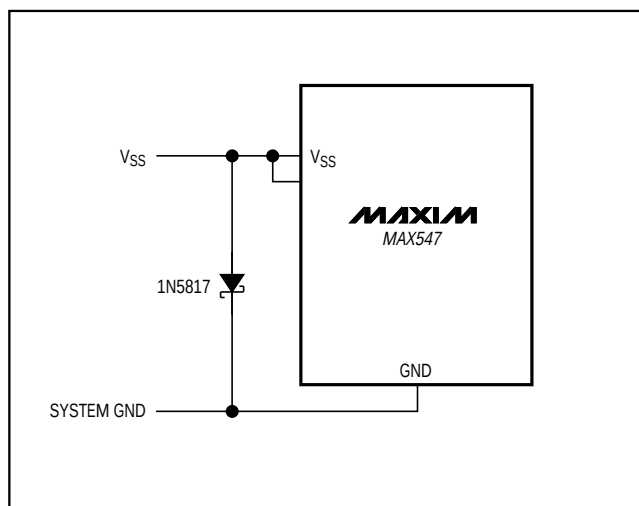


Figure 5. Optional Schottky Diode between V<sub>SS</sub> and GND

influence of board lead resistance by sensing the voltage with a low-current path sense line directly at the reference input.

Adding feedback resistors to individual reference buffer amplifiers enables different reference voltages to be generated from a single reference.

# Octal, 13-Bit Voltage-Output DAC with Parallel Interface

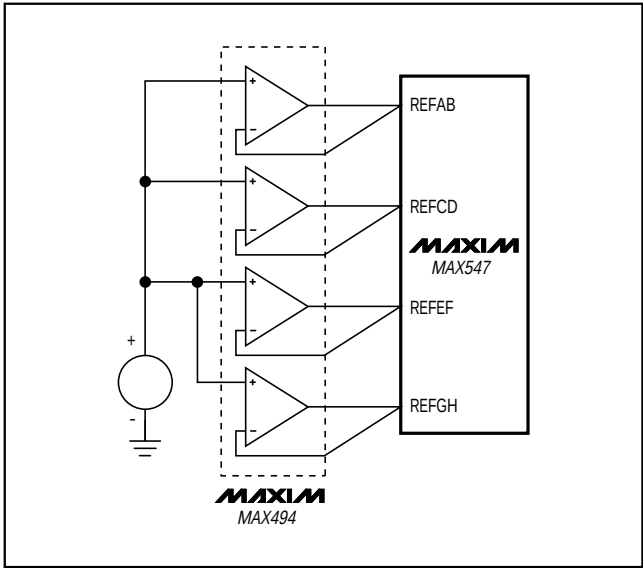


Figure 6. Reference Buffering

## \_Ordering Information (continued)

| PART       | TEMP. RANGE    | PIN-PACKAGE   | INL (LSBs) |
|------------|----------------|---------------|------------|
| MAX547AEQH | -40°C to +85°C | 44 PLCC       | ±2         |
| MAX547BEQH | -40°C to +85°C | 44 PLCC       | ±4         |
| MAX547AEMH | -40°C to +85°C | 44 Plastic FP | ±2         |
| MAX547BEMH | -40°C to +85°C | 44 Plastic FP | ±4         |

### Power-Supply Bypassing and Ground Management

For optimum performance, use a multilayer PC board with an unbroken analog ground. For normal operation, when all AGND\_ pins are at the same potential, connect the four AGND\_ pins directly to the ground plane or connect them together in a “star” configuration. The center of this star point is a good location to connect the digital system ground with the analog ground.

If you are using a single common reference voltage, you can connect the reference inputs together using a “star” configuration. If you are using DC reference voltages, bypass each reference input with a 0.1µF to 1µF capacitor to AGND\_.

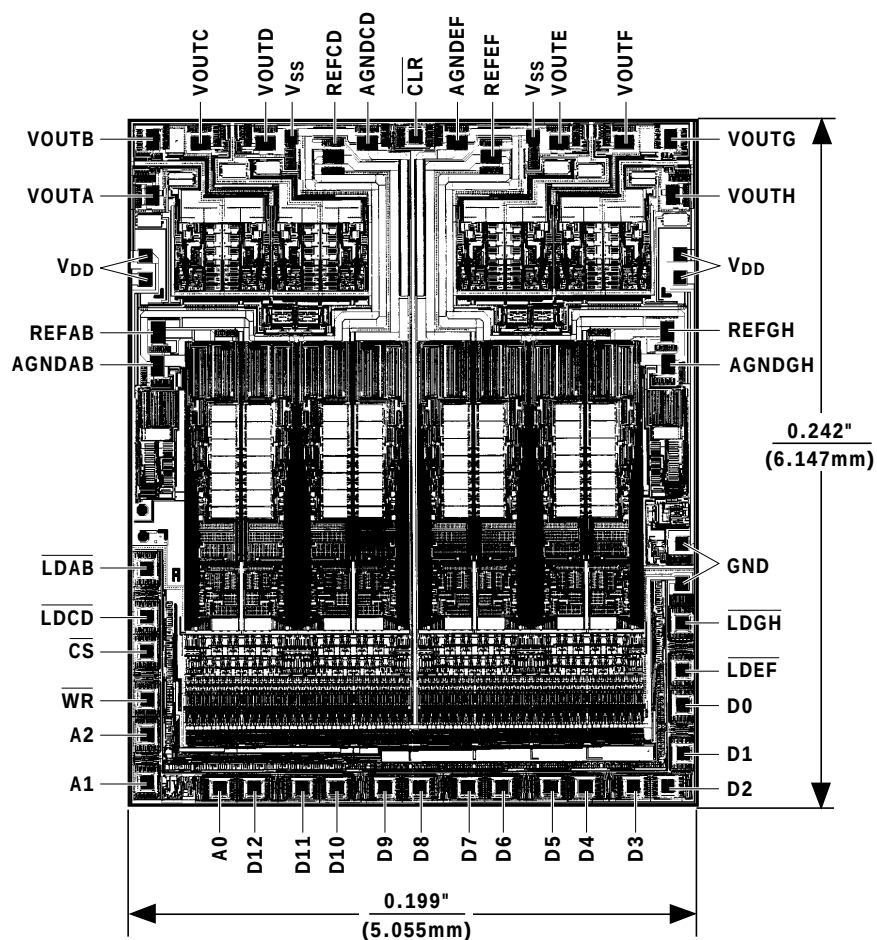
## MAX547

MAX547



# Octal, 13-Bit Voltage-Output DAC with Parallel Interface

Chip Topography

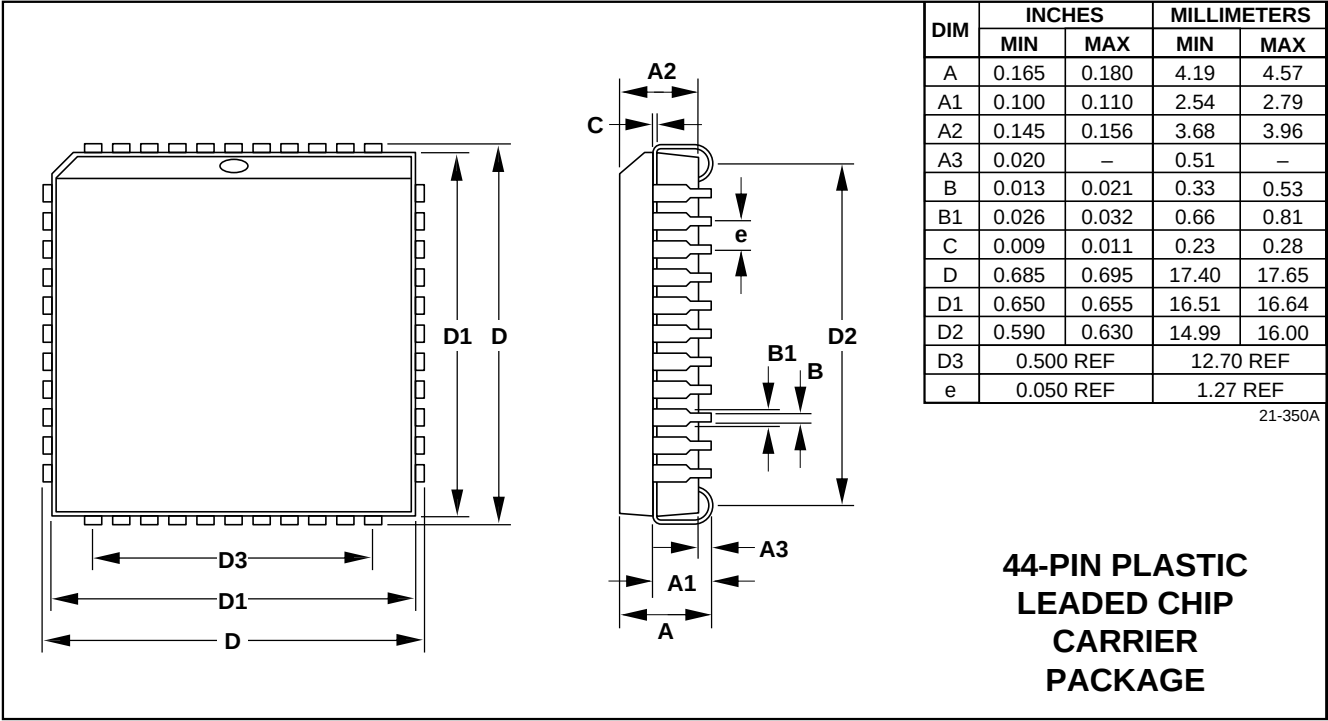


TRANSISTOR COUNT: 8987  
SUBSTRATE CONNECTED TO  $V_{DD}$

# Octal, 13-Bit Voltage-Output DAC with Parallel Interface

## Package Information

MAX547



# *Octal, 13-Bit Voltage-Output DAC with Parallel Interface*

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