CS1680

Dimmable LED Driver IC for Low-voltage Lighting

Features

- Best-in-class Transformer Compatibility
  - Magnetic Transformers
  - Electronic Transformers
- Best-in-class Dimmer Compatibility
  - Leading-edge (TRIAC) Dimmers
  - Trailing-edge Dimmers
- High Efficiency
  - Up to 80% for CS1680-00 Applications
  - Up to 83% for CS1680-02 Applications
- Flicker-free Dimming
- 5% Minimum Dimming Level
- Cascade Boost-buck Topology with Constant-current Output
  - CS1680-00 Output Voltage <15V
  - CS1680-02 Output Voltage <21V
- Fast Startup
- Tight LED Current Regulation: Better than ±10%
- >0.9 Power Factor on Magnetic Transformers
- Soft Start
- Protections:
  - Output Open/Short
  - Boost Overvoltage
  - Overcurrent Detection
  - External Overtemperature Using NTC

Overview

The CS1680 is a cascade boost-buck dimmable LED driver for the 12V halogen lamp-replacement market. The CS1680 uses a Cirrus Logic proprietary intelligent digital control that provides exceptional single-lamp and multi-lamp transformer compatibility for non-dimmer systems and dimmer systems paired with electronic and magnetic low-voltage transformers.

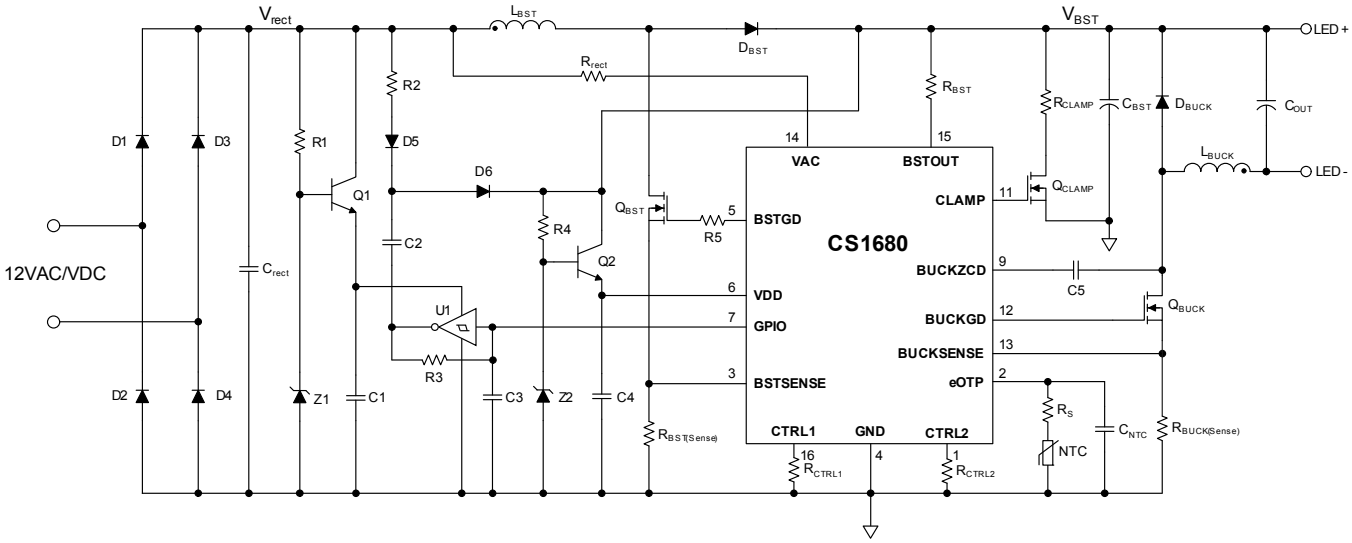
The CS1680 integrates a continuous conduction mode (CCM) boost converter that provides transformer compatibility and dimmer compatibility. An adaptive digital algorithm controls the boost stage and dimmer compatibility operation mode to enable flicker-free operation down to 5% output current with leading-edge and trailing-edge dimmers.

Applications

- MR16 Lamps
- All 12VAC/VDC Low-voltage Lighting Applications

Ordering Information

See **page 15**.



1. INTRODUCTION

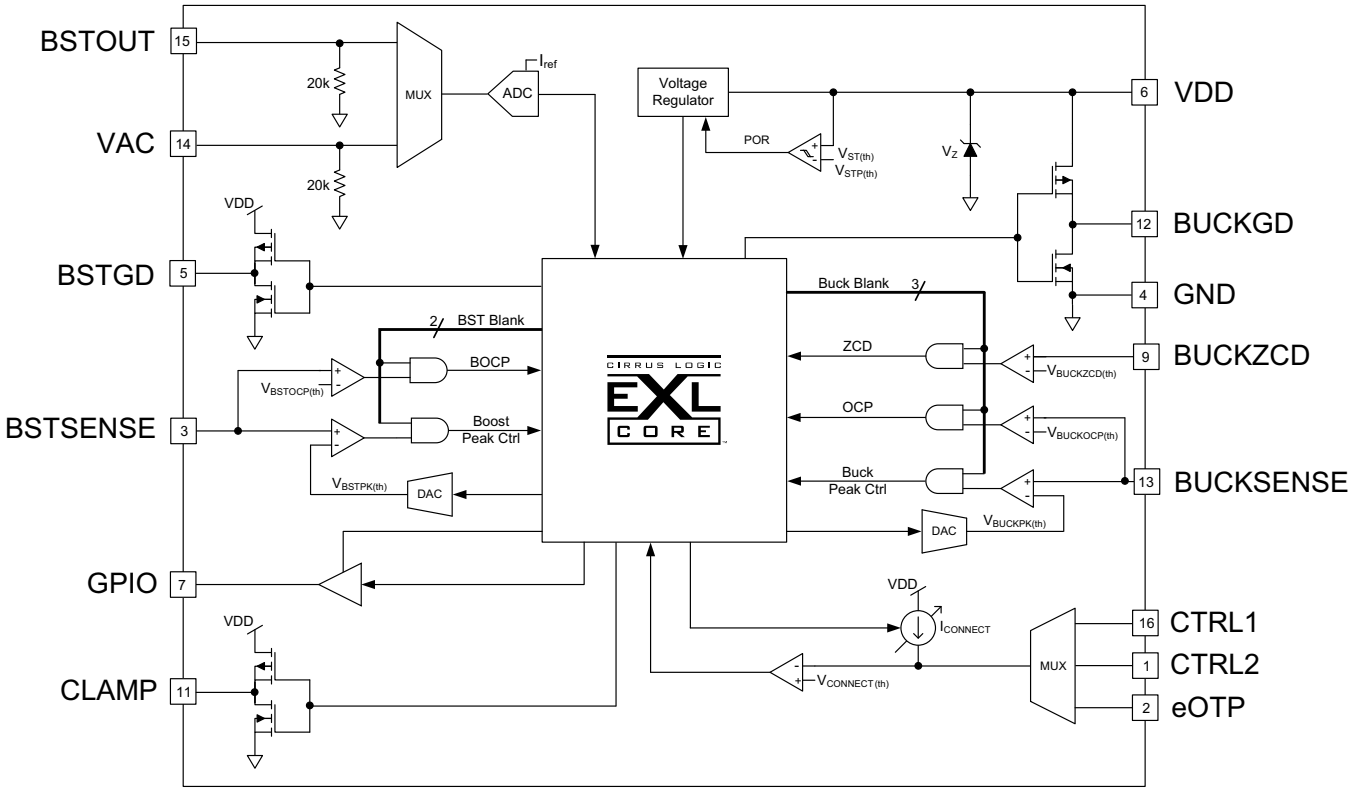


Figure 1. CS1680 Block Diagram

A typical schematic using the CS1680 for boost-buck applications is shown on the previous page.

A startup circuit provides a low-impedance path to improve electronic transformer compatibility. The GPIO pin is used to disable the startup circuit when normal operation is reached.

The CS1680 power supply is connected to an external power supply network. A linear regulator at the output of the boost converter provides steady-state operating current to the IC. The rectified input voltage is sensed as a current into pin VAC and is used to control the adaptive transformer and dimmer compatibility algorithm and extract the phase of the input voltage for output dimming control.

During steady-state operation, the boost stage operates in continuous conduction mode (CCM) to boost the input voltage. This operation allows the boost stage to provide transformer and dimmer compatibility, reduces bulk capacitor ripple current, and provides a regulated input voltage to the buck stage.

The output voltage of the CCM boost is sensed by the current into the boost output voltage sense pin (BSTOUT). The buck stage is implemented with peak-current mode control. Voltage across an external user-selected resistor is sensed through pin BUCKSENSE to control the peak current through the buck stage inductor. Leading-edge blanking on pin BUCKSENSE prevents false triggering.

When an external negative temperature coefficient (NTC) thermistor is connected to the eOTP pin, the CS1680 monitors the system temperature, allowing the controller to reduce the output current of the system. If the temperature reaches a designated high set point, the IC is shutdown and stops switching.

2. PIN DESCRIPTION

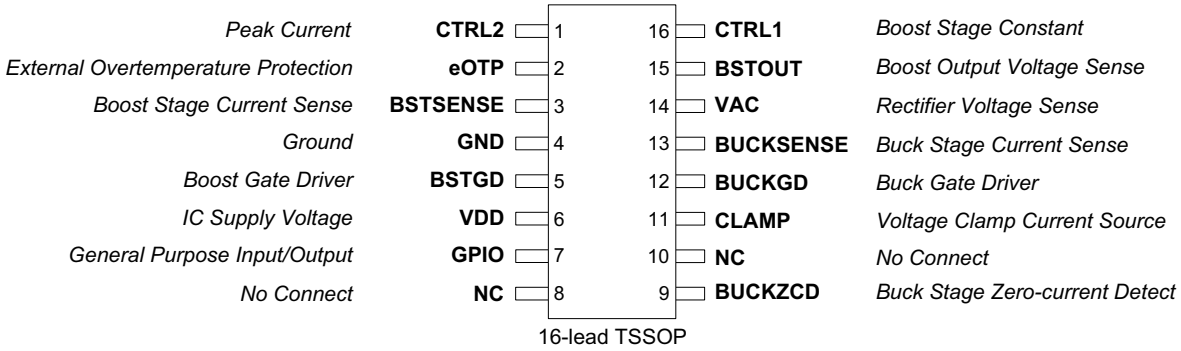


Figure 2. CS1680 Pin Assignments

Pin Name	Pin #	I/O	Description
CTRL2	1	IN	**Peak Current** — Connect a resistor to this pin to set the comparator threshold to reflect the desired boost peak current in Trailing Edge Electronic Transformer Mode (Mode 2).
eOTP	2	IN	**External Overtemperature Protection** — Connect an external NTC thermistor to this pin, allowing the internal A/D converter to sample the change to NTC resistance.
BSTSENSE	3	IN	**Boost Stage Current Sense** — The current flowing in the boost stage FET is sensed across a resistor. The resulting voltage is applied to this pin and digitized for use by the boost stage computational logic to determine the FET duty cycle.
GND	4	PWR	**Ground** — Common reference. Current return for both the input signal portion of the IC and the gate driver.
BSTGD	5	OUT	**Boost Gate Driver** — Gate drive for the boost stage power FET.
VDD	6	PWR	**IC Supply Voltage** — Connect a storage capacitor to this pin to serve as a reservoir for operating current for the device, including the gate drive current to the power transistor.
GPIO	7	IN/OUT	**General Purpose Input/Output** — Used to drive the FET gate for the startup circuit.
NC	8	IN	**No Connect** — Leave pin not connected.
BUCKZCD	9	IN	**Buck Stage Zero-current Detect** — Buck stage inductor sensing input. The pin is connected to the drain of the buck stage power FET with a capacitor.
NC	10	IN	**No Connect** — Leave pin not connected.
CLAMP	11	OUT	**Voltage Clamp Current Source** — Connect to a voltage clamp circuit on the output of the boost stage.
BUCKGD	12	OUT	**Buck Gate Driver** — Gate drive for the buck stage power FET.
BUCKSENSE	13	IN	**Buck Stage Current Sense** — The current flowing in the buck stage FET is sensed across a resistor. The resulting voltage is applied to this pin and digitized for use by the buck stage computational logic to determine the FET duty cycle.
VAC	14	IN	**Rectifier Voltage Sense** — A current proportional to the rectified line voltage is fed into this pin. The current is measured with an A/D converter.
BSTOUT	15	IN	**Boost Output Voltage Sense** — A current proportional to the boost output is fed into this pin. The current is measured with an A/D converter.
CTRL1	16	IN	**Boost Stage Constant** — Connect a resistor to this pin to set the constant ratio for the boost stage current calculations in Leading Edge Electronic Transformer Mode (Mode 3).

3. CHARACTERISTICS AND SPECIFICATIONS

3.1 Electrical Characteristics

Typical characteristics conditions:
- T_A = 25 °C, V_{DD} = 12V, GND = 0 V
- All voltages are measured with respect to GND.
- Unless otherwise specified, all currents are positive when flowing into the IC.

Minimum/Maximum characteristics conditions:
- T_J = -40 °C to +125 °C, V_{DD} = 11 V to 17 V, GND = 0 V

Parameter	Condition	Symbol	Min	Typ	Max	Unit
VDD Supply Voltage						
Operating Range	After Turn-on	V_{DD}	11	-	17	V
Turn-on Threshold Voltage	V_{DD} Increasing	$V_{ST(th)}$	-	8.5	-	V
Turn-off Threshold Voltage (UVLO)	V_{DD} Decreasing	$V_{STP(th)}$	-	7.5	-	V
GPIO Low (Note 1)	$V_{DD} > V_{ST(th)}$	$K_{GPIO(low)}$	-	50.0	-	%
Zener Voltage (Note 2)	I_{DD} = 20 mA	V_Z	18.5	-	19.8	V
VDD Supply Current						
Startup Supply Current	$V_{DD} < V_{ST(th)}$	I_{ST}	-	-	1.0	mA
Operating Supply Current (Note 3)	C_L = 0.25 nF, $f_{sw} \leq$ 70 kHz		-	11	-	mA
Reference						
Reference Current		I_{ref}	-	64	-	µA
Clamp Gate Drive						
Output Source Resistance		$Z_{CLAMP(Source)}$	-	290	-	Ω
Output Sink Resistance		$Z_{CLAMP(Sink)}$	-	208	-	Ω
Boost Output Mode1 Algorithm						
Regulation Target (Notes 1, 4)		$K_{Mode1(target)}$	-	73.3	-	%
Boost Output Mode2 Mode Algorithm						
Regulation Target (Notes 1, 5)		$K_{Mode2(target)}$	-	78.4	-	%
Boost Output Mode3 Algorithm						
Regulation Range Low (Notes 1, 6) CS1680-00 CS1680-02		$K_{Mode3(low)}$	 - -	 60.0 65.9	 - -	 % %
Regulation Range High (Notes 1, 6)		$K_{Mode3(high)}$	-	82.0	-	%
Accelerated Decrease On CS1680-00 CS1680-02		$K_{DEC(on)}$	 - -	 52.2 60.4	 - -	 % %
Accelerated Increase On (Notes 1, 7) Accelerated Increase Off (Notes 1, 7)		$K_{CLAMP(on)}$ $K_{CLAMP(off)}$	- -	87.8 85.1	- -	% %
Boost Pulse Width Modulator						
Minimum On Time		$T1_{BST(min)}$	-	0.1	-	µs
Maximum On Time		$T1_{BST(max)}$	-	800	-	µs
Constant Off Time	Mode1	$T2_{BST(fixed)}$	-	0.5	-	µs
Minimum Off Time	Mode2 & Mode3	$T2_{BST(min)}$	-	0.2	-	µs
Maximum Off Time	Mode2 & Mode3	$T2_{BST(max)}$	-	0.9	-	µs
Minimum Switching Frequency			-	1.3	-	kHz
Maximum Switching Frequency			-	3.3	-	MHz

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Boost Gate Driver						
Output Source Resistance		$Z_{BST(Source)}$	-	19.9	-	Ω
Output Sink Resistance		$Z_{BST(Sink)}$	-	10.5	-	Ω
Rise Time	C_L = 0.25nF		-	11	-	ns
Fall Time	C_L = 0.25nF		-	6	-	ns
Boost Current Sense						
Peak Control Threshold		$V_{BSTPK(th)}$	-	0.33	-	V
Leading-edge Blanking		t_{BSTLEB}	-	100	-	ns
Delay to Output			-	-	100	ns
Boost Protection						
Overcurrent Protection (BOCP)		$V_{BSTOCP(th)}$	-	1.05	-	V
Overvoltage Protection (BOP) (Note 1)		K_{BOP}	-	93.75	-	%
Clamp Turn-on Clamp Turn-off		$K_{CLAMP(on)}$ $K_{CLAMP(off)}$	- -	87.8 85.1	- -	% %
Buck Zero-Current Detect						
BUCKZCD Threshold		$V_{BUCKZCD(th)}$	-	200	-	mV
BUCKZCD Blanking		$t_{BUCKZCD}$	-	250	-	ns
ZCD Sink Current (Note 8)		$I_{BUCKZCD}$	-2	-	-	mA
BUCKAUX Upper Voltage	$I_{BUCKZCD}$ = 1mA		-	V_{DD}+0.6	-	V
Buck Current Sense						
Peak Control Threshold		$V_{BUCKPK(th)}$	-	0.525	-	V
Leading-edge Blanking		$t_{BUCKLEB}$	-	250	-	ns
Delay to Output			-	-	100	ns
Buck Pulse Width Modulator						
Minimum On Time		$T1_{BUCK(min)}$	-	0.55	-	µs
Maximum On Time CS1680-00 CS1680-02		$T1_{BUCK(max)}$	 - -	 12.8 25.6	 - -	 µs µs
Minimum Switching Frequency			-	625	-	Hz
Maximum Switching Frequency			-	200	-	kHz
Buck Gate Driver						
Output Source Resistance		$Z_{BUCK(Source)}$	-	12.7	-	Ω
Output Sink Resistance		$Z_{BUCK(Sink)}$	-	8.2	-	Ω
Rise Time	C_L = 0.25nF		-	7.0	-	ns
Fall Time	C_L = 0.25nF		-	4.5	-	ns
Buck Protection						
Overcurrent Protection (OCP)		$V_{BUCKOCP(th)}$	-	1.05	-	V
External Overtemperature Protection (eOTP), Boost Stage Constant, Peak Current						
Maximum Pull-up Current Source		$I_{CONNECT}$	-	80	-	µA
Conductance Accuracy (Note 9)			-	-	±5	%
Conductance Offset (Note 9)			-	±250	-	nS
Current Source Voltage Threshold		$V_{CONNECT(th)}$	-	1.25	-	V

Parameter		Condition	Symbol	Min	Typ	Max	Unit
Internal Overtemperature Protection (iOTP)							
Thermal Shutdown Threshold	(Note 10)		T_{SD}	-	135	-	ºC
Thermal Shutdown Hysteresis	(Note 10)		$T_{SD(Hy)}$	-	14	-	ºC

Notes:
1. Threshold is characterized as a percentage of the full-scale boost output voltage, $V_{BST(full)}$
2. The CS1680 has an internal shunt regulator that limits the voltage on the VDD pin. V_Z, the shunt regulation voltage, is defined in the *VDD Supply Voltage* section on *page 4*.
3. For test purposes, load capacitance C_L is connected to gate drive pins and is equal to 0.25nF.
4. Mode1 algorithm regulates value at the trough of the rectified waveform.
5. Mode2 algorithm regulates boost output voltage at the phase cut of each rectified waveform.
6. LED output current begins changing if boost output voltage is outside the Mode3 algorithm regulation range.
7. Accelerated increase in LED output current begins at clamp on and continues until the boost output voltage falls to clamp off.
8. External circuitry should be designed to ensure that the ZCD current drawn from the internal clamp diode when it is forward biased does not exceed specification.
9. The conductance is specified in Siemens (S or 1/Ω). Each LSB of the internal ADC corresponds to 250nS or one parallel 4MΩ resistor. Full scale corresponds to 256 parallel 4MΩ resistors or 15.625kΩ.
10. Specifications are guaranteed by design and are characterized and correlated using statistical process methods.

3.2 Thermal Resistance

Symbol	Parameter		TSSOP	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance	2 Layer PCB 4 Layer PCB	138 103	°C/W °C/W
θ_{JC}	Junction-to-Case Thermal Impedance	2 Layer PCB 4 Layer PCB	44 28	°C/W °C/W

3.3 Absolute Maximum Ratings

Characteristics conditions:

All voltages are measured with respect to GND.

Pin	Symbol	Parameter		Value	Unit
6	V_{DD}	IC Supply Voltage		18.5	V
1, 2, 3, 8, 9, 10, 13, 14, 15, 16		Analog Input Maximum Voltage		-0.5 to (V_{DD}+0.5)	V
1, 2, 3, 8, 9, 10, 13, 14, 15, 16		Analog Input Maximum Current	(Note 11)	5	mA
5, 11, 12	V_{GD}	Gate Drive Output Voltage		-0.3 to (V_{DD}+0.3)	V
5, 11, 12	I_{GD}	Gate Drive Output Current		-1.0 / +0.5	A
-	P_D	Total Power Dissipation		100	mW
-	T_J	Junction Temperature Operating Range	(Note 12)	-40 to +125	°C
-	T_{Stg}	Storage Temperature Range		-65 to +150	°C
All Pins	ESD	Electrostatic Discharge Capability	Human Body Model Charged Device Model	2000 500	V V

Note:
11. Transient current of up to 170mA will not cause SCR latch-up
12. Long-term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation at the rate of 50 mW / °C for variation over temperature.

WARNING:

Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

4. TYPICAL PERFORMANCE PLOTS

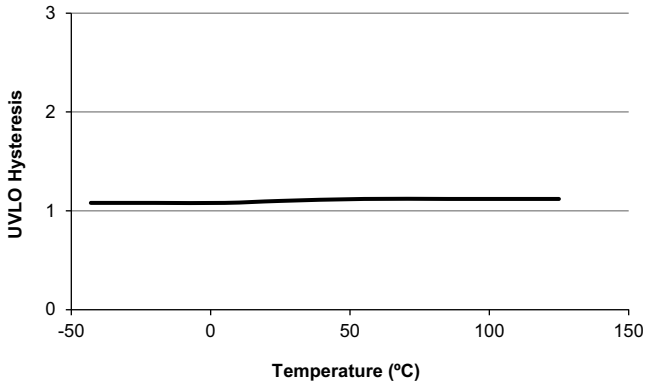


Figure 3. UVLO Characteristics

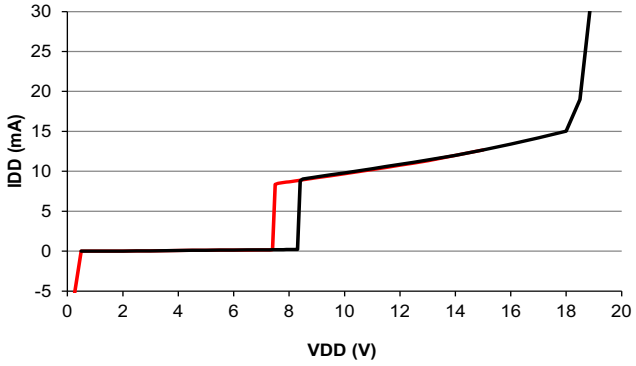


Figure 4. Supply Current vs. Voltage

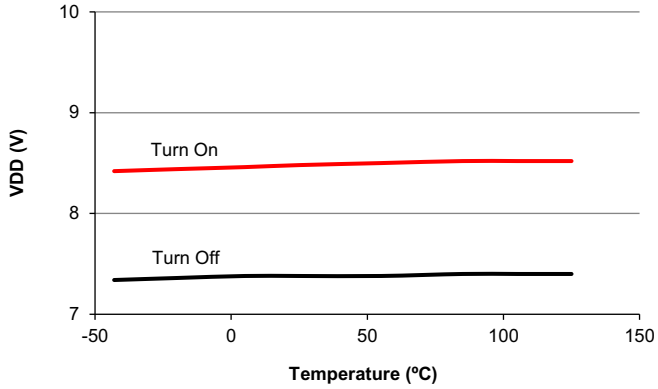


Figure 5. Turn On/Off Threshold Voltage vs. Temperature

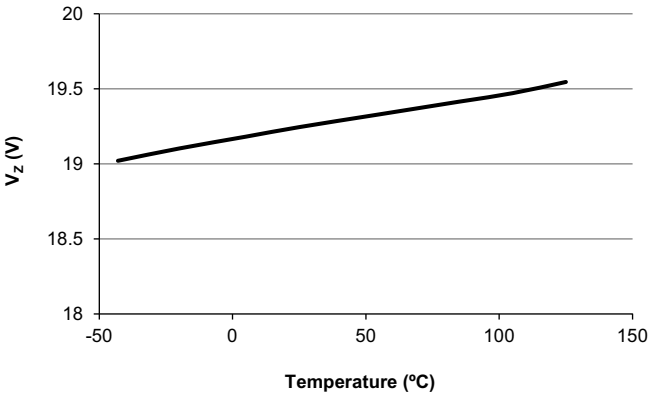


Figure 6. Zener Voltage vs. Temperature

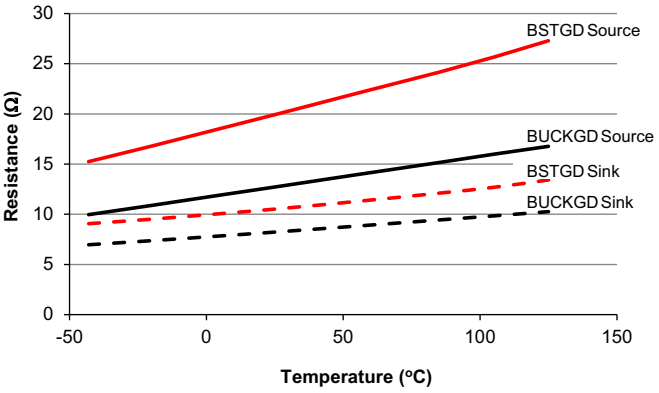


Figure 7. Gate Drive Resistance vs. Temperature

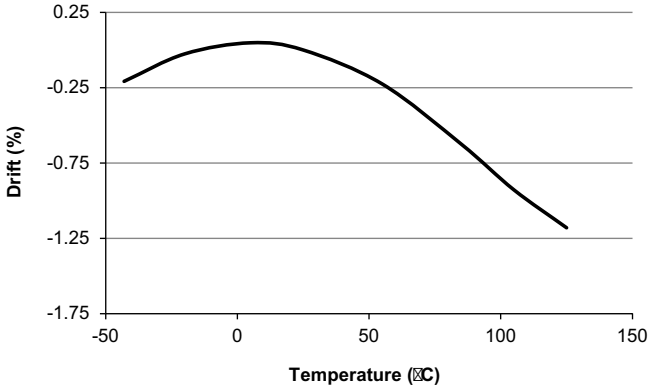


Figure 8. Reference Current I_{ref} Drift vs. Temperature

5. GENERAL DESCRIPTION

5.1 Overview

The CS1680 is a cascade boost-buck dimmable LED driver for the 12V halogen lamp-replacement market. The CS1680 uses a Cirrus Logic proprietary intelligent digital control that provides exceptional single-lamp and multi-lamp transformer compatibility for non-dimmer systems and dimmer systems paired with electronic and magnetic low-voltage transformers.

The CS1680 integrates a continuous conduction mode (CCM) boost converter that provides transformer compatibility and dimmer compatibility. An adaptive digital algorithm controls the boost stage and dimmer compatibility operation mode to enable flicker-free operation down to 5% output current with leading-edge and trailing-edge dimmers.

5.2 IC Startup and Power Supply

The startup circuit is constructed of a linear regulator and charge pump, and is used to supply a power-on voltage to the CS1680. The device provides a GPIO pin that is used to disable the startup circuit once the boost output voltage reaches 50% of full scale.

The linear regulator circuit uses transistor Q1 to provide a supply voltage to a Schmitt-trigger inverter which enables the charge pump circuit. The GPIO pin is tri-stated while the controller is held in reset due to low supply voltage. The charge pump increases the voltage until the device starts converting. Once the supply voltage V_{DD} exceeds threshold voltage $V_{ST(th)}$, the controller polls the boost output voltage for 50% of full scale before driving the GPIO pin low to disable the startup circuit.

5.3 Boost Stage

The boost stage in the CS1680 is a low-side asynchronous boost converter. Once the IC reaches its UVLO start threshold voltage $V_{ST(th)}$ and begins operating, the CS1680 executes a detection algorithm to set the operating state of the IC (see Table 1 on page 8). The boost stage utilizes a continuous current mode (CCM) control algorithm.

5.3.1 Dimmer Compatibility

The CS1680 dimmer switch detection algorithm determines if the solid-state lighting (SSL) system is controlled: first, using a regular switch or a leading-edge dimmer paired with a magnetic transformer, or a 12VAC/VDC source (Mode1); second, by a regular switch or a trailing-edge dimmer paired with an electronic transformer (Mode2); third, by a leading-edge dimmer paired with an electronic transformer (Mode3).

Boost Mode	Source	Line Switch	Digital Control Loop
Mode1	12 VAC/VDC	Non-dimming	Executes a boost peak-current algorithm with PFC based control.
	Magnetic Transformer	Leading-edge Dimmer	
		Non-dimming	
Mode2	Electronic Transformer	Trailing-edge Dimmer	Executes a constant boost peak-current algorithm during the turn-on time of the electronic transformer.
		Non-dimming	
Mode3	Electronic Transformer	Leading-edge Dimmer	Executes a constant power control algorithm where the boost inductor current is controlled by the instantaneous rectified voltage signal.

Table 1. Operating State

Dimmer switch detection is implemented using a process of elimination. The method of elimination progresses through the detection algorithm to find the best matching state of operation. In an attempt to find a dimmer compatible mode, the detection algorithm starts in Mode1, then tries Mode2, if Mode1 and Mode2 are excluded the algorithm defaults to Mode3.

Mode1

In Mode1, the detectable inputs are a leading-edge dimmer paired with a magnetic transformer, no dimmer switch paired with a magnetic transformer, or a 12VDC/VAC source. Upon detection of a magnetic transformer, the CS1680 operates in a PFC conduction mode where the device provides a power factor that is in excess of 0.9. The boost peak current I_{BSTPK} is modulated across the input voltage to follow a constant resistance. The target resistance is modulated to provide boost output regulation. The RMS input voltage is used to determine the output LED current as a fraction of full scale. If a DC input voltage is detected, the controller will set the LED output at 100% of the available RMS energy.

The boost output voltage V_{BST} is measured at the trough of the rectified voltage every half-line cycle and compared against the regulation point, which is set by resistor R_{BST} (see Figure 11 on page 10). The voltage difference, the setting of LED output current I_{OUT}, and the clamp activity are used in the control loop to scale the boost inductor current allowing the boost output

voltage to reach the regulation target set by constant $K_{Mode1(target)}$. If boost output voltage V_{BST} is below the target regulation point or the boost output voltage is falling, the boost inductor current is increased. If the boost output voltage is above the target regulation point, the boost output voltage is rising, or the clamp has been activated recently the boost current is decreased. The LED output current is set using a third-order polynomial of the rectified RMS voltage, computed over a half-line cycle and filtered to avoid lamp flicker.

Mode 2

In Mode 2, the CS1680 will detect if the input is a trailing edge dimmer paired with an electronic transformer or no dimmer switch paired with an electronic transformer. The detection algorithm determines its operation based on the falling edge of the input voltage waveform. To provide proper dimmer operation, the CS1680 executes the boost algorithm on the falling edge of the input line voltage, which will maintain a charge in the dimmer capacitor. To ensure maximum compatibility with dimmer components, the device boosts during this falling edge event using a peak current that must meet a minimum value.

The boost output voltage V_{BST} is measured at the trailing edge of the rectified voltage every half-line cycle and compared against the regulation point, which is set by resistor R_{BST} (see Figure 11 on page 10). The voltage difference, the setting of LED output current I_{OUT}, and the clamp activity are used in the control loop to modulate the boost turn-on time every half-line cycle which allows the boost output voltage to reach the regulation target set by constant $K_{Mode2(target)}$. If boost output voltage V_{BST} is below the target regulation point or the boost output voltage is falling, the total turn-on time over a half-line cycle is increased. If the boost output voltage is above the target regulation point, the boost output voltage is rising, or the clamp has been activated recently, the total turn-on time over a half-line cycle is decreased. The Mode 2 algorithm estimates the turn-on time of the transformer by measuring the conduction angle of the rectified voltage every half-line cycle. The LED output current is set based on the output power requirements for a particular conduction angle by the regulation loop.

Mode 3

In Mode 3, the CS1680 will detect if the input is a leading edge dimmer paired with an electronic transformer. The CS1680 regulates boost output voltage V_{BST} while maintaining the dimmer phase angle. The device executes a CCM boost algorithm that keeps the boost peak current inversely proportional to the boost output voltage. The algorithm attempts to maintain a constant power while limiting the boost peak current to prevent saturating the boost inductor.

The Mode 1 and Mode 2 algorithms use properties of the input waveform on a cycle-by-cycle basis to determine the output current, and then adjusts the boost control parameters to balance the input power with the requested output power. Unlike the Mode 1 and Mode 2 algorithms, the Mode 3 algorithm leaves the boost parameters fixed and adjusts the output current to balance input power and output power. As long as boost output voltage V_{BST} remains between the voltage thresholds set by lower regulation range constant $K_{Mode3(low)}$ and higher regulation range constant $K_{Mode3(high)}$, the LED output current I_{OUT} will remain constant (see Figure 9).

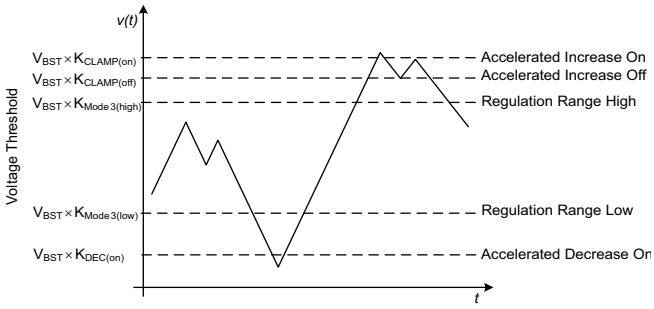


Figure 9. Mode 3 Output Regulation Algorithm

If the boost output voltage V_{BST} rises above the regulation range high voltage threshold set by constant $K_{Mode3(high)}$ (due to the phase angle of the dimmer increasing which allows for the first stage to produce additional power), LED output current I_{OUT} is gradually increased until the boost output voltage V_{BST} falls below the regulation range high threshold. The rate of increase continues to add larger steps as long as boost output voltage V_{BST} stays above the regulation high threshold. If the boost output voltage continues to rise and reaches the clamp-on threshold set by constant $K_{CLAMP(on)}$, the clamp circuit will activate to dissipate the excess power from the boost output. While the clamp is on, the LED output current I_{OUT} increases at an accelerated rate.

If the boost output voltage V_{BST} falls below the regulation range low voltage threshold set by constant $K_{Mode3(low)}$, LED output current I_{OUT} is gradually decreased. The rate of decrease continues to subtract larger steps as long as the boost output voltage stays below the regulation range low threshold. If the

boost output voltage continues to fall and reaches the lowest threshold set by constant $K_{DEC(on)}$, the LED output current is decreased at an accelerated rate.

If the LED output current I_{OUT} is at a maximum and boost output voltage V_{BST} is still above the regulation high threshold, the controller begins scaling down the boost inductor current instead of increasing the LED output current. If this happens, when the boost output voltage falls below the regulation low threshold, the boost input current is gradually increased back to nominal before the LED output current begins to reduce off from the maximum.

5.3.2 Boost Stage Control

The boost stage uses continuous conduction mode operation for high compatibility with electronic transformers. For current regulation, the controller varies the peak current I_{BSTPK} as necessary for dimmer and transformer compatibility. When the dimmer is paired with an electronic transformer, period $T2_{BST}$ is modulated to maintain a constant ripple current on the boost inductor. When the dimmer is paired with a magnetic transformer, the demagnetization period has a constant $T2_{BST(fixed)}$ time.

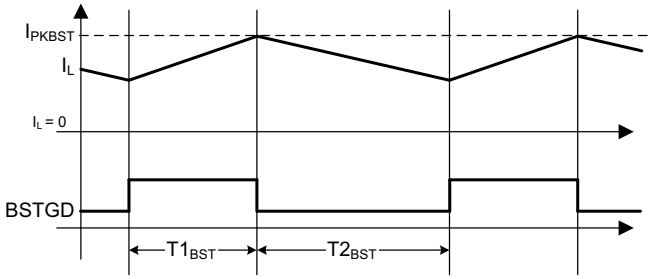


Figure 10. Continuous Conduction Mode Operation

Maximum Peak Current

The maximum boost inductor peak current $I_{BSTPK(max)}$ is set using the current sense resistor $R_{BST(Sense)}$ on pin BSTSENSE, which is sampled by a comparator referenced to an internal DAC. Boost peak current $I_{BSTPK(max)}$ is calculated using Equation 1:

$$I_{BSTPK(max)} = \frac{V_{BSTPK(th)}}{R_{BST(Sense)}} \quad \text{[Eq.1]}$$

Boost overcurrent protection (BOCP) is provided using a higher threshold to detect the event of inductor saturation. If the voltage on the BSTSENSE pin exceeds a threshold voltage $V_{BSTOCP(th)}$ of 1.05V, the controller enters a BOCP fault. The IC output is disabled, the gate drive output pins BSTGD and BUCKGD turn off, and the controller attempts to restart after one second. The boost overcurrent protection current $I_{BSTPK(OCP)}$ is calculated using Equation 2:

$$I_{BSTPK(OCP)} = \frac{V_{BSTOCP(th)}}{R_{BST(Sense)}} \quad \text{[Eq.2]}$$

Output BSTOUT Sense and Input VAC Sense

A current proportional to boost output voltage V_{BST} is supplied to the IC on pin BSTOUT and is used as a control signal (see Figure 11). The ADC is used to measure the magnitude of current I_{BSTOUT} through resistor R_{BST}. The magnitude of current I_{BSTOUT} is then compared to an internal full scale reference current I_{ref} of 64 µA.

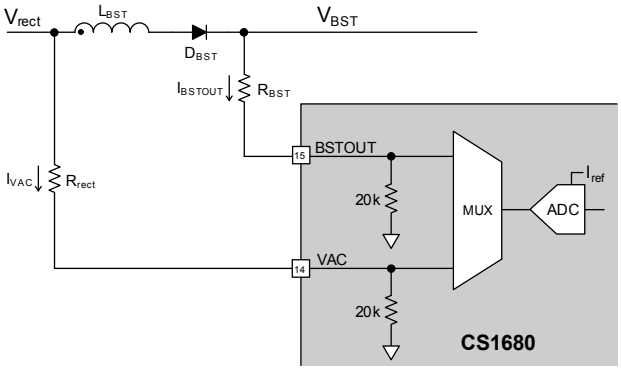


Figure 11. VAC and BSTOUT Input Pin Model

Resistor R_{BST} sets the system full-scale voltage and determines boost output voltage V_{BST} regulation, boost overvoltage protection, and clamp behavior. Full-scale voltage $V_{BST(full)}$ is calculated using Equation 3:

$$V_{BST(full)} = I_{ref} \times (R_{BST} + 20k\Omega) \quad \text{[Eq.3]}$$

The CS1680-00 is designed for a resistor R_{BST} equal to 604 kΩ, creating a full-scale voltage of 40V. The CS1680-02 is designed for a resistor R_{BST} equal to 560 kΩ, creating a full-scale voltage of 37V.

A current proportional to the AC/DC input voltage is supplied to the IC on pin VAC and is used by the boost control algorithm. Dimmer detection and dim level calculations are dependent on specific levels of the line voltage. Resistor R_{rec} is required to be set equal to 604 kΩ.

For optimal performance, resistors R_{rect} and R_{BST} should use 1% or better resistors for best voltage accuracy.

Boost Overvoltage Protection

The CS1680 supports boost overvoltage protection (BOP) to protect bulk capacitor C_{BST} (see Figure 13 on

page 11). If the boost output voltage exceeds the overvoltage protection threshold, a BOP fault signal is generated. Boost overvoltage threshold $V_{BOP(th)}$ is calculated using Equation 4:

$$V_{BOP(th)} = V_{BST(full)} \times K_{BOP} \quad [Eq.4]$$

For a nominal system design where resistor R_{BST} equals 604kΩ and full-scale voltage $V_{BST(full)}$ equals 40V, this sets threshold voltage $V_{BOP(th)}$ to 37.4V.

The control logic continuously averages this BOP fault signal, and if at any point in time the average exceeds a set event threshold, the boost stage is disabled.

5.3.3 Voltage Clamp Circuit

During transient events and interactions with electronic transformers, it is possible for the boost stage to generate more power than is consumed by the second stage. A clamping circuit is added to the system to dissipate the excess power. The CS1680 provides active clamp circuitry on pin CLAMP, as shown in Figure 12.

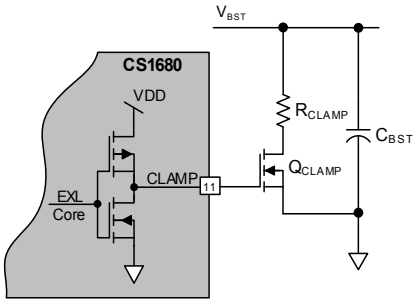


Figure 12. CLAMP Pin Model

The clamp circuit is enabled when boost output voltage V_{BST} exceeds the clamp turn-on threshold voltage $V_{CLAMP(on)}$. The clamp circuit will remain turned on until boost output voltage V_{BST} is lowered below the clamp turn-off threshold voltage $V_{CLAMP(off)}$. Threshold voltage $V_{CLAMP(on)}$ is calculated using Equation 5:

$$V_{CLAMP(on)} = V_{BST(full)} \times K_{CLAMP(on)} \quad [Eq.5]$$

Threshold voltage $V_{CLAMP(off)}$ is calculated using Equation 6:

$$V_{CLAMP(off)} = V_{BST(full)} \times K_{CLAMP(off)} \quad [Eq.6]$$

Clamp Overpower Protection

The CS1680 clamp overpower protection (COP) control logic continuously monitors the turn-on time of the clamp circuit. If the cumulative turn-on time exceeds 200ms during the internally generated 2-second window time, a COP event is actuated, disabling the boost and buck stages. The clamp circuitry is turned off during the fault event.

5.4 Buck Stage

The second stage is a current-regulated buck converter, delivering the highest possible efficiency at a constant current while minimizing line frequency ripple. A buck stage is illustrated in Figure 13. Primary-side control is used to simplify system design and reduce system cost and complexity.

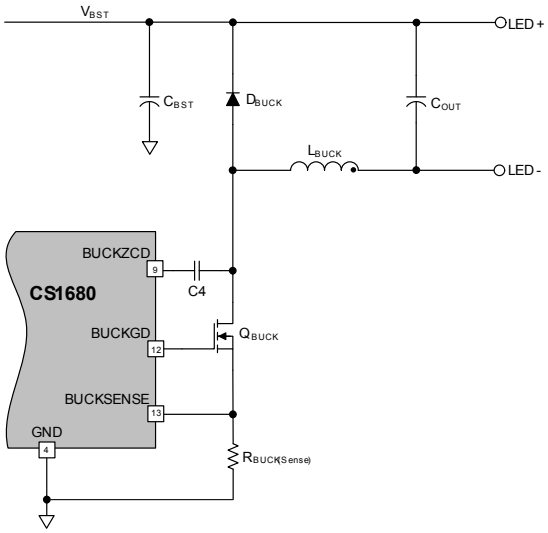


Figure 13. Buck Model

When operating with a dimmer, the dimming signal is extracted in the time domain and is proportional to the conduction angle of the dimmer. A control variable is passed to the second stage to achieve 5% to 100% output currents.

The buck stage control parameters assures the LED current remains constant despite a ±10% line voltage variation (line regulation), and the LED current remains constant over a ±20% variation in buck inductor inductance.

5.4.1 Buck Inductor Model

The BUCKSENSE input is used to sense the buck inductor current. When the current reaches a certain threshold, the gate drive turns off (output on pin BUCKGD). The sensed current and internal calculation are used to determine the switching period TT_{BUCK}. The zero-current detect input on pin BUCKZCD is used to determine the buck inductor zero-crossing

period $T2_{BUCK}$. The controller then uses the time TT_{BUCK} to determine gate turn-on time.

5.4.2 Current Sense Resistor Model

The digital algorithm ensures monotonic dimming from 5% to 100% of the dimming range with a linear relationship between the dimming signal and the LED current. The buck stage is regulated by peak current control with a 1% external sense resistor $R_{BUCK(Sense)}$ connected to the BUCKSENSE pin. Buck peak current $I_{BUCKPK(max)}$ is calculated using Equation 7:

$$I_{BUCKPK(max)} = \frac{V_{BUCKPK(th)}}{R_{BUCK(Sense)}} \quad \text{[Eq.7]}$$

Overcurrent protection (OCP) is implemented by monitoring the voltage across buck sense resistor $R_{BUCK(Sense)}$. If this voltage exceeds a threshold voltage $V_{BUCKOCP(th)}$ of 1.05 V, a fault condition occurs. The IC output is disabled, the gate drive output pins BSTGD and BUCKGD turn off, and the controller attempts to restart after one second. The buck overcurrent protection current $I_{BUCKPK(OCP)}$ is calculated using Equation 8:

$$I_{BUCKPK(OCP)} = \frac{V_{BUCKOCP(th)}}{R_{BUCK(Sense)}} \quad \text{[Eq.8]}$$

5.4.3 Zero-current Detection

Zero-current switching is achieved by detecting the buck inductor current zero-crossing using a capacitive coupling network. The digital control algorithm rejects line-frequency ripple created on the second-stage input by the front-end boost stage, resulting in the highest possible LED efficiency and long LED life.

5.5 Overtemperature Protection

The CS1680 incorporates both internal overtemperature protection (iOTP) and the ability to connect an external overtemperature sense circuit for IC protection. Typically, a negative temperature coefficient (NTC) thermistor is used.

5.5.1 Internal Overtemperature Protection

Internal overtemperature protection (iOTP) is activated, and switching is disabled when the die temperature of the devices exceeds 135°C. There is a hysteresis of about 14°C before resuming normal operation.

5.5.2 External Overtemperature Protection

The external overtemperature protection (eOTP) pin is used to implement overtemperature protection. A negative temperature coefficient (NTC) thermistor resistive network is connected to pin eOTP, usually in the form of a series combination of a resistor R_S and a thermistor R_{NTC} (see Figure 14). The CS1680 cyclically samples the resistance connected to pin eOTP.

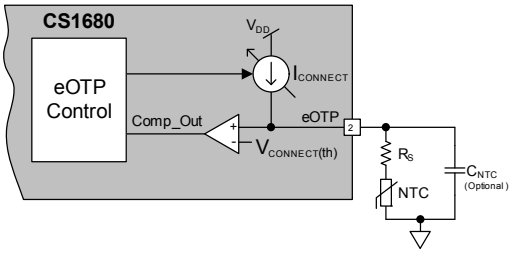


Figure 14. eOTP Functional Diagram

The total resistance on the eOTP pin gives an indication of the temperature and is used in a digital feedback loop to adjust current $I_{CONNECT}$ into the NTC thermistor and series resistor R_S to maintain a constant reference voltage $V_{CONNECT(th)}$ of 1.25V. Current $I_{CONNECT}$ is generated from a controlled current source with a full-scale current of 80µA. When the loop is in equilibrium, the voltage on pin eOTP fluctuates around voltage $V_{CONNECT(th)}$. A resistance ADC is used to generate $I_{CONNECT}$. The ADC output is filtered to suppress noise and compared against a reference that corresponds to 125°C. A second low-pass filter with a time constant of two seconds filters the ADC output and is used to scale down the internal dim level of the system (and hence LED current I_{LED}) if the temperature exceeds 95°C. The large time constant for this filter ensures that the dim scaling does not happen spontaneously and is not noticeable (suppress spurious glitches). The eOTP tracking circuit is designed to function accurately with external capacitance up to 470pF.

The tracking range of this resistance ADC is approximately 15.5kΩ to 4MΩ. The series resistor R_S is used to adjust the resistance of the NTC thermistor to fall within the ADC tracking range, allowing the entire dynamic range of the ADC to be well used. The CS1680 recognizes a resistance (R_S+R_{NTC}) equal to 20.3kΩ, which corresponds to a temperature of 95°C, as the beginning of an overtemperature dimming event and starts reducing the power dissipation. The output current is scaled until the series resistance (R_S+R_{NTC}) value reaches 16.6kΩ (125°C). Beyond this temperature, the IC enters a fault state and shuts down. This fault state is a latched protection state, and the fault state is not cleared until the power to the IC is recycled.

When exiting reset, the chip enters startup and the ADC quickly (<15ms) tracks the external temperature to check if it is below 120°C reference code before the controller is powered up. If this check fails, the chip will wait until this condition becomes true before initializing the rest of the system; that is, until the resistance ($R_S + R_{NTC}$) rises above 17.02kΩ.

For example, a 14kΩ (±1% tolerance) series resistor is required to allow measurements of up to 130°C to be within the eOTP tracking range when a 100kΩ NTC with a Beta of 4275. If the temperature exceeds 95°C, thermistor R_{NTC} is approximately 6.3kΩ and series resistor R_S is 14kΩ, so the eOTP pin has a total resistance of 20.3kΩ. The eOTP pin initiates protective dimming action by reducing the power dissipation. At 125°C, the thermistor R_{NTC} has 2.6kΩ plus a series resistor R_S equal to 14kΩ present a resistance of 16.6kΩ at the eOTP pin reaching the point where a thermal shutdown fault intervenes. The CS1680 fault state is not cleared until the power to the IC is recycled (see Figure 15).

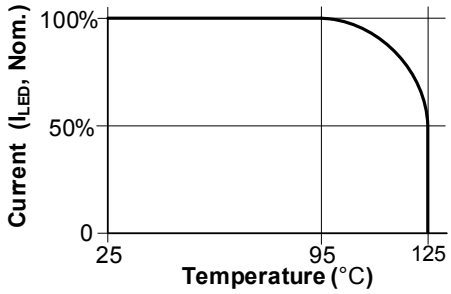
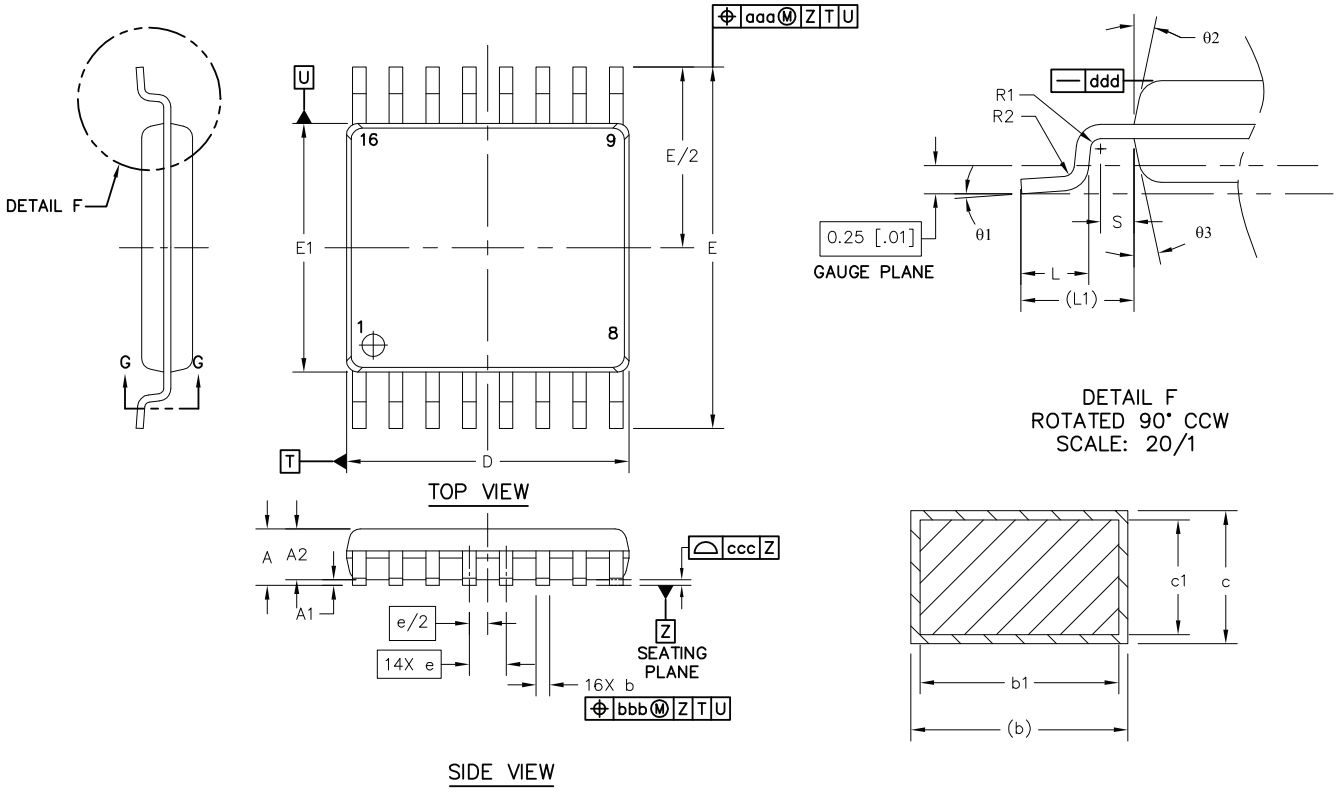


Figure 15. LED Current vs. eOTP Temperature

If the external overtemperature protection feature is not required, connect the eOTP pin to GND using a 50kΩ-to-500kΩ resistor to disable the eOTP feature.

6. PACKAGE DRAWING

16L TSSOP (170 MIL BODY) PACKAGE DRAWING



	mm			inch		
Dimension	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	--	--	1.1	--	--	0.043
A1	0.05	--	0.15	0.002	--	0.006
A2	0.85	--	0.95	0.033	--	0.037
b	0.19	--	0.27	0.007	--	0.011
b1	0.19	--	0.25	0.007	--	0.010
c	0.13	--	0.18	0.005	--	0.007
c1	0.09	--	0.14	0.004	--	0.006
D	4.9	5	5.1	0.193	0.197	0.201
E1	4.3	4.4	4.5	0.169	0.173	0.177
E	6.3	6.4	6.5	0.248	0.252	0.256
e		0.65BSC			0.026BSC	
L	0.5	0.6	0.7	.020	0.024	0.028
L1		1REF			0.039REF	
Θ1	0°	--	8°	0°	--	8°
Θ2		12°TYP			12°TYP	
Θ3		12°TYP			12°TYP	
R1	0.09	--	--	0.004	--	--

	mm			inch		
Dimension	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
R2	0.09	--	--	0.004	--	--
S	0.2	--	--	0.008	-	--
aaa	0.2			0.008		
bbb	0.1			0.004		
ccc	0.1			0.004		
ddd	0.05			0.002		

Notes:

1. Controlling dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M.
3. This drawing conforms to JEDEC outline MS-012, variation AC for standard 16L TSSOP narrow body.
4. Recommended reflow profile is per JEDEC/IPC J-STD-020.

7. ORDERING INFORMATION

Ordering Number		AC Line Voltage	Temperature	Package Description	Configuration Version
CS1680-FZZ	Bulk	12VAC/VDC	-40 °C to +125 °C	16-lead TSSOP, Lead (Pb) Free	3.09.1
CS1680-FZZR	Tape & Reel				3.09.1
CS168002-FZZ	Bulk	12VAC/VDC	-40 °C to +125 °C	16-lead TSSOP, Lead (Pb) Free	3.07.2
CS168002-FZZR	Tape & Reel				3.07.2

8. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Part Number	Peak Reflow Temp	MSL Rating[a]	Max Floor Life[b]
CS1680-FZZ	260 °C	3	7 Days
CS168002-FZZ	260 °C	3	7 Days

a. MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.
b. Stored at 30°C, 60% relative humidity.

REVISION HISTORY

Revision	Date	Changes
PP1	JAN 2014	Content updates for revision B silicon
PP2	FEB 2014	Content update for configuration version 3.07.2
F1	OCT 2014	Final release

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For all product questions and inquiries contact a Cirrus Logic Sales Representative.
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