

# BUK9Y30-75B

## N-channel TrenchMOS logic level FET

Rev. 04 — 10 April 2008

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Q101 compliant
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V, 24 V and 42 V loads
- General purpose power switching
- Automotive systems
- Motors, lamps and solenoids

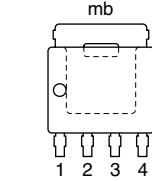
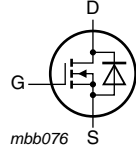
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	75	V
$I_D$	drain current	$V_{GS} = 5\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> and <a href="#">4</a>	-	-	34	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	85	W
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 34\text{ A}$ ; $V_{sup} \leq 75\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped	-	-	78	mJ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 5\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 60\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 14</a>	-	9	-	nC
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$ ; $I_D = 15\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	25	30	m $\Omega$

## 2. Pinning information

**Table 2. Pinning**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>SOT669 (LPAK)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK9Y30-75B	LPAK	plastic single-ended surface-mounted package (LPAK); 4 leads	SOT669

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	75	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$ ; $T_{mb} \geq 25\text{ °C}$ ; $T_{mb} \leq 175\text{ °C}$	-	75	V
$V_{GS}$	gate-source voltage		-15	15	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 1</a> and <a href="#">4</a>	-	34	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 1</a>	-	24	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; see <a href="#">Figure 4</a>	-	137	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	85	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C

### Source-drain diode

$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	34	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	137	A

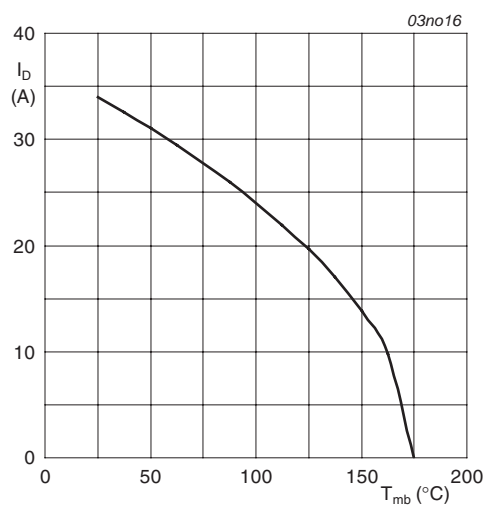
### Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 34\text{ A}$ ; $V_{sup} \leq 75\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped	-	78	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see <a href="#">Figure 3</a>	<a href="#">[1]</a> <a href="#">[2]</a> <a href="#">[3]</a>	-	J

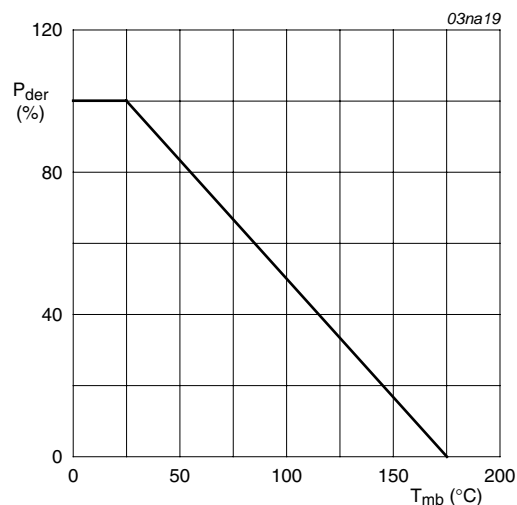
[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[2] Repetitive avalanche rating limited by average junction temperature of 170 °C.

[3] Refer to application note AN10273 for further information.

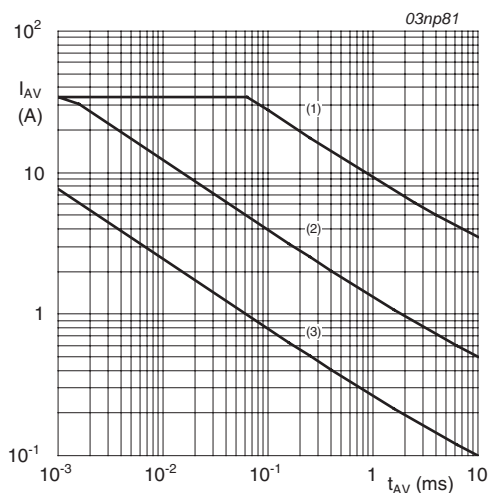

 $V_{GS} \geq 5 \text{ V}$ 

**Fig 1. Normalized continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



(1) Single-pulse;  $T_j = 25^\circ\text{C}$ .

(2) Single-pulse;  $T_j = 150^\circ\text{C}$ .

(3) Repetitive.

**Fig 3. Single-shot and repetitive avalanche rating; avalanche current as a function of avalanche period**

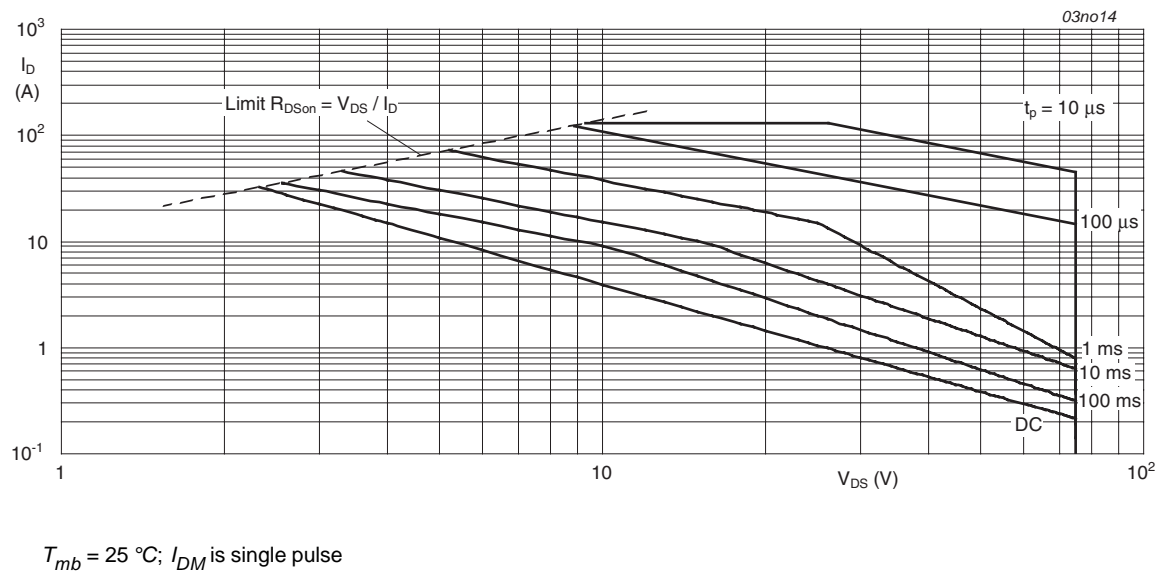


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 5</a>	-	-	1.8	K/W

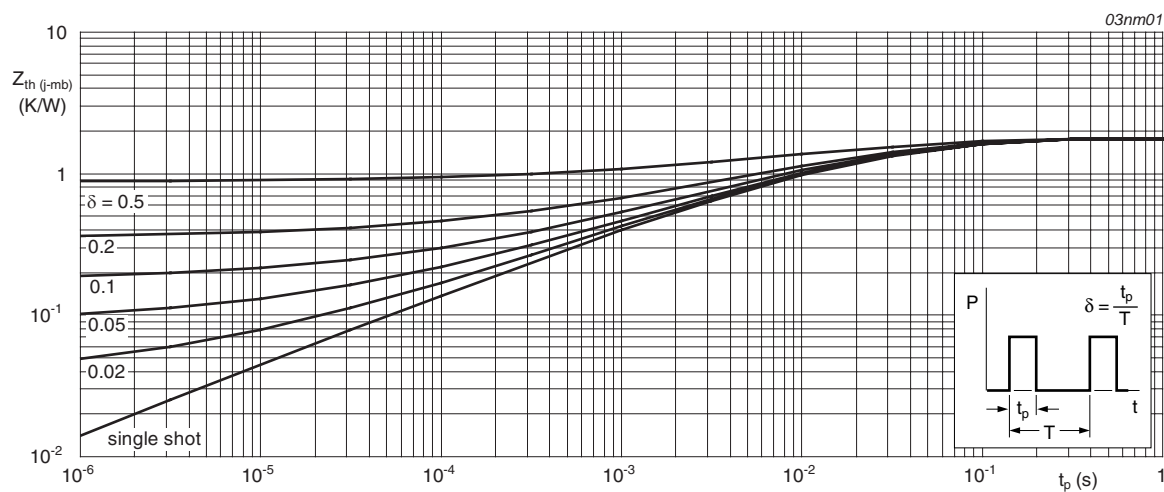


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	75	-	-	V
		I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	70	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 175 °C; see <a href="#">Figure 11</a>	0.5	-	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; see <a href="#">Figure 11</a>	1.1	1.5	2	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = -55 °C; see <a href="#">Figure 11</a>	-	-	2.3	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 75 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	-	500	μA
		V <sub>DS</sub> = 75 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.02	1	μA
I <sub>GSS</sub>	gate leakage current	V <sub>DS</sub> = 0 V; V <sub>GS</sub> = +15 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>DS</sub> = 0 V; V <sub>GS</sub> = -15 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 25 °C	-	-	34	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 175 °C; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	-	72	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C	-	27	32	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	25	30	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 25 °C	-	23	28	mΩ
Source-drain diode						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 16</a>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs;	-	101	-	ns
Q <sub>r</sub>	recovered charge	V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 30 V; T <sub>j</sub> = 25 °C	-	115	-	nC
Dynamic characteristics						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 60 V; V <sub>GS</sub> = 5 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 14</a>	-	19	-	nC
Q <sub>GS</sub>	gate-source charge		-	5	-	nC
Q <sub>GD</sub>	gate-drain charge		-	9	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V;	-	1550	2070	pF
C <sub>oss</sub>	output capacitance	f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 15</a>	-	150	179	pF
C <sub>rss</sub>	reverse transfer capacitance		-	60	80	pF

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\text{ }\Omega;$	-	16	-	ns
$t_r$	rise time	$V_{GS} = 5\text{ V}; R_{G(ext)} = 10\text{ }\Omega;$	-	106	-	ns
$t_{d(off)}$	turn-off delay time	$T_j = 25\text{ }^\circ\text{C}$	-	51	-	ns
$t_f$	fall time		-	83	-	ns

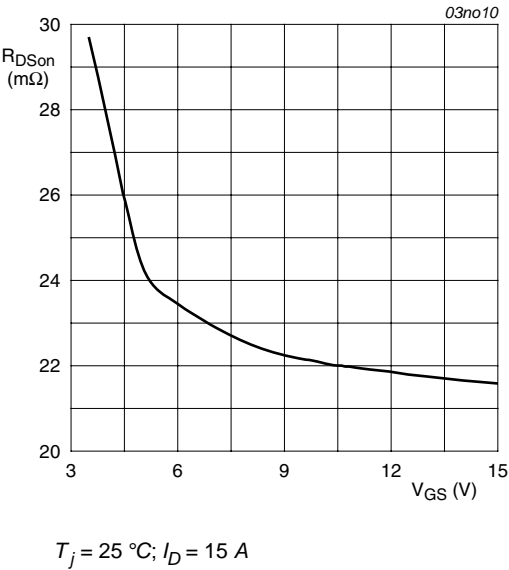


Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

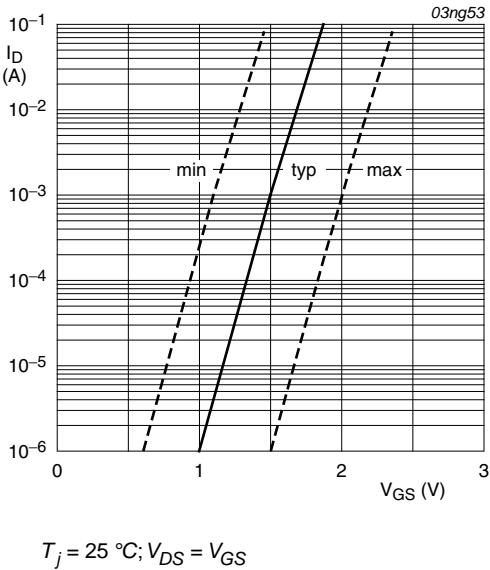


Fig 7. Sub-threshold drain current as a function of gate-source voltage

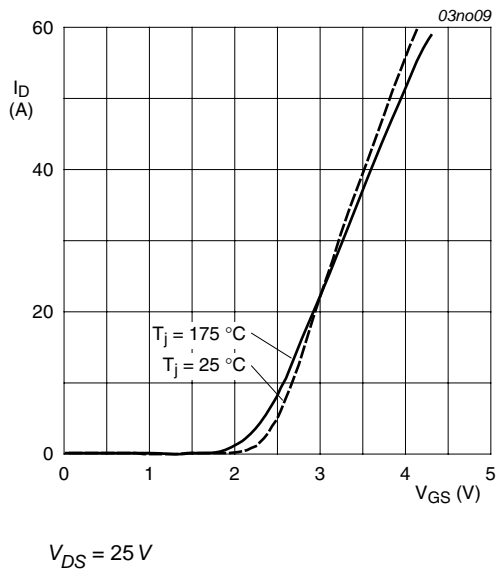


Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

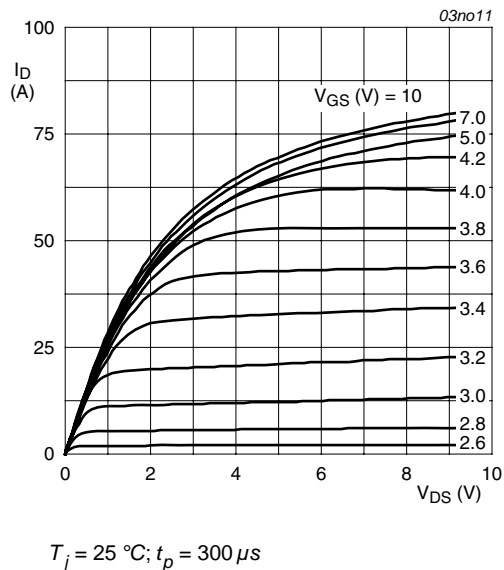


Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values

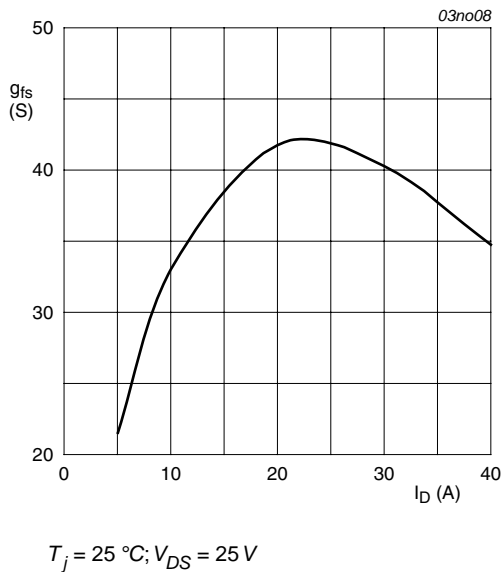


Fig 10. Forward transconductance as a function of drain current; typical values

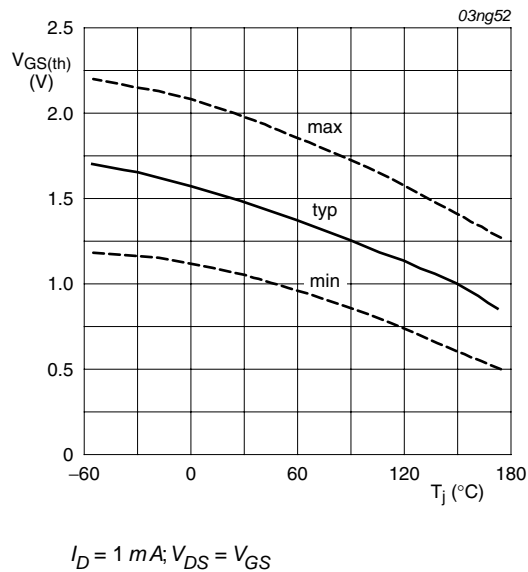


Fig 11. Gate-source threshold voltage as a function of junction temperature

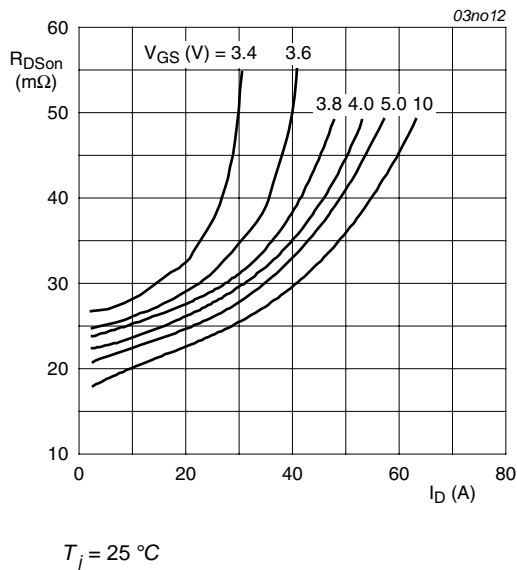


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

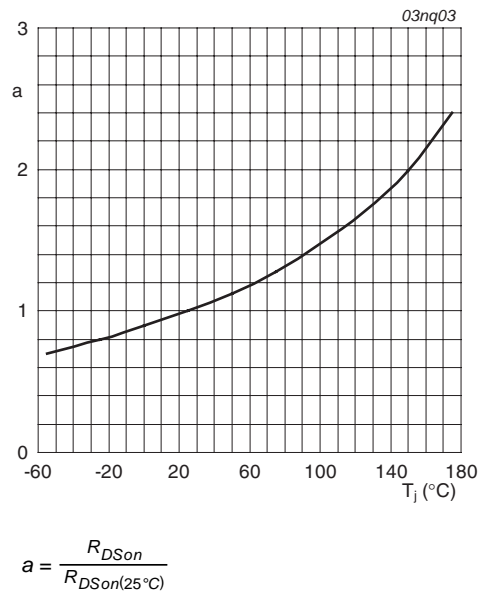


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

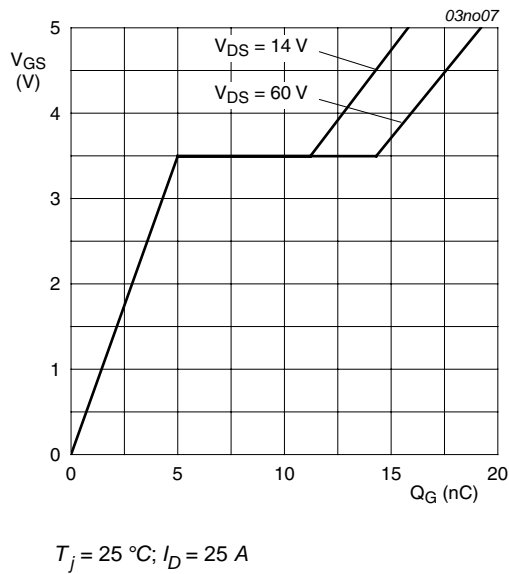


Fig 14. Gate-source voltage as a function of gate charge; typical values

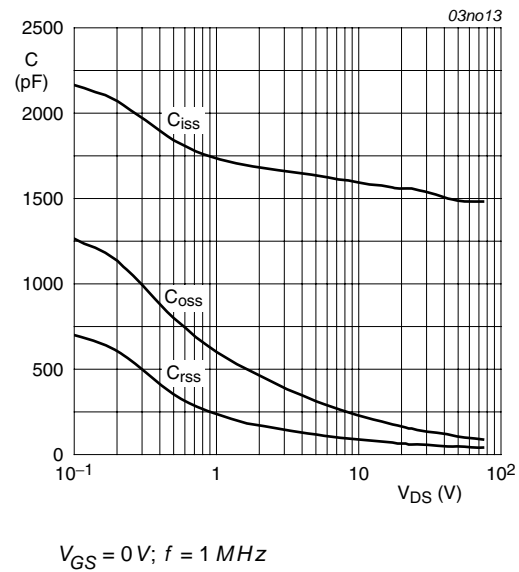


Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



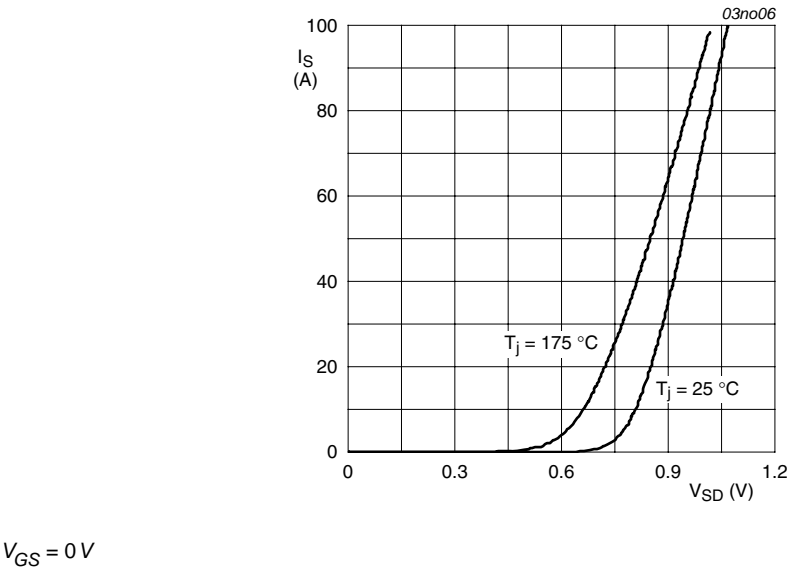


Fig 16. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

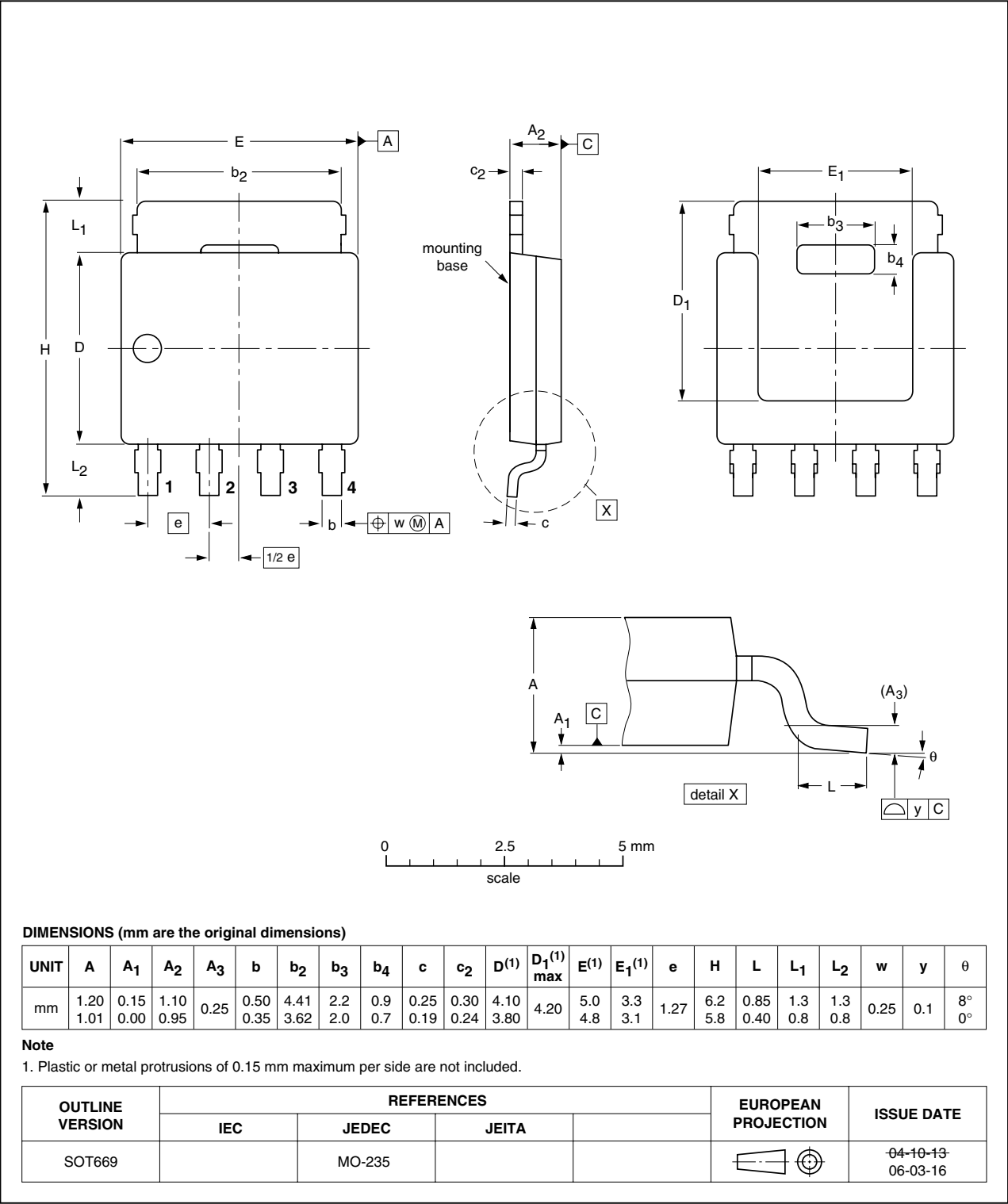


Fig 17. Package outline SOT669 (LPAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9Y30-75B_4	20080410	Product data sheet	-	BUK9Y30-75B_3
Modifications:	• <a href="#">Figure 13</a> : updated			
BUK9Y30-75B_3	20080222	Product data sheet	-	BUK9Y30-75B_2
BUK9Y30-75B_2	20060411	Product data sheet	-	BUK9Y30_75B-01
BUK9Y30_75B-01 (9397 750 13729)	20040714	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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