# QUAD SERIAL INTERFACE LOW-SIDE DRIVER IC

**Check for Samples: DRV8806**

## FEATURES

- **4-Channel Protected Low-Side Driver**
  - **Four NMOS FETs With Overcurrent Protection**
  - **Integrated Inductive Catch Diodes**
  - **Serial Interface**
  - **Open/Shorted Load Detection**
- **2-A (Single Channel On)/1-A (All Channels On) Maximum Drive Current per Channel (at 25°C)**
- **8.2-V to 40-V Operating Supply Voltage Range**
- **Thermally Enhanced Surface Mount Package**

## APPLICATIONS

- **Relay Drivers**
- **Unipolar Stepper Motor Drivers**
- **Solenoid Drivers**
- **General Low-Side Switch Applications**

## DESCRIPTION

The DRV8806 provides a 4-channel low side driver with overcurrent protection. It has built-in diodes to clamp turn-off transients generated by inductive loads and can be used to drive unipolar stepper motors, DC motors, relays, solenoids, or other loads.

The DRV8806 can supply up to 2-A (single channel on) or 1-A (all channels on) continuous output current (with adequate PCB heatsinking at 25°C).

A serial interface is provided to control the output drivers. Fault status can be read through the serial interface. Multiple DRV8806 devices can be chained together to use a single serial interface.

Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature and faults are indicated by a fault output pin.

The DRV8806 is available in a 16-pin HTSSOP package (Eco-friendly: RoHS & no Sb/Br).

**ORDERING INFORMATION(1)**

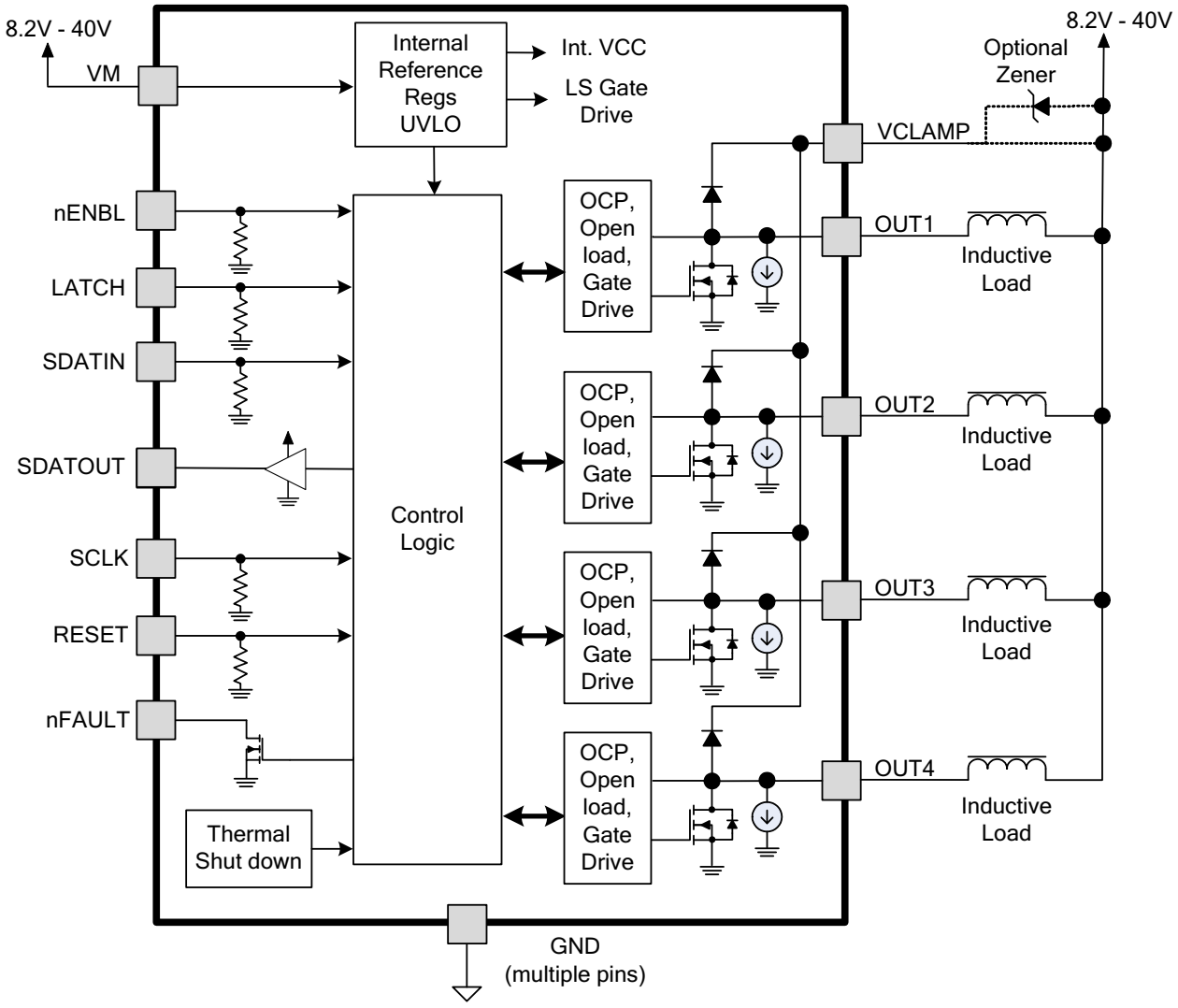
| PACKAGE(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|
| (HTSSOP) - PWP | Reel of 2000 | DRV8806PWPR | DRV8806 |
| | Tube of 90 | DRV8806PWP | DRV8806 |

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## DEVICE INFORMATION

### Functional Block Diagram

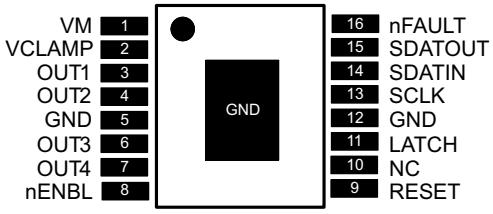


## Table 1. TERMINAL FUNCTIONS

| NAME | PIN (HTSSOP) | I/O(1) | DESCRIPTION | EXTERNAL COMPONENTS OR CONNECTIONS |
|---|---|---|---|---|
| **POWER AND GROUND** | | | | |
| GND | 5, 12, PPAD | - | Device ground | All pins must be connected to GND. |
| VM | 1 | - | Device power supply | Connect to motor supply (8.2 V - 40 V). |
| **CONTROL** | | | | |
| nENBL | 8 | I | Enable input | Active low enables outputs – internal pulldown |
| RESET | 9 | I | Reset input | Active-high reset input initializes internal logic – internal pulldown |
| LATCH | 11 | I | Latch input | Rising edge latches shift register to output stage, falling edge latches fault data into output shift register – internal pulldown |
| SDATIN | 14 | I | Serial data input | Serial data input – internal pulldown |
| SDATOUT | 15 | OD | Serial data output | Serial data output; push-pull structure; see serial interface section for details |
| SCLK | 13 | I | Serial clock | Serial clock input – internal pulldown |
| **STATUS** | | | | |
| nFAULT | 16 | OD | Fault | Logic low when in fault condition (overtemp, overcurrent, open load) - open drain output |
| **OUTPUT** | | | | |
| OUT1 | 3 | O | Output 1 | Connect to load 1 |
| OUT2 | 4 | O | Output 2 | Connect to load 2 |
| OUT3 | 6 | O | Output 3 | Connect to load 3 |
| OUT4 | 7 | O | Output 4 | Connect to load 4 |
| VCLAMP | 2 | - | Output clamp voltage | Connect to VM supply, or zener diode to VM supply |

(1) Directions: I = input, O = output, OD = open-drain output

**PWP (HTSSOP) PACKAGE**
**(TOP VIEW)**



## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

| | | VALUE | UNIT |
|---|---|---|---|
| VM | Power supply voltage range | –0.3 to 43 | V |
| VOUTx | Output voltage range | –0.3 to 43 | V |
| VCLAMP | Clamp voltage range | –0.3 to 43 | V |
| SDATOUT, nFAULT | Output current | 20 | mA |
| | Peak clamp diode current(3) | 2 | A |
| | DC or RMS clamp diode current(3) | 1 | A |
| | Digital input pin voltage range | –0.5 to 7 | V |
| SDATOUT, nFAULT | Digital output pin voltage range | –0.5 to 7 | V |
| | Peak motor drive output current, t < 1 µS | Internally limited | A |
| | Continuous total power dissipation(3) | See Thermal Information table | |
| $T_J$ | Operating virtual junction temperature range(3) | –40 to 150 | °C |
| $T_{stg}$ | Storage temperature range | –60 to 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | DRV8806 PWP 16 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance(2) | 39.6 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance(3) | 24.6 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance(4) | 20.3 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter(5) | 0.7 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter(6) | 20.1 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance(7) | 2.3 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_M$ | Power supply voltage range | 8.2 | | 40 | V |
| $V_{CLAMP}$ | Output clamp voltage range(1) | 0 | | 40 | V |
| $I_{OUT}$ | Continuous output current, single channel on, $T_A$ = 25°C(2) | | | 2 | A |
| | Continuous output current, four channels on, $T_A$ = 25°C(2) | | | 1 | |

(1) VCLAMP is not a power supply input pin - it only connects to the output clamp diodes.
(2) Power dissipation and thermal limits must be observed.

## ELECTRICAL CHARACTERISTICS

$T_A$ = 25°C, over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | | |
| $I_{VM}$ | VM operating supply current | $V_M$ = 24 V | | 1.6 | 3 | mA |
| $V_{UVLO}$ | VM undervoltage lockout voltage | $V_M$ rising | | | 8.2 | V |
| **LOGIC-LEVEL INPUTS (SCHMITT TRIGGER INPUTS WITH HYSTERESIS)** | | | | | | |
| $V_{IL}$ | Input low voltage | | | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2 | | | V |
| $V_{HYS}$ | Input hysteresis | | | 0.45 | | V |
| $I_{IL}$ | Input low current | VIN = 0 | –20 | | 20 | µA |
| $I_{IH}$ | Input high current | VIN = 3.3 V | | | 100 | µA |
| $R_{PD}$ | Pulldown resistance | | | 100 | | kΩ |
| **nFAULT OUTPUT (OPEN-DRAIN OUTPUT)** | | | | | | |
| $V_{OL}$ | Output low voltage | $I_O$ = 5 mA | | | 0.5 | V |
| $I_{OH}$ | Output high leakage current | $V_O$ = 3.3 V | | | 1 | µA |
| **SDATOUT OUTPUT (PUSH-PULL OUTPUT WITH INTERNAL PULLUP)** | | | | | | |
| $V_{OL}$ | Output low voltage | $I_O$ = 5 mA | | 0.5 | | V |
| $V_{OH}$ | Output high voltage | $I_O$ = 100 µA, $V_M$ = 11 V - 60 V, peak | | | 6.5 | V |
| | | $I_O$ = 100 µA, $V_M$ = 11 V - 60 V, steady-state | 3.3 | 4.5 | 5.6 | |
| | | $I_O$ = 100 µA, $V_M$ = 8.2 V - 11 V, steady-state | 2.5 | | | V |
| $I_{SRC}$ | Output source current | $V_M$ = 24 V | | | 1 | mA |
| $I_{SNK}$ | Output sink current | $V_M$ = 24 V | | | 5 | mA |
| **LOW-SIDE FETS** | | | | | | |
| $R_{DS(ON)}$ | FET on resistance | $V_M$ = 24 V, $I_O$ = 700 mA, $T_J$ = 25°C | | 0.5 | | Ω |
| | | $V_M$ = 24 V, $I_O$ = 700 mA, $T_J$ = 85°C | | 0.75 | 0.8 | |
| $I_{OFF}$ | Open load detect current | | 0 | 25 | 50 | µA |
| **HIGH-SIDE DIODES** | | | | | | |
| $V_F$ | Diode forward voltage | $V_M$ = 24 V, $I_O$ = 700 mA, $T_J$ = 25°C | | 0.9 | | V |
| $I_{OFF}$ | Off state leakage current | $V_M$ = 24 V, $T_J$ = 25°C | -50 | | 50 | µA |
| **OUTPUTS** | | | | | | |
| $t_R$ | Rise time | $V_M$ = 24 V, $I_O$ = 700 mA, Resistive load | 50 | | 300 | ns |
| $t_F$ | Fall time | $V_M$ = 24 V, $I_O$ = 700 mA, Resistive load | 50 | | 150 | ns |
| **PROTECTION CIRCUITS** | | | | | | |
| $I_{OCP}$ | Overcurrent protection trip level | | 3 | | 5 | A |
| $t_{OCP}$ | Overcurrent protection deglitch time | | | 3.5 | | µs |
| $t_{OL}$ | Open load detect deglitch time | | | 15 | | µs |
| $t_{RETRY}$ | Overcurrent protection re-try time | | | 1.2 | | ms |
| $t_{TSD}$ | Thermal shutdown temperature | Die temperature | 150 | 160 | 180 | °C |

## TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)(1)

| NO. | PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{CYC}$ | Clock cycle time | 62 | | | ns |
| 2 | $t_{CLKH}$ | Clock high time | 25 | | | ns |
| 3 | $t_{CLKL}$ | Clock low time | 25 | | | ns |
| 4 | $t_{SU(SDATIN)}$ | Setup time, SDATIN to SCLK | 5 | | | ns |
| 5 | $t_{H(SDATIN)}$ | Hold time, SDATIN to SCLK | 1 | | | ns |
| 6 | $t_{D(SDATOUT)}$ | Delay time, SCLK to SDATOUT, no external pullup resistor, $C_{OUT}$ = 100 pF | | 50 | 100 | ns |
| 7 | $t_{W(LATCH)}$ | Pulse width, LATCH | 200 | | | ns |
| 8 | $t_{OE(ENABLE)}$ | Enable time, nENBL to output low | | 60 | | ns |
| 9 | $t_{D(LATCH)}$ | Delay time, LATCH to output change | | 200 | | ns |
| - | $t_{RESET}$ | RESET pulse width | 20 | | | µs |
| 10 | $t_{D(RESET)}$ | Reset delay before clock | 20 | | | µs |
| 11 | $t_{STARTUP}$ | Startup delay VM applied before clock | 55 | | | µs |

(1) Not production tested.

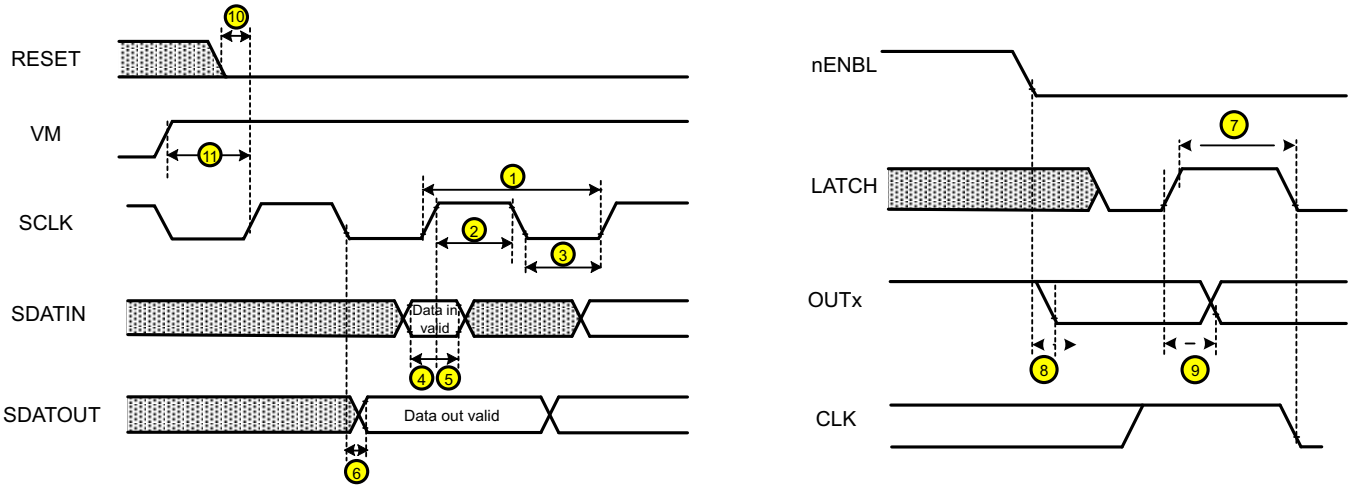



**Figure 1. DRV8806 Timing Requirements**

More than 400 ns of delay should exist between the final SCLK rising edge and the LATCH rising edge. This ensures that the last data bit is shifted into the device properly.

# FUNCTIONAL DESCRIPTION

## Output Drivers

The DRV8806 contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can be connected to the main power supply voltage, VM. It can also be connected to a zener or TVS diode to VM, allowing the switch voltage to exceed the main supply voltage VM. This connection can be beneficial when driving loads that require very fast current decay, such as unipolar stepper motors.

In all cases, the voltage on the outputs must not be allowed to exceed the maximum output voltage specification.

## Serial Interface Operation

The DRV8806 is controlled with a simple serial interface. Logically, the interface is shown in Figure 2.

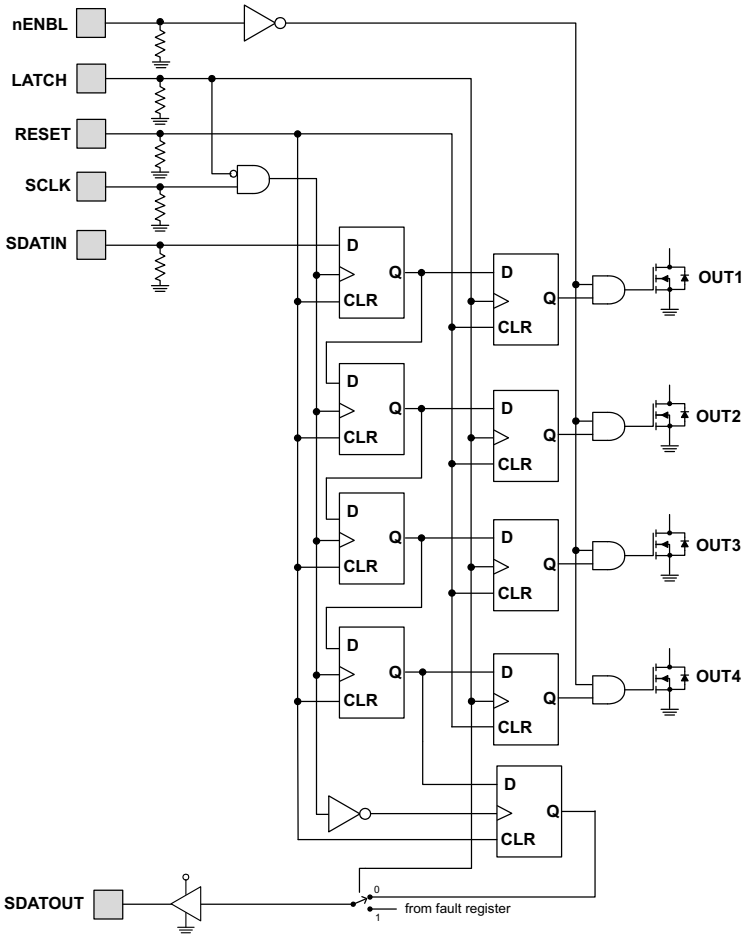



**Figure 2. Serial Interface Operation**

Data is shifted into a temporary holding shift register in the part using the SDATIN pin, one bit at each rising edge of the SCLK pin, while LATCH is low. Data is shifted from the last bit to the SDATOUT pin, so multiple devices may be daisy-chained together using a single serial interface.

Note that the SDATOUT pin has a push-pull driver, which can support driving another DRV8806 SDATIN pin at clock frequencies of up to 1 MHz without an external pullup. A pullup resistor can be used between SDATOUT and an external 5 V logic supply in order to support higher clock frequencies. A resistor value of approximately 1 kΩ is recommended.The SDATOUT pin is capable of approximately 1-mA source and 5-mA sink. In order to supply logic signals to a lower-voltage microcontroller, use a resistor divider from SDATOUT to GND.

A rising edge on the LATCH pin latches the data from the temporary shift register into the output stage.

## Fault Output Register

The DRV8806 contains circuitry to detect open or shorted loads. The status of the loads can be read via the serial interface. The logic is shown in Figure 3.

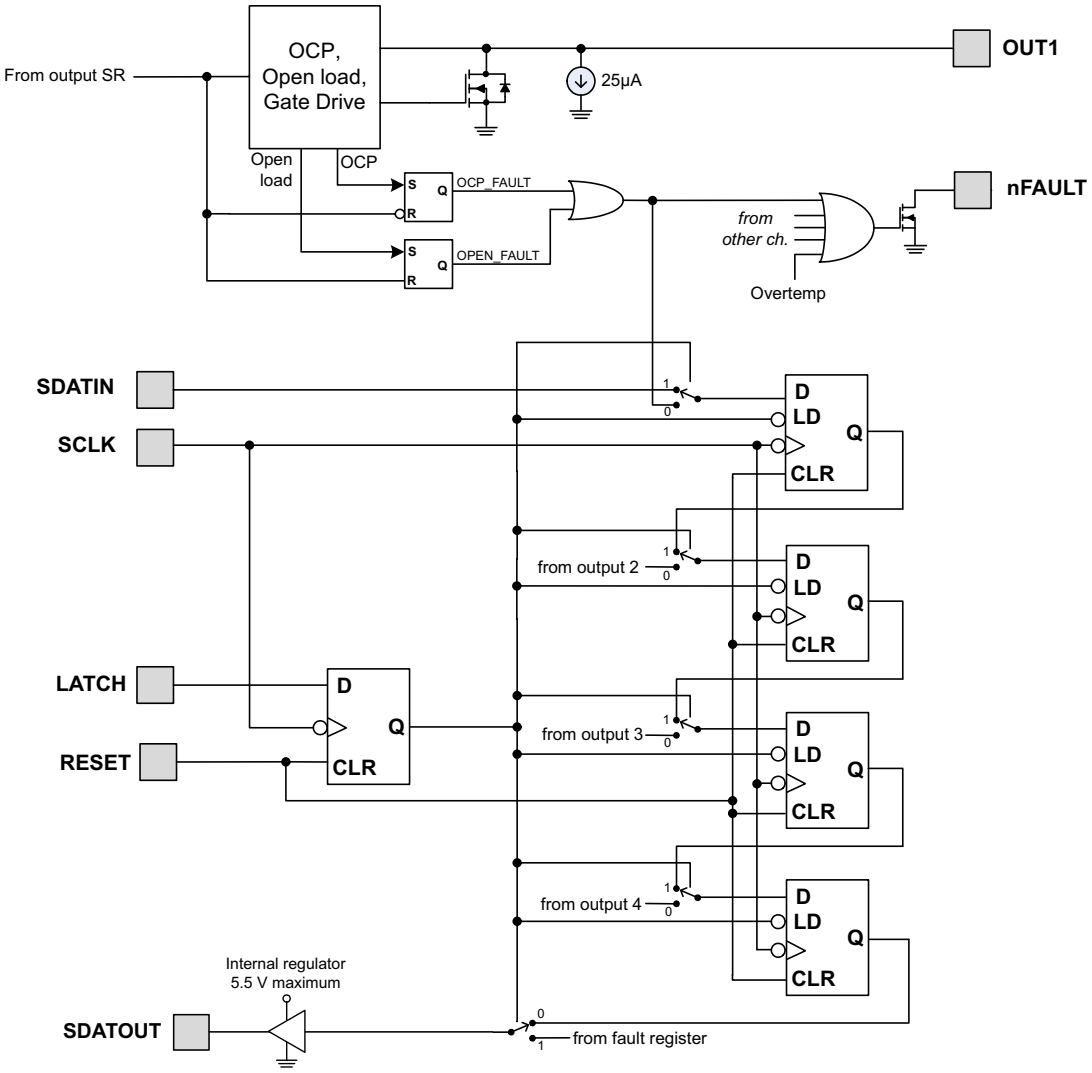



**Figure 3. Fault Output**

To overcome any leakage currents to accurately sense an open load, a small current source is connected to each output pin. This source pulls approximately 25-µA of current to ground. The voltage on the output pin is sensed during the time that the output is off, and if the voltage on the pin is less than 1.2 V (indicating that there is no load connected) after the open load deglitch time, the OPEN_FAULT latch is set. This latch is cleared whenever the output bit is set.

When the output is turned on, if an overcurrent (OCP) fault is detected, the channel will be turned off and the OCP_FAULT latch is set. This latch will be cleared whenever the output bit is cleared.

The state of the OCP_FAULT and OPEN_FAULT signals is combined into a single fault bit per channel, and loaded into a shift register while the LATCH pin is low. When the LATCH pin is taken high, the fault data is latched into the shift register at the first falling edge of SCLK. Data may then be shifted out on the SDATOUT pin on each falling edge of the SCLK pin.

Note that the LATCH signal must be high for a minimum of 200 ns before valid data can be clocked out.

The nFAULT pin will be driven active low whenever any of the OCP_FAULT or OPEN_FAULT latches are set, as well as whenever there is an overtemperature condition.

## Daisy-Chain Connection

Two or more DRV8806 devices may be connected together to use a single serial interface. The SDATOUT pin of the first device in the chain is connected to the SDATIN pin of the next device. The SCLK, LATCH, RESET, and nFAULT pins are connected together.

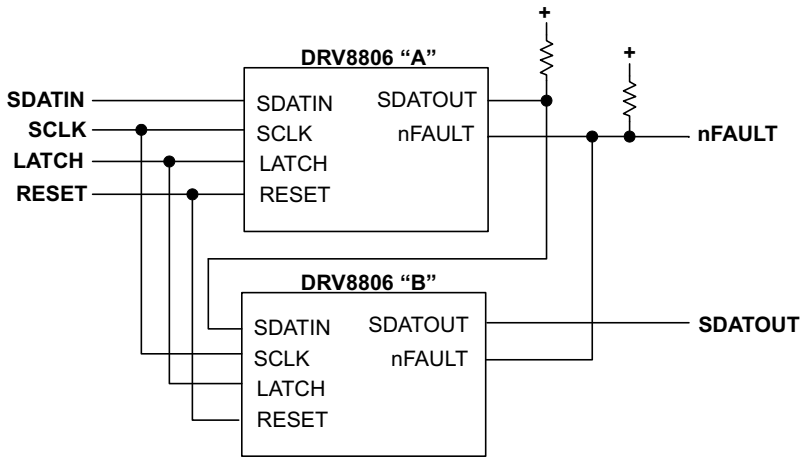



**Figure 4. Daisy-Chain Connection**

Figure 5 shows an example of a serial transaction, writing the output bits, and then reading the fault status bits, using two devices connected together in a daisy-chain.

Note that the LATCH signal must be high for a minimum of 200 ns before valid data can be clocked out.

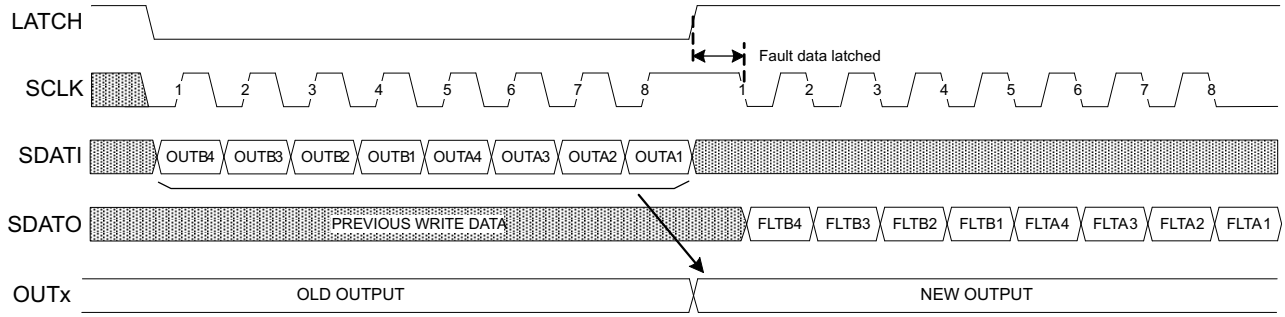



**Figure 5. Daisy-Chain Serial Transaction**

## nENBL and RESET Operation

The nENBL pin enables or disables the output drivers. nENBL must be low to enable the outputs. nENBL does not affect the operation of the serial interface logic. Note that nENBL has an internal pulldown.

The RESET pin, when driven active high, resets internal logic, including the OCP fault. All serial interface registers are cleared. Note that RESET has an internal pulldown. An internal power-up reset is also provided, so it is not required to drive RESET at power-up.

## Protection Circuits

The DRV8806 is fully protected against undervoltage, overcurrent and overtemperature events.

### Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the $t_{OCP}$ deglitch time (approximately 3.5 µs), the driver will be disabled and the nFAULT pin will be driven low. The driver will remain disabled for the $t_{RETRY}$ retry time (approximately 1.2 ms), then the fault will be automatically cleared. The fault will be cleared immediately if either RESET pin is activated or VM is removed and re-applied.

### Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume.

### Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

## THERMAL INFORMATION

### Thermal Protection

The DRV8806 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

### Power Dissipation

Power dissipation in the DRV8806 is dominated by the power dissipated in the output FET resistance, or RDS(ON). Average power dissipation of each FET when running a static load can be roughly estimated by Equation 1:

$$P = R_{DS(ON)} \bullet (I_{OUT})^2 \quad (1)$$

where P is the power dissipation of one FET, $R_{DS(ON)}$ is the resistance of each FET, and $I_{OUT}$ is equal to the average current drawn by the load. Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also need to be taken into consideration. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

### Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI Application Report SLMA002, "PowerPAD™ Thermally Enhanced Package" and TI Application Brief SLMA004, "PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

## REVISION HISTORY

**Changes from Original (June 2012) to Revision A** **Page**

- Changed Functional Block Diagram at SDATOUT ..... 2
- Added comment to Timing Requirements section ..... 6
- Changed Figure 2 at SDATOUT ..... 7
- Changed SDATOUT description in Serial Interface Operation section ..... 7

**Changes from Revision A (November 2013) to Revision B** **Page**

- Changed (OPEN-DRAIN to PUSH-PULL in the elec chara table section SDATAOUT OUTPUT ..... 5
- Added another row below $V_{OH}$ - merge the first two columns together ($V_{OH}$ and Output high voltage). The second row should have test condition "Io = 100 uA, VM = 8.2 V" and be specified as 2.5 V MIN ..... 5
- Added two new rows, $I_{SRC}$ and $I_{SNK}$ in elec chara table, section SDATAOUT OUTPUT ..... 5
- Changed NO. 6 in Timing Requirements table ..... 6
- Added a sentence in second paragraph below Figure 2: A pull up resistor.....1 kohm is recommended. ..... 7

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8806PWP | ACTIVE | HTSSOP | PWP | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | DRV8806 | Samples |
| DRV8806PWPR | ACTIVE | HTSSOP | PWP | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | DRV8806 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

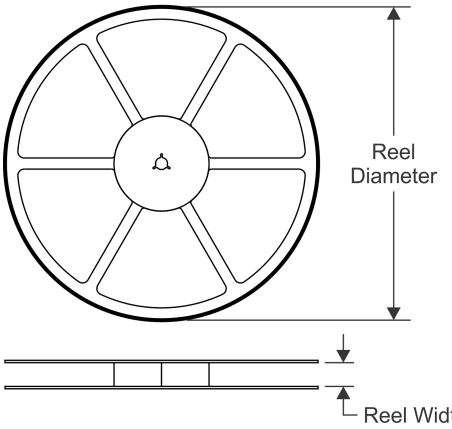
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

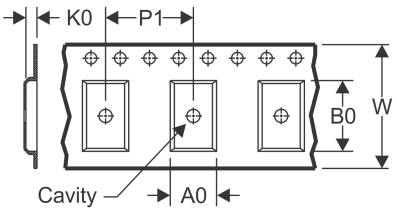
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

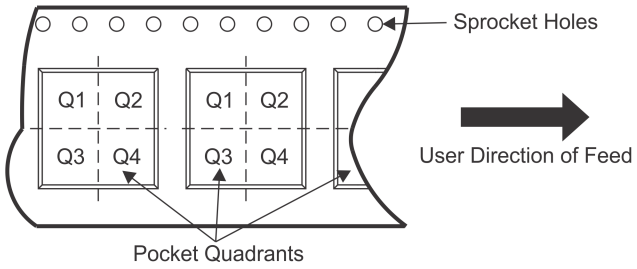



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

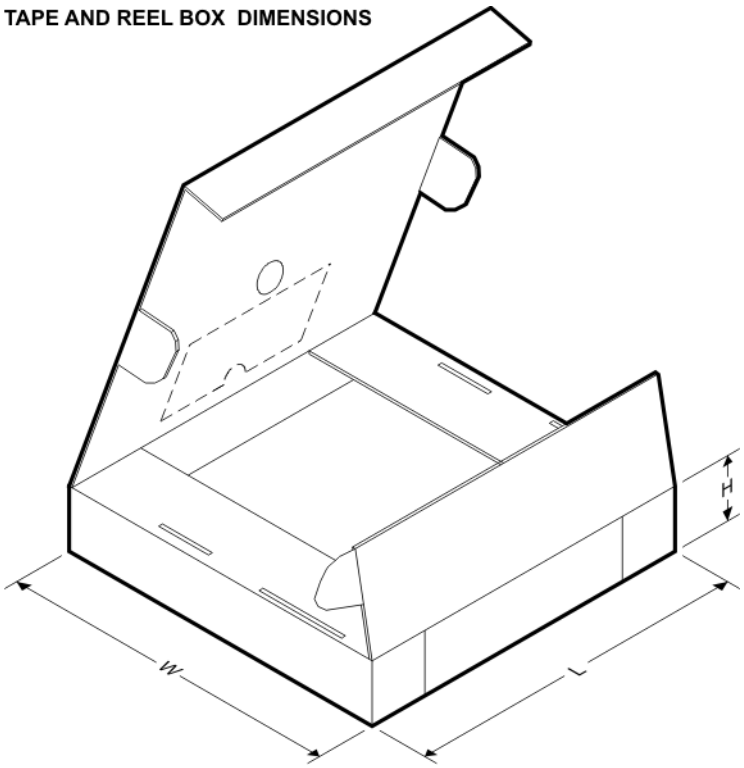
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8806PWPR | HTSSOP | PWP | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

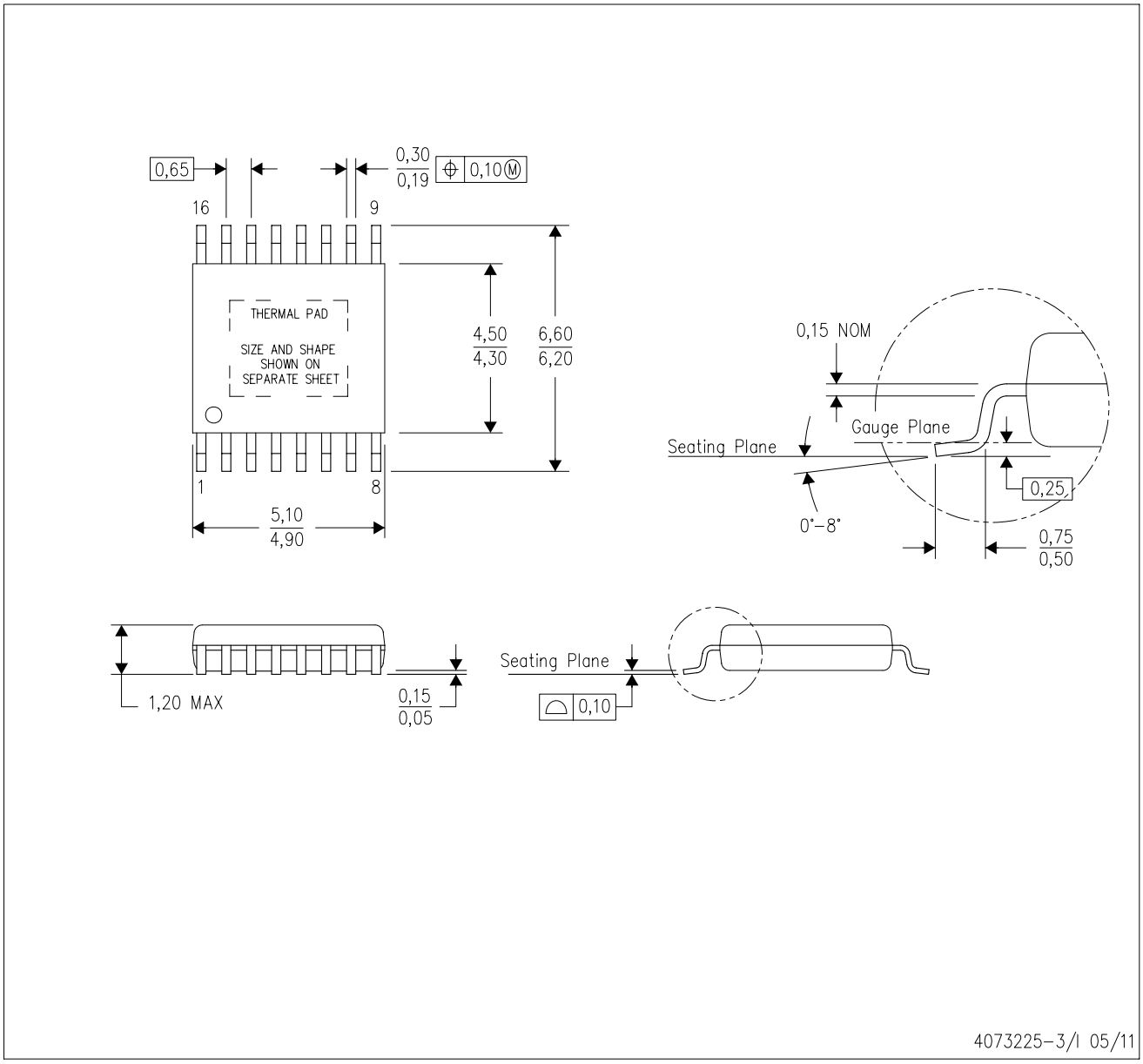
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV8806PWPR | HTSSOP | PWP | 16 | 2000 | 367.0 | 367.0 | 35.0 |

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

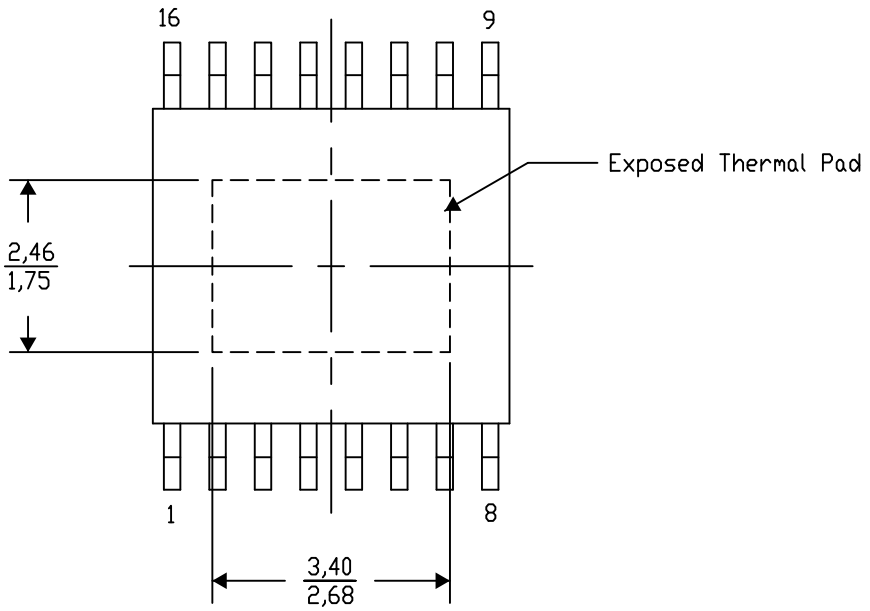
# PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

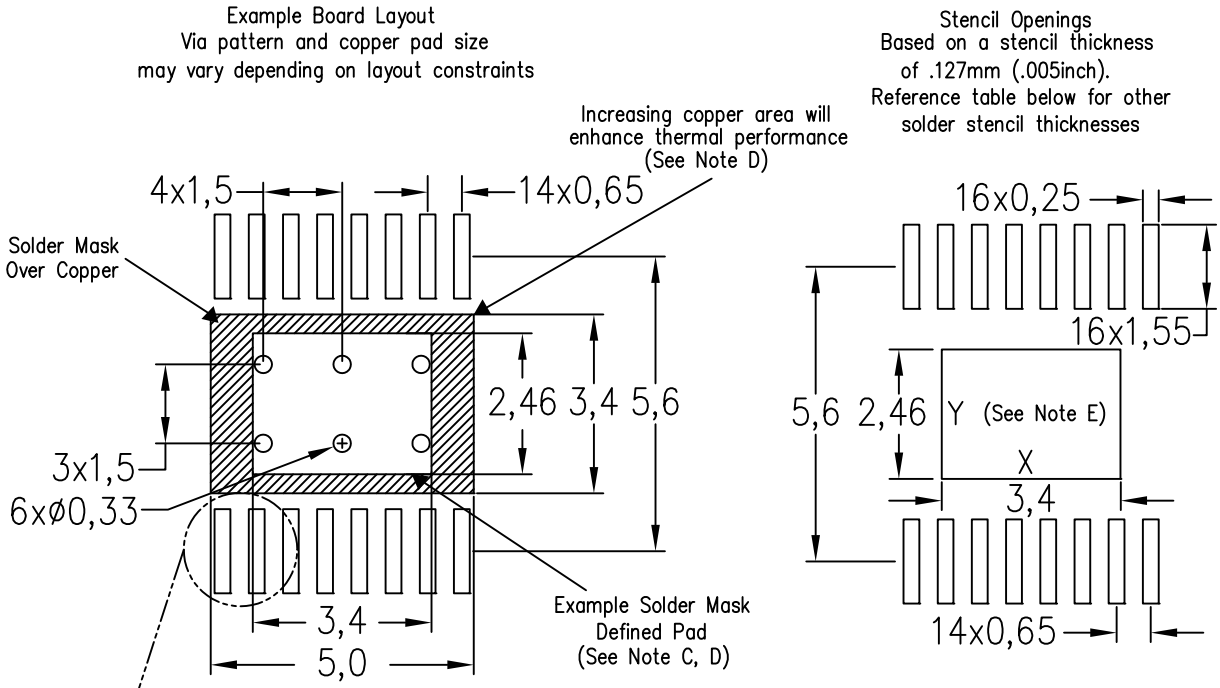
Exposed Thermal Pad Dimensions

4206332–7/AH 11/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

## PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 3.6 | 2.9 |
| 0.127mm | 3.4 | 2.46 |
| 0.152mm | 3.2 | 2.5 |
| 0.178mm | 3.1 | 2.3 |

4207609–4/T 08/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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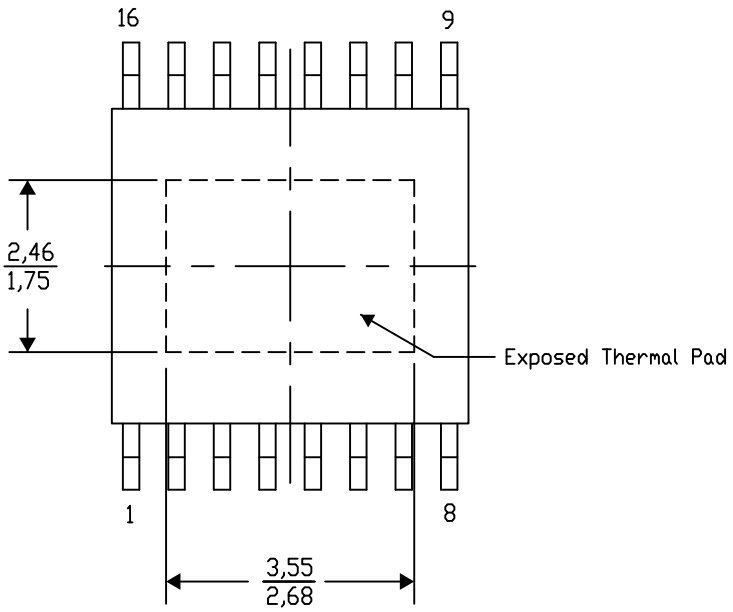
The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

4206332–51/AH 11/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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