Ordering number : EN7332A

LC75344MD

ON Semiconductor®

http://onsemi.com

CMOS LSI

Two-Channel Electronic Volume Control System

Overview

The LC75344MD is a two-channel electronic volume control IC that is controlled by data input over a serial interface.

Functions

- Volume control: 0 dB to –50 dB in 1 dB steps, –52 dB to –78 dB in 2 dB steps, and –∞, for a total of 66 positions. A balance function can be implemented by controlling the left and right channels independently.

Features

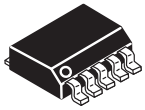
- Built-in buffer amplifiers minimize the number of external components required.
- Fabricated in a silicon gate CMOS process to minimize the switching noise generated by internal switches.
- Built-in reference voltage generation circuit for the analog ground level.
- All settings are controlled by data input over a serial interface that conforms to the CCB specifications.

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage	V_{DD} max	V_{DD}	11	V
Input voltage	V_{IN} max	CE, CL, DI	–0.3 to +11.0	V
		LIN, RIN	V_{SS} –0.3 to V_{DD} +0.3	
Output voltage	$V_{OUT}1$	OSC	–0.3 to V_{DD} +0.3	V
	$V_{OUT}2$	S1 to S87, COM1 to COM4, P1 to P8	–0.3 to V_{LCD} +0.3	
Allowable power dissipation	Pd max	Ta ≤ 75°C *1: When mounted on a PCB.	300	mW
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



SOIC-10 NB

- CCB is ON Semiconductor® 's original format. All addresses are managed by ON Semiconductor® for this format.

- CCB is a registered trademark of Semiconductor Components Industries, LLC.

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

Semiconductor Components Industries, LLC, 2014
May, 2014

51914HK 20120417-S00003/21004TN(OT) No.7332-1/13

Allowable Operating Ranges at Ta = –30 to +75°C, V_{SS} = 0V

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Supply voltage	V_{DD}	V_{DD}		4.5		10	V
High-level input voltage	V_{IH}	CL, DI, CE		2.0		10	V
Low-level input voltage	V_{IL}	CL, DI, CE	7.5 ≤ V_{DD} ≤ 10	V_{SS}		0.8	V
		CL, DI, CE	4.5 ≤ V_{DD} ≤ 7.5	V_{SS}		0.3	V
Input voltage amplitude	V_{IN}	LIN, RIN		V_{SS}		V_{DD}	Vp-p
Input pulse width	tøW	CL		1			μs
Setup time	tsetup	CL, DI, CE		1			μs
Hold time	thold	CL, DI, CE		1			μs
Operating frequency	fopg	CL				500	kHz

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characterristics at Ta = 25°C, V_{DD} = 9V, V_{SS} = 0V

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Input resistance	Rin	LIN, RIN			50		kΩ

Overall Characteristics

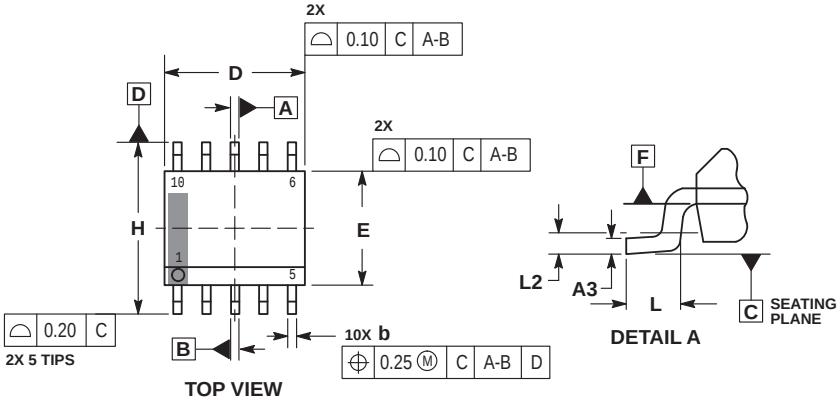
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Total harmonic distortion	THD	V_{IN} = 1 Vrms, f = 1 kHz With all settings flat overall		0.002	0.01	%
		V_{IN} = 1 Vrms, f = 20 kHz With all settings flat overall		0.003		%
Crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz, Rg = 1 kΩ With all settings flat overall	90			dB
Output noise voltage	V_N	80 kHz L.P.F, Rg = 1 kΩ With all settings flat overall		6.0		μV
Maximum attenuation	Vomin	V_{IN} = 1 Vrms, f = 1 kHz With all settings flat overall		–92		dB
Current drain	I_{DD}	V_{DD} – V_{SS} = +9 V		12		mA
High-level input current	I_{IH}	CL, DI, CE: V_{IN} = 10 V, V_{DD} = 10 V			10	μA
Low-level input current	I_{IL}	CL, DI, CE: V_{IN} = 0 V, V_{DD} = 10 V	–10			μA

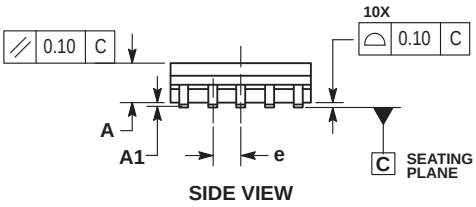
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

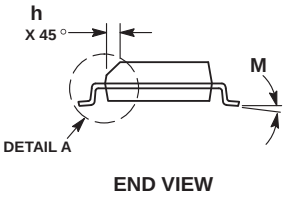
Package Dimensions

unit : mm

SOIC-10 NB
CASE 751BQ
ISSUE B



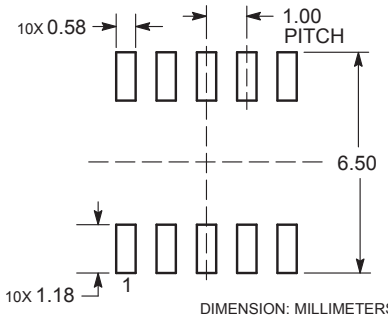




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.75
A1	0.10	0.25
A3	0.17	0.25
b	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.00 BSC	
H	5.80	6.20
h	0.37 REF	
L	0.40	0.80
L2	0.25 BSC	
M	0 °	8 °

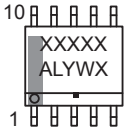
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

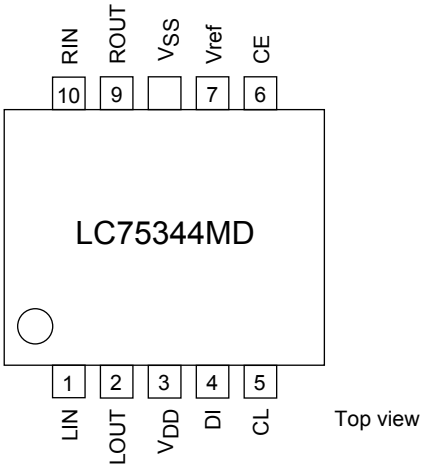
GENERIC MARKING DIAGRAM*



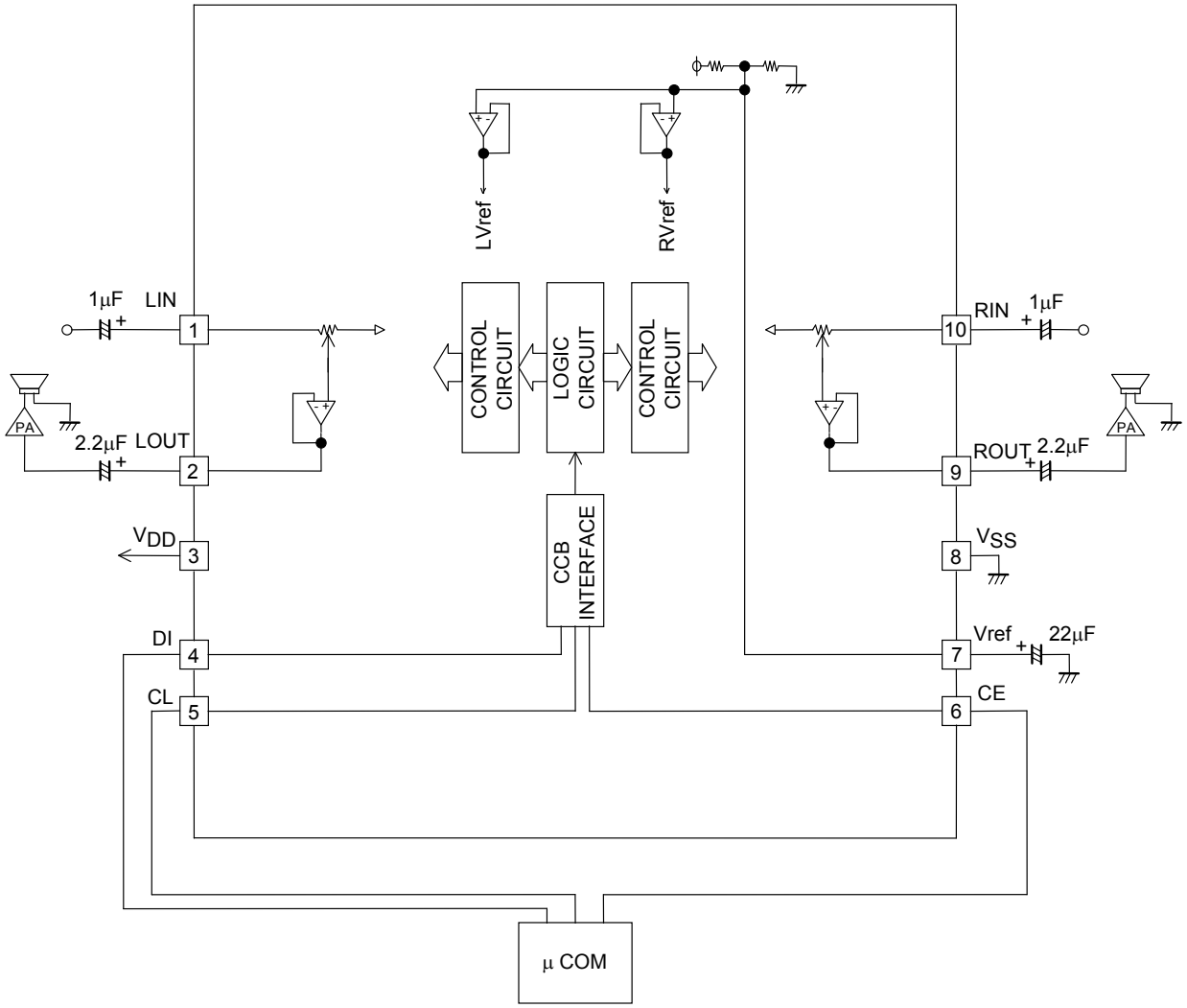
XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G", may or not be present.

Pin Arrangement

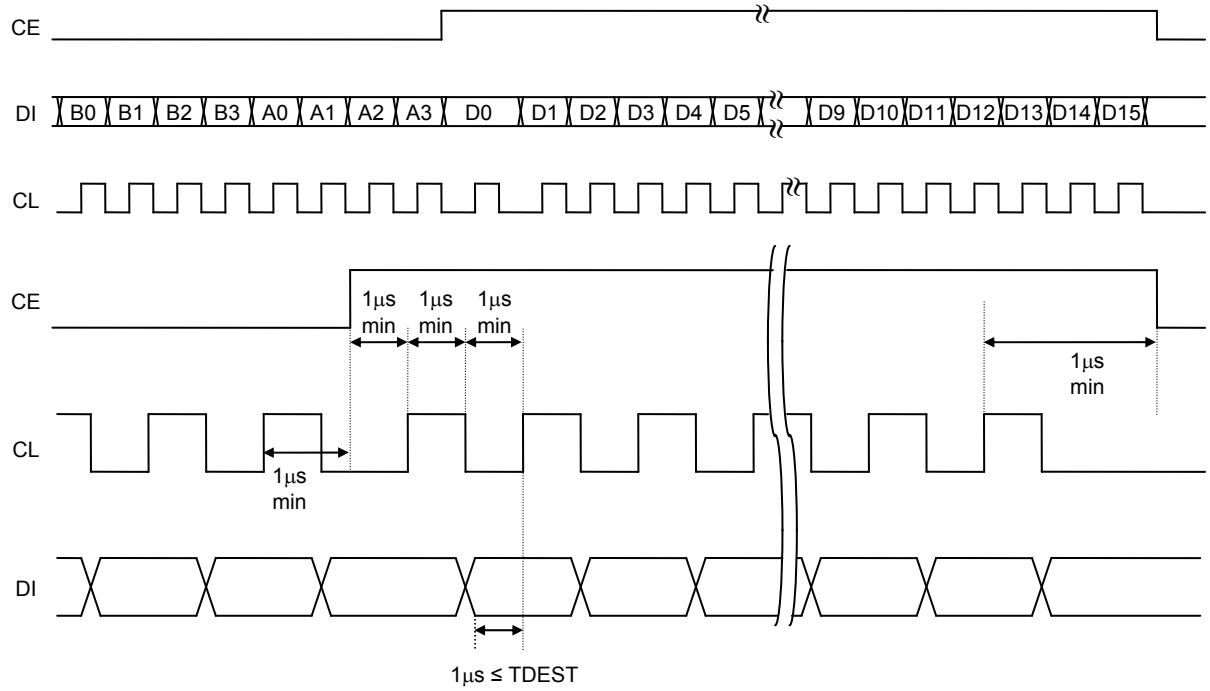


Equivalent Circuit



Control System Timing and Data Format

The LC75344MD is controlled by inputting the stipulated data serially to the CL, DI, and CE pins. The data consists of a total of 24 bits, of which 8 bits are the address and 16 bits are the data.



- Address Code (B0 to A3)

The data has an 8-bit address field, and conforms to the CCB serial bus specifications.

Address code	B0	B1	B2	B3	A0	A1	A2	A3	
(LSB)	0	0	0	1	0	0	0	1	(88HEX)

• Control Code Allocations

Volume control

D0	D1	D2	D3	D4	D5	D6	D7	Operation
0	0	0	0	0	0	0	0	0dB
1	0	0	0	0	0	0	0	–1dB
0	1	0	0	0	0	0	0	–2dB
1	1	0	0	0	0	0	0	–3dB
0	0	1	0	0	0	0	0	–4dB
1	0	1	0	0	0	0	0	–5dB
0	1	1	0	0	0	0	0	–6dB
1	1	1	0	0	0	0	0	–7dB
0	0	0	1	0	0	0	0	–8dB
1	0	0	1	0	0	0	0	–9dB
0	1	0	1	0	0	0	0	–10dB
1	1	0	1	0	0	0	0	–11dB
0	0	1	1	0	0	0	0	–12dB
1	0	1	1	0	0	0	0	–13dB
0	1	1	1	0	0	0	0	–14dB
1	1	1	1	0	0	0	0	–15dB
0	0	0	0	1	0	0	0	–16dB
1	0	0	0	1	0	0	0	–17dB
0	1	0	0	1	0	0	0	–18dB
1	1	0	0	1	0	0	0	–19dB
0	0	1	0	1	0	0	0	–20dB
1	0	1	0	1	0	0	0	–21dB
0	1	1	0	1	0	0	0	–22dB
1	1	1	0	1	0	0	0	–23dB
0	0	0	1	1	0	0	0	–24dB
1	0	0	1	1	0	0	0	–25dB
0	1	0	1	1	0	0	0	–26dB
1	1	0	1	1	0	0	0	–27dB
0	0	1	1	1	0	0	0	–28dB
1	0	1	1	1	0	0	0	–29dB
0	1	1	1	1	0	0	0	–30dB
1	1	1	1	1	0	0	0	–31dB
0	0	0	0	0	1	0	0	–32dB
1	0	0	0	0	1	0	0	–33dB
0	1	0	0	0	1	0	0	–34dB
1	1	0	0	0	1	0	0	–35dB
0	0	1	0	0	1	0	0	–36dB
1	0	1	0	0	1	0	0	–37dB
0	1	1	0	0	1	0	0	–38dB
1	1	1	0	0	1	0	0	–39dB
0	0	0	1	0	1	0	0	–40dB

Continued on next page.

Continued from preceding page.

Volume control

D0	D1	D2	D3	D4	D5	D6	D7	Operation
1	0	0	1	0	1	0	0	–41dB
0	1	0	1	0	1	0	0	–42dB
1	1	0	1	0	1	0	0	–43dB
0	0	1	1	0	1	0	0	–44dB
1	0	1	1	0	1	0	0	–45dB
0	1	1	1	0	1	0	0	–46dB
1	1	1	1	0	1	0	0	–47dB
0	0	0	0	1	1	0	0	–48dB
1	0	0	0	1	1	0	0	–49dB
0	1	0	0	1	1	0	0	–50dB
0	0	1	0	1	1	0	0	–52dB
0	1	1	0	1	1	0	0	–54dB
0	0	0	1	1	1	0	0	–56dB
0	1	0	1	1	1	0	0	–58dB
0	0	1	1	1	1	0	0	–60dB
0	1	1	1	1	1	0	0	–62dB
0	0	0	0	0	0	1	0	–64dB
0	1	0	0	0	0	1	0	–66dB
0	0	1	0	0	0	1	0	–68dB
0	1	1	0	0	0	1	0	–70dB
0	0	0	1	0	0	1	0	–72dB
0	1	0	1	0	0	1	0	–74dB
0	0	1	1	0	0	1	0	–76dB
0	1	1	1	0	0	1	0	–78dB
0	0	0	0	1	0	1	0	–∞

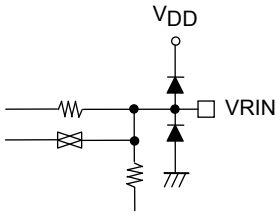
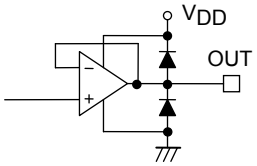
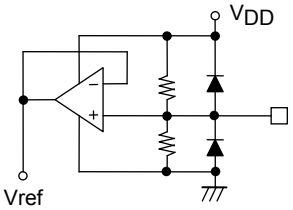
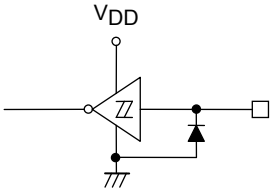
Channel selection

D8	D9	Operation
0	0	Normally not used
1	0	RCH
0	1	LCH
1	1	Left and right channels together

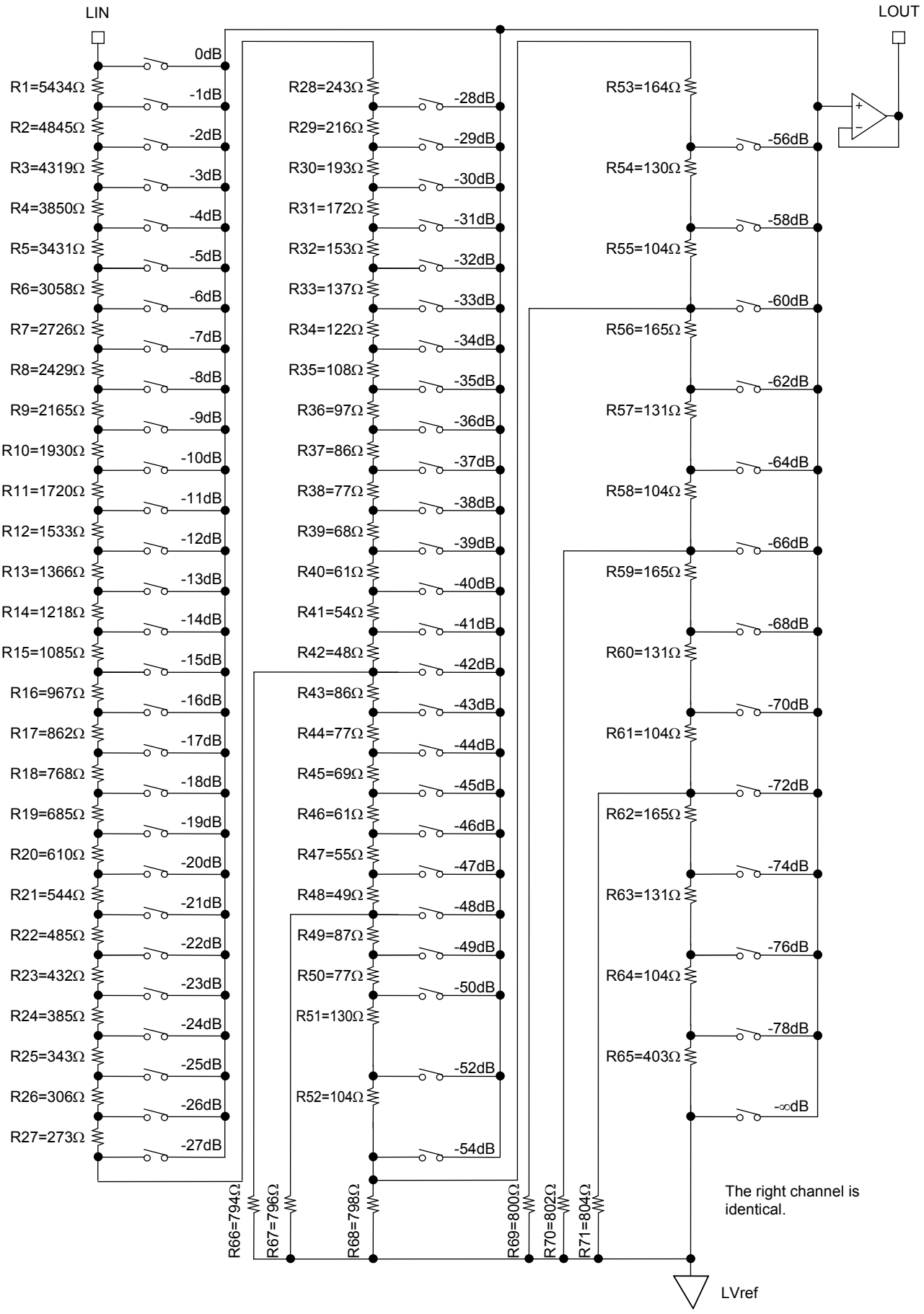
Test mode

D10	D11	D12	D13	D14	D15	Operation
0	0	0	0	0	0	
These bits specify the IC test mode. They must be set to zero for normal operation.						

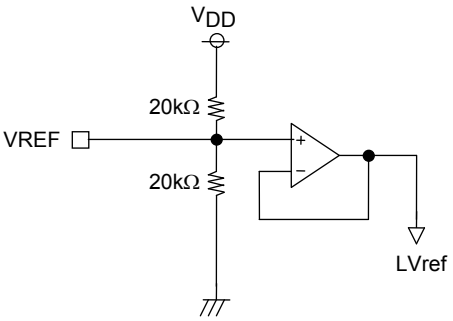
Pin Functions

Pin name	Pin No.	Function	Notes
LIN RIN	1 10	Volume control inputs	
LOUT ROUT	2 9	Volume control outputs	
Vref	7	VDD × 0.5 voltage generator block for the analog ground level. A capacitor with a value a few times 10 μF must be inserted between Vref and AVSS (VSS) to minimize power supply ripple.	
V_{SS}	8	Ground	
V_{DD}	3	Power supply	
CE	6	Chip enable The internal latch data is written and the analog switches operate at the point this pin goes from high to low. Data transfer is enabled when this pin is at the high level.	
DI CL	4 5	Serial data and clock inputs for IC control.	

Equivalent Circuit

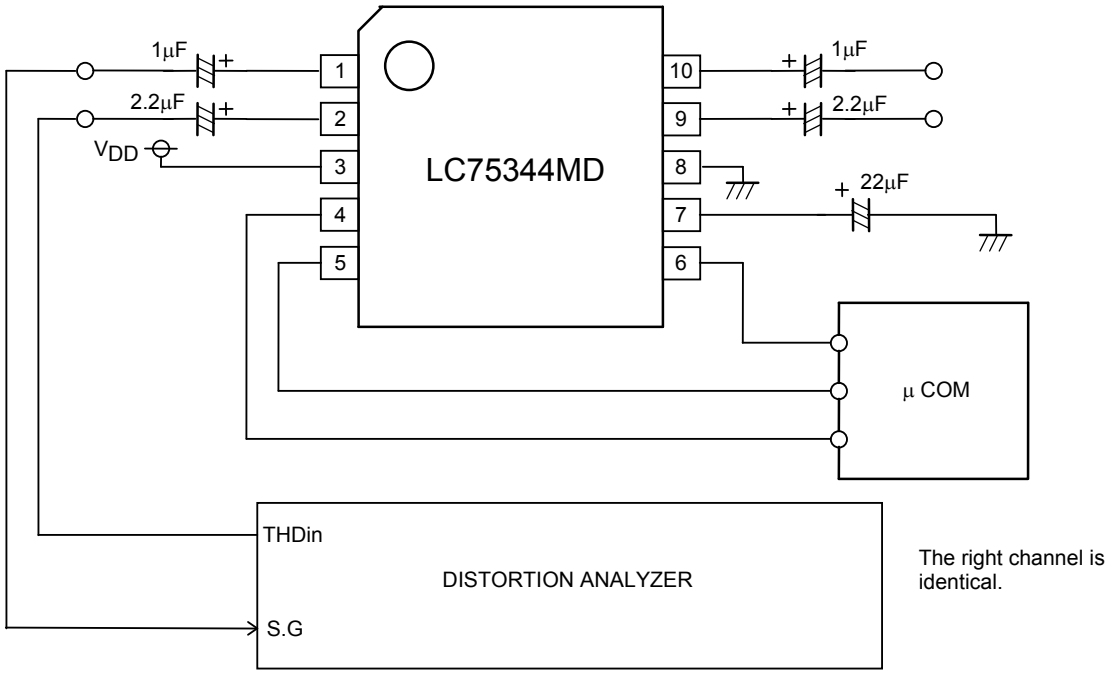


Reference Voltage Generator Equivalent Circuit

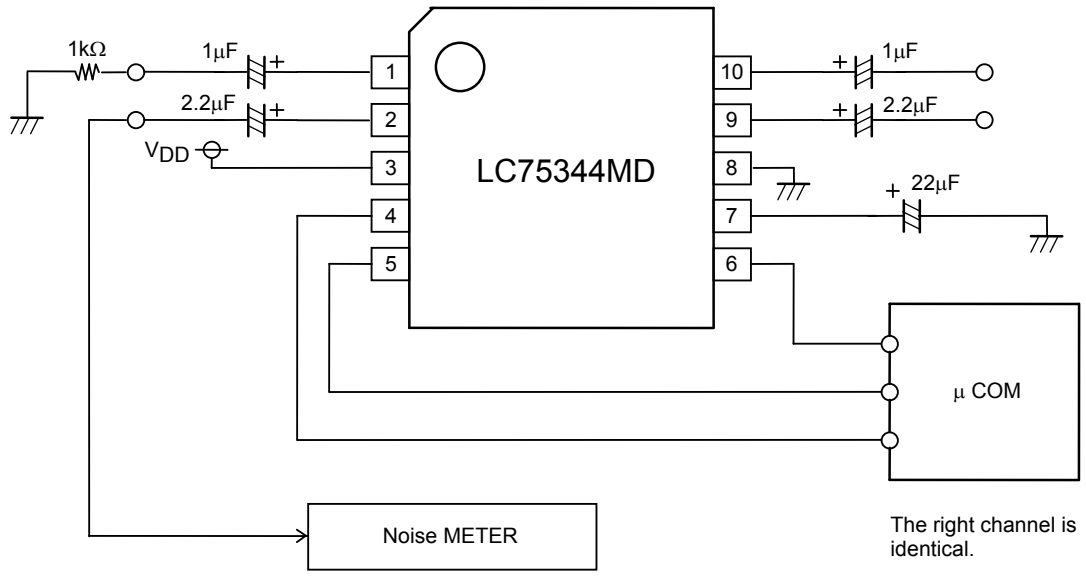


Test Circuit

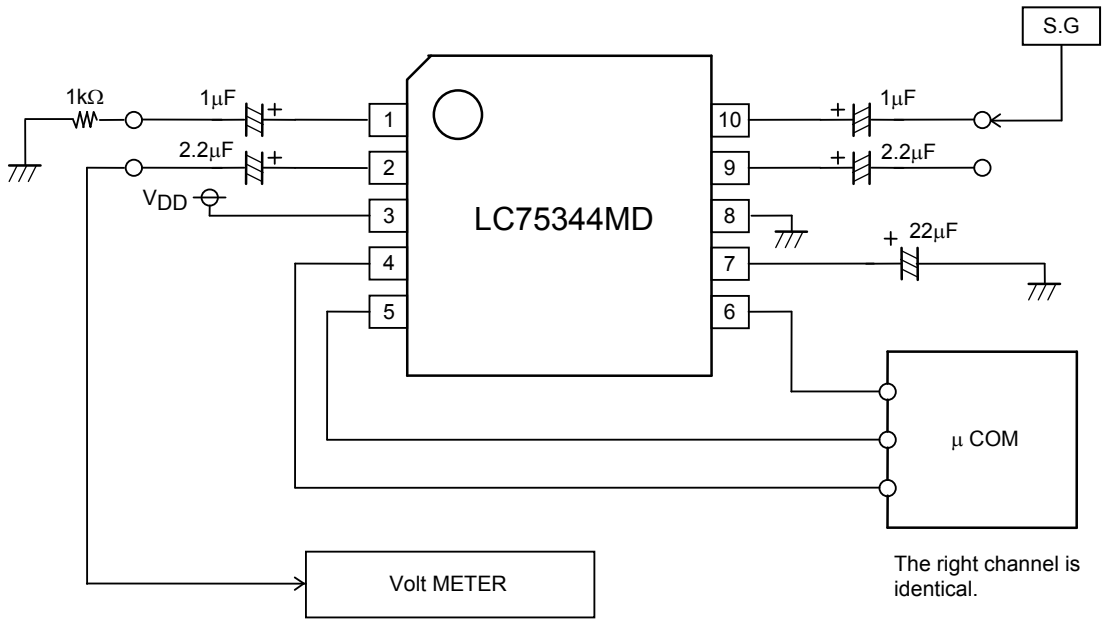
- Total harmonic distortion



• Output noise voltage



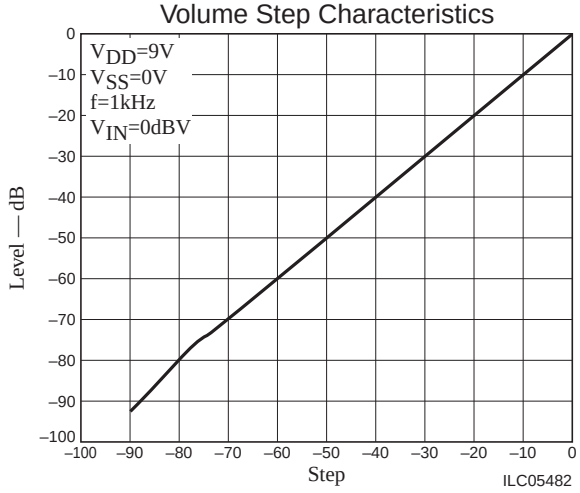
• Crosstalk



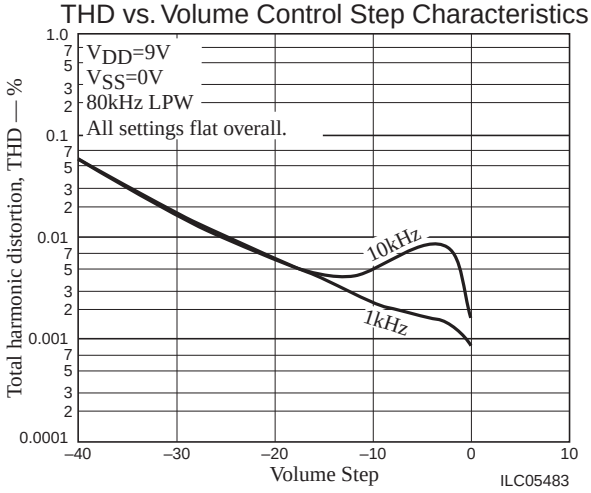
Usage Notes

- The states of the internal analog switches are undefined after power is first applied. Muting must be applied externally until the control data has been sent.
- When performing the initial settings after power is first applied, both the left and right channel initial settings data must be sent before releasing the external mute.
- Either cover the CL, DI, and CE lines with the ground pattern or use shielded lines to prevent high-frequency digital noise from entering the analog signal system from these lines.

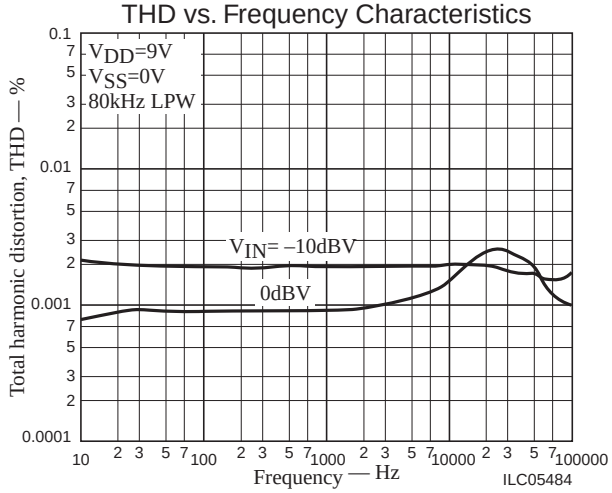
Volume Step Characteristics



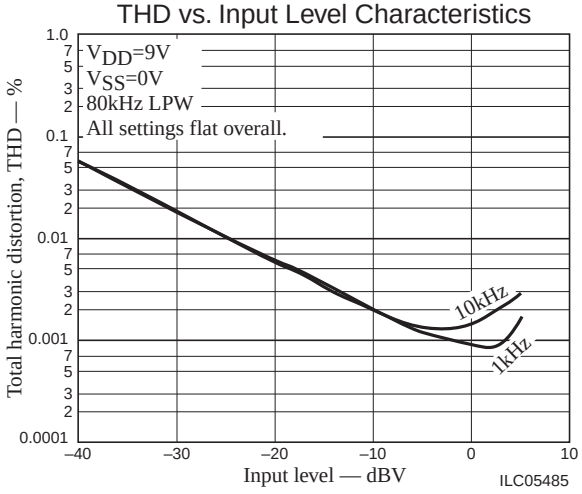
THD vs. Volume Control Step Characteristics



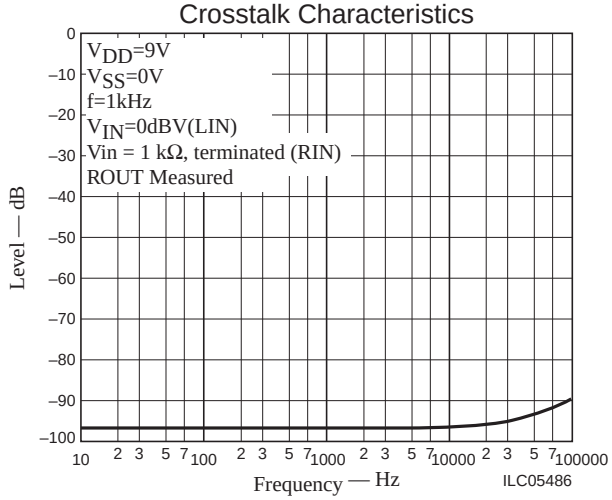
THD vs. Frequency Characteristics



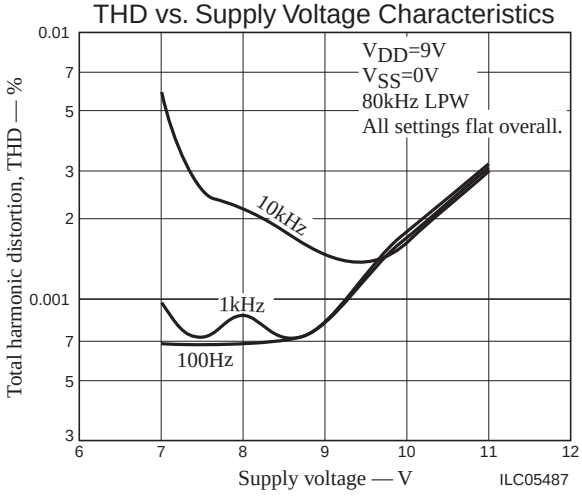
THD vs. Input Level Characteristics



Crosstalk Characteristics



THD vs. Supply Voltage Characteristics



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC75344MD-AH	SOIC-10 NB (Pb-Free / Halogen Free)	2500 / Tape & Reel

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

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