



## High-Bandwidth, VGA 2:1 Switch with $\pm 15\text{kV}$ ESD Protection

**MAX4885AE**

### General Description

The MAX4885AE integrates high-bandwidth analog switches, level-translating buffers, and level-translating FET switches to implement a complete 2:1 multiplexer for VGA signals. The device provides three very high-frequency 900MHz (typ) SPDT switches for RGB signals, two low-frequency clamping switches for the DDC signals, a pair of level-translating buffers for the H<sub>-</sub> and V<sub>-</sub> signals, and integrated extended ESD protection.

Horizontal and vertical synchronization (H<sub>-</sub>/V<sub>-</sub>) inputs feature level-shifting buffers to support low-voltage controllers and standard 5V-TTL-compatible monitors, meeting the VESA requirement. Display Data Channel (DDC), consisting of SDA<sub>-</sub> and SCL<sub>-</sub>, are FET switches that protect the low-voltage VGA source from potential damage from high-voltage presence on the monitor while reducing capacitive load.

All seven output terminals of the MAX4885AE feature high-ESD protection to  $\pm 15\text{kV}$  Human Body Model (HBM) (see the *Pin Description*). All other pins are protected to  $\pm 2\text{kV}$  Human Body Model (HBM).

The MAX4885AE is specified over the extended  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range, and is available in a space-saving, 28-pin, 4mm x 4mm TQFN package.

### Applications

Notebook Computer—MXM/Switchable Graphics  
KVM for Servers

### Features

- ◆ Low  $5\Omega$  (typ) On-Resistance (R<sub>-</sub>, G<sub>-</sub>, B<sub>-</sub> Signals)
- ◆ Low 5.5pF (typ) On-Capacitance (R<sub>-</sub>, G<sub>-</sub>, B<sub>-</sub> Signals)
- ◆ Independent, Selectable Logic Inputs for Switching
- ◆ Similar Pin Configuration to MAX4885
- ◆ Ultra-Small, 28-Pin (4mm x 4mm) TQFN Package
- ◆  $\pm 15\text{kV}$  ESD HBM

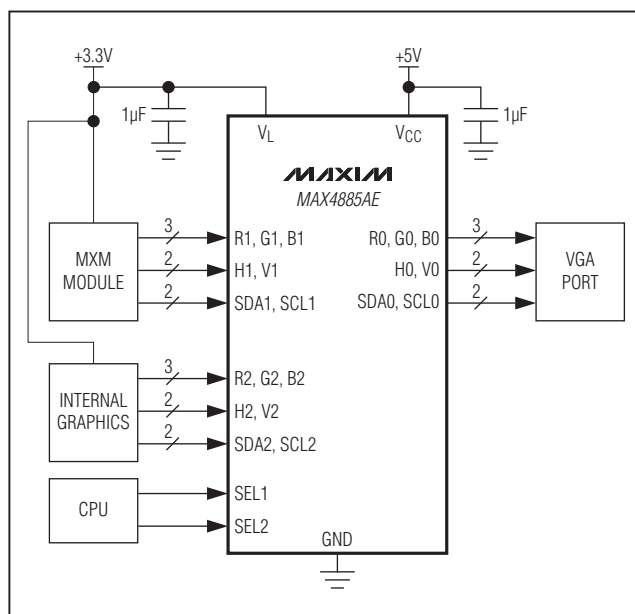
### Ordering Information

| PART          | TEMP RANGE                                     | PIN-PACKAGE |
|---------------|------------------------------------------------|-------------|
| MAX4885AEETI+ | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | 28 TQFN-EP* |

+ Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

### Typical Operating Circuit



# High-Bandwidth, VGA 2:1 Switch with $\pm 15\text{kV}$ ESD Protection

## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND unless otherwise noted.)

|                                                                                           |                                  |
|-------------------------------------------------------------------------------------------|----------------------------------|
| VCC.....                                                                                  | -0.3V to +6V                     |
| V <sub>L</sub> .....                                                                      | -0.3V to (VCC + 0.3V)            |
| R <sub>-</sub> , G <sub>-</sub> , B <sub>-</sub> , H0, V0, SDA0, SCL0.....                | -0.3V to (VCC + 0.3V)            |
| H1, H2, V1, V2, SDA1, SDA2, SCL1,<br>SCL2, SEL1, SEL2.....                                | -0.3V to (V <sub>L</sub> + 0.3V) |
| Continuous Current through R <sub>-</sub> , G <sub>-</sub> , B <sub>-</sub> Switches..... | $\pm 50\text{mA}$                |
| Continuous Current through SDA <sub>-</sub> , SCL <sub>-</sub> Switches.....              | $\pm 50\text{mA}$                |
| Continuous Current into SEL1, SEL2, H1, H2, V1, V2.....                                   | $\pm 20\text{mA}$                |
| Peak Current through all Switches<br>(pulsed at 1ms, 10% duty cycle).....                 | $\pm 100\text{mA}$               |

Continuous Power Dissipation (T<sub>A</sub> = +70°C)

28-Pin TQFN (derate 28.6mW/°C above +70°C).....2285.7mW  
Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) (Note 1)

28-Pin TQFN.....35°C/W  
Junction-to-Case Thermal Resistance ( $\theta_{JC}$ ) (Note 1)

28-Pin TQFN.....3°C/W

Operating Temperature Range.....-40°C to +85°C

Storage Temperature Range.....-65°C to +150°C

Junction Temperature.....+150°C

Lead Temperature (soldering, 10s).....+300°C

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maxim-ic.com/thermal-tutorial](http://www.maxim-ic.com/thermal-tutorial).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(VCC = +4.5V to +5.5V, V<sub>L</sub> = +2.2V to VCC, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

| PARAMETER                                                                  | SYMBOL                | CONDITIONS                                                                                   | MIN  | TYP | MAX  | UNITS |
|----------------------------------------------------------------------------|-----------------------|----------------------------------------------------------------------------------------------|------|-----|------|-------|
| Supply Voltage                                                             | VCC                   |                                                                                              | +4.5 |     | +5.5 | V     |
| Logic Supply Voltage                                                       | V <sub>L</sub>        | V <sub>L</sub> ≤ VCC                                                                         | +2.2 |     | VCC  | V     |
| VCC Supply Current                                                         | I <sub>CC</sub>       | VCC = +5.5V, V <sub>L</sub> = +3.6V,<br>SEL <sub>-</sub> = H1 = H2 = V1 = V2 = GND           |      | 2   | 5    | μA    |
| V <sub>L</sub> Supply Current                                              | I <sub>L</sub>        | VCC = +5.5V, V <sub>L</sub> = +3.6V,<br>SEL <sub>-</sub> = H1 = H2 = V1 = V2 = GND           |      |     | 1    | μA    |
| <b>ANALOG SWITCHES</b>                                                     |                       |                                                                                              |      |     |      |       |
| On-Resistance (R <sub>-</sub> , G <sub>-</sub> , B <sub>-</sub> )          | R <sub>HF-ON</sub>    | V <sub>IN</sub> = +0.7V, I <sub>IN</sub> = ±10mA                                             |      | 5   | 8    | Ω     |
| On-Resistance Match (R <sub>-</sub> , G <sub>-</sub> , B <sub>-</sub> )    | ΔR <sub>ON</sub>      | 0 ≤ V <sub>IN</sub> ≤ +0.7V, I <sub>IN</sub> = -10mA                                         |      |     | 1    | Ω     |
| On-Resistance Flatness (R <sub>-</sub> , G <sub>-</sub> , B <sub>-</sub> ) | R <sub>FLAT(ON)</sub> | 0 ≤ V <sub>IN</sub> ≤ +0.7V, I <sub>IN</sub> = -10mA                                         |      | 0.5 | 1    | Ω     |
| Off Leakage Current (R <sub>-</sub> , G <sub>-</sub> , B <sub>-</sub> )    | I <sub>OFF</sub>      | V <sub>R-</sub> , V <sub>G-</sub> , V <sub>B-</sub> = 0V or VCC                              | -1   |     | +1   | μA    |
| On-Resistance (SDA <sub>-</sub> , SCL <sub>-</sub> )                       | R <sub>DDCON</sub>    | V <sub>IN</sub> = +0.7V, I <sub>IN</sub> = ±10mA                                             |      | 15  |      | Ω     |
| Off-Leakage Current (SDA <sub>-</sub> , SCL <sub>-</sub> )                 | I <sub>OFF</sub>      | V <sub>SDA-</sub> , V <sub>SCL-</sub> = 0V or V <sub>L</sub> ,<br>VCC = V <sub>L</sub> = +5V | -1   |     | +1   | μA    |

# High-Bandwidth, VGA 2:1 Switch with $\pm 15\text{kV}$ ESD Protection

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +4.5\text{V}$  to  $+5.5\text{V}$ ,  $V_L = +2.2\text{V}$  to  $V_{CC}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .)

| PARAMETER                                    | SYMBOL            | CONDITIONS                                                                                | MIN               | TYP      | MAX               | UNITS         |
|----------------------------------------------|-------------------|-------------------------------------------------------------------------------------------|-------------------|----------|-------------------|---------------|
| <b>DIGITAL INPUTS (SEL_, H1, H2, V1, V2)</b> |                   |                                                                                           |                   |          |                   |               |
| Input Threshold Low                          | $V_{IL}$          |                                                                                           | $0.25 \times V_L$ |          |                   | V             |
| Input Threshold High                         | $V_{IH}$          |                                                                                           |                   |          | $0.55 \times V_L$ | V             |
| Input Hysteresis                             | $V_{HYST}$        |                                                                                           |                   | 100      |                   | mV            |
| Input Leakage Current                        | $I_L$             |                                                                                           | -1                |          | +1                | $\mu\text{A}$ |
| SEL_ Enable/Disable Time                     | $t_{ON}, t_{OFF}$ | $R_L = 2.2\text{k}\Omega$ , $C_L = 10\text{pF}$ , Figure 1                                |                   | 300      |                   | ns            |
| <b>DIGITAL OUTPUTS (H0, V0)</b>              |                   |                                                                                           |                   |          |                   |               |
| Output-Voltage Low                           | $V_{OL}$          | $I_{OUT} = 8\text{mA}$ , $V_{CC} = +4.5\text{V}$                                          |                   |          | 0.8               | V             |
| Output-Voltage High                          | $V_{OH}$          | $I_{OUT} = -8\text{mA}$ , $V_{CC} = +4.5\text{V}$                                         | 2.4               |          |                   | V             |
| Rise/Fall Time                               | $t_R, t_F$        | $R_L = 2.2\text{k}\Omega$ , $C_L = 10\text{pF}$ , Figure 2                                |                   |          | 8                 | ns            |
| <b>RGB AC PERFORMANCE</b>                    |                   |                                                                                           |                   |          |                   |               |
| Bandwidth                                    | $f_{MAX}$         | $R_S = R_L = 50\Omega$                                                                    |                   | 900      |                   | MHz           |
| On-Loss                                      | $I_{LOSS}$        | $f = 10\text{MHz}$ , $R_S = R_L = 50\Omega$ , $0 \leq V \leq +0.7\text{V}$ , Figure 3     |                   | 0.4      |                   | dB            |
| Crosstalk $R_-, G_-, B_-$                    | $V_{CT}$          | $f = 50\text{MHz}$ , $R_S = R_L = 50\Omega$ , Figure 3                                    |                   | -40      |                   | dB            |
| Off-Capacitance                              | $C_{OFF}$         | $f = 1\text{MHz}$ , $R_0$ to $R_1/R_2$ , $G_0$ to $G_1/G_2$ , $B_0$ to $B_1/B_2$ (Note 2) |                   | 2.5      |                   | pF            |
| On-Capacitance                               | $C_{ON}$          | $f = 1\text{MHz}$ , $R_0$ to $R_1/R_2$ , $G_0$ to $G_1/G_2$ , $B_0$ to $B_1/B_2$ (Note 2) |                   | 5.5      | 8                 | pF            |
| <b>ESD PROTECTION</b>                        |                   |                                                                                           |                   |          |                   |               |
| $R_0, G_0, B_0, SDA_0, SCL_0, H_0, V_0$      | $V_{ESD}$         | HBM (Notes 2, 3)                                                                          |                   | $\pm 15$ |                   | kV            |
| $R_0, G_0, B_0, SDA_0, SCL_0, H_0, V_0$      | $V_{ESD}$         | IEC 61000-4-2 Contact (Notes 2, 3)                                                        |                   | $\pm 8$  |                   | kV            |
| All Other Terminals                          | $V_{ESD}$         | HBM (Note 2)                                                                              |                   | $\pm 2$  |                   | kV            |

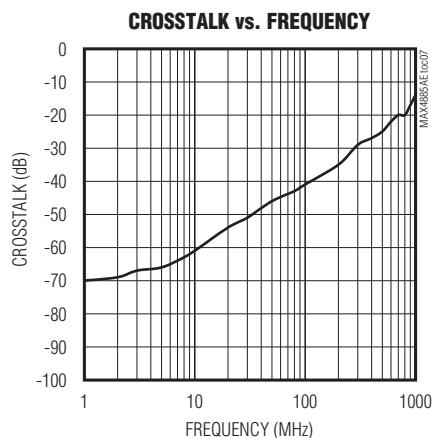
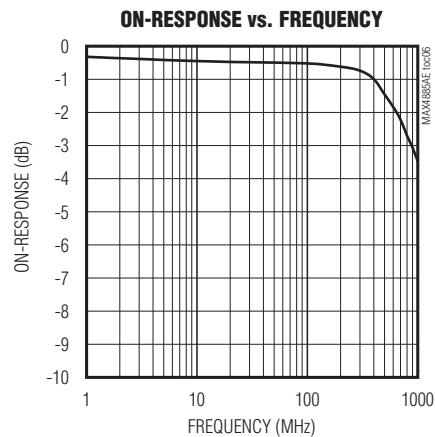
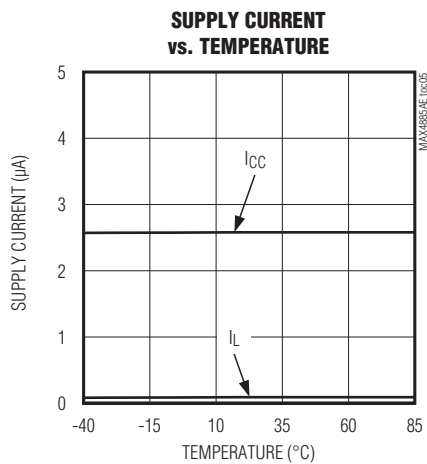
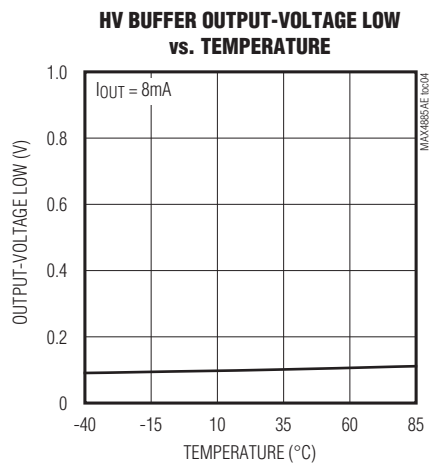
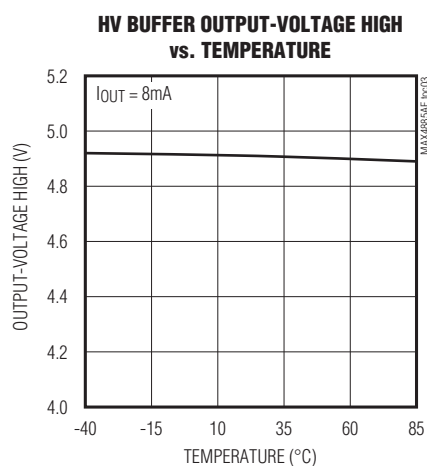
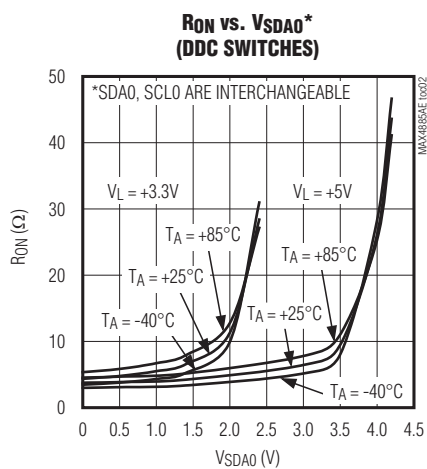
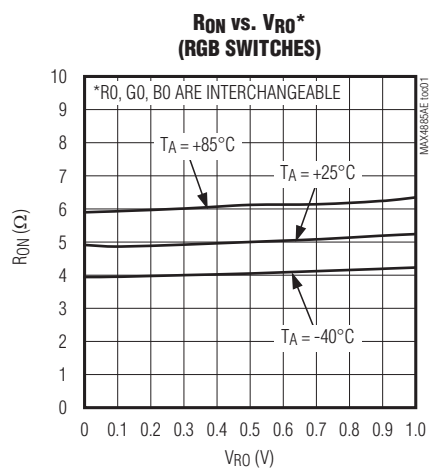
**Note 2:** Guaranteed by design. Not production tested.

**Note 3:** Tested terminal to GND,  $1\mu\text{F}$  bypass capacitors on  $V_{CC}$  and  $V_L$ .

# High-Bandwidth, VGA 2:1 Switch with $\pm 15\text{kV}$ ESD Protection

## Typical Operating Characteristics

( $V_{CC} = +5.0\text{V}$ ,  $V_L = +3.3\text{V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)



# High-Bandwidth, VGA 2:1 Switch with $\pm 15\text{kV}$ ESD Protection

## Test Circuits/Timing Diagrams

MAX4885AE

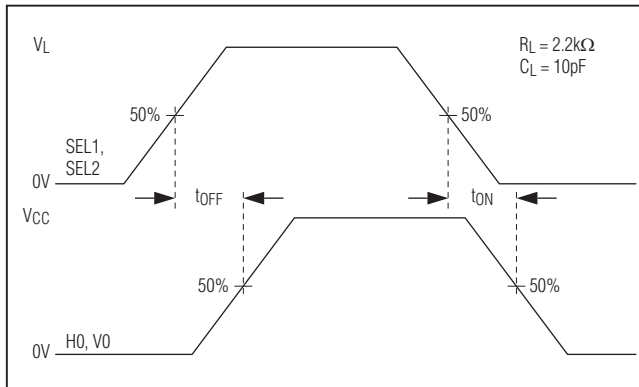


Figure 1. Enable/Disable Time

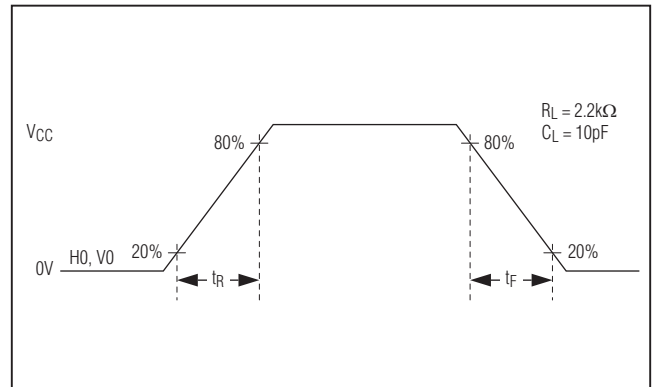


Figure 2. Rise/Fall Time

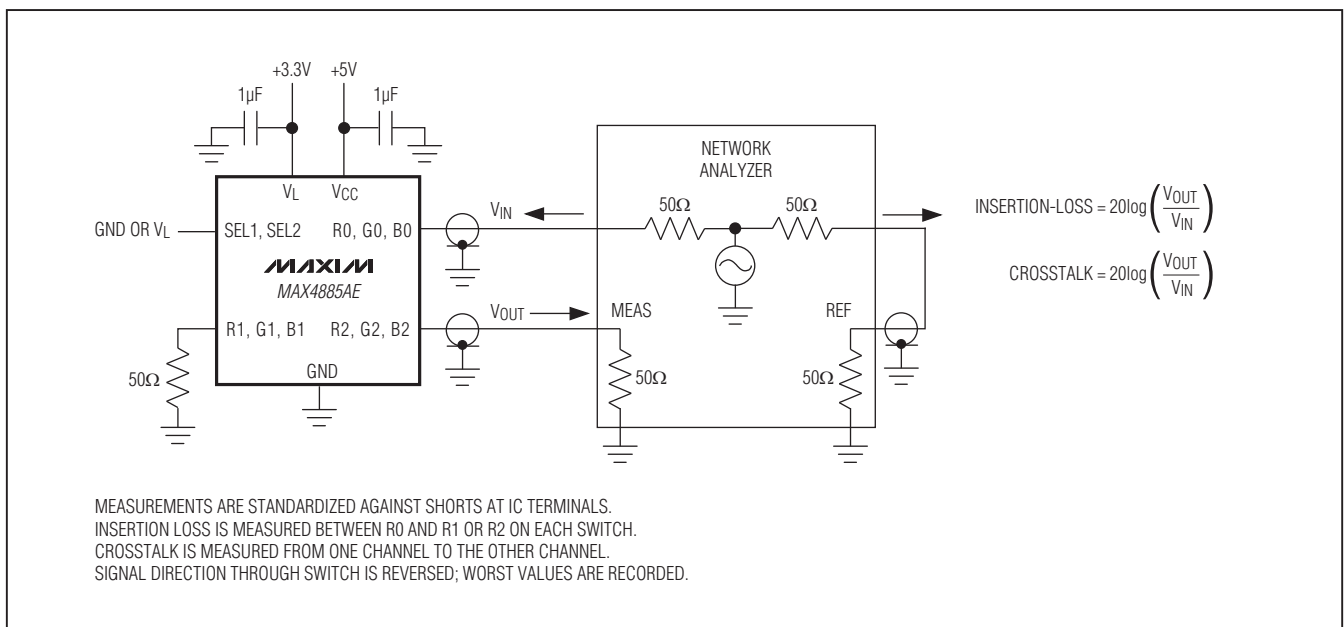
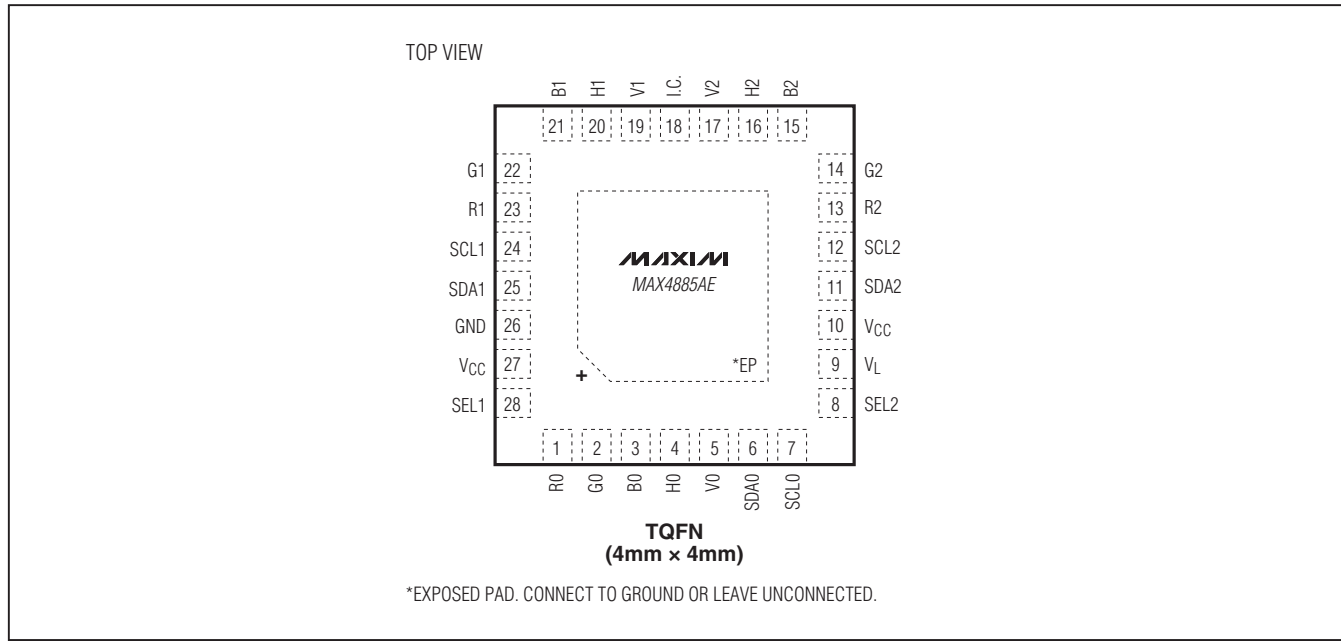


Figure 3. Insertion Loss and Crosstalk

# High-Bandwidth, VGA 2:1 Switch with $\pm 15\text{kV}$ ESD Protection

## Pin Configuration



## Pin Description

| PIN    | NAME | FUNCTION                                                                                                                             |
|--------|------|--------------------------------------------------------------------------------------------------------------------------------------|
| 1      | R0   | RGB Red Output (Note 4)                                                                                                              |
| 2      | G0   | RGB Green Output (Note 4)                                                                                                            |
| 3      | B0   | RGB Blue Output (Note 4)                                                                                                             |
| 4      | H0   | Horizontal Sync Output (Note 4)                                                                                                      |
| 5      | V0   | Vertical Sync Output (Note 4)                                                                                                        |
| 6      | SDA0 | I <sup>2</sup> C Data Output (Note 4)                                                                                                |
| 7      | SCL0 | I <sup>2</sup> C Clock Output (Note 4)                                                                                               |
| 8      | SEL2 | Select Input 2. Switches SDA <sub>-</sub> and SCL <sub>-</sub> signals.                                                              |
| 9      | VL   | Supply Voltage. $+2.2\text{V} \leq \text{VL} \leq \text{VCC}$ . Bypass VL to GND with a 1 $\mu\text{F}$ or larger ceramic capacitor. |
| 10, 27 | VCC  | Supply Voltage. $\text{VCC} = +5.0\text{V} \pm 10\%$ . Bypass VCC to GND with a 1 $\mu\text{F}$ or larger ceramic capacitor.         |
| 11     | SDA2 | I <sup>2</sup> C Input Data 2 (Note 5)                                                                                               |
| 12     | SCL2 | I <sup>2</sup> C Input Clock 2 (Note 5)                                                                                              |
| 13     | R2   | RGB Red Input 2 (Note 6)                                                                                                             |
| 14     | G2   | RGB Green Input 2 (Note 6)                                                                                                           |
| 15     | B2   | RGB-Blue Input 2 (Note 6)                                                                                                            |
| 16     | H2   | Horizontal Sync Input 2 (Note 7)                                                                                                     |
| 17     | V2   | Vertical Sync Input 2 (Note 7)                                                                                                       |
| 18     | I.C. | Internal Connection. Connect to ground or leave unconnected.                                                                         |
| 19     | V1   | Vertical Sync Input 1 (Note 7)                                                                                                       |
| 20     | H1   | Horizontal Sync Input 1 (Note 7)                                                                                                     |
| 21     | B1   | RGB Blue Input 1 (Note 6)                                                                                                            |

# High-Bandwidth, VGA 2:1 Switch with $\pm 15\text{kV}$ ESD Protection

## Pin Description (continued)

| PIN | NAME | FUNCTION                                                                                                                 |
|-----|------|--------------------------------------------------------------------------------------------------------------------------|
| 22  | G1   | RGB Green Input 1 (Note 6)                                                                                               |
| 23  | R1   | RGB Red Input 1 (Note 6)                                                                                                 |
| 24  | SCL1 | I <sup>2</sup> C Clock Input 1 (Note 5)                                                                                  |
| 25  | SDA1 | I <sup>2</sup> C Data Input 1 (Note 5)                                                                                   |
| 26  | GND  | Ground                                                                                                                   |
| 28  | SEL1 | Select Input 1. Switches R <sub>-</sub> , G <sub>-</sub> , B <sub>-</sub> , H <sub>-</sub> , and V <sub>-</sub> signals. |
| —   | EP   | Exposed Pad. Connect exposed pad to ground or leave unconnected.                                                         |

**Note 4:** Terminal with  $\pm 15\text{kV}$  HBM protection.

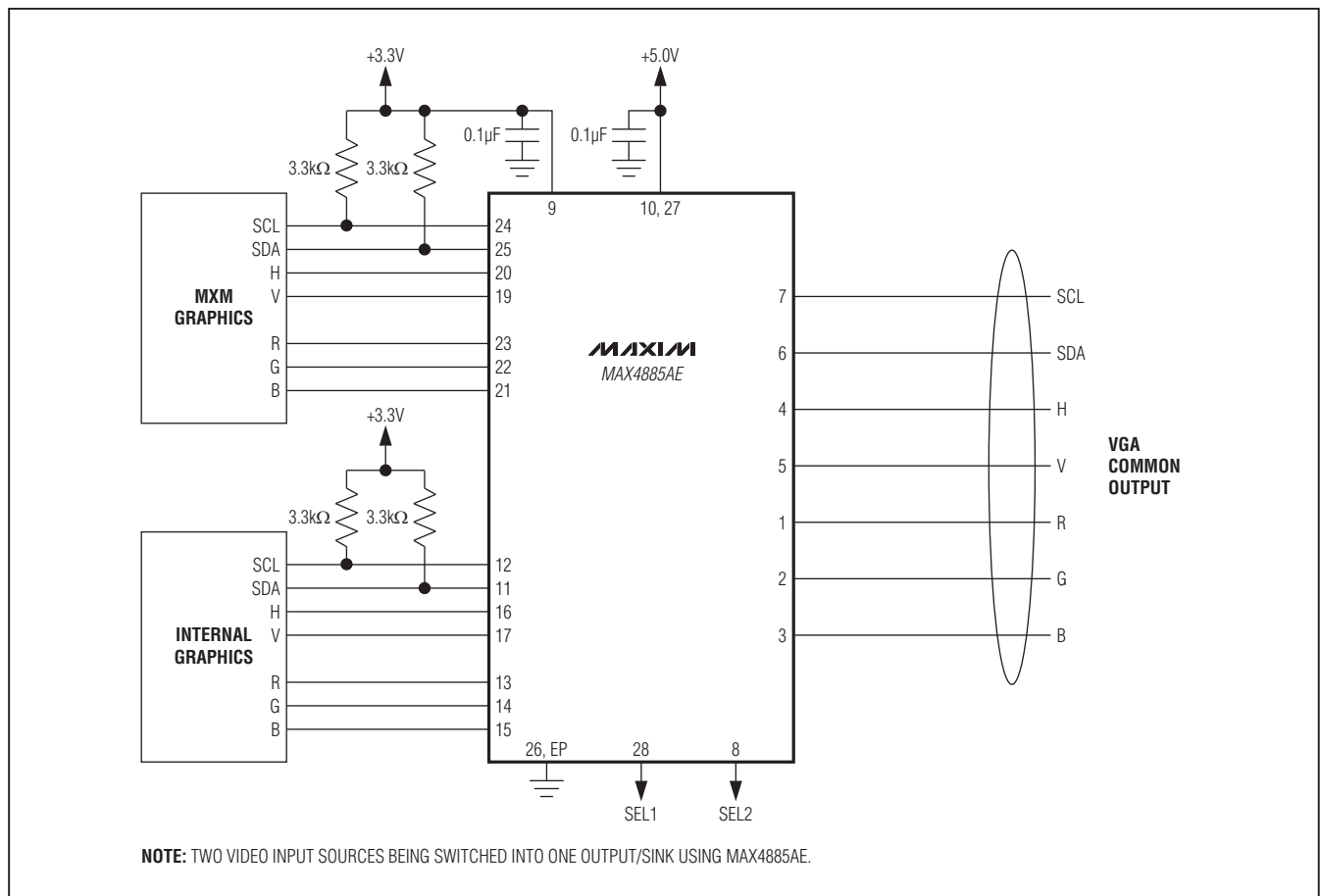
**Note 5:** SCL1, SCL2, SDA1, and SDA2 are identical and can be used interchangeably.

**Note 6:** R1, R2, G1, G2, B1, and B2 are identical and can be used interchangeably.

**Note 7:** H1, H2, V1, and V2 are identical and can be used interchangeably.

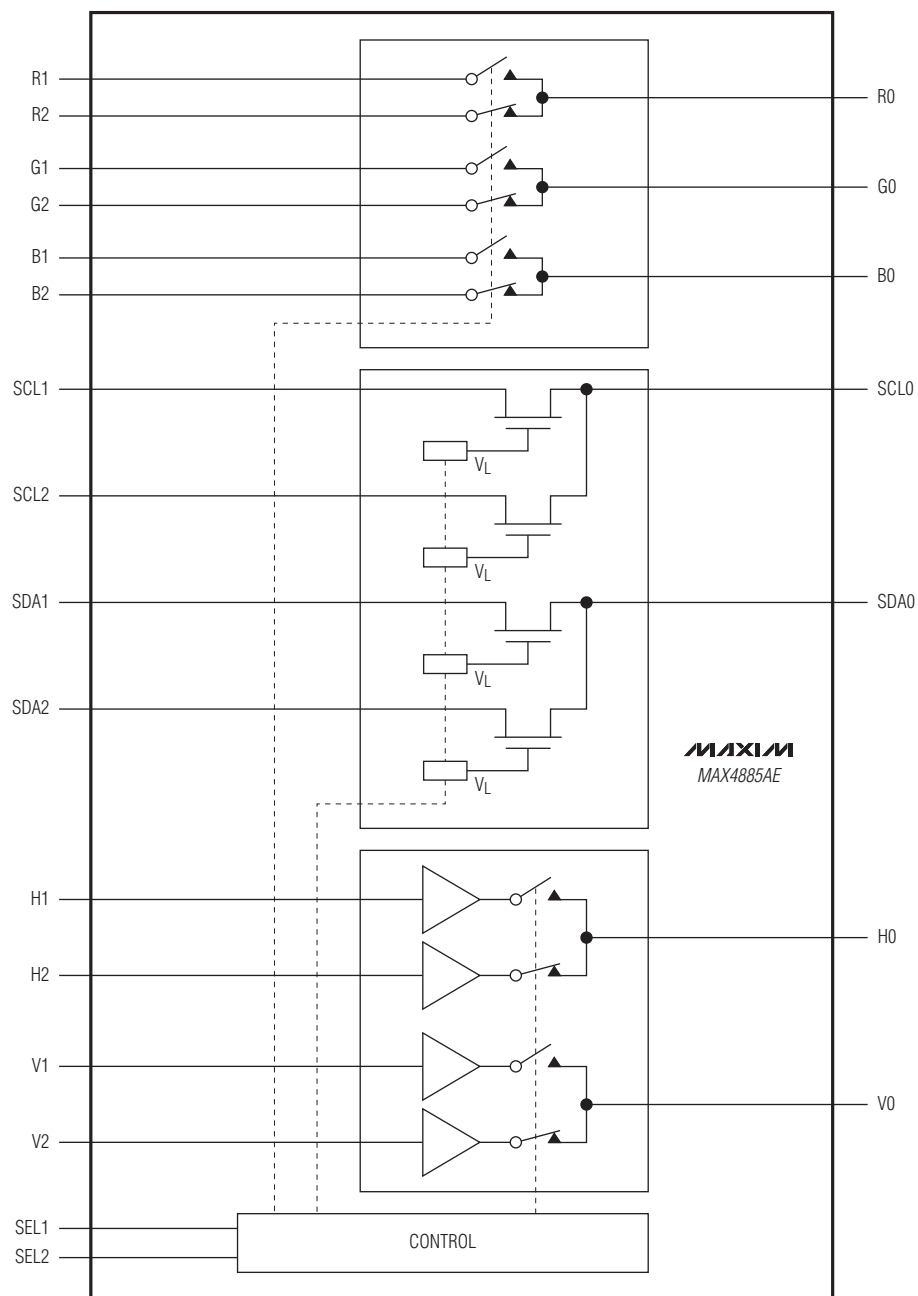
MAX4885AE

## Typical Applications Circuit



# High-Bandwidth, VGA 2:1 Switch with $\pm 15\text{kV}$ ESD Protection

## Functional Diagram





# High-Bandwidth, VGA 2:1 Switch with $\pm 15\text{kV}$ ESD Protection

## Detailed Description

The MAX4885AE integrates high-bandwidth analog switches and level-translating buffers to implement a complete 2:1 multiplexer for VGA signals. The device provides switching for RGB, HSYNC, VSYNC, SDA, and SCL signals. These signals are required in notebook VGA switching applications.

The HSYNC and VSYNC inputs feature level-shifting buffers to support 5V-TTL output logic levels from low-voltage graphics controllers. These buffered switches can be driven from +2.0V up to +5.5V. RGB signals are routed with high-performance analog switches. SDA\_ and SCL\_ are I<sup>2</sup>C signals with pullups to their respective voltages. The MAX4885AE protects the low-voltage side while effectively translating up to the high-voltage level.

Two select inputs are provided to individually select groups of switches.

RGB, HSYNC, and VSYNC signals are controlled by SEL1; and both SDA\_ and SCL\_ signals are controlled by SEL2.

**Table 1. RGB/HV Truth Table**

| SEL1 | FUNCTION                         |                      |
|------|----------------------------------|----------------------|
| 0    | R1 to R0<br>G1 to G0<br>B1 to B0 | H1 to H0<br>V1 to V0 |
| 1    | R2 to R0<br>G2 to G0<br>B2 to B0 | H2 to H0<br>V2 to V0 |

**Table 2. DDC Truth Table**

| SEL2 | FUNCTION                     |
|------|------------------------------|
| 0    | SDA1 to SDA0<br>SCL1 to SCL0 |
| 1    | SDA2 to SDA0<br>SCL2 to SCL0 |

## RGB Switches

The MAX4885AE provides three SPDT high-bandwidth switches to route standard VGA R\_, G\_, and B\_ signals (see Table 1). The R\_, G\_, and B\_ analog switches are identical and any of the three switches can be used to route red, green, or blue video signals. The R0, G0, and B0 outputs are ESD protected to  $\pm 15\text{kV}$  (HBM).

## Horizontal/Vertical Sync Level Shifter

H1, H2, V1, and V2 inputs are buffered to provide level-shifting and drive capability for horizontal/vertical sync signals that meet the VESA specification. The H\_ and V\_ level-shifters are identical, and each level-shifter can be used for either horizontal or vertical signals. The H0 and V0 outputs are ESD protected to  $\pm 15\text{kV}$  (HBM).

## Display-Data Channel Multiplexer

The MAX4885AE provides two logic-level translating switches to route DDC signals (see Table 2). V<sub>L</sub> is normally set to +3.3V to provide logic-shifting for VESA I<sup>2</sup>C-compatible signals. The MAX4885AE protects the low-voltage graphics controller from +5V that could be present in VESA-compatible monitors. In some applications, such as KVM, where logic-level shifting is not required, then V<sub>L</sub> can be connected to V<sub>CC</sub>. The SDA\_ and SCL\_ switches are identical, and each switch can be used to route either SDA\_ or SCL\_ signals. The SDA0 and SCL0 outputs are ESD protected to  $\pm 15\text{kV}$  (HBM).

## ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. Additionally, the R0, G0, B0, H0, V0, SDA0, and SCL0 terminals of the MAX4885AE are designed for protection to the following limit:  $\pm 15\text{kV}$  using the HBM.

For optimum ESD performance, bypass V<sub>CC</sub> and V<sub>L</sub> pins to ground with 1 $\mu\text{F}$  or larger ceramic capacitors as close as possible to these supply pins.

# High-Bandwidth, VGA 2:1 Switch with $\pm 15\text{kV}$ ESD Protection

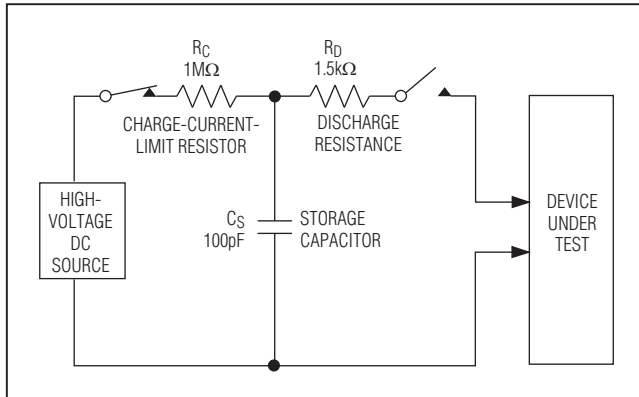


Figure 4. Human Body ESD Test Model

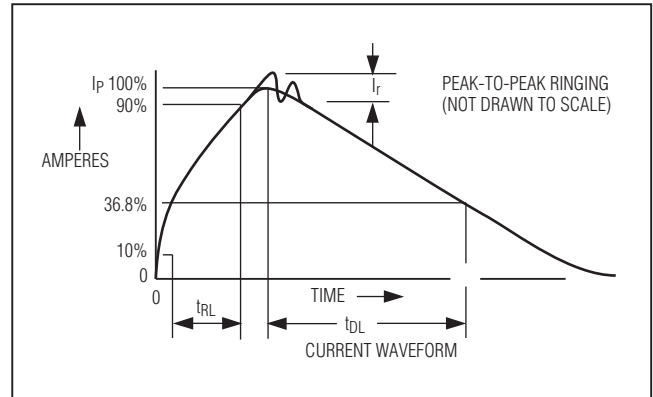


Figure 5. Human Body Model Current Waveform

## Human Body Model

Figure 4 shows the HBM, and Figure 5 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

## ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report, test setup, methodology, and results.

## Applications Information

The MAX4885AE provides the switching and level-shifting necessary to drive a standard VGA port from either an internal graphics controller or an add-in module (MXM or GPU—see *Typical Applications Circuit*). The R<sub>-</sub>, G<sub>-</sub>, and B<sub>-</sub> signals are switched through the three low-capacitance SPDT switches. Internal buffers drive the HSYNC and VSYNC signals to VGA standard 5V-TTL levels. The DDC multiplexer provides level-shifting. Connect V<sub>L</sub> to +3.3V for normal operation, or to V<sub>CC</sub> to disable level-shifting for DDC signals as for KVM application.

## Power-Supply Decoupling

Bypass each V<sub>CC</sub> pin and V<sub>L</sub> pin to ground with a 1μF or larger ceramic capacitor as close as possible to the device.

## PCB Layout

High-speed switches such as the MAX4885AE requires proper PCB layout for optimum performance. Ensure that impedance-controlled PCB traces for high-speed signals are matched in length and as short as possible. Connect the exposed pad to ground or leave unconnected.

## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO.            |
|--------------|--------------|-------------------------|
| 28 TQFN-EP   | T2844+1      | <a href="#">21-0139</a> |

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401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd  
Minhang District, Shanghai , China

➤ Sales :

Direct    +86 (21) 6401-6692  
Email     amall@ameya360.com  
QQ        800077892  
Skype     ameyasales1 ameyasales2

➤ Customer Service :

Email     service@ameya360.com

➤ Partnership :

Tel        +86 (21) 64016692-8333  
Email     mkt@ameya360.com