PRELIMINARY PRODUCT SPECIFICATION



Z8S180/Z8L180 ENHANCED Z180 MICROPROCESSOR OFFERS FASTER EXECUTION, POWER-SAVER MODE, LOW EMI

FEATURES

- Code Compatible with ZiLOG Z80[®] CPU
- Extended Instructions
- Two Chain-Linked DMA Channels
- Low Power-Down Modes
- On-Chip Interrupt Controllers
- Three On-Chip Wait-State Generators
- On-Chip Oscillator/Generator
- Expanded MMU Addressing (Up to 1 MB)
- Clocked Serial I/O Port

- Two 16-Bit Counter/Timers
- Two Enhanced UARTs (up to 512 Kbps)
- Clock Speeds: 10, 20, 33 MHz
- Operating Range: 5V (3.3V@ 20 MHz)
- Operating Temperature Range: 0°C to +70°C
- -40°C to +85°C Extended Temperature Range
- Three Packaging Styles
 - 68-Pin PLCC
 - 64-Pin DIP
 - 80-Pin QFP

GENERAL DESCRIPTION

The enhanced Z8S180/Z8L180TM significantly improves on previous Z80180 models, while still providing full backward compatibility with existing ZiLOG Z80 devices. The Z8S180/Z8L180 now offers faster execution speeds, power-saving modes, and EMI noise reduction.

This enhanced $Z180^{TM}$ design also incorporates additional feature enhancements to the ASCIs, DMAs, and STANDBY mode power consumption. With the addition of ESCC-like Baud Rate Generators (BRGs), the two ASCIs offer the flex-ibility and capability to transfer data asynchronously at rates of up to 512 Kbps. In addition, the ASCI receiver features a 4-byte first in/first out (FIFO) buffer which reduces the likelihood of overrun errors. The DMAs have been modified to allow for chain-linking of the two DMA channels when set to take their DMA requests from the same peripherals device. This feature allows for nonstop DMA operation between the two DMA channels.

Not only does the Z8S180/Z8L180 consume less power during normal operations than the previous model, it offers three modes intended to further reduce power consumption. Power consumption during STANDBY Mode is reduced to 10 μ A by stopping the external oscillators and internal clock. The SLEEP mode reduces power by placing the CPU into a stopped state, consuming less current while the on-chip I/O devices still operate. The SYSTEM STOP mode places both the CPU and the on-chip peripherals into a stopped mode, reducing power consumption even further.

A new clock-doubler feature in the Z8S180/Z8L180 allows the internal clock speed to be twice the external clock speed. As a result, system cost is reduced by allowing the use of lower-cost, lower-frequency crystals.

The Enhanced Z180 is housed in 80-pin QFP, 68-pin PLCC, and 64-pin DIP packages.

Note: All Signals with an overline are active Low. For example: B/\overline{W} , in which WORD is active Low; or \overline{B}/W , in which BYTE is active Low.

GENERAL DESCRIPTION (Continued)

Power connections follow the conventional descriptions below:

Connection	Circuit	Device	Device		
Power	V _{CC}	V _{DD}			
Ground	GND	V _{SS}			





PIN IDENTIFICATION





PIN IDENTIFICATION (Continued)



Figure 3. Z8S180/Z8L180 68-Pin PLCC Pin Configuration





Pin Num	Pin Number and Package Type		Default Secondary				
QFP	PLCC	DIP	Function	Function	Control		
1	9	8	NMI				
2			NC				
3			NC				
4	10	9	INTO				
5	11	10	INT1				
6	12	11	INT2				
7	13	12	ST				
8	14	13	AO				
9	15	14	A1				
10	16	15	A2				
11	17	16	A3				
12	18		V _{SS}				

	Table 1.	Z8S180/Z8L	.180 Pin	Identification
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PIN IDENTIFICATION (Continued)

Table 1.	Z8S180/Z8L180	Pin Identification	(Continued)
	200100/202100		(Continucu)

Pin Num	Pin Number and Package Type		Default	Secondary			
QFP	PLCC	DIP	Function	Function	Control		
13	19	17	A4				
14			NC				
15	20	18	A5				
16	21	19	A6				
17	22	20	A7				
18	23	21	A8				
19	24	22	A9				
20	25	23	A10				
21	26	24	A11				
22			NC				
23			NC				
24	27	25	A12				
25	28	26	A13				
26	29	27	A14				
27	30	28	A15				
28	31	29	A16				
29	32	30	A17				
30			NC				
31	33	31	A18	T _{OUT}	Bit 2 or Bit 3 of TCR		
32	34	32	V _{DD}				
33	35		A19				
34	36	33	V _{SS}				
35	37	34	D0				
36	38	35	D1				
37	39	36	D2				
38	40	37	D3				
39	41	38	D4				
40	42	39	D5				
41	43	40	D6				
42			NC				
43			NC				
44	44	41	D7				
45	45	42	RTSO				
46	46	43	CTS0				
47	47	44	DCD0				
48	48	45	TXA0				
49	49	46	RXA0				
50	50	47	CKA0	DREQO	Bit 3 or Bit 5 of DMODE		
51			NC				
52	51	48	TXA1				

Pin Num	ber and Packa	ige Type	Default	Secondary	
QFP	PLCC	DIP	Function	Function	Control
53	52		TEST		
54	53	49	RXA1		
55	54	50	CKA1	TENDO	Bit 4 of CNTLA1
56	55	51	TXS		
57	56	52	RXS	CTS1	Bit 2 of STAT1
58	57	53	CKS		
59	58	54	DREQ1		
60	59	55	TEND1		
61	60	56	HALT		
62			NC		
63			NC		
64	61	57	RFSH		
65	62	58	IORQ		
66	63	59	MREQ		
67	64	60	E		
68	65	61	<u>M1</u>		
69	66	62	WR		
70	67	63	RD		
71	68	64	PHI		
72	1	1	V _{SS}		
73	2		V _{SS}		
74	3	2	XTAL		
75			NC		
76	4	3	EXTAL		
77	5	4	WAIT		
78	6	5	BUSACK		
79	7	6	BUSREQ		
80	8	7	RESET		

Table 1. Z8S180/Z8L180 Pin Identification (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes

$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Pin Num	ber and Packa	ige Type			Pin Status		
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$				Default	Secondary			
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	QFP	PLCC	DIP	Function	Function	RESET	BUSACK	SLEEP
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	1	9	8	NMI		IN	IN	IN
3 NC 4 10 9 INTO IN IN IN IN 5 11 10 INTT IN IN IN IN 6 12 11 INTZ IN IN IN IN 7 13 12 ST High High High 8 14 13 AO 3T 3T High 9 15 14 A1 3T 3T High 10 16 15 A2 3T 3T High 11 17 16 A3 3T 3T High 14 NC NC NC 14 NC NC NG 15 20 18 A5 3T 3T High 16 21 19 A6 3T 3T	2			NC				
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	3			NC				
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	4	10	9	INTO		IN	IN	IN
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	5	11	10	INT1		IN	IN	IN
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	6	12	11	INT2		IN	IN	IN
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	7	13	12	ST		High	High	High
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	8	14	13	AO		3Т	3Т	High
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	9	15	14	A1		3Т	3Т	High
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	10	16	15	A2		3Т	3Т	High
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	11	17	16	A3		3Т	3Т	High
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	12	18		V _{SS}		V _{SS}	V _{SS}	V_{SS}
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	13	19	17	A4		3Т	3Т	High
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	14			NC				
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	15	20	18	A5		ЗТ	3Т	High
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	16	21	19	A6		ЗТ	3Т	High
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	17	22	20	A7		ЗТ	3Т	High
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	18	23	21	A8		3Т	3Т	High
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	19	24	22	A9		3Т	3Т	High
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	20	25	23	A10		3Т	3Т	High
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	21	26	24	A11		3Т	3Т	High
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	22			NC				
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	23			NC				
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	24	27	25	A12		3Т	3Т	High
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	25	28	26	A13		3Т	3Т	High
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	26	29	27	A14		3Т	3Т	High
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	27	30	28	A15		3Т	3Т	High
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	28	31	29	A16		3Т	3T	High
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	29	32	30	A17		3Т	3Т	High
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	30			NC				
$\begin{tabular}{ c c c c c c c c c c c c c c c c } \hline T_{OUT} & N/A & OUT & OUT & OUT \\ \hline 32 & 34 & 32 & V_{DD} & V_{DD} & V_{DD} & V_{DD} \\ \hline 33 & 35 & $A19$ & $3T$ & $3T$ & $High$ \\ \hline 34 & 36 & 33 & V_{SS} & V_{SS} & V_{SS} & V_{SS} \\ \hline 35 & 37 & 34 & $D0$ & $3T$ & $3T$ & $3T$ \\ \hline 36 & 38 & 35 & $D1$ & $3T$ & $3T$ & $3T$ \\ \hline 37 & $3T$ & $3T$ & $3T$ \\ \hline 37 & 38 & 35 & $D1$ & $3T$ & $3T$ & $3T$ \\ \hline 37 & $3T$ & $3T$ & $3T$ & $3T$ \\ \hline 37 & 38 & 35 & $D1$ & $3T$ & $3T$ & $3T$ \\ \hline 37 & $3T$ & $3T$ & $3T$ & $3T$ & $3T$ & $3T$ \\ \hline 36 & 38 & 35 & $D1$ & $3T$ & $3T$ & $3T$ & $3T$ \\ \hline 37 & $3T$ $	31	33	31	A18		3Т	3Т	High
				T _{OUT}		N/A	OUT	OUT
33 35 A19 3T 3T High 34 36 33 V _{SS} V _{SS} V _{SS} V _{SS} 35 37 34 D0 3T 3T 3T 3T 36 38 35 D1 3T 3T 3T 3T	32	34	32	V_{DD}		V_{DD}	V_{DD}	V_{DD}
34 36 33 V _{SS} V _{SS} V _{SS} V _{SS} 35 37 34 D0 3T 3T 3T 36 38 35 D1 3T 3T 3T	33	35		A19		3Т	3Т	High
35 37 34 D0 3T 3T 3T 36 38 35 D1 3T 3T 3T	34	36	33	V _{SS}		V _{SS}	V _{SS}	V _{SS}
36 38 35 D1 3T 3T 3T	35	37	34	DO		3Т	3Т	ЗT
	36	38	35	D1		3Т	3Т	ЗT
37 39 36 D2 3T 3T 3T	37	39	36	D2		3Т	3Т	3T
38 40 37 D3 3T 3T 3T	38	40	37	D3		3T	ЗТ	3T

Pin Number and Package Type **Pin Status** Default Secondary QFP PLCC DIP Function Function RESET BUSACK SLEEP D4 39 41 38 3T 3T 3T 40 42 39 D5 ЗT 3T ЗT 41 43 40 D6 ЗT ЗT ЗT 42 NC NC 43 D7 44 ЗT ЗT 44 41 3T 45 45 42 **RTSO** OUT High High 46 46 43 CTS0 OUT IN IN DCD0 47 47 44 IN IN IN OUT OUT 48 48 45 TXA0 High 49 49 46 RXA0 IN IN IN 47 ЗT I/O I/O 50 50 CKA0 **DREQ0** N/A IN IN 51 NC 52 51 48 TXA1 OUT OUT High 52 TEST 53 53 49 RXA1 IN IN IN 54 I/O I/O 55 54 50 CKA1 ЗT **TENDO** N/A High High TXS OUT OUT 56 55 51 High 57 56 52 RXS IN IN IN CTS1 N/A IN IN 58 57 53 CKS 3T I/O I/O 58 54 DREQ1 IN ЗT IN 59 60 59 55 TEND1 OUT High High HALT 60 56 High 61 High Low 62 NC NC 63 RFSH 57 OUT 64 61 High High 58 IORQ 3T 65 62 High High 66 63 59 MREQ High ЗT High 67 64 Е Low OUT 60 OUT M1 68 65 61 High High High WR 69 66 62 3T High High 70 67 63 RD ЗT High High 71 68 64 PHI OUT OUT OUT V_{SS} 72 1 1 GND GND GND 73 2 GND V_{SS} GND GND 3 74 **XTAL** OUT OUT 2 OUT NC 75

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

PIN IDENTIFICATION (Continued)

Pin Num	ber and Packa	age Type	Pin Status				
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
76	4	3	EXTAL		IN	IN	IN
77	5	4	WAIT		IN	IN	IN
78	6	5	BUSACK		High	OUT	OUT
79	7	6	BUSREQ		IN	IN	IN
80	8	7	RESET		IN	IN	IN

PIN DESCRIPTIONS

A0–A19 Address Bus (Output, 3-state). A0–A19 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 1 MB) and I/O data bus exchanges (up to 64 KB). The address bus enters a high–impedance state during reset and external bus acknowledge cycles. Address line A18 is multiplexed with the output of PRT channel 1 (T_{OUT} , selected as address output on reset), and address line A19 is not available in DIP versions of the Z8S180.

BUSACK. Bus Acknowledge (Output, active Low). BUSACK indicates that the requesting device, the MPU address and data bus, and some control signals enter their high-impedance state.

BUSREQ. Bus Request (Input, active Low). This input is used by external devices (such as DMA controllers) to request access to the system bus. This request demands a higher priority than $\overline{\text{NMI}}$ and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions, places addresses, data buses, and other control signals into the high-impedance state.

CKAO, **CKA1**. Asynchronous Clock 0 and 1 (bidirectional). When in output mode, these pins are the transmit and receive clock outputs from the ASCI baud rate generators. When in input mode, these pins serve as the external clock inputs for the ASCI baud rate generators. CKAO is multiplexed with DREQO, and CKA1 is multiplexed with TENDO.

CKS. Serial Clock (bidirectional). This line is the clock for the CSI/O channel.

CTSO–**CTS1**. Clear to send 0 and 1 (Inputs, active Low). These lines are modem control signals for the ASCI channels. $\overline{CTS1}$ is multiplexed with RXS.

D0–D7. Data Bus = (bidirectional, 3-state). D0–D7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high-impedance state during reset and external bus acknowledge cycles.

DCDO. Data Carrier Detect 0 (Input, active Low); a programmable modem control signal for ASCI channel 0.

DREQO, **DREQ1**. DMA Request 0 and 1 (Input, active Low). **DREQ** is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a READ or WRITE operation. These inputs can be programmed to be either level or edge sensed. **DREQO** is multiplexed with CKAO.

E. Enable Clock (Output). This pin functions as a synchronous, machine-cycle clock output during bus transactions.

EXTAL. External Clock Crystal (Input). Crystal oscillator connections. An external clock can be input to the Z8S180/Z8L180 on this pin when a crystal is not used. This input is Schmitt triggered.

HALT. HALT/SLEEP (Output, active Low). This output is asserted after the CPU executes either the HALT or SLEEP instruction and is waiting for either a nonmaskable or a maskable interrupt before operation can resume. It is also used with the $\overline{M1}$ and ST signals to decode the status of the CPU machine cycle.

INTO. Maskable Interrupt Request 0 (Input, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$ and $\overline{\text{BUSREQ}}$ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ signals become active.

INT1, **INT2**. Maskable Interrupt Request 1 and 2 (Inputs, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the NMI, BUSREQ, and INTO signals are inactive. The CPU acknowledges these requests with an interrupt acknowledge cycle. Unlike the acknowledgment for INTO, neither the M1 or IORQ signals become active during this cycle.

IORQ. I/O Request (Output, active Low, 3-state). **IORQ** indicates that the address bus contains a valid I/O address for an I/O READ or I/O WRITE operation. **IORQ** is also generated, along with $\overline{M1}$, during the acknowledgment of the INTO input signal to indicate that an interrupt response vector can be place onto the data bus. This signal is analogous to the IOE signal of the Z64180.

M1. Machine Cycle 1 (Output, active Low). Together with $\overline{\text{MREQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is the opcodefetch cycle of instruction execution. Together with $\overline{\text{IORQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is for interrupt acknowledgment. It is also used with the $\overline{\text{HALT}}$ and ST signal to decode the status of the CPU machine cycle. This signal is analogous to the $\overline{\text{LIR}}$ signal of the Z64180.

MREQ. Memory Request (Output, active Low, 3-state). **MREQ** indicates that the address bus holds a valid address for a memory READ or memory WRITE operation. This signal is analogous to the $\overline{\text{ME}}$ signal of Z64180.

NMI. Nonmaskable Interrupt (Input, negative edge triggered). $\overline{\text{NMI}}$ demands a higher priority than $\overline{\text{INT}}$ and is al-

PIN DESCRIPTIONS (Continued)

ways recognized at the end of an instruction, regardless of the state of the interrupt-enable flip-flops. This signal forces CPU execution to continue at location 0066H.

PHI. System Clock (Output). The output is used as a reference clock for the MPU and the external system. The frequency of this output may be one-half, equal to, or twice the crystal or input clock frequency.

RD. Read (Output, active Low, 3-state). **RD** indicates that the CPU wants to read data from either memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

RFSH. Refresh (Output, active Low). Together with $\overline{\text{MREQ}}$, RFSH indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low-order 8 bits of the address bus (A7–A0) contain the refresh address. *This signal is analogous* to the \overline{REF} signal of the Z64180.

RTSO. Request to Send 0 (Output, active Low); a programmable MODEM control signal for ASCI channel 0.

RXA0, RXA1. Receive Data 0 and 1 (Input). These signals are the receive data for the ASCI channels.

RXS. Clocked Serial Receive Data (Input). This line is the receive data for the CSI/O channel. RXS is multiplexed with the $\overline{\text{CTS1}}$ signal for ASCI channel 1.

ST. Status (Output). This signal is used with the $\overline{M1}$ and \overline{HALT} output to decode the status of the CPU machine cycle. See Table 3.

Table 3. Status Summary

ST	HALT	M1	Operation
0	1	0	CPU Operation (1st Opcode Fetch)
1	1	0	CPU Operation (2nd Opcode and 3rd Opcode Fetch)
1	1	1	CPU Operation (MC Except Opcode Fetch)
0	Х	1	DMA Operation
0	0	0	HALT Mode
1	0	1	SLEEP Mode (Including SYSTEM STOP Mode)
Note	s:		
X =	Do not o	care.	

MC = Machine Cycle.

TENDO, **TEND1**. Transfer End 0 and 1 (Outputs, active Low). This output is asserted active during the most recent WRITE cycle of a DMA operation. It is used to indicate the end of the block transfer. **TENDO** is multiplexed with CKA1.

TEST. Test (Output, not in DIP version). This pin is for test and should be left open.

 T_{OUT} . Timer Out (Output). T_{OUT} is the output from PRT channel 1. This line is multiplexed with A18 of the address bus.

TXA0, TXA1. Transmit Data 0 and 1 (Outputs). These signals are the transmitted data from the ASCI channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

TXS. Clocked Serial Transmit Data (Output). This line is the transmitted data from the CSI/O channel.

WAIT. Wait (Input, active Low). WAIT indicates to the MPU that the addressed memory or I/O devices are not ready for data transfer. This input is sampled on the falling edge of T2 (and subsequent WAIT states). If the input is sampled Low, then the additional WAIT states are inserted until the WAIT input is sampled High, at which time execution continues.

WR. WRITE (Output, active Low, 3-state). WR indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

XTAL. Crystal Oscillator Connection (Input). This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (see <u>DC Characteristics</u>).

Several pins are used for different conditions, depending on the circumstance.

A18/TOUT	During RESET, this pin is initialized as A18. If either the TOC1 or the TOC0 bit of the Timer Control register (TCR) is set to 1, the T_{OUT} function is selected. If TOC1 and TOC0 are cleared to 0, the A18 function is selected.
CKA0/DREQ0	During RESET, this pin is initialized as CKA0. If either DM1 or SM1 in the DMA Mode register (DMODE) is set to 1, the DREQ0 function is selected.
CKA1/TENDO	During RESET, this pin is initialized as CKA1. If the CKA1D bit in ASCI control register ch1 (CNTLA1) is set to 1, the TENDO function is selected. If the CKA1D bit is set to 0, the CKA1 function is selected.
RXS/CTS1	During RESET, this pin is initialized as RXS. If the CTS1E bit in the ASCI status register ch1 (STAT1) is set to 1, the $\overline{\text{CTS1}}$ function is selected. If the CTS1E bit is set to 0, the RXS function is selected.

Table 4. Multiplexed Pin Descriptions

ARCHITECTURE

The Z180 combines a high-performance CPU core with a variety of system and I/O resources useful in a broad range of applications. The CPU core consists of five functional blocks: clock generator, bus state controller, Interrupt controller, memory management unit (MMU), and the central processing unit (CPU). The integrated I/O resources make up the remaining four functional blocks: direct memory access (DMA) control (2 channels), asynchronous serial communication interface (ASCI, 2 channels) programmable reload timers (PRT, 2 channels), and a clock serial I/O (CSI/O) channel.

Clock Generator. This logic generates a system clock from an external crystal or clock input. The external clock is divided by 2 or 1 and provides the timing for both internal and external devices.

Bus State Controller. This logic performs all of the status and bus-control activity associated with the CPU and some on-chip peripherals. Also includes wait-state timing, reset cycles, DRAM refresh, and DMA bus exchanges.

Interrupt Controller. This logic monitors and prioritizes the variety of internal and external interrupts and traps to provide the correct responses from the CPU. To maintain compatibility with the Z80 CPU, three different interrupts modes are supported.

Memory Management Unit. The MMU allows the user to map the memory used by the CPU (logically only 64KB) into the 1-MB addressing range supported by the Z8S180/Z8L180. The organization of the MMU object

Central Processing Unit. The CPU is microcoded to provide a core that is object-code compatible with the Z80 CPU. It also provides a superset of the Z80 instruction set, including 8-bit multiplication. The core is modified to allow many of the instructions to execute in fewer clock cycles.

DMA Controller. The DMA controller provides highspeed transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory to/from I/O, and I/O-to-I/O. Transfer modes supported are request, burst, and cycle steal. DMA transfers can access the full 1-MB address range with a block length up to 64 KB, and can cross over 64K boundaries.

Asynchronous Serial Communication Interface (ASCI).

The ASCI logic provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels can also support a multiprocessor communication format as well as break detection and generation

Programmable Reload Timers (PRT). This logic consists of two separate channels, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is derived from the system clock (divided by 20) before reaching the counter. PRT channel 1 provides an optional output to allow for waveform generation.



Figure 5. Timer Initialization, Count Down, and Reload Timing



Clocked Serial I/O (CSI/O). The CSI/O channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another microprocessor or microcomputer. TRDR is used for both CSI/O transmission and reception. Thus, the system design must ensure that the constraints of half-duplex operation are met (Transmit and Receive operation cannot occur simultaneously). For example, if a CSI/O transmission is attempted while the CSI/O is receiving data, a CSI/O does not work.

Note: TRDR is not buffered. Performing a CSI/O transmit while the previous transmission is still in progress causes the data to be immediately updated and corrupts the transmit operation. Similarly, reading TRDR while a transmit or receive is in progress should be avoided.



Figure 7. CSI/O Block Diagram

OPERATION MODES

Z80 versus 64180 Compatibility. The Z8S180/Z8L180 is descended from two different "ancestor" processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR), illustrated in Figure 8, can be programmed to select between certain Z80 and 64180 differences.



Figure 8. Operating Control Register (OMCR: I/O Address = 3EH)

M1E ($\overline{M1}$ Enable). This bit controls the $\overline{M1}$ output and is set to a 1 during RESET.

When M1E = 1, the $\overline{M1}$ output is asserted Low during opcode fetch cycles, Interrupt Acknowledge cycles, and the first machine cycle of an \overline{NMI} acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch a RETI instruction one time. When fetching a RETI from a zero-wait-state memory location, the processor uses three clock bus cycles. These bus cycles are not fully Z80-timing compatible.

When M1E = 0, the processor does not drive $\overline{M1}$ Low during the instruction fetch cycles. After fetching a RETI instruction with normal timing, the processor goes back and refetches the instruction using fully Z80-compatible cycles that include driving $\overline{M1}$ Low. This option may be required by some external Z80 peripherals to properly decode the RETI instruction. Figure 9 and Table 5 show the RETI sequence when M1E is 0.



Figure 9. RETI Instruction Sequence with M1E = 0

Machine Cycle	States	Address	Data	RD	WR	MREQ	IORQ	<u>Μ1</u> Μ1Ε= 1	<u>Μ1</u> Μ1Ε = 0	HALT	ST
1	T1–T3	1st Opcode	EDH	0	1	0	1	0	1	1	0
2	T1 - T3	2nd Opcode	4DH	0	1	0	1	0	1	1	0
	Ti	NA	3-state	1	1	1	1	1	1	1	1
	Ti	NA	3-state	1	1	1	1	1	1	1	1
	Ti	NA	3-state	1	1	1	1	1	1	1	1
3	T1 - T3	1st Opcode	EDH	0	1	0	1	0	0	1	1
	Ti	NA	3-state	1	1	1	1	1	1	1	1
4	T1–T3	2nd Opcode	4DH	0	1	0	1	0	1	1	1
5	T1–T3	SP	Data	0	1	0	1	1	1	1	1
6	T1–T3	SP + 1	Data	0	1	0	1	1	1	1	1

Table 5. RETI Control Signal States

M1TE (**M1 Temporary Enable**). This bit controls the temporary assertion of the $\overline{M1}$ signal. It is always read back as a 1 and is set to 1 during RESET.

When M1E is set to 0 to accommodate certain external Z80 peripheral(s), those same device(s) may require a pulse on $\overline{M1}$ after programming certain of their registers to complete the function being programmed.

For example, when a control word is written to the Z80 PIO to enable interrupts, no enable actually takes place until the PIO sees an active $\overline{M1}$ signal. When $\overline{M1TE} = 1$, there is no change in the operation of the $\overline{M1}$ signal, and M1E controls its function. When $\overline{M1TE} = 0$, the $\overline{M1}$ output is asserted during the next opcode fetch cycle regardless of the state programmed into the M1E bit. This condition is only momentary (one time) and it is not necessary to preprogram a 1 to disable the function (see Figure 10).



Figure 10. M1 Temporary Enable Timing

IOC (I/O Compatibility). This bit controls the timing of the \overline{IORQ} and \overline{RD} signals. The bit is set to 1 by RESET.

When $\overline{\text{IOC}} = 1$, the $\overline{\text{IORQ}}$ and $\overline{\text{RD}}$ signals function the same as the Z64180 (Figure 11).





When $\overline{IOC} = 0$, the timing of the \overline{IORQ} and \overline{RD} signals match the timing of the Z80. The \overline{IORQ} and \overline{RD} signals go active as a result of the rising edge of T2. (Figure 12.)



HALT and Low-Power Operating Modes. $Th\,e$

Z8S180/Z8L180 can operate in seven modes with respect to activity and power consumption:

- Normal Operation
- HALT Mode
- IOSTOP Mode
- SLEEP Mode
- SYSTEM STOP Mode
- IDLE Mode
- STANDBY Mode (with or without QUICK RECOV-ERY)

Normal Operation. In this state, the Z8S180/Z8L180 processor is fetching and running a program. All enabled functions and portions of the device are active, and the \overline{HALT} pin is High.

HALT Mode. This mode is entered by the HALT instruction. Thereafter, the Z8S180/Z8L180 processor continually fetches the following opcode but does not execute it and drives the HALT, ST and $\overline{M1}$ pins all Low. The oscillator and PHI pin remain Active. Interrupts and bus granting to external Masters, and DRAM refresh can occur, and all onchip I/O devices continue to operate including the DMA channels.

OPERATION MODES (Continued)

The Z8S180/Z8L180 leaves HALT mode in response to:

- Low on RESET
- Interrupt from an enabled on-chip source
- External request on NMI
- Enabled external request on INTO, INT1, or INT2

In case of an interrupt, the return address is the instruction following the HALT instruction. The program can either branch back to the HALT instruction to wait for another interrupt or can examine the new state of the system/application and respond appropriately.





SLEEP Mode. This mode is entered by keeping the IOSTOP bit (ICR5) and bits 3 and 6 of the CPU Control Register (CCR3, CCR6) all zero and executing the SLP instruction. The oscillator and PHI output continue operating, but are blocked from the CPU core and DMA channels to reduce power consumption. DRAM refresh stops, but interrupts and granting to an external Master can occur. Except when the bus is granted to an external Master, A19–0 and all control signals except \overline{HALT} are maintained High. \overline{HALT} is Low. I/O operations continue as before the SLP instruction, except for the DMA channels.

The Z8S180/Z8L180 leaves SLEEP mode in response to a Low on RESET, an interrupt request from an on-chip source,

an external request on $\overline{\text{NMI}}$, or an external request on $\overline{\text{INTO}}$, $\overline{\text{INT1}}$, or $\overline{\text{INT2}}$.

If an interrupt source is individually disabled, it cannot bring the Z8S180/Z8L180 out of SLEEP mode. If an interrupt source is individually enabled, and the IEF bit is 1 so that interrupts are globally enabled (by an EI instruction), the highest priority active interrupt occurs with the return address being the instruction after the SLP instruction. If an interrupt source is individually enabled, but the IEF bit is 0 so that interrupts are globally disabled (by a DI instruction), the Z8S180/Z8L180 leaves SLEEP mode by simply executing the following instruction(s). This condition provides a technique for synchronization with high-speed external events without incurring the latency imposed by an interrupt-response sequence. Figure 14 depicts the timing for exiting SLEEP mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes about 1.5 clock ticks to restart.



IOSTOP Mode. IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is performed by resetting the IOSTOP bit in ICR to 0.

SYSTEM STOP Mode. SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption, but the PHI output continues to operate. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode except that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

IDLE Mode. Software puts the Z8S180/Z8L180 into this mode by performing the following actions:

- Set the IOSTOP bit (ICR5) to 1
- Set CCR6 to 0
- Set CCR3 to 1
- Execute the SLP instruction

The oscillator keeps operating but its output is blocked to all circuitry including the PHI pin. DRAM refresh and all

internal devices stop, but external interrupts can occur. Bus granting to external Masters can occur if the BREST bit in the CPU control Register (CCR5) was set to 1 before IDLE mode was entered.

The Z8S180/Z8L180 leaves IDLE mode in response to a Low on RESET, an external interrupt request on NMI, or an external interrupt request on INTO, INT1 or INT2 that is enabled in the INT/TRAP Control Register. As previously described for SLEEP mode, when the Z8S180/Z8L180 leaves IDLE mode due to an NMI, or due to an enabled external interrupt request when the IEF flag is 1 due to an El instruction, the device starts by performing the interrupt with the return address of the instruction after the SLP instruction.

If an external interrupt enables the INT/TRAP control register while the IEF1 bit is 0, Z8S180/Z8L180 leaves IDLE mode; specifically, the processor restarts by executing the instructions following the SLP instruction.

Figure 15 indicates the timing for exiting IDLE mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes about 9.5 clocks to restart.



Figure 15. Z8S180/Z8L180 IDLE Mode Exit Due To External Interrupt

While the Z8S180/Z8L180 is in IDLE mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 16 depicts the timing for this sequence.

Note: A response to a bus request takes 8 clock cycles longer than in normal operation.

After the external Master negates the Bus Request, the Z8S180/Z8L180 disables the PHI clock and remains in IDLE mode.



STANDBY Mode (With or Without QUICK RECOVERY).

Software can put the Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10μ A.

As with IDLE mode, the Z8S180/Z8L180 leaves STANDBY mode in response to a Low on $\overline{\text{RESET}}$, on $\overline{\text{NMI}}$, or a Low on $\overline{\text{INTO-2}}$ that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register. This action grants the bus to an external Master if the BREXT bit in the CPU Control Register (CCR5) is 1. The time required for all of these operations is greatly increased by the necessity for restarting the on-chip oscillator, and ensuring that it stabilizes to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins and the external clock runs continuously, there is little necessity to use STANDBY mode because no time is required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding HALT Low and M1 High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives **RESET** Low to bring the device out of **STANDBY** mode, and a crystal is in use or an external clock source is stopped, the external logic must hold **RESET** Low until the on-chip oscillator or external clock source is restarted and stabilized.

The clock-stability requirements of the Z8S180/Z8L180 are much less in the divide-by-two mode that is selected by a RESET sequence and controlled by the Clock Divide bit in the CPU Control Register (CCR7). As a result, software performs the following actions:

- 1. Sets CCR7 to 0 for divide-by-two mode before an SLP instruction and STANDBY mode.
- 2. Delays setting CCR7 back to 1 for divide-by-one mode as long as possible to allow additional clock stabilization time after a RESET, interrupt, or in-line RESTART after an SLP 01 instruction.

If CCR6 is set to 1 before the SLP instruction places the MPU in STANDBY mode, the value of the CCR3 bit determines the length of the delay before the oscillator restarts and stabilizes when it leaves STANDBY mode due to an external interrupt request. When CCR3 is 0, the Z8S180/Z8L180 waits 2^{17} (131,072) clock cycles. When CCR3 is 1, it waits 64 clock cycles. This state is called QUICK RECOVERY mode. The same delay applies to grant-

ing the bus to an external Master during STANDBY mode, when the BREXT bit in the CPU Control Register (CCR5) is 1.

As described previously for SLEEP and IDLE modes, when the MPU leaves STANDBY mode due to $\overline{\text{NMI}}$ Low or an enabled $\overline{\text{INTO}}$ - $\overline{\text{INT2}}$ Low when the IEF, flag is 1 due to an IE instruction, it starts by performing the interrupt with the return address being that of the instruction following the SLP instruction. If the Z8S180/Z8L180 leaves STANDBY mode due to an external interrupt request that's enabled in the INT/TRAP Control Register, but the IEF, bit is 0 due to a DI instruction, the processor restarts by executing the instruction(s) following the SLP instruction. If \overline{INTO} , or $\overline{INT1}$ or $\overline{INT2}$ goes inactive before the end of the clock stabilization delay, the Z8S180/Z8L180 stays in STANDBY mode.

Figure 17 indicates the timing for leaving STANDBY mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes either 64 or 2^{17} (131,072) clocks to restart, depending on the CCR3 bit.



While the Z8S180/Z8L180 is in STANDBY mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 18 indicates the timing of this sequence. The device takes 64 or 2^{17} (131,072) clock cycles to grant the bus depending on the CCR3 bit. The latter (not the QUICK RE-COVERY) case may be prohibitive for many demand-driven external Masters. If so, QUICK RECOVERY or IDLE mode can be used.



Figure 18. Bus Granting to External Master During STANDBY Mode

STANDARD TEST CONDITIONS

The following standard test conditions_apply to <u>DC Characteristics</u>, unless otherwise noted. All voltages are referenced to V_{SS} (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add a 10-ns delay for each 50-pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to V_{OL} MAX or V_{OL} MIN as indicated in Figures 20 through 30 (except for CLOCK, which is referenced to the 10% and 90% points). Ordering Information lists temperature ranges and product numbers. Find package drawings in Package Information.



Figure 19. AC Parameter Test Circuit

ABSOLUTE MAXIMUM RATINGS

ltem	Symbol	Value	Unit	
Supply Voltage	V _{DD}	-0.3 ~ +7.0	V	
Input Voltage	V _{IN}	$-0.3 \sim V_{cc} + 0.3$	V	
Operating Temperature	T _{OPR}	0 ~ 70	°C	
Extended Temperature	T _{EXT}	-40 ~ 85	°C	
Storage Temperature	T _{STG}	$-55 \sim +150$	°C	

Note: Permanent damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability.

DC CHARACTERISTICS-Z8S180

Table 6.	Z8S1	80 DC (Chara	cteristics
V _{DD} :	= 5V	±10%;	V _{SS}	= 0V

Symbol	ltem	Condition	Min	Тур	Max	Unit
V _{IH1}	Input H Voltage RESET, EXTAL, NMI		V _{DD} -0.6	—	V _{DD} +0.3	V
V _{IH2}	Input H Voltage Except RESET, EXTAL, NMI		2.0	_	V _{DD} +0.3	V
V _{IH3}	Input H Voltage CKS, CKA0, CKA1		2.4	_	V _{DD} +0.3	V
V _{IL1}	Input L Voltage RESET, EXTAL, NMI		-0.3	_	0.6	V
V _{IL2}	Input L Voltage Except RESET, EXTAL, NMI		-0.3	_	0.8	V
V _{OH}	Outputs H Voltage	$I_{OH} = -200 \mu A$	2.4	_		V
	All outputs	$I_{OH} = -20 \ \mu A$	V _{DD} –1.2	—	_	
V _{OL}	Outputs L Voltage All outputs	$I_{OL} = 2.2 \text{ mA}$	_	_	0.45	V
I	Input Leakage Current All Inputs Except XTAL, EXTAL	$V_{IN} = 0.5 \sim V_{DD} - 0.5$	_	_	1.0	μA
I _{TL}	Three State Leakage Current	$V_{IN} = 0.5 \sim V_{DD} - 0.5$		_	1.0	μA
¹ ا _{مم} ا	Power Dissipation	F = 10 MHz	_	25	60	mA
	(Normal Operation)	20		30	50	
		33		60	100	
	Power Dissipation	F = 10 MHz		2	5	
	(SYSTEM STOP mode)	20		3	6	
		33		5	9	
C _P	Pin Capacitance	$V_{IN} = 0_V$, f = 1 MHz $T_A = 25^{\circ}C$	_	_	12	pF
Note: 1. V _{IHmi}	$_{n}$ = V _{DD} -1.0V, V _{ILmax} = 0.8V (All	output terminals are at NO LO	AD.) V _{DD} = 5.	.0V.		

Table 7. Z8L180 DC Characteristics V_{DD} = 3.3V ±10%; V_{SS} = 0V

Symbol	Item	Condition	Min	Тур	Max	Unit
V _{IH1}	Input H Voltage RESET, EXTAL, NMI		V _{DD} -0.6		V _{DD} +0.3	V
V_{H2}	Input H Voltage Except RESET, EXTAL, NMI		2.0		V _{DD} +0.3	V
V _{IL1}	Input L Voltage RESET, EXTAL, NMI		-0.3		0.6	V
V _{IL2}	Input L Voltage Except RESET, EXTAL, NMI		-0.3		0.8	V
V _{OH}	Outputs H Voltage	I _{OH} = -200 μA	2.15			V
	All outputs	$I_{OH} = -20 \ \mu A$	V _{DD} -0.6			V
V _{OL}	Outputs L Voltage All Outputs	$I_{OL} = 4 \text{ mA}$			0.4	V
I _{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL	$V_{IN} = 0.5 \sim V_{DD} - 0.5$			1.0	μΑ
I _{TL}	Three State Leakage Current	$V_{\rm IN} = 0.5 \sim V_{\rm DD} - 0.5$			1.0	μA
I _{DD1}	Power Dissipation	F = 20 MHz		30	60	mA
	(Normal Operation)	4 MHz		4	10	
	Power Dissipation (SYSTEM STOP mode)	F = 20 MHz		5	10	
		4 MHz		2	5	
C _P	Pin Capacitance	$V_{\rm IN} = 0V$, f = 1 MHz T_A = 25° C			12	pF

AC CHARACTERISTICS-Z8S180

			Z8S180	–20 MHz	Z8S180	—33 MHz	
Number	Symbol	Item	Min	Max	Min	Max	Unit
1	t _{CYC}	Clock Cycle Time	50	DC	30	DC	ns
2	t _{CHW}	Clock "H" Pulse Width	15	_	10	_	ns
3	t _{CLW}	Clock "L" Pulse Width	15	_	10	—	ns
4	t _{CF}	Clock Fall Time		10	_	5	ns
5	t _{CR}	Clock Rise Time		10	_	5	ns
6	t _{AD}	PHI Rise to Address Valid Delay	_	30	_	15	ns
7	t _{AS}	Address Valid to MREQ Fall or IORQ Fall)	5	_	5	_	ns
8	t _{MED1}	PHI Fall to MREQ Fall Delay		25	_	15	ns
9	t _{RDD1}	PHI Fall to \overline{RD} Fall Delay $\overline{IOC} = 1$		25	_	15	ns
		PHI Rise to \overline{RD} Rise Delay $\overline{IOC} = 0$	_	25	_	15	
10	t _{M1D1}	PHI Rise to $\overline{M1}$ Fall Delay	—	35	_	15	ns
11	t _{AH}	Address Hold Time from MREQ, IOREQ, RD, WR High	5	—	5	—	ns
12	t _{MED2}	PHI Fall to MREQ Rise Delay		25	_	15	ns
13	t _{RDD2}	PHI Fall to RD Rise Delay	_	25	_	15	ns
14	t _{M1D2}	PHI Rise to $\overline{M1}$ Rise Delay	_	40	_	15	ns
15	t _{DRS}	Data Read Set-up Time	10	_	5	_	ns
16	t _{DRH}	Data Read Hold Time	0	_	0	_	ns
17	t _{STD1}	PHI Fall to ST Fall Delay	_	30	_	15	ns
18	t _{STD2}	PHI Fall to ST Rise Delay		30	_	15	ns
19	t _{WS}	WAIT Set-up Time to PHI Fall	15	_	10	_	ns
20	t _{WH}	WAIT Hold Time from PHI Fall	10	_	5	—	ns
21	t _{WDZ}	PHI Rise to Data Float Delay	_	35	_	20	ns
22	t _{WRD1}	PHI Rise to WR Fall Delay		25	_	15	ns
23	t _{WDD}	PHI Fall to Write Data Delay Time		25	_	15	ns
24	t _{WDS}	Write Data Set-up Time to WR Fall	10	_	10	_	ns
25	t _{WRD2}	PHI Fall to WR Rise Delay		25	_	15	ns
26	t _{WRP}	WR Pulse Width (Memory Write Cycle)	80	_	45	_	ns
26a		WR Pulse Width (I/O Write Cycle)	150	_	70		ns
27	t _{WDH}	Write Data Hold Time from \overline{WR} Rise	10	_	5	—	ns
28	t _{IOD1}	PHI Fall to \overline{IORQ} Fall Delay $\overline{IOC} = 1$	_	25	_	15	ns
		PHI Rise to $\overline{\text{IORQ}}$ Fall Delay $\overline{\text{IOC}} = 0$		25	_	15	
29	t _{IOD2}	PHI Fall to IORQ Rise Delay		25		15	ns

Table 8. Z8S180 AC Characteristics

 $t_{\rm IOD3}$

t_{INTS}

30

31

125

20

_

—

80

15

M1 Fall to IORQ Fall Delay

INT Set-up Time to PHI Fall

ns

ns

AC CHARACTERISTICS – Z8S180 (Continued)

Table	e 8. Z8S180 AC Characteristics (Continued)	
V_{DD} = 5V $\pm 10\%$ or V_{DD} =	\pm 3.3V \pm 10%; 33-MHz Characteristics Apply Only to 5V C	Operation

			Z8S180—20 MHz Z8S180—33 MH				
Number	Symbol	Item	Min	Max	Min	Max	Unit
32	t _{INTH}	INT Hold Time from PHI Fall	10	_	10	_	ns
33	t _{NMIW}	NMI Pulse Width	35		25	_	ns
34	t _{BRS}	BUSREQ Set-up Time to PHI Fall	10		10	_	ns
35	t _{BRH}	BUSREQ Hold Time from PHI Fall	10	_	10		ns
36	t _{BAD1}	PHI Rise to BUSACK Fall Delay	_	25	_	15	ns
37	t _{BAD2}	PHI Fall to BUSACK Rise Delay	_	25	_	15	ns
38	t _{BZD}	PHI Rise to Bus Floating Delay Time	_	40	_	30	ns
39	t _{MEWH}	MREQ Pulse Width (High)	35	_	25	—	ns
40	t _{MEWL}	MREQ Pulse Width (Low)	35	_	25	_	ns
41	t _{RFD1}	PHI Rise to RFSH Fall Delay	_	20	_	15	ns
42	t _{RFD2}	PHI Rise to RFSH Rise Delay	—	20	_	15	ns
43	t _{HAD1}	PHI Rise to HALT Fall Delay	—	15	_	15	ns
44	t _{HAD2}	PHI Rise to HALT Rise Delay	_	15	_	15	ns
45	t _{DRQS}	DREQ1 Set-up Time to PHI Rise	20	_	15	_	ns
46	t _{DRQH}	DREQ1 Hold Time from PHI Rise	20	_	15	_	ns
47	t _{TED1}	PHI Fall to TENDi Fall Delay	_	25	_	15	ns
48	t _{TED2}	PHI Fall to TENDi Rise Delay	_	25	—	15	ns
49	t _{ED1}	PHI Rise to E Rise Delay	_	30	—	15	ns
50	t _{ED2}	PHI Fall or Rise to E Fall Delay	_	30	_	15	ns
51	P _{WEH}	E Pulse Width (High)	25	_	20	_	ns
52	P_{WEL}	E Pulse Width (Low)	50	_	40	_	ns
53	t _{Er}	Enable Rise Time	_	10	_	10	ns
54	t _{Ef}	Enable Fall Time	_	10	_	10	ns
55	t _{TOD}	PHI Fall to Timer Output Delay	_	75	_	50	ns
56	t _{STDI}	CSI/O Transmit Data Delay Time (Internal Clock Operation)	_	2	_	2	tcyc
57	t _{STDE}	CSI/O Transmit Data Delay Time (External Clock Operation)	_	7.5 t _{CYC} +75	-	75 t _{CYC} +60	ns
58	t _{SRSI}	CSI/O Receive Data Set-up Time (Internal Clock Operation)	1	_	1	_	tcyc
59	t _{SRH}	CSI/O Receive Data Hold Time (Internal Clock Operation)	1	_	1	_	tcyc
60	t _{SRSE}	CSI/O Receive Data Set-up Time (External Clock Operation)	1	_	1	_	tcyc
61	t _{SRHE}	CSI/O Receive Data Hold Time (External Clock Operation)	1	_	1	_	tcyc
62	t _{RES}	RESET Set-up Time to PHI Fall	40	—	25	_	ns

			Z8S180—20 MHz Z8S180—33 MHz				
Number	Symbol	Item	Min	Max	Min	Max	Unit
63	t _{REH}	RESET Hold Time from PHI Fall	25		15	_	ns
64	t _{OSC}	Oscillator Stabilization Time		20		20	ns
65	t _{EXR}	External Clock Rise Time (EXTAL)		5	_	5	ns
66	t _{EXF}	External Clock Fall Time (EXTAL)	_	5	_	5	ns
67	t _{RR}	RESET Rise Time		50	—	50	ms
68	t _{RF}	RESET Fall Time		50	_	50	ms
69	t _{IR}	Input Rise Time (except EXTAL, RESET)		50	_	50	ns
70	t _{IF}	Input Fall Time (except EXTAL, RESET)		50	_	50	ns

Table 8. Z8S180 AC Characteristics (Continued) $V_{DD} = 5V \pm 10\%$ or $V_{DD} = 3.3V \pm 10\%$; 33-MHz Characteristics Apply Only to 5V Operation

TIMING DIAGRAMS



Note: *Memory Read/Write Cycle timing is the same as I/O Read/Write Cycle except there are no automatic wait states (T_W), and MREQ is active instead of IORQ.

Figure 20. CPU Timing (Opcode Fetch Cycle, Memory Read Cycle, Memory Write Cycle, I/O Write Cycle, I/O Read Cycle)



Figure 21. CPU Timing (INTO Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode, HALT Mode, SLEEP Mode, SYSTEM STOP Mode)

TIMING DIAGRAMS (Continued)



Notes:

 $^{*}T_{\text{DRQS}}$ and T_{DRQH} are specified for the rising edge of the clock followed by $T_{3}.$

 $^{*\,*}T_{DRQS}$ and T_{DRQH} are specified for the rising edge of the clock.

Figure 23. DMA Control Signals





Figure 24. E Clock Timing (Memory Read/Write Cycle, I/O Read/Write Cycle)



Figure 25. E Clock Timing (BUS RELEASE Mode, SLEEP Mode, SYSTEM STOP Mode)



Figure 26. E Clock Timing (Minimum Timing Example of $P_{\rm WEL}$ and $P_{\rm WEH}$)

TIMING DIAGRAMS (Continued)



Figure 27. Timer Output Timing



Figure 28. SLP Execution Cycle


Figure 29. CSI/O Receive/Transmit Timing



External Clock Rise Time and Fall Time Input Rise Time and Fall Time (Except EXTAL, RESET)

Figure 30. Rise Time and Fall Times

CPU CONTROL REGISTER

CPU Control Register (CCR). This register controls the basic clock rate, certain aspects of Power-Down modes, and output drive/low-noise options (Figure 31).



Figure 31. CPU Control Register (CCR) Address 1FH

Bit 7. Clock Divide Select. If this bit is 0, as it is after a RE-SET, the Z8S180/Z8L180 divides the frequency on the XTAL pin(s) by two to obtain its Master clock PHI. If this bit is programmed as 1, the part uses the XTAL frequency as PHI without division.

If an external oscillator is used in divide-by-one mode, the minimum pulse width requirement provided in the AC Characteristics must be satisfied.

Bits 6 and 3. STANDBY/IDLE Control. When these bits are both 0, a SLP instruction makes the Z8S180/Z8L180 enter SLEEP or SYSTEM STOP mode, depending on the IOSTOP bit (ICR5).

When D6 is 0 and D3 is 1, setting the IOSTOP bit (ICR5) and executing a SLP instruction puts the Z8S180/Z8L180 into IDLE mode in which the on-chip oscillator runs, but its output is blocked from the rest of the part, including PHI out.

When D6 is 1 and D3 is 0, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into STANDBY mode, in which the on-chip oscillator is stopped and the part allows 2^{17} (128K) clock cycles for the oscillator to stabilize when it restarts.

When D6 and D3 are both 1, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into QUICK RE-COVERY STANDBY mode, in which the on-chip oscillator is stopped, and the part allows only 64 clock cycles for the oscillator to stabilize when it restarts.

The latter section, HALT and LOW POWER modes, describes the subject more fully.

Bit 5 BREXT. This bit controls the ability of the Z8S180/Z8L180 to honor a bus request during STANDBY mode. If this bit is set to 1 and the part is in STANDBY mode, a BUSREQ is honored after the clock stabilization timer is timed out.

Bit 4 LNPHI. This bit controls the drive capability on the PHI Clock output. If this bit is set to 1, the PHI Clock output is reduced to 33 percent of its drive capability.

ZiLOG

Bit 2 LNIO. This bit controls the drive capability of certain external I/O pins of the Z8S180/Z8L180. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

RTSO	TxS
CKA1/TEND0	CKA0/DREQ0
TXA0	TXA1
TENDi	CKS

Bit 1 LNCPUCTL. This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

BUSACK	RD
WR	M1
MREQ	IORQ
RFSH	HALT
E	TEST
ST	

Bit O LNAD/DATA. This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output drive capability of the Address and Data bus outputs is reduced to 33 percent of its original drive capability.

ASCI REGISTER DESCRIPTION





ASCI Transmit Shift Register 0,1. When the ASCI Transmit Shift Register (TSR) receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TXA pin. When transmission is completed, the next byte (if available) is automatically loaded from TDR into TSR and the next transmission starts. If no data is available for trans-

mission, TSR idles by outputting a continuous High level. This register is not program-accessible

ASCI Transmit Data Register 0,1 (TDR0, 1: I/O address = 06H, 07H). Data written to the ASCI Transmit Data Register is transferred to the TSR as soon as TSR is empty. Data can be written while TSR is shifting out the previous byte of data. Thus, the ASCI transmitter is double buffered. Data can be written into and read from the ASCI Transmit Data Register. If data is read from the ASCI Transmit Data Register, the ASCI data transmit operation is not affected by this READ operation.

ASCI Receive Shift Register 0,1 (RSR0,1). This register receives data shifted in on the RXA pin. When full, data is automatically transferred to the ASCI Receive Data Register (RDR) if it is empty. If RSR is not empty when the next incoming data byte is shifted in, an overrun error occurs. This register is not program accessible.

ASCI Receive Data FIFO 0,1 (RDR0, 1:I/O Address = **08H**, **09H**). The ASCI Receive Data Register is a read-only register. When a complete incoming data byte is assembled in RSR, it is automatically transferred to the 4 character Receive Data First-In First-Out (FIFO) memory. The oldest character in the FIFO (if any) can be read from the Receive Data Register (RDR). The next incoming data byte can be shifted into RSR while the FIFO is full. Thus, the ASCI receiver is well buffered.

ASCI STATUS FIFO

This four-entry FIFO contains Parity Error, Framing Error, Rx Overrun, and Break status bits associated with each character in the receive data FIFO. The status of the oldest character (if any) can be read from the ASCI status registers.

ASCI CHANNEL CONTROL REGISTER A



Figure 33. ASCI Channel Control Register A

MPE: Multi-Processor Mode Enable (Bit 7). The ASCI features a multiprocessor communication mode that utilizes an extra data bit for selective communication when a number of processors share a common serial bus. Multiprocessor data format is selected when the MP bit in CNTLB is set to 1. If multiprocessor mode is not selected (MP bit in CNTLB = 0), MPE has no effect. If multiprocessor mode is selected, MPE enables or disables the wake-up feature as follows. If MBE is set to 1, only received bytes in which the multiprocessor bit (MPB) = 1 can affect the RDRF and error flags. Effectively, other bytes (with MPB = 0) are *ignored* by the ASCI. If MPE is reset to 0, all bytes, regardless of

the state of the MPB data bit, affect the REDR and error flags. MPE is cleared to 0 during RESET.

RE: Receiver Enable (Bit 6). When RE is set to 1, the ASCI transmitter is enabled. When TE is reset to 0, the transmitter is disables and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

TE: Transmitter Enable (Bit 5). When TE is set to 1, the ASCI receiver is enabled. When \overline{TE} is reset to 0, the transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the pre-

ASCI CHANNEL CONTROL REGISTER A (Continued)

vious contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

RTSO: Request to Send Channel 0 (Bit 4 in CNTLA0 Only). If bit 4 of the System Configuration Register is 0, the RTSO/TXS pin exhibits the RTSO function. RTSO allows the ASCI to control (start/stop) another communication devices transmission (for example, by connecting to that device's \overline{CTS} input). \overline{RTSO} is essentially a 1-bit output port, having no side effects on other ASCI registers or flags.

Bit 4 in CNTLA1 is used.

 $CKA1D = 1, CKA1/\overline{TEND0} pin = \overline{TEND0}$

 $CKA1D = 0, CKA1/\overline{TEND0} pin = CKA1$

These bits are cleared to 0 on reset.

MPBR/EFR: Multiprocessor Bit Receive/Error Flag Reset (Bit 3). When multiprocessor mode is enabled (MP in CNTLB = 1), MPBR, when read, contains the value of the MPB bit for the most recent receive operation. When written to 0, the EFR function is selected to reset all error flags (OVRN, FE, PE and BRK in the ASEXT Register) to 0. MPBR/EFR is undefined during RESET.

MOD2, 1, 0: ASCI Data Format Mode 2,1,0 (bits 2-0).

These bits program the ASCI data format as follows.

MOD2

- $= 0 \rightarrow 7$ bit data
- = 1 \rightarrow 8 bit data

MOD1

- $= 0 \rightarrow No parity$
- = 1→Parity enabled

MOD0

= $0 \rightarrow 1$ stop bit = $1 \rightarrow 2$ stop bits

The data formats available based on all combinations of MOD2, MOD1, and MOD0 are indicated in Table 9.

Table 9. Data Formats

MOD2	MOD1	MOD0	Data Format
0	0	0	Start + 7 bit data + 1 stop
0	0	1	Start + 7 bit data + 2 stop
0	1	0	Start + 7 bit data + parity +
			1 stop
0	1	1	Start + 7 bit data + parity +
			2 stop
1	0	0	Start + 8 bit data + 1 stop
1	0	1	Start + 8 bit data + 2 stop
1	1	0	Start + 8 bit data + parity +
			1 stop
1	1	1	Start + 8 bit data + parity +
			2 stop

- (

ASCI CHANNEL CONTROL REGISTER B



MPBT: Multiprocessor Bit Transmit (Bit 7). When multiprocessor communication format is selected (MP bit = 1), MPBT is used to specify the MPB data bit for transmission. If MPBT = 1, then MPB = 1 is transmitted. If MPBT = 0, then MPB = 0 is transmitted. The MPBT state is undefined during and after RESET.

MP: Multiprocessor Mode (Bit 6). When MP is set to 1, the data format is configured for multiprocessor mode based on MOD2 (number of data bits) and MOD0 (number of stop bits) in CNTLA. The format is as follows:

Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits

Multiprocessor (MP = 1) format offers no provision for parity. If MP = 0, the data format is based on MODO, MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

 $\overline{\text{CTS}}/\text{PS}$: Clear to Send/Prescale (Bit 5). When read, $\overline{\text{CTS}}/\text{PS}$ reflects the state of the external $\overline{\text{CTS}}$ input. If the $\overline{\text{CTS}}$ input pin is High, $\overline{\text{CTS}}/\text{PS}$ is read as 1.

Note: When the \overline{CTS} input pin is High, the TDRE bit is inhibited (that is, held at 0).

For channel 1, the $\overline{\text{CTS}}$ input is multiplexed with RXS pin (Clocked Serial Receive Data). Thus, $\overline{\text{CTS}}/\text{PS}$ is only valid when read if the channel 1 CTS1E bit = 1 and the $\overline{\text{CTS}}$ input pin function is selected. The READ data of $\overline{\text{CTS}}/\text{PS}$ is not affected by $\overline{\text{RESET}}$.

If the SS2-0 bits in this register are not 111, and the BRG mode bit in the ASEXT register is 0, then writing to this bit sets the prescale (PS) control. Under those circumstances, a 0 indicates a divide-by-10 prescale function while a 1 indicates divide-by-30. The bit resets to 0.

PEO: Parity Even Odd (Bit 4) . PEO selects oven or odd parity. PEO does not affect the enabling/disabling of parity (MOD1 bit of CNTLA). If PEO is cleared to 0, even parity is selected. If PEO is set to 1, odd parity is selected. PEO is cleared to 0 during RESET.

DR: Divide Ratio (Bit 3). If the X1 bit in the ASEXT register is 0, this bit specifies the divider used to obtain baud rate from the data sampling clock. If DR is reset to 0, divide-by-16 is used, while if DR is set to 1, divide-by-64 is used. DR is cleared to 0 during RESET.

SS2,1,0: Source/Speed Select 2,1,0 (Bits 2–0). First, if these bits are 111, as they are after a RESET, the CKA pin is used as a clock input, and is divided by 1, 16, or 64 depending on the DR bit and the X1 bit in the ASEXT register.

If these bits are not 111 and the BRG mode bit is ASEXT is 0, then these bits specify a power-of-two divider for the PHI clock as indicated in Table 10.

Setting or leaving these bits as 111 makes sense for a channel only when its CKA pin is selected for the CKA function. CKAO/CKS offers the CKAO function when bit 4 of the System Configuration Register is 0. $\overline{DCDO}/CKA1$ offers the CKA1 function when bit 0 of the Interrupt Edge register is 1.

Table 10. Divide Ratio

SS2	SS1	SS0	Divide Ratio
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	External Clock

ASCI STATUS REGISTER 0,1

Each ASCI channel status register (STAT0,1) allows interrogation of ASCI communication, error and modem control signal status, and the enabling or disabling of ASCI interrupts.





RDRF: Receive Data Register Full (Bit 7). RDRF is set to 1 when an incoming data byte is loaded into an empty Rx FIFO. If a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO. RDRF is cleared to 0 by reading RDR and most recently received character in the FIFO from IOSTOP mode, during RESET and for ASCI0 if the DCD0 input is auto-enabled and is negated (High).

OVRN: Overrun Error (Bit 6). An overrun condition occurs if the receiver finishes assembling a character but the Rx FIFO is full so there is no room for the character. However, this status bit is not set until the most recent character received before the overrun becomes the oldest byte in the FIFO. This bit is cleared when software writes a 1 to the EFR bit in the CNTLA register. The bit may also be cleared by RESET in IOSTOP mode or ASCIO if the DCDO pin is auto enabled and is negated (High).

Note: When an overrun occurs, the receiver does not place the character in the shift register into the FIFO, nor any subsequent characters, until the most recent good character enters the top of the FIFO so that OVRN is set. Software then writes a 1 to EFR to clear it.

PE: Parity Error (Bit 5). A parity error is detected when parity checking is enabled. When the MOD1 bit in the

CNTLA register is 1, a character is assembled in which the parity does not match the PEO bit in the CNTLB register. However, this status bit is not set until or unless the error character becomes the oldest one in the Rx FIFO. PE is cleared when software writes a 1 to the EFR bit in the CNTRLA register. PE is also cleared by RESET in IOSTOP mode, or on ASCIO, if the DCDO pin is auto-enabled and is negated (High).

FE: Framing Error (Bit 4). A framing error is detected when the stop bit of a character is sampled as O/SPACE. However, this status bit is not set until/unless the error character becomes the oldest one in the Rx FIFO. FE is cleared when software writes a 1 to the EFR bit in the CNTLA register. FE is also cleared by RESET in IOSTOP mode, or on ASCIO, if the DCDO pin is auto-enabled and is negated (High).

REI: Receive Interrupt Enable (Bit 3). RIE should be set to 1 to enable ASCI receive interrupt requests. When RIE is 1, the Receiver requests an interrupt when a character is received and RDRF is set, but only if neither DMA channel requires its request-routing field to be set to receive data from this ASCI. That is, if SM1–0 are 11 and SAR17–16 are 10, or DIM1 is 1 and IAR17–16 are 10, then ASCI1 does not request an interrupt for RDRF. If RIE is 1, either ASCI requests an interrupt when OVRN, PE or FE is set, and ASCIO requests an interrupt when $\overline{\text{DCDO}}$ goes High. RIE is cleared to 0 by RESET.

DCDO: Data Carrier Detect (Bit 2 STATO). This bit is set to 1 when the pin is High. It is cleared to 0 on the first READ of STATO following the pin's transition from High to Low and during RESET. When bit 6 of the ASEXTO register is 0 to select auto-enabling, and the pin is negated (High), the receiver is reset and its operation is inhibited.

CTS1E: **Clear To Send (Bit 2 STAT1).** Channel 1 features an external $\overline{\text{CTS1}}$ input, which is multiplexed with the receive data pin RSX for the CSI/O. Setting this bit to 1 selects the CTS1 function; clearing the bit to 0 selects the RXS function.

TDRE: Transmit Data Register Empty (Bit 1). TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. On ASCIO, if the CTSO pin is auto-enabled in the ASEXTO register and the pin is High, TDRE is reset to 0.

TIE: Transmit Interrupt Enable (Bit 0). TIE should be set to 1 to enable ASCI transmit interrupt requests. If TIE = 1, an interrupt is requested when TDRE = 1. TIE is cleared to 0 during RESET.

ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

ASCI Transmit Data Registers Channel 0

Mnemonic TDR0 Address 06H



Figure 36. ASCI Register

ASCI Transmit Data Registers Channel 1

Mnemonic TDR1 Address 07H



Figure 37. ASCI Register

ASCI RECEIVE REGISTER

Register addresses 08H and 09H hold the ASCI receive data for channel 0 and channel 1, respectively.

ASCI Receive Register Channel 0

Mnemonic RDR0 Address 08H



Figure 38. ASCI Receive Register Channel 0

ASCI Receive Register Channel 1

Mnemonic RDR1 Address 09H



Figure 39. ASCI Receive Register Channel 1

CSI/O CONTROL/STATUS REGISTER

The CSI/O Control/Status Register (CNTR) is used to monitor CSI/O status, enable and disable the CSI/O, enable and disable interrupt generation, and select the data clock speed and source.



Figure 40. CSI/O Control Register (CNTR: I/O Address = 000AH)

EF: End Flag (Bit 7). EF is set to 1 by the CSI/O to indicate completion of an 8-bit data transmit or receive operation. If End Interrupt Enable (EIE) bit = 1 when EF is set to 1, a CPU interrupt request is generated. Program access of TRDR only occurs if EF = 1. The CSI/O clears EF to 0 when TRDR is read or written. EF is cleared to 0 during RESET and IOSTOP mode.

EIE: End Interrupt Enable (Bit 6). EIE is set to 1 to generate a CPU interrupt request. The interrupt request is inhibited if EIE is reset to 0. EIE is cleared to 0 during RESET.

RE: Receive Enable (Bit 5). A CSI/O receive operation is started by setting RE to 1. When RE is set to 1, the data clock is enabled. In internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted in on the RXS

pin in synchronization with the (internal or external) data clock. After receiving 8 bits of data, the CSI/O automatically clears RE to 0, EF is set to 1, and an interrupt (if enabled by EIE = 1) is generated. RE and TE are never both set to 1 at the same time. RE is cleared to 0 during RESET and IOSTOP mode.

TE: Transmit Enable (Bit 4). A CSI/O transmit operation is started by setting TE to 1. When TE is set to 1, the data clock is enabled. When in internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted out on the TXS pin synchronous with the (internal or external) data clock. After transmitting 8 bits of data, the CSI/O automatically clears TE to 0, sets EF to 1, and requests an interrupt if enabled by EIE = 1. TE and RE are never both set to 1 at the same time. TE is cleared to 0 during RESET and IOSTOP mode.

SS2, **1**, **0**: **Speed Select 2**, **1**, **0** (**Bits 2–0**). SS2, SS1 and SS0 select the CSI/O transmit/receive clock source and speed. SS2, SS1 and SS0 are all set to 1 during RESET. Table 11 indicates CSI/O Baud Rate Selection.

Table	11.	CSI/O	Baud	Rate	Selection
-------	-----	-------	------	------	-----------

SS2	SS1	SS0	Divide Ratio
0	0	0	÷20
0	0	1	÷40
0	1	0	÷80
0	1	1	÷160
1	0	0	÷320
1	0	1	÷640
1	1	0	÷1280
1	1	1	External Clock Input
			(Less Than ÷20)

After $\overline{\text{RESET}}$, the CKS pin is configured as an external clock input (SS2, SS1, SS0 = 1). Changing these values causes CKS to become an output pin and the selected clock is output when transmit or receive operations are enabled.

CSI/O Transmit/Receive Data Register

Mnemonic TRDR Address 0BH





Timer Data Register Channel 0 Low

Mnemonic TMDR0L Address 0CH



Figure 42. Timer Register Channel 0 Low

Timer Data Register Channel OH

Mnemonic TMDR0H Address 0DH



Figure 43. Timer Data Register Channel 0 High

Timer Reload Register Channel 0 Low

Mnemonic RLDROL Address 0EH



Figure 44. Timer Reload Register Low

Timer Reload Register Channel 0 High

Mnemonic RLDROH Address OFH



Figure 45. Timer Reload Register Channel 0 High

TIMER CONTROL REGISTER

The Timer Control Register (TCR) monitors both channels (PRT0, PRT1) TMDR status. It also controls the enabling

and disabling of down-counting and interrupts, and controls the output pin A18/T $_{OUT}$ for PRT1.





TIF1: Timer Interrupt Flag 1 (Bit 7). When TMDR1 decrements to 0, TIF1 is set to 1. This condition generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0.

TIFO: Timer Interrupt Flag 0 (Bit 6). When TMDR0 decrements to 0, TIFO is set to 1. This condition generates an interrupt request if enabled by TIEO = 1. TIFO is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIFO is cleared to 0.

TIE1: Timer Interrupt Enable 1 (Bit 5). When TIEO is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIEO is reset to 0, the interrupt request is inhibited. During RESET, TIEO is cleared to 0.

TOC1, 0: Timer Output Control (Bits 3, 2). TOC1 and TOC0 control the output of PRT1 using the multiplexed A18/ T_{OUT} pin as indicated in Table 12. During RESET, TOC1 and TOC0 are cleared to 0. If bit 3 of the IAR1B register is 1, the T_{OUT} function is selected. By programming

TOC1 and TOC0, the A18/ T_{OUT} pin can be forced High, Low, or toggled when TMDR1 decrements to 0.

Table 12. Timer Output Control

TOC1	тосо		Output
0	0	Inhibited	The A18/T _{OUT} pin is not
			affected by the PRT
0	1	Toggled	If bit 3 of IAR1B is 1, the
1	0	0	A18/T _{OUT} pin is toggled or
1	1	1	⁻ set Low or High as indicated

TDE1, 0: Timer Down Count Enable (Bits 1, 0). TDE1 and TDE0 enable and disable down-counting for TMDR1 and TMDR0, respectively. When TDEn (n = 0,1) is set to 1, down-counting is stopped and TMDRn is freely read or written. TDE1 and TDE0 are cleared to 0 during RESET and TMDRn does not decrement until TDEn is set to 1. The ASCI Extension Control Registers (ASEXTO and ASEXT1) control functions that have been added to the

ASCIs in the Z8S180/Z8L180 family. All bits in this register reset to 0.



DCD0 Disable (Bit 6, ASCIO Only). If this bit is 0, then the $\overline{\text{DCD0}}$ pin auto-enables the ASCIO receiver, such that when the pin is negated/High, the Receiver is held in a RE-SET state. If this bit is 1, the state of the $\overline{\text{DCD}}$ -pin has no effect on receiver operation. In either state of this bit, software can read the state of the $\overline{\text{DCD0}}$ pin in the STATO register, and the receiver interrupts on a rising edge of $\overline{\text{DCD0}}$.

CTSO Disable (Bit 5, ASCIO Only). If this bit is 0, then the $\overline{\text{CTSO}}$ pin auto-enables the ASCIO transmitter, in that when the pin is negated/High, the TDRE bit in the STATO register is forced to 0. If this bit is 1, the state of the $\overline{\text{CTSO}}$ pin has no effect on the transmitter. Regardless of the state of this bit, software can read the state of the $\overline{\text{CTSO}}$ pin the CNTLBO register.

X1 (Bit 4). If this bit is 1, the clock from the Baud Rate Generator or CKA pin is taken as a 1X-bit clock (sometimes called *isochronous mode*). In this mode, receive data on the RXA pin must be synchronized to the clock on the CKA pin, regardless of whether CKA is an input or an output. If this bit is 0, the clock from the Baud Rate Generator or CKA pin is divided by 16 or 64 per the DR bit in the CNTLB register, to obtain the actual bit rate. In this mode, receive data on the RXA pin is not required to be synchronized to a clock.

BRG Mode (Bit 3). If the SS2–0 bits in the CNTLB register are not 111, and this bit is 0, the ASCI Baud Rate Generator

divides PHI by 10 or 30, depending on the PS bit in CNTLB, and factored by a power of two (selected by the SS2–0 bits), to obtain the clock that is presented to the transmitter and receiver and output on the CKA pin. If SS2–0 are not 111, and this bit is 1, the Baud Rate Generator divides PHI by twice the sum of the 16-bit value (programmed into the Time Constant registers) and 2. This mode is identical to the operation of the baud rate generator in the ESCC.

Break Enable (Bit 2). If this bit is 1, the receiver detects BREAK conditions and report them in bit 1, and the transmitter sends BREAKs under the control of bit 0.

Break Detect (Bit 1). The receiver sets this read-only bit to 1 when an all-zero character with a Framing Error becomes the oldest character in the Rx FIFO. The bit is cleared when software writes a 0 to the EFR bit in CNTLA register, also by RESET, by IOSTOP mode, and for ASCIO, if the DCDO pin is auto-enabled and is negated (High).

Send Break (Bit 0). If this bit and bit 2 are both 1, the transmitter holds the TXA pin Low to send a BREAK condition. The duration of the BREAK is under software control (one of the PRTs or CTCs can be used to time it). This bit resets to 0, in which state TXA carries the serial output of the transmitter.

ASCI EXTENSION CONTROL REGISTER CHANNEL 0 AND CHANNEL 1 (Continued)

Timer Data Register Channel 1 Low

Mnemonic TMDR1L Address 14H





Timer Data Register Channel 1 High

Mnemonic TMDR1H Address 15H



Figure 49. Timer Data Register 1 High

Timer Reload Register Channel 1 Low

Mnemonic RLDR1L Address 16





Timer Reload Register Channel 1 High

Mnemonic RLDR1H Address 17H



Figure 51. Timer Reload Register Channel 1 High

Free Running Counter (Read Only)

Mnemonic FRC Address 18H



Figure 52. Free Running Counter

ASCI TIME CONSTANT REGISTERS

If the SS2–0 bits of the CNTLB register are not 111, and the BRG mode bit in the ASEXT register is 1, the ASCI divides the PHI clock by two times the registers' 16-bit value, plus two. As a result, the clock is presented to the transmitter and receiver for division by 1, 16, or 64, and is output on the CKA pin.

If the SS2–0 bits in an ASCI CNTLB register are not 111, and the BRG mode bit in its Extension Control Register is 1, its *new* baud rate generator divides PHI for serial clocking, as follows:

bits/second =
$$f_{PHI}/(2*(TC+2) \times sampling rate)$$

where TC is the 16-bit value programmed into the ASCI Time Constant High and Low registers. If the ASCI multiplexed CKA pin is selected for the CKA function, it outputs the clock before the final division by the sampling rate, as follows:

$$f_{CKAout} = f_{PHI}/(2*(TC+2))$$

Find the TC value for a particular serial bit rate as follows:

 $TC = (f_{PHI}/(2 \text{ x bits/second x sampling rate})) - 2$



Figure 53. ASCI Time Constant Registers

CLOCK MULTIPLIER REGISTER

(Z180 MPU Address 1EH)



Figure 54. Clock Multiplier Register

Bit 7. X2 Clock Multiplier Mode. When this bit is set to 1, the programmer can double the internal clock speed from the speed of the external clock. This feature only operates effectively with frequencies of 10-16 MHz (20-32 MHz internal). When this bit is set to 0, the Z8S180/Z8L180 device operates in normal mode. At power-up, this feature is disabled.

Bit 6. Low Noise Crystal Option. Setting this bit to 1 enables the low-noise option for the EXTAL and XTAL pins. This option reduces the gain in addition to reducing the output drive capability to 30% of its original drive capability. The Low Noise Crystal Option is recommended in the use of crystals for PCMCIA applications, where the crystal may be driven too hard by the oscillator. Setting this bit to 0 is selected for normal operation of the EXTAL and XTAL pins. The default for this bit is 0.

Note: Operating restrictions for device operation are listed below. If a low-noise option is required, and normal device operation is required, use the clock multiplier feature.

Table 13. Low Noise Option

Low Noise ADDR 1E, bit 6 = 1	Normal ADDR 1E, bit 6 = 0
20 MHz @ 4.5V, 100°C	33 MHz @ 4.5V, 100°C
10 MHz @ 3.0V, 100°C	20 MHz @ 3.0V, 100°C

DMA SOURCE ADDRESS REGISTER CHANNEL 0

The DMA Source Address Register Channel 0 specifies the physical source address for channel 0 transfers. The register contains 20 bits and can specify up to 1024 KB memory addresses or up to 64-KB I/O addresses. Channel 0 source can be memory, I/O, or memory mapped I/O. For I/O, bits 17–16 of this register identify the Request Handshake signal.

DMA Source Address Register, Channel 0 Low

Mnemonic SAR0L Address 20H





DMA Source Address Register, Channel 0 High

Mnemonic SAR0H Address 21H





DMA Source Address Register Channel OB

Mnemonic SAR0B Address 22H



Figure 57. DMA Source Address Register 0B

If the source is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

Bit 1 (A17)	Bit 0 (A16)	DMA Transfer Request
0	0	DREQ0 (external)
0	1	RDRF (ASCI0)
1	0	RDRF (ASCI1)
1	1	Reserved

DMA DESTINATION ADDRESS REGISTER CHANNEL 0

The DMA Destination Address Register Channel 0 specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024-KB memory addresses or up to 64-KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal for channel 0.

DMA Destination Address Register Channel 0 Low

Mnemonic DAR0L Address 23H



Figure 58. DMA Destination Address Register Channel 0 Low

DMA Destination Address Register Channel 0 High

Mnemonic DAR0H Address 24H



Figure 59. DMA Destination Address Register Channel 0 High

DMA Destination Address Register Channel 0B

Mnemonic DAR0B Address 25H



Figure 60. DMA Destination Address Register Channel 0B

If the DMA destination is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

0 0 DREQ0 (external) 0 1 TDR0 (ASCI0) 1 0 TDR1 (ASCI1) 1 1 Not Used	Bit 1 (A17)	Bit 0 (A16)	DMA Transfer Request
0 1 TDR0 (ASCI0) 1 0 TDR1 (ASCI1) 1 1 Not Used	0	0	DREQ0 (external)
1 0 TDR1 (ASCI1) 1 1 Not Used	0	1	TDR0 (ASCI0)
1 1 Not Used	1	0	TDR1 (ASCI1)
	1	1	Not Used

DMA BYTE COUNT REGISTER CHANNEL 0

The DMA Byte Count Register Channel 0 specifies the number of bytes to be transferred. This register contains 16 bits and may specify up to 64-KB transfers. When one byte is transferred, the register is decremented by one. If n bytes should be transferred, n must be stored before the DMA operation.

Note: All DMA Count Register channels are undefined during RESET.

DMA Byte Count Register Channel 0 Low

Mnemonic BCR0L Address 26H





DMA Byte Count Register Channel 0 High

Mnemonic BCR0H Address 27H



Figure 62. DMA Byte Count Register 0 High

DMA Byte Count Register Channel 1 Low

Mnemonic BCR1L Address 2EH



Figure 63. DMA Byte Count Register 1 Low

DMA Byte Count Register Channel 1 High

Mnemonic BCR1H Address 2FH



Figure 64. DMA Byte Count Register 1 High

DMA MEMORY ADDRESS REGISTER CHANNEL 1

The DMA Memory Address Register Channel 1 specifies the physical memory address for channel 1 transfers. The address may be a destination or a source memory location. The register contains 20 bits and may specify up to 1024 KB memory addresses.

DMA Memory Address Register, Channel 1L

Mnemonic MAR1L Address 28H



Figure 65. DMA Memory Address Register, Channel 1L

DMA Memory Address Register, Channel 1H

Mnemonic MAR1H Address 29H



Figure 66. DMA Memory Address Register, Channel 1H

DMA Memory Address Register, Channel 1B

Mnemonic MAR1B Address 2AH



Figure 67. DMA Memory Address Register, Channel 1B

DMA I/O ADDRESS REGISTER

The DMA I/O Address Register specifies the I/O device for channel 1 transfers. This address may be a destination or source I/O device. IAR1L and IAR1H each contain 8 address bits. The most significant byte identifies the Request Handshake signal and controls the Alternating Channel feature.

DMA I/O Address Register Channel 1 Low

Mnemonic IAR1L Address 2BH



Figure 68. DMA I/O Address Register Channel 1 Low

DMA I/O Address Register Channel 1 High

Mnemonic IAR1H Address 2CH



Figure 69. DMA I/O Address Register Channel 1 High

DMA I/O Address Register Channel 1 B

Mnemonic IAR1B Address 2DH





AltE. The AltE bit should be set only when both DMA channels are programmed for the same I/O source or I/O destination. In this case, a *channel end* condition (byte count = 0) on channel 0 sets bit 6 (AltC), which subsequently enables the channel 1 request and blocks the channel 0 request. Similarly, a channel end condition on channel 1 clears bit 6 (AltC), which then enables the channel 0 request and blocks the channel 1 request. For external requests, the request from the device must be routed or connected to both the DREQO and DREQ1 pins.

AltC. If bit (AltE) is 0, the AltC bit has no effect. When bit 7 (AltE) is 1 and the AltC bit is 0, the request signal selected by bits 2–0 is not presented to channel 1; however, the channel 0 request operates normally. When AltE is 1 and AltC is 1, the request selected by SAR18–16 or DAR18–16 is not presented to channel 0; however, the channel 1 request operates normally. The AltC bit can be written by software to select which channel should operate first; however, this operation should be executed only when both channels are stopped (both DE1 and DE0 are 0).

Req1Sel. If bit DIM1 in the DCNTL register is 1, indicating an I/O source, the following bits select which source hand-shake signal should control the transfer:

DREQ1 pin
ASCI0 RDRF
ASCI1 RDRF
Reserved, do not program

If DIM1 is 0, indicating an I/O destination, the following bits select which destination handshake signal should control the transfer:

000	DREQ1 pin
001	ASCI0 TDRE
010	ASCI1 TDRE
Other	Reserved, do not program

DMA STATUS REGISTER

The DMA Status Register (DSTAT) is used to enable and disable DMA transfer and DMA termination interrupts.

DMA Status Register

Mnemonic DSTAT Address 30H



Figure 71. DMA Status Register (DSTAT: I/O Address = 30H)

DE1: DMA Enable Channel 1 (Bit 7). When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DIE1 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE1, DWE1 should be written with a 0 during the same register WRITE access. Writing DE1 to 0 disables channel 1 DMA, but DMA is restartable. Writing DE1 to 1 enables channel 1 DMA and automatically sets DMA Main Enable (DME) to 1. DE1 is cleared to 0 during RESET.

DEO: DMA Enable Channel 0 (Bit 6). When DEO = 1 and DME = 1, channel 0 DMA is enabled. When a DMA transfer terminates (BCRO = 0), DEO is reset to 0 by the DMAC. When DEO = 0 and the DMA interrupt is enabled (DIEO = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DEO, $\overline{\text{DWEO}}$ should be written with 0 during the same register WRITE access. Writing DEO to 0 disables channel 0 DMA. Writing DEO to 1 enables channel 0 DMA and automatically sets DMA Main Enable (DME) to 1. DEO is cleared to 0 during RESET.

DWE1: DE1 Bit Write Enable (Bit 5). When performing any software WRITE to DE1, this bit should be written with 0 during the same access. DWE1 always reads as 1.

DWEO: DEO Bit Write Enable (Bit 4). When performing any software WRITE to DEO, this bit should be written with 0 during the same access. DWEO always reads as 1.

DIE1: DMA Interrupt Enable Channel 1 (Bit 3). When DIE0 is set to 1, the termination channel 1 DMA transfer (indicated when DE1 = 0) causes a CPU interrupt request to be generated. When DIEO = 0, the channel 0 DMA termination interrupt is disabled. DIEO is cleared to 0 during RESET.

DIEO: DMA Interrupt Enable Channel 0 (Bit 2). When DIEO is set to 1, the termination channel 0 of DMA transfer (indicated when DEO = 0) causes a CPU interrupt request to be generated. When DIEO = 0, the channel 0 DMA termination interrupt is disabled. DIEO is cleared to 0 during RESET.

DME: DMA Main Enable (Bit 0). A DMA operation is only enabled when its DE bit (DE0 for channel 0, DE1 for channel 1) and the DME bit is set to 1.

When $\overline{\text{NMI}}$ occurs, DME is reset to 0, thus disabling DMA activity during the $\overline{\text{NMI}}$ interrupt service routine. To restart DMA, DE- and/or DE1 should be written with a 1 (even if the contents are already 1). This condition automatically sets DME to 1, allowing DMA operations to continue.

Note: DME cannot be directly written. The bit is cleared to 0 by $\overline{\text{NMI}}$ or indirectly set to 1 by setting DEO and/or DE1 to 1. DME is cleared to 0 during RESET.

DMA MODE REGISTER

The DMA Mode Register (DMODE) is used to set the addressing and transfer mode for channel 0.

DMA Mode Register

Mnemonic DMODE Address 31H





DM1, DM0: Destination Mode Channel 0 (Bits 5,4). This mode specifies whether the destination for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred. DM1 and DM0 are cleared to 0 during RESET.

SM1, SM0: Source Mode Channel 0 (Bits 3, 2). This mode specifies whether the source for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred.

T	able	15.	Channel	0	Source
				_	

Table 14. Channel 0 Destination					
Memory DM1 DM0 Memory I/O Increment/Decreme					
0	0	Memory	+ 1		
0	1	Memory	-1		
1	0	Memory	fixed		
1	1	I/O	fixed		

SM1	SM0	Memory I/O	Memory Increment/Decrement
0	0	Memory	+ 1
0	1	Memory	-1
1	0	Memory	fixed
1	1	I/O	fixed

Table 16 indicates all DMA transfer mode combinations of DMO, DM1, SMO, and SM1. Because I/O to/from I/O transfers are not implemented, 12 combinations are available.

DM1	DM0	SM1	SM0	Transfer Mode	Address Increment/Decrement
0	0	0	0	Memory→Memory	SAR0 + 1, DAR0 + 1
0	0	0	1	Memory→Memory	SAR0-1, DAR0+1
0	0	1	0	Memory*→Memory	SAR0 fixed, DAR0+1
0	0 1 1 I/O→Memory SAR0 fixed, DAR0 + 1				
0 1 0 0 Memory→Mem				Memory→Memory	SAR0+1, DAR0-1
0	1	0	1	Memory→Memory	SAR0-1, DAR0-1
0	1	1	0	Memory*→Memory	SAR0 fixed, DAR0-1
0	1	1 1 I/O→Memory SAR0 fixed, DAR0-		SAR0 fixed, DAR0-1	
1	0	0	0	0 Memory \rightarrow Memory* SAR0+1, DAR0	
1	0	0	1	Memory→Memory*	SAR0-1, DAR0 fixed
1	0	1	0	Reserved	
1	0	1	1	Reserved	
1	1	0	0	Memory→I/O	SAR0+1, DAR0 fixed
1	1	0	1	Memory→I/O	SAR0-1, DAR0 fixed
1	1	1	0	Reserved	
1	1	1	1	Reserved	
Note: * Inc	ludes memo	bry mapped	I/O.		

Table 16. Transfer Mode Combinations

MMOD: Memory Mode Channel 0 (Bit 1). When channel 0 is configured for memory to/from memory transfers there is no Request Handshake signal to control the transfer timing. Instead, two automatic transfer timing modes are selectable: burst (MMOD = 1) and cycle steal (MMOD = 0). For burst memory to/from memory transfers, the DMAC takes control of the bus continuously until the DMA transfer

completes (as indicated by the byte count register = 0). In cycle steal mode, the CPU is provided a cycle for each DMA byte transfer cycle until the transfer is completed.

For channel 0 DMA with I/O source or destination, the selected Request signal times the transfer ignoring MMOD. MMOD is cleared to 0 during RESET.

DMA/WAIT CONTROL REGISTER

The DMA/WAIT Control Register (DCNTL) controls the insertion of wait states into DMAC (and CPU) accesses of memory or I/O. Also, the register defines the Request signal

for each channel as level or edge sense. DCNTL also sets the DMA transfer mode for channel 1, which is limited to memory to/from I/O transfers.



Figure 73. DMA/WAIT Control Register (DCNTL: I/O Address = 32H)

MWI1, MWI0: Memory Wait Insertion (Bits 7–6). This bit specifies the number of wait states introduced into CPU or DMAC memory access cycles. MWI1 and MWI0 are set to 1 during RESET.

MWI1	MWIO	Wait State
0	0	0
0	1	1
1	0	2
1	1	3

IWI1, IWI0: I/O Wait Insertion (Bits 5–4). This bit specifies the number of wait states introduced into CPU or DMAC I/O access cycles. IWI1 and IWI0 are set to 1 during RESET.

IWI1	IWIO	Wait State
0	0	1
0	1	2
1	0	3
1	1	4

Note: These wait states are added to the 3-clock I/O cycle that is used to access the on-chip I/O registers. It is equally valid to regard these as 0 to 3 wait states added to a 4-clock external I/O cycle.

DMS1, DMS0: DMA Request Sense (Bits 3–2). DMS1 and DMS0 specify the DMA request sense for channel 0 and channel 1 respectively. When reset to 0, the input is level sense. When set to 1, the input is edge sense. DMS1 and DMS0 are cleared to 0 during RESET.

DMSi	Sense
1	Edge Sense
0	Level Sense

Typically, for an input/source device, the associated DMS bit should be programmed as 0 for level sense. The device takes a relatively long time to update its Request signal after the DMA channel reads data (in the first of the two machine cycles involved in transferring a byte).

An output/destination device takes much less time to update its Request signal after the DMA channel starts a WRITE operation to it (the second machine cycle of the two cycles involved in transferring a byte). With zero-wait state I/O cycles, a device cannot update its request signal in the required time, so edge sensing must be used.

A one-wait-state I/O cycle also does not provide sufficient time for updating, so edge sensing is again required.

DIM1, DIM0: DMA Channel 1 I/O and Memory Mode (**Bits 1–0**). Specifies the source/destination and address modifier for channel 1 memory to/from I/O transfer modes. DIM1 and DIMO are cleared to 0 during RESET.

Table 17. Channel 1 Transfer Mode

DIM1	DMI0	Transfer Mode	Address Increment/Decrement
0	0	Memory→I/0	MAR1 +1, IAR1 fixed
0	1	Memory→I/O	MAR1 -1, IAR1 fixed
1	0	I/O→Memory	IAR1 fixed, MAR1 +1
1	1	I/O→Memory	IAR1 fixed, MAR1 -1

INTERRUPT VECTOR LOW REGISTER

Bits 7–5 of the Interrupt Vector Low Register (I_L) are used as bits 7–5 of the synthesized interrupt vector during interrupts for the INT1 and INT2 pins and for the DMAs, ASCIs,

Interrupt Vector Low Register

Mnemonic: IL Address 33H



RESET (Figure 74).

Figure 74. Interrupt Vector Low Register (IL: I/O Address = 33H)

CTCs

INT/TRAP CONTROL REGISTER

This register is used in handling TRAP interrupts and to enable or disable Maskable Interrupt Level 0 and the $\overline{INT1}$ and $\overline{INT2}$ pins.

INT/TRAP Control Register Mnemonics ITC Address 34H



TRAP (Bit 7). This bit is set to 1 when an undefined opcode is fetched. TRAP can be reset under program control by writing it with a 0; however, TRAP cannot be written with 1 under program control. TRAP is reset to 0 during RESET.

UFO: Undefined Fetch Object (Bit 6). When a TRAP interrupt occurs, the contents of UFO allow the starting address of the undefined instruction to be determined. This interrupt is necessary because the TRAP may occur on either the second or third byte of the opcode. UFO allows the stacked PC value to be correctly adjusted. If UFO = 0, the first opcode should be interpreted as the stacked PC-1. If UFO = 1, the first opcode address is stacked PC-2. UFO is Read-Only.

ITE2, **1**, **0**: **Interrupt Enable 2**, **1**, **0** (**Bits 2–0**). ITE2 and ITE1 enable and disable the external interrupt inputs

INT2 and INT1, respectively. ITEO enables and disables interrupts from:

PRTs, and CSI/O. These three bits are cleared to 0 during

- ESCC Bidirectional Centronics controller
 - External interrupt input INTO

A 1 in a bit enables the corresponding interrupt level while a 0 disables it. A RESET sets ITE0 to 1 and clears ITE1 and ITE2 to 0.

TRAP Interrupt. The Z8S180/Z8L180 generates a TRAP sequence when an undefined opcode fetch occurs. This feature can be used to increase software reliability, implement an *extended* instruction set, or both. TRAP may occur during opcode fetch cycles and also if an undefined opcode is fetched during the interrupt acknowledge cycle for INTO when Mode O is used.

When a TRAP sequence occurs, the Z8S180/Z8L180:

- 1. Sets the TRAP bit in the Interrupt TRAP/Control (ITC) register to 1.
- 2. Saves the current Program Counter (PC) value, reflecting the location of the undefined opcode, on the stack.
- 3. Resumes execution at logical address 0.

Note: If logical address 0000H is mapped to physical address 00000H, the vector is the same as for RESET. In this case, testing the TRAP bit in ITC reveals whether the restart at physical address 00000H was caused by RESET or TRAP.

All TRAPs occur after fetching an undefined second opcode byte following one of the prefix opcodes (CBH, DDH, EDH, or FDH) or after fetching an undefined third opcode byte following one of the double-prefix opcodes (DDCBH or FDCBH). The state of the Undefined Fetch Object (UFO) bit in ITC allows TRAP software to correctly *adjust* the stacked PC, depending on whether the second or third byte of the opcode generated the TRAP. If UFO = 0, the starting address of the invalid instruction is the stacked PC-1. If UFO = 1, the starting address of the invalid instruction is equal to the stacked PC-2.



Figure 75. TRAP Timing – 2nd Opcode Undefined



Figure 76. TRAP Timing-3rd Opcode Undefined

REFRESH CONTROL REGISTER

Mnemonic RCR Address 36H





The Refresh Control Register (RCR) specifies the interval and length of refresh cycles, while enabling or disabling the refresh function. **REFE: Refresh Enable (Bit 7).** REFE = 0 disables the refresh controller, while REFE = 1 enables refresh cycle insertion. REFE is set to 1 during RESET.

REFW: Refresh Wait (Bit 6). REFW = 0 causes the refresh cycle to be two clocks in duration. REFW = 1 causes the refresh cycle to be three clocks in duration by adding a refresh wait cycle (TRW). REFW is set to 1 during RESET.

CYC1, 0: Cycle Interval (Bit 1,0). CYC1 and CYC0 specify the interval (in clock cycles) between refresh cycles. When dynamic RAM requires 128 refresh cycles every 2 ms (or 256 cycles in every 4 ms), the required refresh interval is less than or equal to $15.625 \,\mu$ s. Thus, the underlined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared to 0 during RESET (see Table 18).

	Table	18.	DRAM	Refresh	Intervals
--	-------	-----	------	---------	-----------

					Time Interval		
CYC1	CYC0	Insertion Interval	PHI: 10 MHz	8 MHz	6 MHz	4 MHz	2.5 MHz
0	0	10 states	(1.0 <i>µ</i> s)*	(1.25 <i>µ</i> s)*	1.66 <i>µ</i> s	2.5 <i>µ</i> s	4.0 <i>μ</i> s
0	1	20 states	(2.0 <i>µ</i> s)*	(2.5 <i>µ</i> s)*	3.3 <i>µ</i> s	5.0 <i>µ</i> s	8.0 <i>µ</i> s
1	0	40 states	(4.0 μs)*	(5.0 <i>μ</i> s)*	6.6 <i>µ</i> s	10.0 <i>μ</i> s	16.0 <i>μ</i> s
1	1	80 states	(8.0 <i>µ</i> s)*	(10.0 <i>µ</i> s)*	13.3 <i>μ</i> s	20.0 <i>µ</i> s	32.0 <i>µ</i> s
Note: *ca	alculated interva	al.					

Refresh Control and Reset. After RESET, based on the initialized value of RCR, refresh cycles occur with an interval of 10 clock cycles and be 3 clock cycles in duration.

Dynamic RAM Refresh Operation

- 1. Refresh Cycle insertion is stopped when the CPU is in the following states:
 - a. During RESET
 - b. When the bus is released in response to BUSREQ
 - c. During SLEEP mode
 - d. During \overline{WAIT} states
- 2. Refresh cycles are suppressed when the bus is released in response to $\overline{\text{BUSREO}}$. However, the refresh timer continues to operate. The time at which the first refresh cycle occurs after the Z8S180/Z8L180 reacquires the bus depends on the refresh timer. This cycle offers no timing relationship with the bus exchange.
- 3. Refresh cycles are suppressed during SLEEP mode. If a refresh cycle is requested during SLEEP mode, the refresh cycle request is internally latched (until replaced with the next refresh request). The latched refresh cycle is inserted at the end of the first machine cycle after SLEEP mode is exited. After this initial cycle, the time at which the next refresh cycle occurs depends on the refresh time and offers no relationship with the exit from SLEEP mode.
- 4. The refresh address is incremented by one for each successful refresh cycle, not for each refresh. Thus, independent of the number of missed refresh requests, each refresh bus cycle uses a refresh address incremented by one from that of the previous refresh bus cycles.

MMU COMMON BASE REGISTER

The Common Base Register (CBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit phys-

MMU Common Base Register

Mnemonic CBR Address 38H



Figure 78. MMU Common Base Register (CBR: I/O Address = 38H)

0 during RESET.

MMU BANK BASE REGISTER

The Bank Base Register (BBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical ad-

MMU Bank Base Register

Mnemonic BBR Address 39H



Figure 79. MMU Bank Base Register (BBR: I/O Address = 39H)

MMU COMMON/BANK AREA REGISTER

The Common/Bank Area Register (CBAR) specifies boundaries within the Z8S180/Z8L180 64-KB logical address space for up to three areas; Common Area), Bank Area and Common Area 1.

ical address for Common Area 1 accesses. All bits of CBR

dress for Bank Area accesses. All bits of BBR are reset to

are reset to 0 during RESET.

MMU Common/Bank Area Register

Mnemonic CBAR Address 3AH

Bit	7	6	5	4	3	2	1	0
	CA3	CA2	CA1	CA0	BA3	BA2	BA1	BAO
	R/W							

Figure 80. MMU Common/Bank Area Register (CBAR: I/O Address = 3AH)

CA3–CA0:CA (Bits 7–4). CA specifies the start (Low) address (on 4-KB boundaries) for Common Area 1. This condition also determines the most recent address of the Bank Area. All bits of CA are set to 1 during RESET.

OPERATION MODE CONTROL REGISTER

The Z8S180/Z8L180 is descended from two different ancestor processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.

Operation Mode Control Register

Mnemonic OMCR Address 3EH



Figure 81. Operating Control Register (OMCR: I/O Address = 3EH)

BA3–BA0 (Bits 3–0). BA specifies the start (Low) address (on 4-KB boundaries) for the Bank Area. This condition also determines the most recent address of Common Area 0. All bits of BA are set to 1 during RESET.

M1E ($\overline{M1}$ Enable). This bit controls the $\overline{M1}$ output and is set to a 1 during reset.

When M1E = 1, the $\overline{M1}$ output is asserted Low during the opcode fetch cycle, the $\overline{INT0}$ acknowledge cycle, and the first machine cycle of the \overline{NMI} acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch one RETI instruction. When fetching a RETI from zero-wait-state memory, the processor uses three clock machine cycles that are not fully Z80-timing-compatible.

When M1E = 0, the processor does not drive $\overline{M1}$ Low during instruction fetch cycles. After fetching one RETI instruction with normal timing, the processor returns and refetches the instruction using Z80-compatible cycles that drive $\overline{M1}$ Low. This timing compatibility may be required by external Z80 peripherals to properly decode the RETI instruction.



Figure 82. RETI Instruction Sequence with M1E = 0

I/O CONTROL REGISTER

The I/O Control Register (ICR) allows relocation of the internal I/O addresses. ICR also controls the enabling and disabling of IOSTOP mode (Figure 83).



Figure 83. I/O Control Register (ICR: I/O Address = 3FH)

IOA7, 6: I/O Address Relocation (Bits 7,6). IOA7 and IOA6 relocate internal I/O as indicated in Figure 84.

Note: The high-order 8 bits of 16-bit internal I/O address are always 0. IOA7 and IOA6 are cleared to 0 during RESET.





IOSTP: IOSTOP Mode (Bit 5). IOSTOP mode is enabled when IOSTP is set to 1. Normal I/O operation resumes when IOSTP is reprogrammed or RESET to 0.

PACKAGE INFORMATION



Figure 85. 64-Pin DIP Package Diagram



Figure 86. 80-Pin QFP Package Diagram



Figure 87. 68-Pin PLCC Package Diagram

ORDERING INFORMATION

Codes	
Speed	10 = 10 MHz
	20 = 20 MHz
	33 = 33 MHz
Package	P = 60-Pin Plastic DIP
	V = 68-Pin PLCC
	F = 80-Pin QFP
Temperature	$S = 0^{\circ}C \text{ to } + 70^{\circ}C$
	$E = -40^{\circ}C \text{ to } +85^{\circ}C$
Environmental	C = Plastic Standard

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Example:



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