XR22800

Hi-Speed USB to 10/100 Ethernet Bridge

A New Direction in Mixed-Signal

General Description

The XR22800 is a Hi-Speed USB 2.0 compound device with an embedded hub and 3 downstream USB functions: 10/100 Ethernet Controller, multi-master capable I^2C controller, and an Enhanced Dedicated GPIO Entity (EDGE) controller.

The upstream USB interface has an integrated USB 2.0 PHY and device controller that is compliant with both Hi-Speed (480Mbps) and Full-Speed (12Mbps) USB 2.0. The vendor ID, product ID, power mode, remote wakeup support and maximum power consumption are amongst the values that can be programmed using the on-chip One-Time Programmable (OTP) memory.

The Ethernet controller has an integrated 10/100 Ethernet MAC and PHY and is compliant with IEEE 802.3. The Ethernet controller supports auto-negotiation, auto-MDIX, checksum offload, auto-polarity correction in 10Base-T and remote wakeup capabilities.

The multi-master capable I^2C controller and EDGE controller (8 GPIOs) can be accessed via the USB HID interface. The EDGE pins or I^2C interface can be used for controlling and monitoring other peripherals. Up to 2 EDGE pins can be configured as a PWM generator.

FEATURES

- USB 2.0 Compliant Interface
- 10/100 Ethernet Controller
- I^2C Multi-master
- Enhanced Dedicated GPIO Entity (EDGE)
- Single +5.0V Power Supply Input
- Regulated +3.3V Output Power
- Single 25MHz Crystal
- ±15kV HBM ESD Protection on USB data pins
- ±8kV HBM ESD Protection on all other pins

APPLICATIONS

- USB to Ethernet Dongles
- POS Terminals
- Test Instrumentation
- Networking
- Factory Automation and Process Controls
- Industrial Applications

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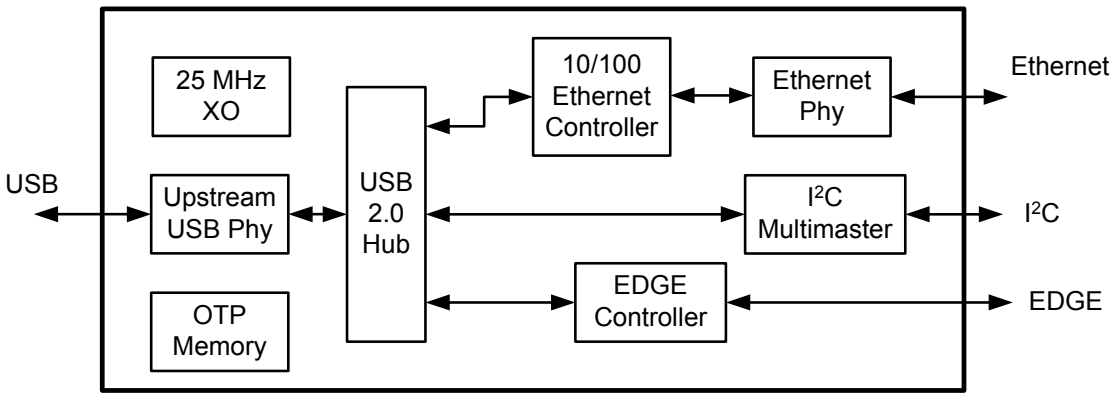
Block Diagram



Extended Features

- USB 2.0 Compliant Interface
  - Integrated USB 2.0 PHY
  - Supports 480 Mbps USB Hi-Speed and 12 Mbps USB Full-Speed data rate
  - Supports USB suspend, resume and remote wakeup operations
  - Compatible with USB CDC-ECM
- 10/100 Ethernet Controller
  - Compliant with IEEE 802.3
  - Integrated 10/100 Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full-duplex and half-duplex support
  - Full-duplex and half-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Diagnostic loop-back modes
  - TCP/UDP/IP/ICMP checksum offload support
  - Flexible Address filtering modes
  - Wakeup packet support
  - Support for 2 status LEDs
- I^2C Multi-master
  - Up to 400 kbps transfers
  - Multi-master capable
- Enhanced Dedicated GPIO Entity (EDGE)
  - Parallel GPIO access
  - Two PWM generators
- Custom Ethernet software drivers
  - Windows 2000, XP, Vista, Win 7 and Win 8
  - Windows CE 5.0, 6.0, 7.0
  - Linux
  - OS X

Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

V_{CC} Supply Voltage.....+5.75V

Input Voltage

(all pins except SCL, SDA, USBD+, USBD–).....-0.3 to +4.0V

Input Voltage (USBD+ and USBD–).....-0.3V to +5.75V

Input Voltage (SCL and SDA).....-0.3V to +6.0V

Junction Temperature.....125°C

Operating Conditions

Operating Temperature Range.....-40°C to +85°C

V_{CC} Supply Voltage.....+4.4V to +5.25V

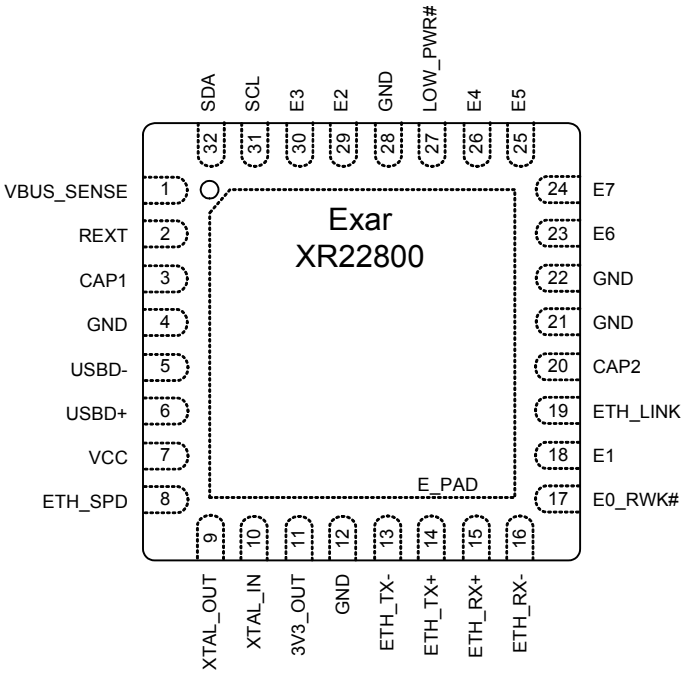
Electrical Characteristics

Unless otherwise noted: T_A = -40°C to +85°C, V_{CC} = 4.4V to 5.25V

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Power Consumption							
I_{CC}	Operating Current	No load on GPIO pins or 3V3_OUT			185	250	mA
I_{SUSP}	Suspend Mode Current	No load on GPIO pins or 3V3_OUT			3	4.5	mA
VBUS_SENSE, LOW_PWR# and EDGE Pins							
V_{IL}	Input Low Voltage			-0.3		0.8	V
V_{IH}	Input High Voltage			2.0		3.6	V
V_{OL}	Output Low Voltage	I_{OL} = 4mA				0.3	V
V_{OH}	Output High Voltage	I_{OL} = -4mA		2.2			V
I_{IL}	Input Low Leakage Current					±10	µA
I_{IH}	Input High Leakage Current					±10	µA
C_{IN}	Input Pin Capacitance					5	pF
USB I/O Pins							
V_{OL}	Output Low Voltage	Full-speed USB. External 15kΩ to GND on USBD+ and USBD- pins		0		0.3	V
V_{OH}	Output High Voltage	Full-speed USB. External 15kΩ to GND on USBD+ and USBD- pins		2.8		3.6	V
V_{OL}	Output Low Voltage	Hi-speed USB. External 45 Ω to GND on USBD+ and USBD- pins		-300		300	mV
V_{OH}	Output High Voltage	Hi-speed USB. External 45 Ω to GND on USBD+ and USBD- pins		360		440	mV
V_{DrvZ}	Driver Output Impedance				45		Ω
I_{OSC}	Output Short Circuit Current	1.5V on USBD+ and USBD- pins				52	mA

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Ethernet I/O Pins - 100Base-TX transmit mode							
V_{PPH}	Peak Differential Output Voltage High	Measured at line side of transformer, line replaced by differential resistance of 100 ohms.		950		1050	mV
V_{PPL}	Peak Differential Output Voltage Low			-950		-1050	mV
V_{SAS}	Signal Amplitude Symmetry			98		102	%
T_{RF}	Signal Rise and Fall Time			3		5	ns
D_{CD}	Duty Cycle Distortion			0		0.5	ns
V_{OS}	Overshoot and Undershoot			0		5	%
-	Transmit Jitter	Measured differentially		0		1.4	ns
Ethernet I/O Pins - 10Base-T transmit mode							
V_{PPH}	Peak Differential Output Voltage High	Measured at line side of transformer, line replaced by differential resistance of 100 ohms.		2.2		2.8	V
3.3V Regulated Power Output							
V_{OUT}	Output Voltage	Max load current 50 mA		3.0	3.3	3.6	V

Pin Configuration



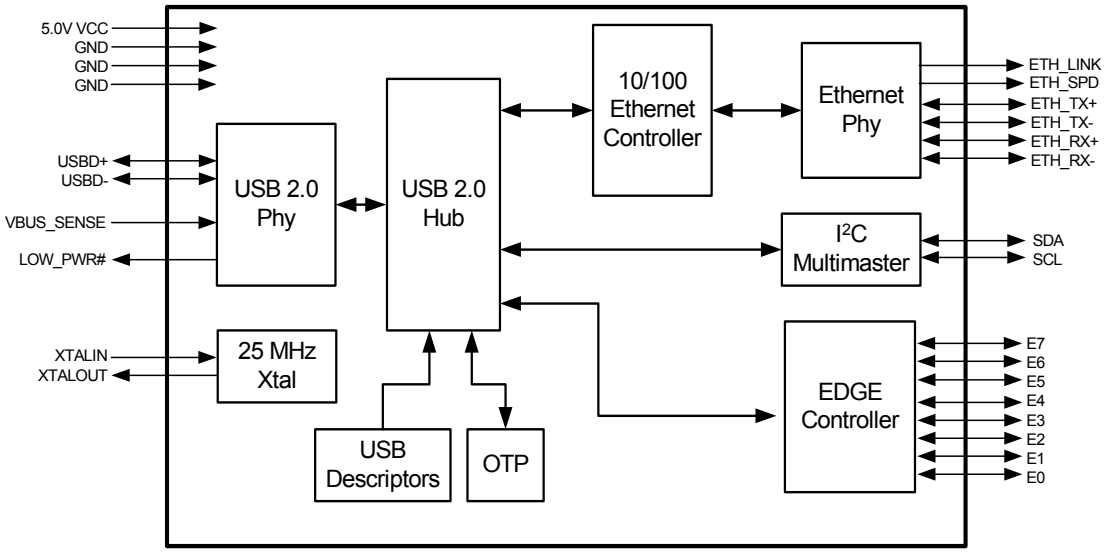
Pin Assignments

Pin No.	Pin Name	Type	Description
1	VBUS_SENSE	I	VBUS Sense input. In self-powered mode, the VBUS from the USB connector needs to be connected to this pin through a voltage divider circuit (VBUS = 5V, VBUS_SENSE = 3.3V input) using large resistance values to minimize power. It should also be decoupled by a 0.1uF capacitor. This feature must be enabled via the OTP whenever the hub function is configured for bus powered mode. This VBUS_SENSE input is used to disable the pull-up resistor on the USBD+ signal when VBUS is not present. In bus-powered mode, this pin is ignored.
2	REXT	I	Connect externally using short trace to 226 ohm 1% resistor to ground
3	CAP1	I	Connect externally to CAP2 and 3V3_OUT using short trace
4	GND	PWR	Power supply common, ground
5	USBD–	I/O	USB port differential data negative.
6	USBD+	I/O	USB port differential data positive.
7	VCC	PWR	5.0V power supply input
8	ETH_SPD	O	Ethernet 100 Mbps Speed Indicator
9	XTALOUT	O	Crystal or buffered clock output.
10	XTALIN	I	25 MHz +/- 50 ppm Crystal or external clock input.
11	3V3_OUT	PWR	3.3 V output power. Connect externally to CAP1 and CAP2 using short trace and decouple with minimum of 4.7uF capacitor
12	GND	PWR	Power supply common, ground
13	ETH_TX–	O	Ethernet transmit data out negative

Pin No.	Pin Name	Type	Description
14	ETH_TX+	O	Ethernet transmit data out positive
15	ETH_RX+	I	Ethernet receive data in positive
16	ETH_RX–	I	Ethernet receive data in negative
17	E0	I/O	Enhanced general purpose IO
18	E1	I/O	Enhanced general purpose IO
19	ETH_LINK	O	Ethernet 10/100 Activity Indicator
20	CAP2	I	Connect externally to CAP1 and 3V3_OUT using short trace
21	GND	PWR	Power supply common, ground
22	GND	PWR	Power supply common, ground
23	E6	I/O	Enhanced general purpose IO
24	E7	I/O	Enhanced general purpose IO
25	E5	I/O	Enhanced general purpose IO
26	E4	I/O	Enhanced general purpose IO
27	LOW_PWR#	O	The LOW_PWR# pin will be asserted whenever it is not safe to draw the amount of current requested from VBUS in the Device Maximum Power field of the Configuration Descriptor. The LOW_PWR# pin is asserted when the XR22800 is in suspend mode or when it is not yet configured. The LOW_PWR# pin will be de-asserted whenever it is safe to draw the amount of current requested in the Device Maximum Power field. Note that the XR22800 device is a high power device. The default polarity of the LOW_PWR# output pin is active low and is programmable via the OTP.
28	GND	PWR	Power supply common, ground
29	E2	I/O	Enhanced general purpose IO.
30	E3	I/O	Enhanced general purpose IO.
31	SCL	I/O OD	I^2C Master controller serial clock (open-drain) External pull-up resistor required on this pin.
32	SDA	I/O OD	I^2C Master controller data (open-drain). External pull-up resistor required on this pin.

Type: I = Input, O = Output, I/O = Input/Output, PWR = Power, OD = Open-Drain

Functional Block Diagram



Functional Description

USB Interface

The XR22800 is a USB compound device with an embedded hub and 3 downstream USB functions. The downstream functions of the XR22800 are 10/100 Ethernet, an I^2C function, and an Enhanced Dedicated GPIO Entity (EDGE) function. The upstream USB interface of the XR22800 is compliant with both USB 2.0 full and hi-speed specifications. All functions downstream of the hub are hi-speed functions.

The XR22800 will have a single vendor ID and vendor string. Each function in the XR22800 will have an individual product string and serial string. The default serial number strings will be based upon the uniquely assigned Ethernet MAC address for each XR22800 device. The serial strings for multiple functions within the same device will differ only by a single character which will be assigned a value between 0 and 7. All string and ID values can be overridden via OTP.

The XR22800 can be placed into a low power or suspended state by the USB host. By default the XR22800 hub is configured for bus powered mode with a maximum power of 250 mA. All other functions in the XR22800 are configured for self-powered mode. In bus powered mode, the Ethernet Phy must be powered down during suspended state to meet USB suspend power requirements. The Ethernet Phy may remain enabled to support Ethernet remote wakeup during suspend if the OTP is modified to report the hub function as self-powered in the USB descriptors. See Ethernet Remote Wakeup section on page 10.

Each function of the XR22800 supports one configuration and utilizes the following USB endpoints:

- USB hub
  - Control endpoint
  - Interrupt-in endpoint
- Ethernet function
  - Control endpoint
  - Interrupt-in endpoint
  - Bulk-in and bulk-out endpoints
- I^2C function
  - Control endpoint
  - Interrupt-in and interrupt-out endpoints
- EDGE Controller function
  - Control endpoint
  - Interrupt-in and interrupt-out endpoints

USB Vendor ID

Exar's USB vendor ID is 0x04E2. This is the default vendor ID that is used for the XR22800. Companies may obtain their own vendor ID, by becoming members of USB.org. The XR22800 OTP can then be modified to report this vendor ID in the USB descriptors.

USB Product ID

Each function in the XR22800 has an individual USB product ID. The default product IDs for each of the functions are shown in Table 1. These values can be modified by programming the OTP. Companies using their own vendor ID may also select their own product IDs. Additionally, upon request Exar will provide a selection of different product IDs for use with Exar's vendor ID for companies that do not wish to become members of USB.org, but wish to use their own product ID.

Table 1: Default XR22800 Product IDs

XR22800 Function	Default Product ID
Hub	0x0801
Ethernet 10/100	0x1300
I^2C	0x1100
EDGE	0x1200

USB Suspend

All USB peripheral devices must support the USB suspend mode. Per USB standard, the XR22800 device will begin to enter the suspend state if it does not detect any activity, (including Start of Frame or SOF packets) on its USB data lines for 3 ms. The peripheral device must then reduce power consumption from VBUS power within the next 7 ms to the allowed limit of 2.5 mA per function for the suspended state. Because the XR22800 is a compound device with 4 functions, the suspend state power limit is 10 mA for the device. Note that in this context, the "device" is all circuitry (including the XR22800) that draws power from the host VBUS.

USB Strings

USB specifies three character string descriptors that are provided to the USB host during enumeration in string descriptors: the manufacturer, product and serial strings. In a compound device such as the XR22800, each function provides these strings to the USB host. The default manufacturer string for the XR22800 device is "Exar Corp.". The default product strings for the hub, Ethernet function, I^2C function and EDGE function are shown in Table 2. The serial number string is a unique alpha-numeric ASCII string programmed into the device at the factory.

Table 2: Default XR22800 Product Strings

XR22800 Function	Default Product String
Hub	Exar's XR22800 Hub
Ethernet 10/100	Exar USB Ethernet
I^2C	Exar USB I^2C
EDGE	Exar USB EDGE

The OTP may be used to override these strings. However, to ensure unique serial numbers for each device, it is recommended that the factory pre-programmed serial number string be used and not be overwritten via OTP.

USB Device Drivers

Each of the functions in the XR22800 require a USB device driver for operation. Both the I^2C and EDGE functions conform to the HID device class and as such, utilize the embedded HID driver that is native to each Operating System. The Ethernet function conforms to the CDC device class and as such can utilize an embedded CDC-ECM driver. However, at the time of this writing, none of the Microsoft OS provide support for CDC-ECM embedded drivers. Both Linux and Mac OS-X platforms do support CDC-ECM drivers.

The CDC-ECM is a "standard" driver which implements functionality on a specific class of devices. They operate without any ability to access device specific register sets. In some cases, this can limit the functionality and / or throughput capability of the XR22800. Exar provides a custom Ethernet device driver which has been optimized for the best possible data through-put in Windows and Linux platforms. This custom driver also allows for access to the device register set and thus full control of the XR22800 device functionality. Refer to 10/100 Ethernet section on page 10 for more details.

10/100 Ethernet

The Ethernet port is a 10/100 Ethernet MAC and Phy compliant with IEEE 802.3. The Ethernet port supports speed / duplex auto-negotiation, auto-MDIX, 10 Mbps data auto-polarity, full and half duplex data rates at 10 and 100 Mbps, generates and validates the 32-bit FCS, and performs unicast and multicast filtering. The XR22800 also performs TCP, UDP and ICMP checksum offload over IPV4 and IPV6 as well as header checksum offload in IPV4. On chip RAM provides all required packet buffering.

In Windows OS, using the Exar custom Ethernet driver, the properties dialog, advanced properties can be used to set the pause frame flow control, speed and duplex, auto-negotiation, checksum offload, and Ethernet remote wakeup settings. By default, the Ethernet MAC will honor incoming pause frames sent by a peer Ethernet device, but will not generate pause frames. Auto-MDIX is always enabled.

Ethernet Remote Wakeup

If the XR22800 hub is configured as a self-powered device and has Ethernet remote wakeup enabled, the XR22800 will request the USB host to resume in response to a magic packet or a link state change on the Ethernet port. When the USB host is suspended, the Ethernet Phy remains active and the XR22800 is able to both meet USB suspend mode power requirements as well as respond to magic packet and link state changes.

The magic packet is an Ethernet packet with specific content, i.e. 6 bytes of 0xFF, followed by 16 repetitions of the target MAC address (MAC address of the XR22800 device). This content can occur anywhere in the incoming packet payload. The link state change will wake the USB host if the link is down when the USB host is suspended and then the link goes up, or if the link is up when the USB host is suspended and then the link goes down.

EDGE - Enhanced Dedicated GPIO Entity

The XR22800 has 8 EDGE IO pins The EDGE controller allows for GPIO signals to be individually set or cleared or to be grouped, such that the all pins in the group can be simultaneously accessed for reads or writes. Note that on write accesses, output pins will change in 4-bit subgroups on core clock (60 MHz) boundaries. For example, if an 8 bit data group is defined and the data value is written from 0x00 to 0xFF, 4 bits would change from ’0’ to ’1’ followed by the next 4 bits one clock cycle (~ 17 ns) later.

EDGE IOs can be configured as inputs or outputs. Outputs can be configured as push-pull or open drain and can be tri-stated. Inputs can be configured to generate interrupts to the USB host on either negative or postive edge transitions.

Another feature of the EDGE controller is that up to 2 GPIO pins within the EDGE can be assigned to pulse width modulated (PWM) outputs. Each of the PWM outputs can be used to generate an output clock or pulse of varying duty cycle. Both low and high cycles can be configured in steps of 267 ns up to 1.092 ms. The output can be controlled to generate a single "one-shot" pulse or to free run. Refer to the EDGE_PWM0_CTRL and EDGE_PWM1_CTRL registers on page 19 for control of PWM outputs.

I^2C

The XR22800 implements an I^2C multi-master using the control endpoint of the full-speed USB function to transfer data to and from the I^2C interface. The I^2C master supports both standard (100 kbps) and fast (400 kbps) modes and supports multiple master configurations to allow other devices to access slave devices on the I^2C. The I^2C function is an HID function and uses the native HID driver. It supports both 7 and 10 bit addressing modes.

Regulated 3.3V Power Output

The XR22800 internal voltage regulator provides 3.3 VDC output power which can be utilized by other circuitry. Refer to Electrical Characteristics” on page 3 for maximum power capability. For bus powered devices, significant utilization of the 3V3 output power may require increasing the maximum power request above the 250 mA default value from the USB host by programming the OTP.

OTP

The OTP is an on-chip non-volatile memory, that is one-time programmable via the USB interface. Bit locations within the memory may be programmed at various times allowing for customization of the XR22800. Some bits are pre-programmed at the factory and caution must be taken not to program any locations except user defined addresses. Contact the factory uarttechsupport@exar.com for information and assistance in programming the XR22800 OTP.

USB Control Commands

The following table shows all of the USB Control Commands that are supported by the XR22800. Commands include standard USB commands and USB vendor specific Exar commands.

Table 3: Supported USB Control Commands

Name	Request Type	Request	Value		Index		Length		Description
			LSB	MSB	LSB	MSB	LSB	MSB	
DEV GET_STATUS	0x80	0x0	0x0	0x0	0x0	0x0	0x2	0x0	Device: remote wake-up + self-powered
IF GET_STATUS	0x81	0x0	0x0	0x0	0x0	0x0	0x2	0x0	Interface: zero
EP GET_STATUS	0x82	0x0	0x0	0x0	0x0, 0x4, 0x84	0x0	0x2	0x0	Endpoint: halted
DEV CLEAR_FEATURE	0x00	0x1	0x1	0x0	0x0	0x0	0x0	0x0	Device remote wake-up
EP CLEAR_FEATURE	0x02	0x1	0x0	0x0	0x0, 0x4, 0x84	0x0	0x0	0x0	Endpoint halt
DEV SET_FEATURE	0x00	0x3	0x1	0x0	0x0	0x0	0x0	0x0	Device remote wake-up
EP SET_FEATURE	0x02	0x3	0x0	0x0	0x0, 0x4, 0x84	0x0	0x0	0x0	Endpoint halt
SET_ADDRESS	0x00	0x5	addr	0x0	0x0	0x0	0x0	0x0	addr = 1 to 127
GET_DESCRIPTOR	0x80	0x6	0x0	0x1	0x0	0x0	len MSB	len MSB	Device descriptor
GET_DESCRIPTOR	0x80	0x6	0x0	0x2	LangID	LangID	len MSB	len MSB	Configuration descriptor
GET_DESCRIPTOR	0x80	0x6	0x0	0x3	0x0	0x0	len MSB	len MSB	String descriptor
GET_CONFIGURATION	0x80	0x8	0x0	0x0	0x0	0x0	0x1	0x0	
SET_CONFIGURATION	0x00	0x9	n	0x0	0x0	0x0	0x0	0x0	n = 0, 1
XR_GET_CHIP_ID	0xC0	0xFF	0x0	0x0	0x0	0x0	0x6	0x0	Get Exar VID (2 bytes), PID (2 bytes) and bcdDevice (2 bytes)

HID Reports

The I²C and EDGE functions in the XR22800 are both HID functions. Register access for these HID functions is performed via HID feature reports. These reports use indirect addressing such that for register reads, the address must first be written and then data can be read. Registers accessible via the HID reports along with the register descriptions are given in the following sections.

WRITE_HID_REGISTER

Transfer Type: Control Out
Transfer Size: 5 bytes
The WRITE_HID_REGISTER report writes 2 bytes of data to the specified register address.

Field	Offset	Size	Value	Description
Report ID	0	1	0x3C	Write HID register
Write Address LSB	1	1		Write address
Write Address MSB	2	1		
Write Data LSB	3	1		Write data
Write Data MSB	4	1		

SET_HID_READ_ADDRESS

Transfer Type: Control Out
Transfer Size: 3 bytes
The SET_HID_READ_ADDRESS report sets the address for the READ_HID_REGISTER report.

Field	Offset	Size	Value	Description
Report ID	0	1	0x4B	Set address for HID register read
Read Address LSB	1	1		Read address
Read Address MSB	2	1		

READ_HID_REGISTER

Transfer Type: Control In
Transfer Size: 3 bytes
The READ_HID_REGISTER report reads register data from the address set by the SET_HID_READ_ADDRESS report.

Field	Offset	Size	Value	Description
Report ID	0	1	0x5A	Read HID register
Read Data LSB	1	1		Read data
Read Data MSB	2	1		

HID Register Map

Table 4: XR22800 HID Register Map

Address	Register Name	Bit 7 (15)	Bit 6 (14)	Bit 5 (13)	Bit 4 (12)	Bit 3 (11)	Bit 2 (10)	Bit 1 (9)	Bit 0 (8)
I^2C Registers									
0x341	I^2C_SCL_LOW MSB [BITS 15:8]	VALUE (MSB)							
	I^2C_SCL_LOW LSB [BITS 7:0]	VALUE (LSB)							
0x342	I^2C_SCL_HIGH MSB [BITS 15:8]	VALUE (MSB)							
	I^2C_SCL_HIGH LSB [BITS 7:0]	VALUE (LSB)							
EDGE Registers									
0x3C1	EDGE_DIR	E7	E6	E5	E4	E3	E2	E1	E0
0x3C2	EDGE_SET	E7	E6	E5	E4	E3	E2	E1	E0
0x3C3	EDGE_CLEAR	E7	E6	E5	E4	E3	E2	E1	E0
0x3C4	EDGE_STATE	E7	E6	E5	E4	E3	E2	E1	E0
0x3C5	EDGE_TRI_STATE	E7	E6	E5	E4	E3	E2	E1	E0
0x3C6	EDGE_OPEN_DRAIN	E7	E6	E5	E4	E3	E2	E1	E0
0x3C7	EDGE_PULL_UP	E7	E6	E5	E4	E3	E2	E1	E0
0x3C8	EDGE_PULL_DOWN	E7	E6	E5	E4	E3	E2	E1	E0
0x3C9	EDGE_INTR_MASK	E7	E6	E5	E4	E3	E2	E1	E0
0x3CA	EDGE_INTR_POS_ EDGE	E7	E6	E5	E4	E3	E2	E1	E0
0x3D8	EDGE_PWM0_CTRL MSB [BITS 15:8]	0	0	0	0	0	0	0	CMD[2]
	EDGE_PWM0_CTRL LSB [BITS 7:0]	CMD[1:0]		EN	0	0	PIN		
0x3D9	EDGE_PWM0_HIGH MSB [BITS 15:8]	0	0	0	0	VALUE[11:8]			
	EDGE_PWM0_HIGH LSB [BITS 7:0]	VALUE [7:0]							
0x3DA	EDGE_PWM0_LOW MSB [BITS 15:8]	0	0	0	0	VALUE[11:8]			
	EDGE_PWM0_LOW LSB [BITS 7:0]	VALUE [7:0]							

Table 4: XR22800 HID Register Map

Address	Register Name	Bit 7 (15)	Bit 6 (14)	Bit 5 (13)	Bit 4 (12)	Bit 3 (11)	Bit 2 (10)	Bit 1 (9)	Bit 0 (8)
0x3DB	EDGE_PWM1_CTRL MSB [BITS 15:8]	0	0	0	0	0	0	0	CMD[2]
	EDGE_PWM1_CTRL LSB [BITS 7:0]	CMD[1:0]		EN	0	0	PIN		
0x3DC	EDGE_PWM1_HIGH MSB [BITS 15:8]	0	0	0	0	VALUE[11:8]			
	EDGE_PWM1_HIGH LSB [BITS 7:0]	VALUE [7:0]							
0x3DD	EDGE_PWM1_LOW MSB [BITS 15:8]	0	0	0	0	VALUE[11:8]			
	EDGE_PWM1_LOW LSB [BITS 7:0]	VALUE [7:0]							

HID Register Descriptions

Note that all register reset default values are '0' unless otherwise specified. All registers are 16 bits.

I²C_SCL_LOW (0x341) - Read/Write

Bit	Default	Description
15:0	0x0144	**Value** Specifies the number of periods that SCL will be asserted low by the XR22800 I²C master. Note that in clock stretching, the I²C slave may extend the SCL low period to delay the next transaction. For 100 kbps transfer rate this value must be at least 252 (0x00FC) and the sum of high and low periods must be at least 600 (0x0258). For 400kbps transfer rate this value must be at least 78 (0x004E) and the sum of the high and low periods must be at least 150 (0x0096). Measured in 60 MHz core clock periods, i.e. approximately 16.7 ns.

I²C_SCL_HIGH (0x342) - Read/Write

Bit	Default	Description
15:0	0x0114	**Value** Specifies the number of periods that SCL will be asserted high by the XR22800 I²C master. Note that another multi-master may assert SCL low before the XR22800 high period is completed. For 100 kbps transfer rate this value must be at least 240 (0x00F0) and the sum of the high and low periods must be at least 600 (0x0258). For 400 kbps transfer rate this value must be at least 36 (0x0024) and the sum of the high and low periods must be at least 150 (0x0096). Measured in 60 MHz core clock periods, i.e. approximately 16.7 ns

EDGE_DIR (0x3C1) - Read/Write

Note that when setting direction of an EDGE IO to output, the EDGE_PULL_UP for that IO pin should also be disabled and when setting an EDGE IO pin to input, the EDGE_PULL_UP for that IO pin should also be enabled.

Bit	Default	Description
15:8	0x00	**Reserved** These bits are reserved and should be written as '0'.
7:0	0x00	**E[7:0]** 0: IO pin assigned to EDGE function is configured as an input 1: IO pin assigned to EDGE function is configured as an output.

EDGE_SET (0x3C2) - Write Only

Bit	Default	Description
15:8	0x00	**Reserved** These bits are reserved and should be written as '0'.
7:0	0x00	**E[7:0]** 0: No effect 1: Set IO pin assigned to EDGE function and configured as an output to a logic '1'

EDGE_CLEAR (0x3C3) - Write Only

Bit	Default	Description
15:8	0x00	**Reserved** These bits are reserved and should be written as '0'.
7:0	0x00	**E[7:0]** 0: No effect 1: Clear IO pin assigned to EDGE function and configured as an output to a logic '0'

EDGE_STATE (0x3C4) - Read/Write

Bit	Default	Description
15:8	0xFF	**Reserved** These bits are reserved and should be written as '1'.
7:0	0x00	**E[7:0]** Writing in this register sets or clears the EDGE IO pin(s) configured as an output. Writing to an EDGE pin configured as an input has no effect. Reading this register returns the state of each IO pin configured as an EDGE pin irrespective of whether it is configured as an input or output. Note that output transitions across multiple IO pins may be slightly staggered. Refer to page 10. 0: Write clears the corresponding bit to a '0'. Read returns the current state. 1: Write sets the corresponding bit to a '1'. Read returns the current state.

EDGE_TRI_STATE (0x3C5) - Read/Write

Bit	Default	Description
15:8	0x00	**Reserved** These bits are reserved and should be written as '0'.
7:0	0x00	**E[7:0]** 0: IO pin assigned to EDGE function and configured as an output is actively driven 1: IO pin assigned to EDGE function and configured as an output is tri-stated

EDGE_OPEN_DRAIN (0x3C6) - Read/Write

Bit	Default	Description
15:8	0x00	**Reserved** These bits are reserved and should be written as '0'.

Bit	Default	Description
7:0	0x00	**E[7:0]** Note that XR22800 open drain outputs have a weak internal pull-up. 0: IO pin assigned to EDGE function and configured as an output is a push-pull output 1: IO pin assigned to EDGE function and configured as an output is an open drain output

EDGE_PULL_UP (0x3C7) - Read/Write

Bit	Default	Description
15:8	0xFF	**Reserved** These bits are reserved and should be written as '1'.
7:0	0xFF	**E[7:0]** 0: Disable internal pull-up resistor on IO pin assigned to EDGE function and configured as an input 1: Enable internal pull-up resistor on IO pin assigned to EDGE function and configured as an input

EDGE_PULL_DOWN (0x3C8) - Read/Write

Bit	Default	Description
15:8	0x00	**Reserved** These bits are reserved and should be written as '0'.
7:0	0x00	**E[7:0]** 0: Disable internal pull-down resistor on IO pin assigned to EDGE function and configured as an input 1: Enable internal pull-down resistor on IO pin assigned to EDGE function and configured as an input

EDGE_INTR_MASK (0x3C9) - Read/Write

Bit	Default	Description
15:8	0x00	**Reserved** These bits are reserved and should be written as '0'.
7:0	0x00	**E[7:0]** Writing a '1' in this register enables an input pin for the corresponding bit position EDGE IO pin(s) configured as an input to generate an interrupt if either EDGE_INTR_POS_EDGE and / or EDGE _INTR_NEG_EDGE registers has also been enabled. An EDGE pin configured as an output has no effect. 0: IO pin will not generate an interrupt 1: IO pin assigned to EDGE function and configured as an input will generate an interrupt

EDGE_INTR_POS_EDGE (0x3CA) - Read/Write

Bit	Default	Description
15:8	0xFF	**Reserved** These bits are reserved and should be written as '1'.
7:0	0xFF	**E[7:0]** Writing a '1' in this register enables an interrupt to be generated on the rising edge of the corresponding bit position EDGE IO pin(s) configured as an input if the EDGE_INTR_MASK register is enabled for that pin. If the EDGE_INTR_NEG_EDGE register is also enabled, interrupts will be generated on both edges. Writing to an EDGE pin configured as an output has no effect. 0: IO pin will not generate an interrupt on rising edge 1: IO pin assigned to EDGE function and configured as an input will generate an interrupt on rising edge if corresponding EDGE_INTR_MASK bit is set

EDGE_INTR_NEG_EDGE (0x3CB) - Read/Write

Bit	Default	Description
15:8	0xFF	**Reserved** These bits are reserved and should be written as '1'.
7:0	0xFF	**E[7:0]** Writing a '1' in this register enables an interrupt to be generated on the falling edge of the corresponding bit position EDGE IO pin(s) configured as an input if the EDGE_INTR_MASK register is enabled for that pin. If the EDGE_INTR_POS_EDGE register is also enabled, interrupts will be generated on both edges. Writing to an EDGE pin configured as an output has no effect. 0: IO pin will not generate an interrupt on falling edge 1: IO pin assigned to EDGE function and configured as an input will generate an interrupt on falling edge if corresponding EDGE_INTR_MASK bit is set

EDGE_PWM0_CTRL (0x3D8) - Read/Write

Bit	Default	Description
15:9	0x00	**Reserved** These bits are reserved and should be written as '0'.
8:6	0x0	**Cmd** 000: Idle. output pin remains at same state 001: Undefined, do not use 010: Undefined, do not use 011: Undefined, do not use 100: Assert logic '0' 101: One-shot -If previous state was assert '0', one-shot pulse will be high, If previous state was assert '1', one-shot pulse will be low 110: Free run output 111: Assert logic '0'

Bit	Default	Description
5	0	**Enable** 0: PWM0 output is not enabled 1: PWM0 output is enabled on pin specified in Pin field using mode specified in Cmd field
4:3	0x0	**Reserved** These bits are reserved and should be written as '0'.
2:0	0x0	**Pin** Specifies which pin (E7 - E0) will be assigned to PWM0 output.

EDGE_PWM0_HIGH (0x3D9) - Read/Write

Bit	Default	Description
15:12	0x0	**Reserved** These bits are reserved and should be written as '0'.
11:0	0x001	**Value** This register specifies the high period for PWM0 in increments of 266.667ns. High period must be in the range of 1 to 4095 (266.667 ns to 1.092 ms)

EDGE_PWM0_LOW (0x3DA) - Read/Write

Bit	Default	Description
15:12	0x0	**Reserved** These bits are reserved and should be written as '0'.
11:0	001	**Value** This register specifies the low period for PWM0 in increments of 266.667ns. Low period must be in the range of 1 to 4095 (266.667 ns to 1.092 ms)

EDGE_PWM1_CTRL (0x3DB) - Read/Write

Bit	Default	Description
15:9	0x00	**Reserved** These bits are reserved and should be written as '0'.
8:6	0x0	**Cmd** 000: Idle. output pin remains at same state 001: Undefined, do not use 010: Undefined, do not use 011: Undefined, do not use 100: Assert logic '0' 101: One-shot -If previous state was assert '0', one-shot pulse will be high, If previous state was assert '1', one-shot pulse will be low 110: Free run output 111: Assert logic '0'

Bit	Default	Description
5	0	**Enable** 0: PWM1 output is not enabled 1: PWM1 output is enabled on pin specified in Pin field using mode specified in Cmd field
4:3	0x0	**Reserved** These bits are reserved and should be written as '0'.
2:0	0x0	**Pin** Specifies which pin (E7 - E0) will be assigned to PWM1 output.

EDGE_PWM1_HIGH (0x3DC) - Read/Write

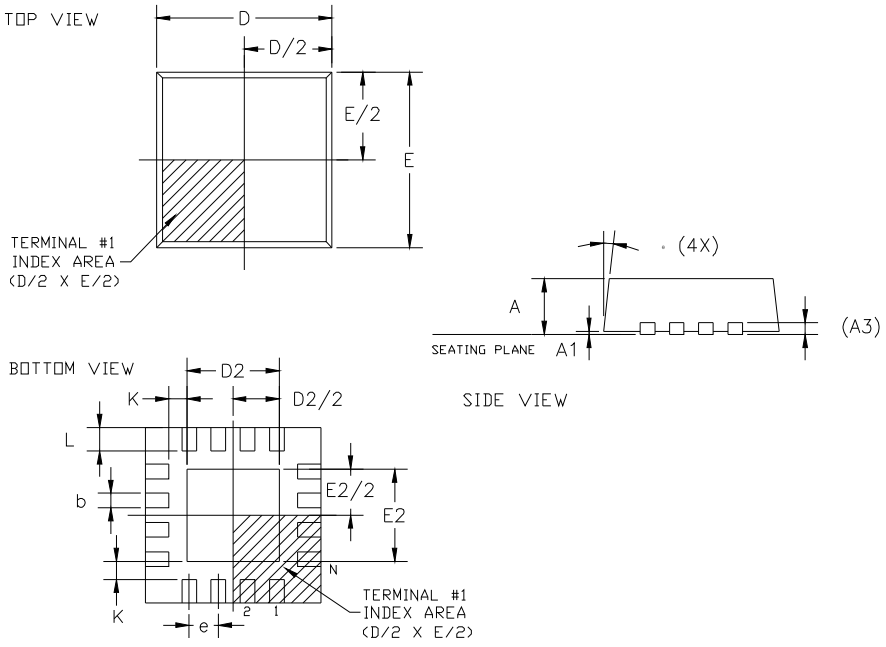
Bit	Default	Description
15:12	0x0	**Reserved** These bits are reserved and should be written as '0'.
11:0	0x001	**Value** This register specifies the high period for PWM1 in increments of 266.667ns. High period must be in the range of 1 to 4095 (266.667 ns to 1.092 ms)

EDGE_PWM1_LOW (0x3DD) - Read/Write

Bit	Default	Description
15:12	0x0	**Reserved** These bits are reserved and should be written as '0'.
11:0	0x001	**Value** This register specifies the low period for PWM1 in increments of 266.667ns. Low period must be in the range of 1 to 4095 (266.667 ns to 1.092 ms)

Mechanical Dimensions

32-Pin QFN



32LD 5x5 QFN (OPTION 3) JEDEC MO-220 Variation VHHD-4						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
D2	3.50	3.65	3.80	0.138	0.144	0.150
E	5.00 BSC			0.197 BSC		
E2	3.50	3.65	3.80	0.138	0.144	0.150
e	0.50 BSC			0.020 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
K	0.20	—	—	0.008	—	—
θ	0°	—	14°	0°	—	14°
N	32			32		
ND	8			8		
NE	8			8		

Ordering Information

Part Number	Package	Green	Operating Temperature Range	Packaging Quantity	Marking
XR22800IL32-F	32-pin QFN	Yes	-40°C to +85°C	490 / Tray	XR22800
XR22800IL32TR-F	32-pin QFN	Yes	-40°C to +85°C	3000 / Reel	XR22800

Revision History

Revision	Date	Description
1A	July 2014	Initial Release

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