MAX9210/MAX9214/ MAX9220/MAX9222

Programmable DC-Balance 21-Bit Deserializers

General Description

The MAX9210/MAX9214/MAX9220/MAX9222 deserialize three LVDS serial data inputs into 21 single-ended LVCMOS/ LVTTL outputs. A parallel rate LVDS clock received with the LVDS data streams provides timing for deserialization. The outputs have a separate supply, allowing 1.8V to 5V output logic levels.

The MAX9210/MAX9214/MAX9220/MAX9222 feature programmable DC balance, which allows isolation between a serializer and deserializer using AC-coupling. Each deserializer decodes data transmitted by one of MAX9209/MAX9213 serializers.

The MAX9210/MAX9214 have rising-edge output strobes, and when DC balance is not programmed, are compatible with non-DC-balanced 21-bit deserializers such as the DS90CR216A and DS90CR218A. The MAX9220/MAX9222 have falling-edge output strobes.

Two frequency versions and two DC-balance default conditions are available for maximum replacement flexibility and compatibility with popular non-DC-balanced deserializers. The transition time of the single-ended outputs is increased on the low-frequency version parts (MAX9210/MAX9220) for reduced EMI. The LVDS inputs meet IEC 61000-4-2 Level 4 ESD specification, ±15kV for Air Discharge and ±8kV Contact Discharge.

The MAX9210/MAX9214/MAX9220/MAX9222 are available in a TSSOP package, and operate over the -40°C to +85°C temperature range.

Applications

- Digital Copiers
- Laser Printers

Features

- Programmable DC Balance or Non-DC Balance
- DC Balance Allows AC-Coupling for Wider Input Common-Mode Voltage Range
- As Low as 8MHz Operation (MAX9210/MAX9220)
- Falling-Edge Output Strobe (MAX9220/MAX9222)
- Slower Output Transitions for Reduced EMI (MAX9210/MAX9220)
- High-Impedance Outputs when $\overline{\text{PWRDWN}}$ is Low Allow Output Busing
- Pin Compatible with DS90CR216A/DS90CR218A (MAX9210/MAX9214)
- Fail-Safe Inputs in Non-DC-Balanced Mode
- 5V Tolerant $\overline{\text{PWRDWN}}$ Input
- PLL Requires No External Components
- Up to 1.785Gbps Throughput
- Separate Output Supply Pins Allow Interface to 1.8V, 2.5V, 3.3V, and 5V Logic
- LVDS Inputs Meet IEC 61000-4-2 Level and ISO 10605 ESD Requirements
- LVDS Inputs Conform to ANSI TIA/EIA-644 LVDS Standard
- Low-Profile 48-Lead TSSOP Package
- +3.3V Main Power Supply
- -40°C to +85°C Operating Temperature Range

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9210EUM	-40°C to +85°C	48 TSSOP
MAX9214EUM	-40°C to +85°C	48 TSSOP
MAX9220EUM	-40°C to +85°C	48 TSSOP
MAX9222EUM	-40°C to +85°C	48 TSSOP

Functional Diagram and Pin Configuration appear at end of data sheet.

19-2864; Rev 6; 5/14

maxim integrated™

Absolute Maximum Ratings

V_{CC} to GND .....-0.5V to +4.0V
V_{CCO} to GND.....-0.5V to +6.0V
RxIN_, RxCLK IN_ to GND .....-0.5V to +4.0V
$\overline{PWRDWN}$ to GND .....-0.5V to +6.0V
DCB/NC to GND.....-0.5V to (V_{CC} + 0.5V)
RxOUT_, RxCLK OUT to GND .....-0.5V to (V_{CCO} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
TSSOP (derate 16mW/°C above +70°C).....1282mW
Storage Temperature Range..... -65°C to +150°C
Junction Temperature.....+150°C

ESD Protection
Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
All Pins to GND .....±5kV
IEC 61000-4-2 (R_D = 330Ω, C_S = 150pF)
Contact Discharge (RxIN_, RxCLK IN_) to GND .....±8kV
Air Discharge (RxIN_, RxCLK IN_) to GND .....±15kV
ISO 10605 (R_D = 2kΩ, C_S = 330pF)
Contact Discharge (RxIN_, RxCLK IN_) to GND .....±8kV
Air Discharge (RxIN_, RxCLK IN_) to GND .....±25kV
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{CC} = +3.0V to +3.6V, V_{CCO} = +3.0V to +5.5V, $\overline{PWRDWN}$ = high, DCB/NC = high or low, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID/2}|$ to 2.4V - $|V_{ID/2}|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = V_{CCO} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.25V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS ($\overline{PWRDWN}$, DCB/NC)								
High-Level Input Voltage	V_{IH}	$\overline{PWRDWN}$			2.0		5.5	V
		DCB/NC			2.0		V_{CC} + 0.3	
Low-Level Input Voltage	V_{IL}				-0.3		+0.8	V
Input Current	I_{IN}	V_{IN} = high or low, $\overline{PWRDWN}$ = high or low			-20		+20	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA					-1.5	V
SINGLE-ENDED OUTPUTS (RxOUT_, RxCLK OUT)								
High-Level Output Voltage	V_{OH}	I_{OH} = -100µA			V_{CCO} - 0.1			V
		I_{OH} = -2mA	MAX9210/ MAX9220	RxCLK OUT	V_{CCO} - 0.25			
				RxOUT_	V_{CCO} - 0.40			
			MAX9214/MAX9222		V_{CCO} - 0.25			
Low-Level Output Voltage	V_{OL}	I_{OL} = 100µA					0.1	V
		I_{OL} = 2mA	MAX9210/ MAX9220	RxCLK OUT			0.2	
				RxOUT_			0.26	
			MAX9214/MAX9222				0.2	
High-Impedance Output Current	I_{OZ}	$\overline{PWRDWN}$ = low, $V_{OUT\_}$ = -0.3V to V_{CCO} + 0.3V			-20		20	µA

DC Electrical Characteristics (continued)

(V_{CC} = +3.0V to +3.6V, V_{CCO} = +3.0V to +5.5V, $\overline{PWRDWN}$ = high, DCB/NC = high or low, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID/2}|$ to 2.4V - $|V_{ID/2}|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = V_{CCO} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.25V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Short-Circuit Current (**Note:** Short one output at a time.)	I_{OS}	V_{CCO} = 3.0V to 3.6V, V_{OUT} = 0	MAX9210/ MAX9220	RxCLK OUT	-10		-40	mA
				RxOUT_	-5		-20	
			MAX9214/MAX9222		-10		-40	
		V_{CCO} = 4.5V to 5.5V, V_{OUT} = 0	MAX9210/ MAX9220	RxCLK OUT	-28		-75	
				RxOUT_	-14		-37	
			MAX9214/MAX9222		-28		-75	
LVDS INPUTS								
Differential Input High Threshold	V_{TH}						50	mV
Differential Input Low Threshold	V_{TL}				-50			mV
Input Current	I_{IN+}, I_{IN-}	$\overline{PWRDWN}$ = high or low			-25		+25	µA
Power-Off Input Current	I_{INO+}, I_{INO-}	V_{CC} = V_{CCO} = 0 or open, DCB/NC, $\overline{PWRDWN}$ = 0 or open			-25		+25	µA
Input Resistor 1	R_{IN1}	$\overline{PWRDWN}$ = high or low, Figure 1			42		78	kΩ
		V_{CC} = V_{CCO} = 0 or open, Figure 1						
Input Resistor 2	R_{IN2}	$\overline{PWRDWN}$ = high or low, Figure 1			246		410	kΩ
		V_{CC} = V_{CCO} = 0 or open, Figure 1						
POWER SUPPLY								
Worst-Case Supply Current	I_{CCW}	C_L = 8pF, worst-case pattern, DC-balanced mode; V_{CC} = V_{CCO} = 3.0V to 3.6V, Figure 2	MAX9210/ MAX9220	8MHz		32	42	mA
				16MHz		46	57	
				34MHz		81	98	
			MAX9214/ MAX9222	16MHz		52	63	
				34MHz		86	106	
				66MHz		152	177	
		C_L = 8pF, worst case pattern, non-DC-balanced mode; V_{CC} = V_{CCO} = 3.0V to 3.6V, Figure 2	MAX9210/ MAX9220	10MHz		33	42	
				20MHz		46	58	
				33MHz		67	80	
				40MHz		78	94	
			MAX9214/ MAX9222	20MHz		53	64	
				33MHz		72	85	
				40MHz		81	99	
				66MHz		127	149	
				85MHz		159	186	
Power-Down Supply Current	I_{CCZ}	$\overline{PWRDWN}$ = low					50	µA

AC Electrical Characteristics

(V_{CC} = V_{CCO} = +3.0V to +3.6V, 100mV_{P-P} at 200kHz supply noise, C_L = 8pF, $\overline{PWRDWN}$ = high, DCB/NC = high or low, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common mode voltage V_{CM} = $|V_{ID/2}|$ to 2.4V - $|V_{ID/2}|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = V_{CCO} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.25V, T_A = 25°C.) (Notes 3, 4, 5)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Rise Time	CLHT	0.1V_{CCO} to 0.9V_{CCO}, Figure 3	MAX9210/ MAX9220	RxOUT_	3.52	5.04	6.24	ns
				RxCLK OUT	2.2	3.15	3.9	
			MAX9214/MAX9222		2.2	3.15	3.9	
Output Fall Time	CHLT	0.9V_{CCO} to 0.1V_{CCO}, Figure 3	MAX9210/ MAX9220	RxOUT_	1.95	3.18	4.35	ns
				RxCLK OUT	1.3	2.12	2.9	
			MAX9214/MAX9222		1.3	2.12	2.9	
RxIN Skew Margin	RSKM	DC-balanced mode, Figure 4 (Note 6)		8MHz	6600	7044		ps
				16MHz	2560	3137		
				34MHz	900	1327		
				66MHz	330	685		
		Non-DC-balanced mode, Figure 4 (Note 6)		10MHz	6600	7044		
				20MHz	2500	3300		
				40MHz	960	1448		
				85MHz	330	685		
RxCLK OUT High Time	RCOH	Figures 5a, 5b			0.35 x RCOP			ns
RxCLK OUT Low Time	RCOL	Figures 5a, 5b			0.35 x RCOP			ns
RxOUT Setup to RxCLK OUT	RSRC	Figures 5a, 5b			0.30 x RCOP			ns
RxOUT Hold from RxCLK OUT	RHRC	Figures 5a, 5b			0.45 x RCOP			ns
RxCLK IN to RxCLK OUT Delay	RCCD	Figures 6a, 6b			4.9	6.17	8.1	ns
Deserializer Phase-Locked Loop Set	RPLLS	Figure 7					32800 x RCIP	ns
Deserializer Power-Down Delay	RPDD	Figure 8					100	ns

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH} and V_{TL}.

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +25°C.

Note 3: AC parameters are guaranteed by design and characterization, and are not production tested. Limits are set at ±6 sigma.

Note 4: C_L includes probe and test jig capacitance.

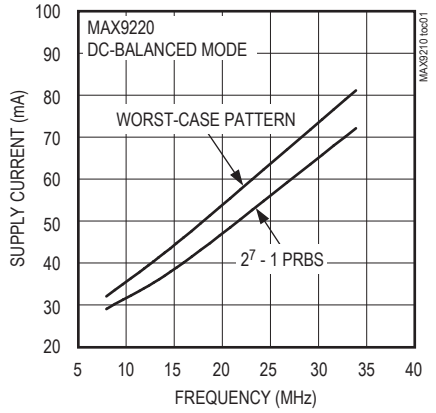
Note 5: RCIP is the period of RxCLK IN. RCOP is the period of RxCLK OUT. RCIP = RCOP.

Note 6: RSKM measured with ≤ 150ps cycle-to-cycle jitter on RxCLK IN.

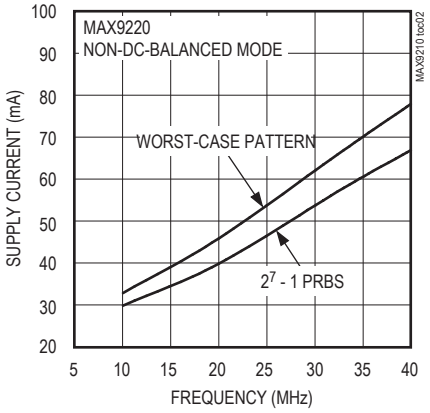
Typical Operating Characteristics

(V_{CC} = V_{CCO} = +3.3V, C_L = 8pF, $\overline{PWRDWN}$ = high, differential input voltage $|V_{ID}|$ = 0.2V, input common-mode voltage V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.)

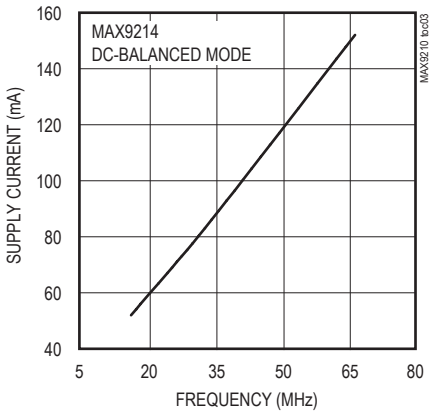
WORST-CASE PATTERN AND PRBS SUPPLY CURRENT vs. FREQUENCY



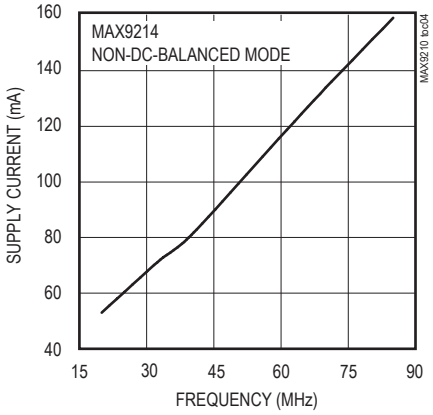
WORST-CASE PATTERN AND PRBS SUPPLY CURRENT vs. FREQUENCY



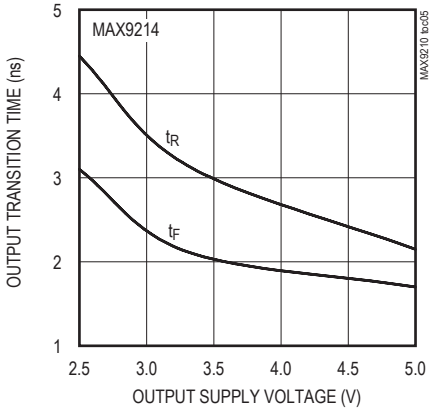
WORST-CASE PATTERN SUPPLY CURRENT vs. FREQUENCY



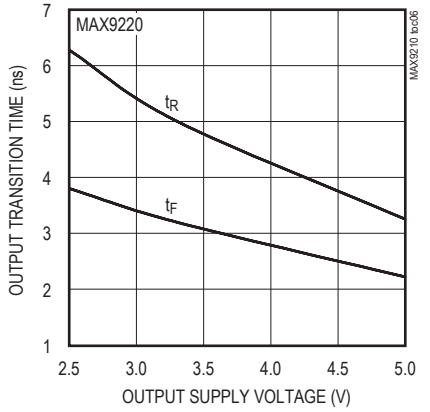
WORST-CASE PATTERN SUPPLY CURRENT vs. FREQUENCY



OUTPUT TRANSITION TIME vs. OUTPUT SUPPLY VOLTAGE (V_{CCO})



OUTPUT TRANSITION TIME vs. OUTPUT SUPPLY VOLTAGE (V_{CCO})



Pin Description

PIN	NAME	FUNCTION
1, 2, 4, 5, 45, 46, 47	RxOUT14–RxOUT20	Channel 2 Single-Ended Outputs
3, 25, 32, 38, 44	GND	Ground
6	DCB/NC	LVTTL/LVCMOS DC-Balance Programming Input: MAX9210: pulled up to V_{CC} MAX9214: pulled up to V_{CC} MAX9220: pulled up to V_{CC} MAX9222: pulled up to V_{CC} See Table 1.
7, 13, 18	LVDS GND	LVDS Ground
8	RxIN0-	Inverting Channel 0 LVDS Serial Data Input
9	RxIN0+	Noninverting Channel 0 LVDS Serial Data Input
10	RxIN1-	Inverting Channel 1 LVDS Serial Data Input
11	RxIN1+	Noninverting Channel 1 LVDS Serial Data Input
12	LVDS V_{CC}	LVDS Supply Voltage
14	RxIN2-	Inverting Channel 2 LVDS Serial Data Input
15	RxIN2+	Noninverting Channel 2 LVDS Serial Data Input
16	RxCLK IN-	Inverting LVDS Parallel Rate Clock Input
17	RxCLK IN+	Noninverting LVDS Parallel Rate Clock Input
19, 21	PLL GND	PLL Ground
20	PLL V_{CC}	PLL Supply Voltage
22	$\overline{PWRDWN}$	5V Tolerant LVTTL/LVCMOS Power-Down Input. Internally pulled down to GND. Outputs are high impedance when $\overline{PWRDWN}$ = low or open.
23	RxCLK OUT	Parallel Rate Clock Single-Ended Output. MAX9210/MAX9214, rising edge strobe. MAX9220/MAX9222, falling edge strobe.
24, 26, 27, 29, 30, 31, 33	RxOUT0–RxOUT6	Channel 0 Single-Ended Outputs
28, 36, 48	V_{CCO}	Output Supply Voltage
34, 35, 37, 39, 40, 41, 43	RxOUT7–RxOUT13	Channel 1 Single-Ended Outputs
42	V_{CC}	Digital Supply Voltage

Table 1. DC-Balance Programming

DEVICE	DCB/NC	OUTPUT STROBE EDGE	OPERATING MODE	OPERATING FREQUENCY (MHz)
MAX9210	High or open	Rising	DC balanced	8 to 34
	Low		Non-DC balanced	10 to 40
MAX9214	High or open	Rising	DC balanced	16 to 66
	Low		Non-DC balanced	20 to 85
MAX9220	High or open	Falling	DC balanced	8 to 34
	Low		Non-DC balanced	10 to 40
MAX9222	High or open	Falling	DC balanced	16 to 66
	Low		Non-DC balanced	20 to 85

Detailed Description

The MAX9210/MAX9220 operate at a parallel clock frequency of 8MHz to 34MHz in DC-balanced mode and 10MHz to 40MHz in non-DC-balanced mode. The MAX9214/MAX9222 operate at a parallel clock frequency of 16MHz to 66MHz in DC-balanced mode and 20MHz to 85MHz in non-DC-balanced mode. The transition times of the single-ended outputs are increased on the MAX9210/MAX9220 for reduced EMI.

DC-balanced or non-DC-balanced operation is controlled by the DCB/NC pin (see Table 1 for DCB/NC default settings and operating modes). In non-DC-balanced mode, each channel deserializes 7 bits every cycle of the parallel clock. In DC-balanced mode, 9 bits are deserialized every clock cycle (7 data bits + 2 DCbalance bits). The highest data rate in DC-balanced mode for the MAX9214 and MAX9222 is 66MHz x 9 = 594Mbps. In non-DC-balanced mode, the maximum data rate is 85MHz x 7 = 595Mbps.

DC Balance

Data coding by the MAX9209/MAX9213 serializers (which are companion devices to the MAX9210/MAX9214/MAX9220/MAX9222 deserializers) limits the imbalance of ones and zeros transmitted on each channel. If +1 is assigned to each binary 1 transmitted and -1 is assigned to each binary 0 transmitted, the variation in the running sum of assigned values is called the digital sum variation (DSV). The maximum DSV for the data channels is 10. At most, 10 more zeros than ones, or 10 more ones than zeros, are transmitted. The maximum DSV for the clock channel is five. Limiting the DSV and choosing the correct coupling capacitors maintains differential signal amplitude and reduces jitter due to droop on AC-coupled links.

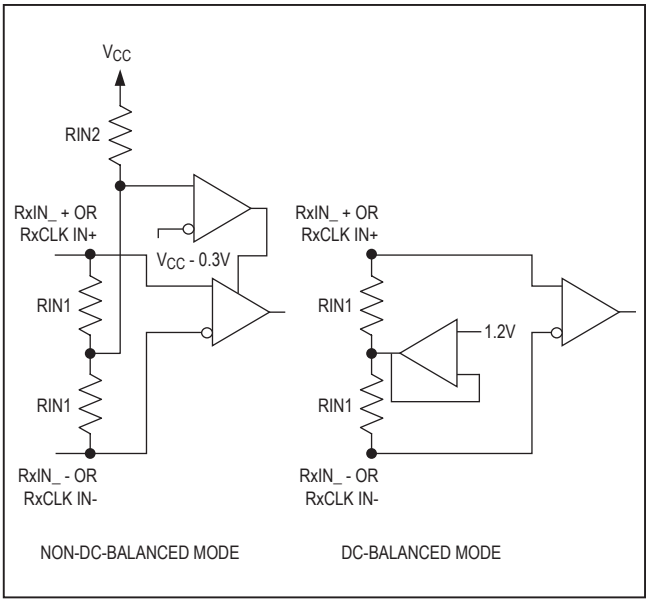


Figure 1. LVDS Input Circuits

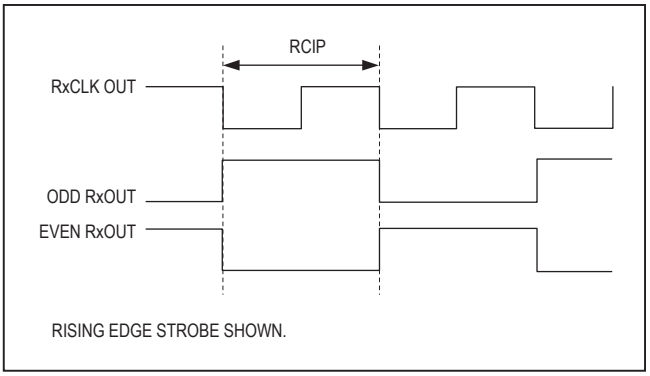


Figure 2. Worst-Case Test Pattern

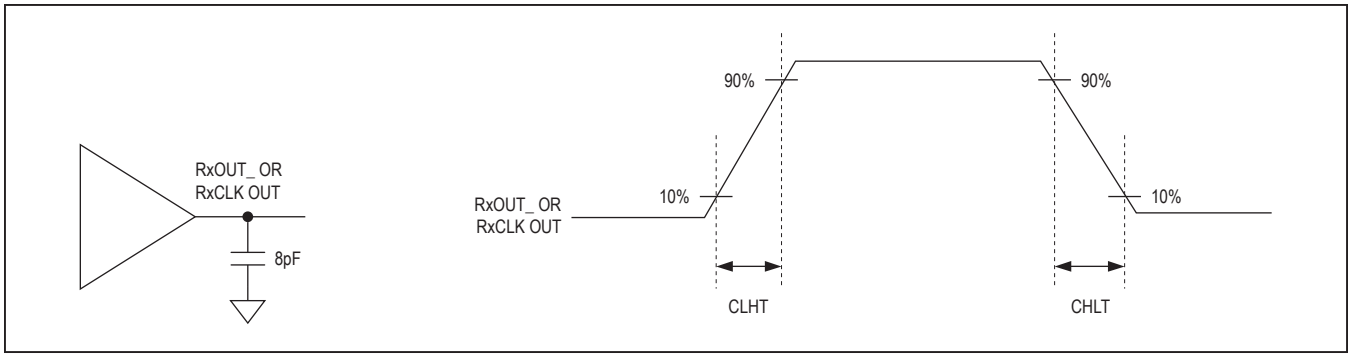


Figure 3. Output Load and Transition Times

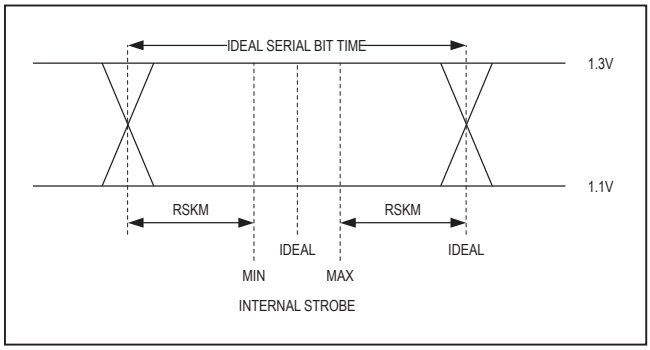


Figure 4. LVDS Receiver Input Skew Margin

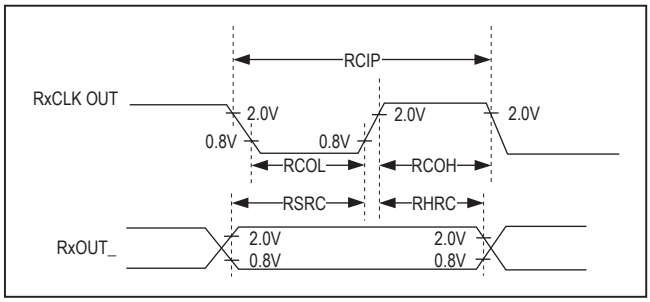


Figure 5a. Rising-Edge Output Setup/Hold and High/Low Times

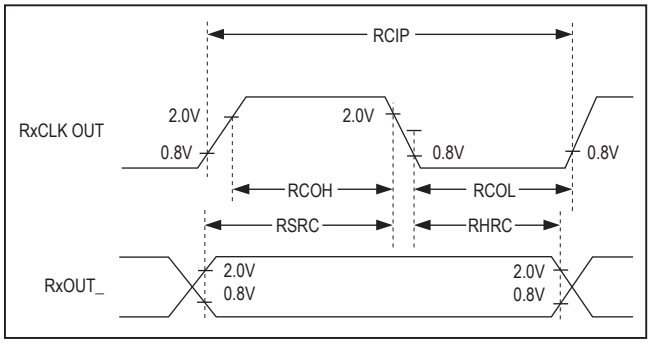


Figure 5b. Falling-Edge Output Setup/Hold and High/Low Times

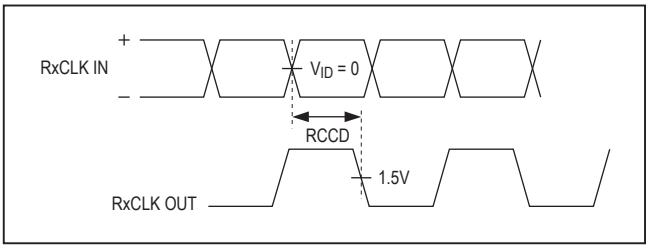


Figure 6a. Rising-Edge Clock-IN to Clock-OUT Delay

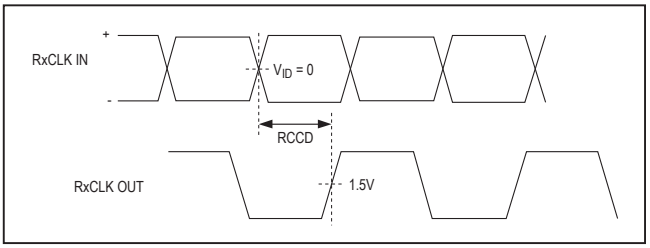


Figure 6b. Falling-Edge Clock-IN to Clock-OUT Delay

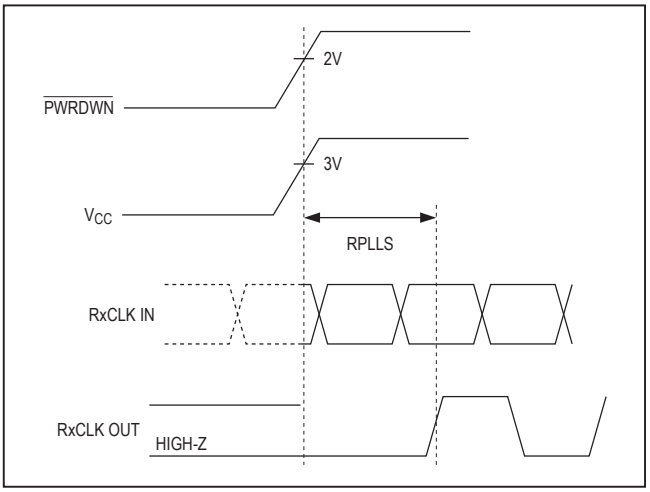


Figure 7. Phase-Locked Loop Set Time

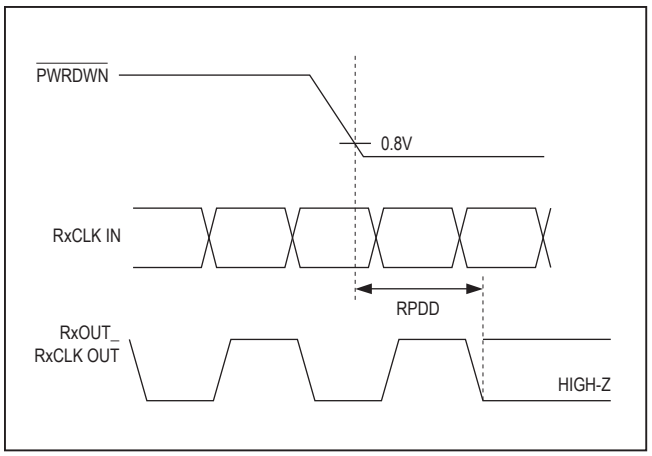


Figure 8. Power-Down Delay

To obtain DC balance on the data channels, the serializer parallel data is inverted or not inverted, depending on the sign of the digital sum at the word boundary. Two complementary bits are appended to each group of 7 parallel input data bits to indicate to the MAX9210/MAX9214/MAX9220/MAX9222 deserializers whether the data bits are inverted (see Figures 9 and 10). The deserializer restores the original state of the parallel data. The LVDS clock signal alternates duty cycles of 4/9 and 5/9, which maintain DC balance.

AC-Coupling Benefits

Bit errors experienced with DC-coupling can be eliminated by increasing the receiver common-mode voltage range by AC-coupling. AC-coupling increases the common-mode voltage range of an LVDS receiver to nearly

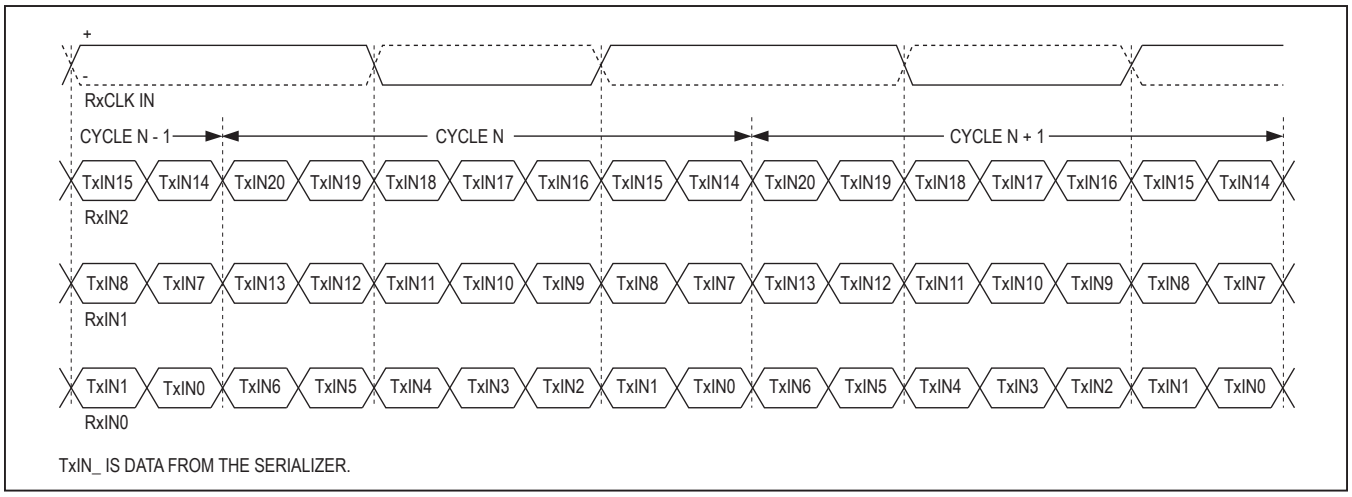


Figure 9. Deserializer Serial Input in Non-DC-Balanced Mode

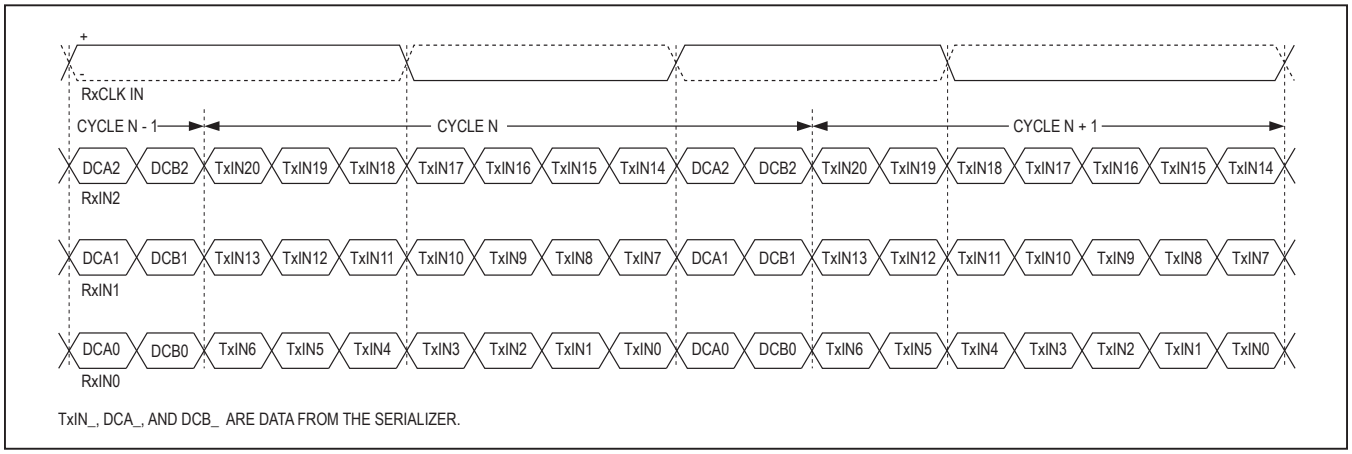


Figure 10. Deserializer Serial Input in DC-Balanced Mode

the voltage rating of the capacitor. The typical LVDS driver output is 350mV centered on an offset voltage of 1.25V, making single-ended output voltages of 1.425V and 1.075V. An LVDS receiver accepts signals from 0 to 2.4V, allowing approximately ±1V common-mode difference between the driver and receiver on a DC-coupled link (2.4V - 1.425V = 0.975V and 1.075V - 0V = 1.075V). Common-mode voltage differences may be due to ground potential variation or common-mode noise. If there is more than ±1V of difference, the receiver is not guaranteed to read the input signal correctly and may cause bit errors. AC-coupling filters low-frequency ground shifts and common-mode noise and passes high-frequency data. A common-mode voltage difference up to the voltage rating of the coupling capacitor (minus half the differential swing) is tolerated. DC-balanced coding of the data is required to maintain the differential signal amplitude and limit jitter on an AC-coupled link. A capacitor in series with each output of the LVDS driver is sufficient for AC-coupling. However, two capacitors—one at the serializer output and one at the deserializer input—provide protection in case either end of the cable is shorted to a high voltage.

Applications Information

Selection of AC-Coupling Capacitors

Voltage droop and the DSV of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is finite, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level.

The RC network for an AC-coupled link consists of the LVDS receiver termination resistor (R_T), the LVDS driver output resistor (R_O), and the series AC-coupling capacitors (C). The RC time constant for two equal-value series

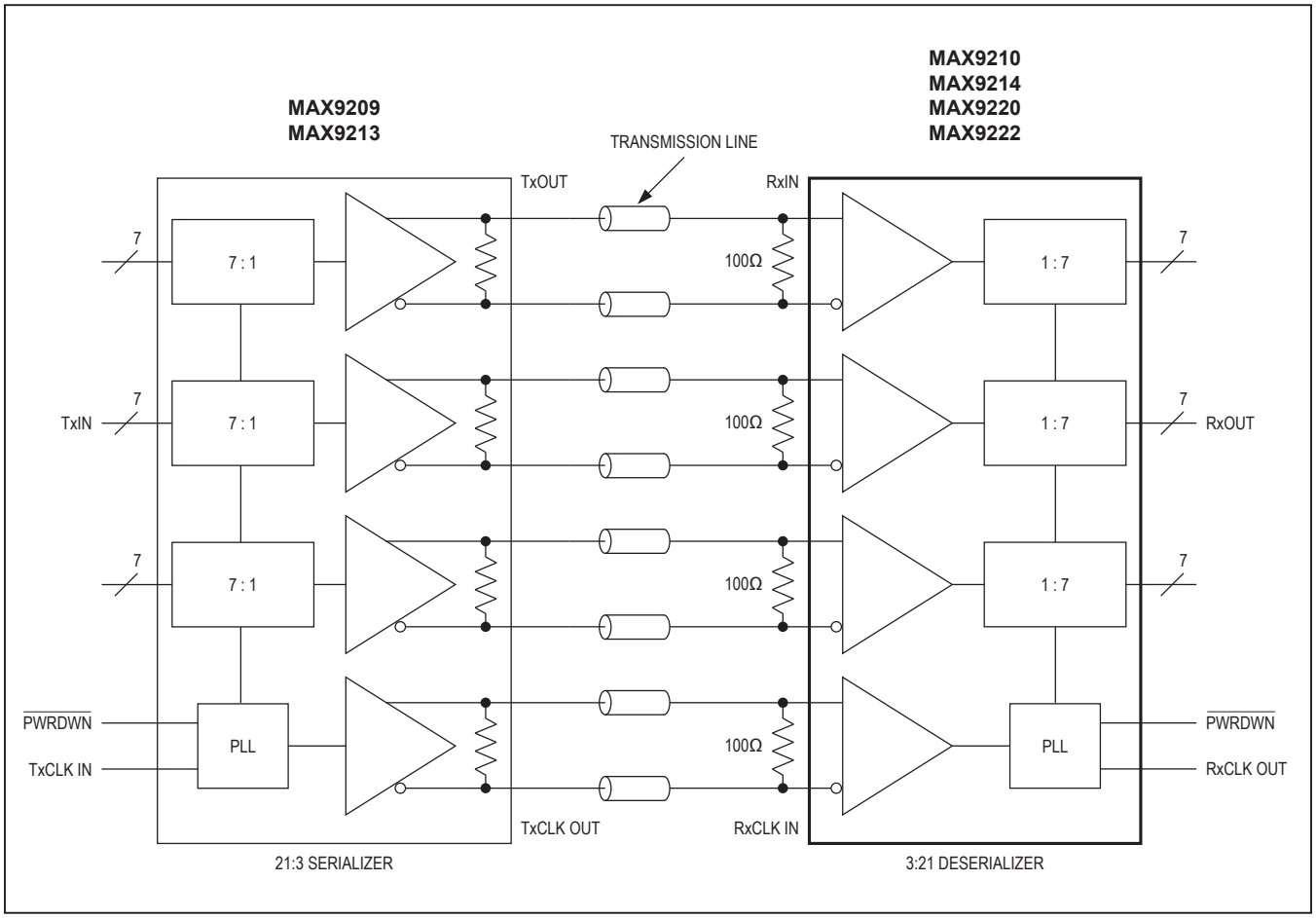


Figure 11. DC-Coupled Link, Non-DC-Balanced Mode

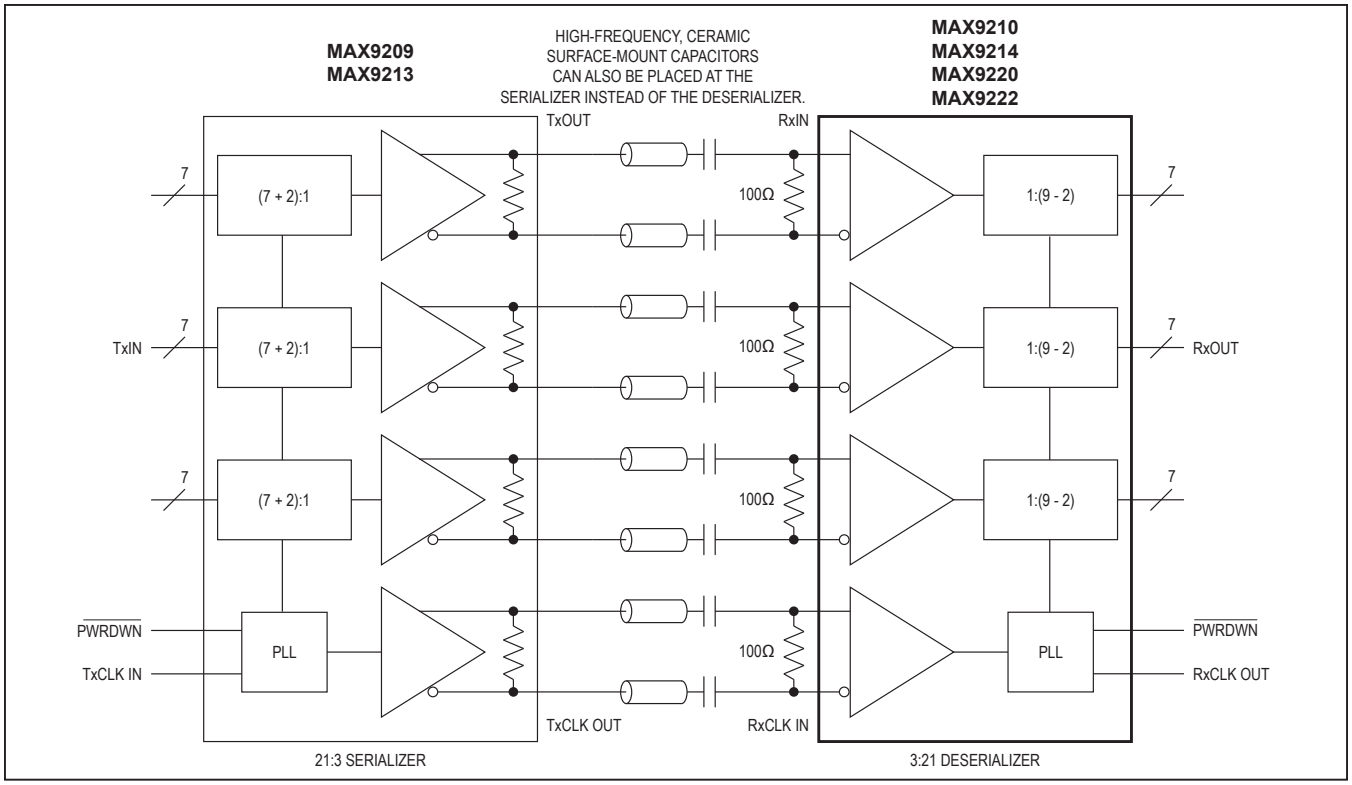


Figure 12. Two Capacitors per Link, AC-Coupled, DC-Balanced Mode

capacitors is (C x (R_T + R_O))/2 (Figure 12). The RC time constant for four equal-value series capacitors is (C x (R_T + R_O))/4 (Figure 13).

R_T is required to match the transmission line impedance (usually 100Ω) and R_O is determined by the LVDS driver design (the minimum differential output resistance of 78Ω for the MAX9209/MAX9213 serializers is used in the following example). This leaves the capacitor selection to change the system time constant.

In the following example, the capacitor value for a droop of 2% is calculated. Jitter due to this droop is then calculated assuming a 1ns transition time:

$$C = - (2 \times t_B \times DSV)/(\ln (1 - D) \times (R_T + R_O)) \quad \text{(Eq 1)}$$

where:

C = AC-coupling capacitor (F).

t_B = bit time (s).

DSV = digital sum variation (integer).

ln = natural log.

D = droop (% of signal amplitude).

R_T = termination resistor (Ω).

R_O = output resistance (Ω).

Equation 1 is for two series capacitors (Figure 12). The bit time (t_B) is the period of the parallel clock divided by 9. The DSV is 10. See equation 3 for four series capacitors (Figure 13).

The capacitor for 2% maximum droop at 8MHz parallel rate clock is:

$$C = - (2 \times t_B \times DSV)/(\ln (1 - D) \times (R_T + R_O))$$

$$C = - (2 \times 13.9ns \times 10)/(\ln (1 - 0.02) \times (100\Omega + 78\Omega))$$

$$C = 0.0773\mu F$$

Jitter due to droop is proportional to the droop and transition time:

$$t_J = t_T \times D \quad \text{(Eq 2)}$$

where:

t_J = jitter (s).

t_T = transition time (s) (0 to 100%).

D = droop (% of signal amplitude).

Jitter due to 2% droop and assumed 1ns transition time is:

$$t_J = 1ns \times 0.02$$

$$t_J = 20ps$$

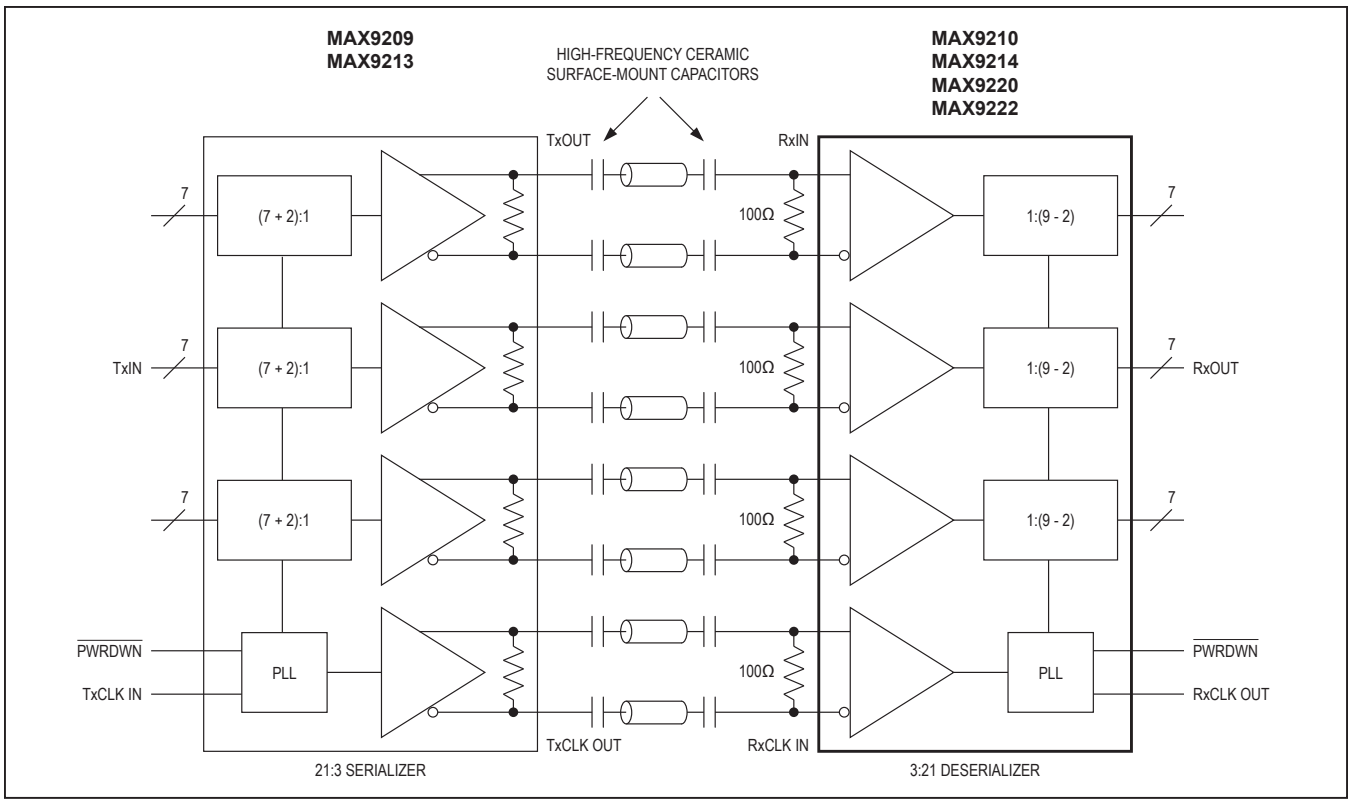


Figure 13. Four Capacitors per Link, AC-Coupled, DC-Balanced Mode

The transition time in a real system depends on the frequency response of the cable driven by the serializer. The capacitor value decreases for a higher frequency parallel clock and for higher levels of droop and jitter. Use high-frequency, surface-mount ceramic capacitors.

Equation 1 altered for four series capacitors (Figure 13) is:

$$C = - (4 \times t_B \times DSV)/(\ln (1 - D) \times (R_T + R_O)) \quad \text{(Eq 3)}$$

Fail-Safe

The MAX9210/MAX9214/MAX9220/MAX9222 have fail-safe LVDS inputs in non-DC-balanced mode (Figure 1). Fail-safe drives the outputs low when the corresponding LVDS input is open, undriven and shorted, or undriven and parallel terminated. The fail-safe on the LVDS clock input drives all outputs low. Fail-safe does not operate in DC-balanced mode.

Input Bias and Frequency Detection

In DC-balanced mode, the inverting and noninverting LVDS inputs are internally connected to +1.2V through 42kΩ (min) to provide biasing for AC-coupling (Figure 1). A frequency-detection circuit on the clock input detects when the input is not switching, or is switching at low frequency. In this case, all outputs are driven low. To prevent switching due to noise when the clock input is not driven, bias the clock input to differential +15mV by connecting a 10kΩ ±1% pullup resistor between the noninverting input and V_{CC}, and a 10kΩ ±1% pulldown resistor between the inverting input and ground. These bias resistors, along with the 100Ω ±1% tolerance termination resistor, provide +15mV of differential input. However, the +15mV bias causes degradation of RSKM proportional to the slew rate of the clock input. For example, if the clock transitions 250mV in 500ps, the slew rate of 0.5mV/ps reduces RSKM by 30ps.

Unused LVDS Data Inputs

In non-DC-balanced mode, leave unused LVDS data inputs open. In non-DC balanced mode, the input failsafe circuit drives the corresponding outputs low and no pullup or pulldown resistors are needed. In DC-balanced mode, at each unused LVDS data input, pull the inverting input up to V_{CC} using a 10kΩ resistor, and pull the noninverting input down to ground using a 10kΩ resistor. Do not connect a termination resistor. The pullup and pulldown resistors drive the corresponding outputs low and prevent switching due to noise.

PWRDWN

Driving PWRDWN low puts the outputs in high impedance, stops the PLL, and reduces supply current to 50µA or less. Driving PWRDWN high drives the outputs low until the PLL locks. The outputs of two deserializers ca be bused to form a 2:1 mux with the outputs controlled by PWRDWN. Wait 100ns between disabling one deserializer (driving PWRDWN low) and enabling the second one (driving PWRDWN high) to avoid contention of the bused outputs.

Input Clock and PLL Lock Time

There is no required timing sequence for the application or reapplication of the parallel rate clock (RxCLK IN) relative to PWRDWN, or to a power-supply ramp for proper PLL lock. The PLL lock time is set by an internal counter. The maximum time to lock is 32,800 clock periods. Power and clock should be stable to meet the lock time specification. When the PLL is locking, the outputs are low.

Power-Supply Bypassing

There are separate on-chip power domains for digital circuits, outputs, PLL, and LVDS inputs. Bypass each V_{CC}, V_{CCO}, PLL V_{CC}, and LVDS V_{CC} pin with high-frequency, surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.

Cables and Connectors

Interconnect for LVDS typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

Board Layout

Keep the LVTTL/LVCMOS outputs and LVDS input signals separated to prevent crosstalk. A four-layer printedcircuit board (PCB) with separate layers for power, ground, LVDS inputs, and digital signals is recommended.

ESD Protection

The MAX9210/MAX9214/MAX9220/MAX9222 ESD tolerance is rated for IEC 61000-4-2, Human Body Model and ISO 10605 standards. IEC 61000-4-2 and ISO 10605 specify ESD tolerance for electronic systems. The IEC 61000-4-2 discharge components are CS = 150pF and R_D = 330Ω (Figure 14). For IEC 61000-4-2, the LVDS inputs are rated for ±8kV Contact Discharge and ±15kV Air Discharge. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 15). For the Human Body Model, all pins are rated for ±5kV Contact Discharge. The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 16). For ISO 10605, the LVDS inputs are rated for ±8kV Contact Discharge and ±25kV Air Discharge.

5V Tolerant Input

PWRDWN is 5V tolerant and is internally pulled down to GND. DCB/NC is not 5V tolerant. The input voltage range for DCB/NC is nominally ground to V_{CC}. Normally, DCB/NC is connected to V_{CC} or ground.

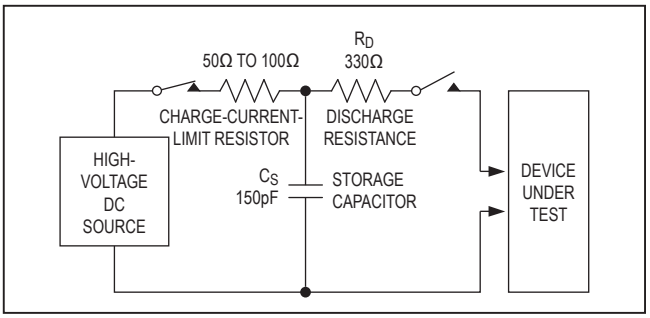


Figure 14. IEC 61000-4-2 Contact Discharge ESD Test Circuit

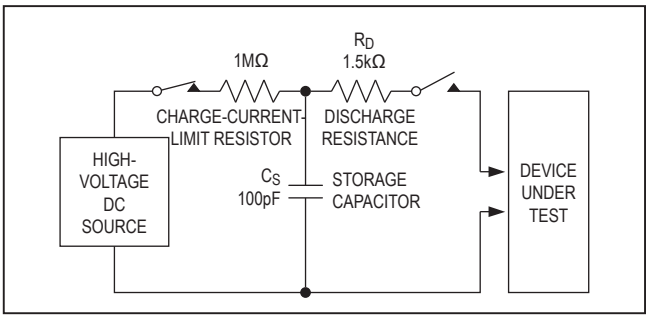


Figure 15. Human Body ESD Test Circuit

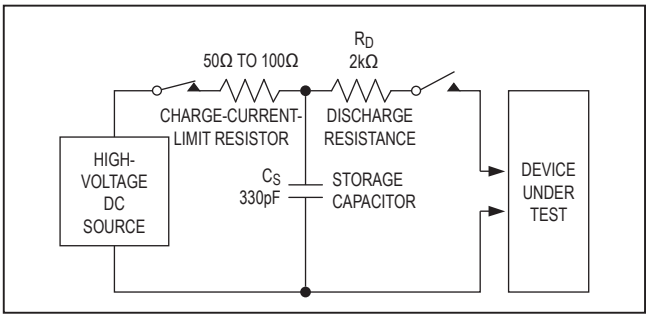


Figure 16. ISO 10605 Contact Discharge ESD Test Circuit

Skew Margin (RSKM)

Skew margin (RSKM) is the time allowed for degradation of the serial data sampling setup and hold times by sources other than the deserializer. The deserializer sampling uncertainty is accounted for and does not need to be subtracted from RSKM. The main outside contributors of jitter and skew that subtract from RSKM are interconnect intersymbol interference, serializer pulse position uncertainty, and pair-to-pair path skew.

V_{CCO} Output Supply and Power Dissipation

The outputs have a separate supply (V_{CCO}) for interfacing to systems with 1.8V to 5V nominal input logic levels. The *DC Electrical Characteristics* table gives the maximum supply current for V_{CCO} = 3.6V with 8pF load at several switching frequencies with all outputs switching in the worst-case switching pattern. The approximate incremental supply current for V_{CCO} other than 3.6V **with the same 8pF** load and worst-case pattern can be calculated using:

$$I_I = C_T V_I\ 0.5 f_C \times 21 \text{ (data outputs)} + C T V_I f_C \times 1 \text{ (clock output)}$$

where:

I_I = incremental supply current.

C_T = total internal (C_{INT}) and external (C_L) load capacitance.

V_I = incremental supply voltage.

f_C = output clock switching frequency.

The incremental current is added to (for V_{CCO} > 3.6V) or subtracted from (for V_{CCO} < 3.6V) the *DC Electrical Characteristics* table maximum supply current. The internal output buffer capacitance is C_{INT} = 6pF. The worst-case pattern switching frequency of the data outputs is half the switching frequency of the output clock.

In the following example, the incremental supply current is calculated for V_{CCO} = 5.5V, f_C = 34MHz, and C_L = 8pF:

$$V_I = 5.5V - 3.6V = 1.9V$$

$$C_T = C_{INT} + C_L = 6pF + 8pF = 14pF$$

where:

$I_I = C_T V_I\ 0.5 F_C \times 21$ (data outputs) + $C_T V_I f_C \times 1$ (clock output).

I_I = (14pF x 1.9V x 0.5 x 34MHz x 21) + (14pF x 1.9V x 34MHz).

I_I = 9.5mA + 0.9mA = 10.4mA.

The maximum supply current in DC-balanced mode for V_{CC} = V_{CCO} = 3.6V at f_C = 34MHz is 106mA (from the *DC Electrical Characteristics* table). Add 10.4mA to get the total approximate maximum supply current at V_{CCO} = 5.5V and V_{CC} = 3.6V.

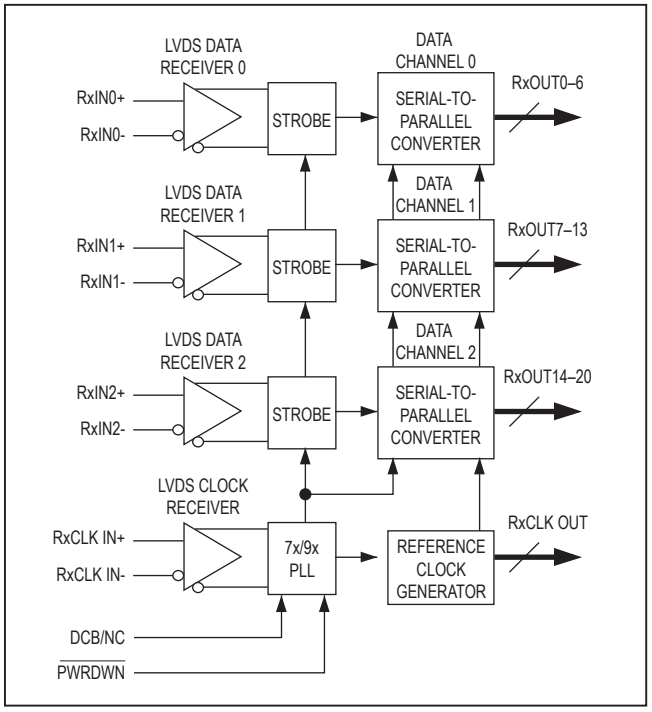
If the output supply voltage is less than V_{CCO} = 3.6V, the reduced supply current can be calculated using the same formula and method.

At high switching frequency, high supply voltage, and high capacitive loading, power dissipation can exceed the package power dissipation rating. Do not exceed the maximum package power dissipation rating. See the *Absolute Maximum Ratings* for maximum package power dissipation capacity and temperature derating.

Rising- or Falling-Edge Output Strobe

The MAX9210/MAX9214 have a rising-edge output strobe, which latches the parallel output data into the next chip on the rising edge of RxCLK OUT. The MAX9220/MAX9222 have a falling-edge output strobe, which latches the parallel output data into the next chip on the falling edge of RxCLK OUT. The deserializer output strobe polarity does not need to match the serializer input strobe polarity. A deserializer with rising or falling edge output strobe can be driven by a serializer with a rising edge input strobe.

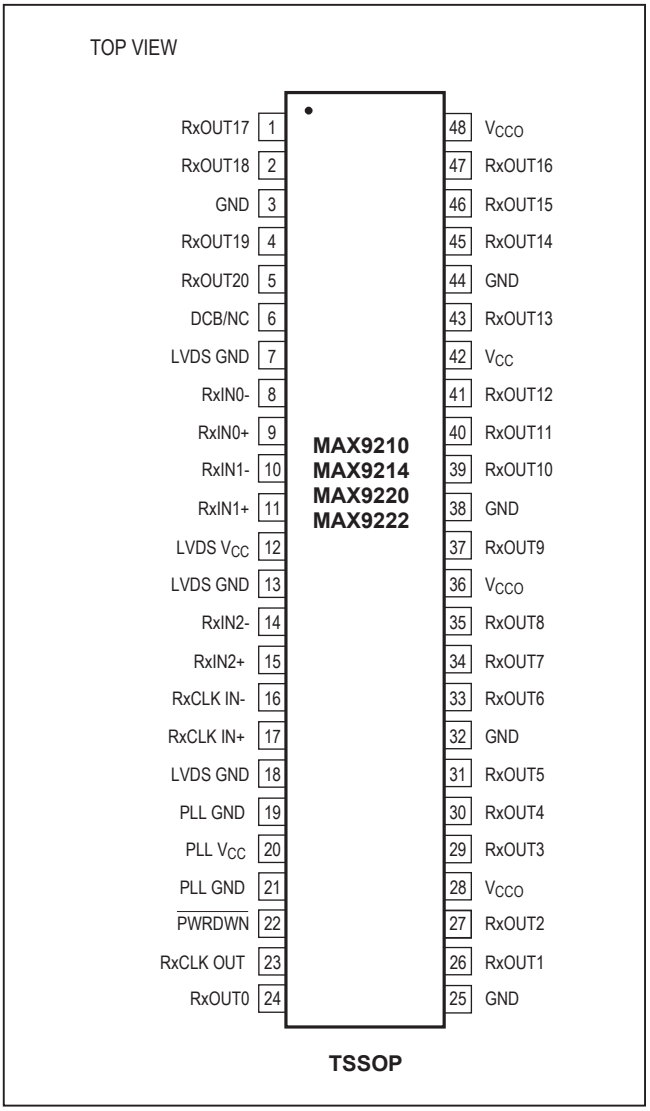
Functional Diagram



Chip Information

PROCESS: CMOS

Pin Configuration



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TSSOP	U48-1	**21-0155**	**90-0124**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	3/05	Various changes	—
5	11/07	Removed all references to MAX9212/MAX9216 and thin QFN-EP package; various style edits; and updated package outline for TSSOP	1–17
6	5/14	Removed automotive references from the *Applications* section	1

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