TOSHIBA Photocoupler GaAℓAs Ired & Photo IC

TLP2530, TLP2531

Digital Logic Isolation

Line Receiver

Power Supply Control

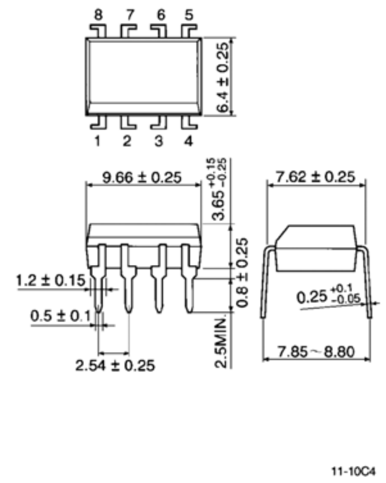
Switching Power Supply

Transistor Inverter

The TOSHIBA TLP2530 and TLP2531 dual photocouplers consist of a pair of GaAℓAs light emitting diode and integrated photodetector.
This unit is 8−lead DIP.
Separate connection for the photodiode bias and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base−collector capacitance.

- TTL compatible
- Switching speed: t_{pHL}=0.3μs, t_{pLH}=0.3μs(typ.) (@R_L=1.9kΩ)
- Guaranteed performance over temp: 0~70°C
- Isolation voltage: 2500 Vrms(min.)
- UL recognized: UL1577, file no. E67349

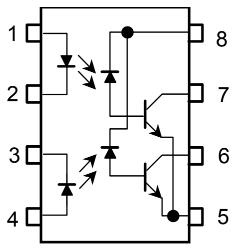
Unit in mm



TOSHIBA 11−10C4

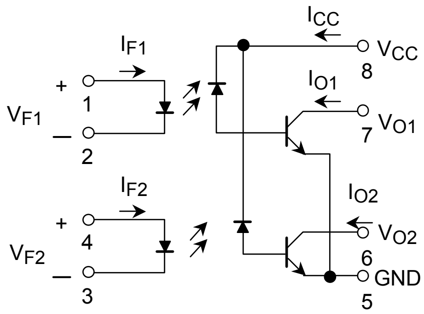
Weight: 0.54 g (typ.)

Pin Configuration (top view)



1. : Anode.1
2. : Cathode.1
3. : Cathode.2
4. : Anode.2
5. : Gnd
6. : V_{O2}(output 2)
7. : V_{O1}(output 1)
8. : V_{CC}

Schematic



Absolute Maximum Ratings

Characteristic		Symbol	Rating	Unit
LED	Forward current(each channel) (Note 1)	I_F	25	mA
	Pulse forward current (Each Channel) (Note 2)	I_{FP}	50	mA
	Total pulse forward current (each channel) (Note 3)	I_{FPT}	1	A
	Reverse voltage(each channel)	V_R	5	V
	Diode power dissipation (each channel) (Note 4)	P_D	45	mW
Detector	Output current(each channel)	I_O	8	mA
	Peak output current (each channel)	I_{OP}	16	mA
	Supply voltage	V_{CC}	−0.5~15	V
	Output voltage(each channel)	V_O	−0.5~15	V
	Output power dissipation (each channel) (Note 5)	P_O	35	mW
Operating temperature range		T_{opr}	−55~100	°C
Storage temperature range		T_{stg}	−55~125	°C
Lead solder temperature(10s)**		T_{sol}	260	°C
Isolation voltage (AC, 1min., R.H.≤ 60%) (Note 7)		BV_S	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note 1) Derate 0.8mA above 70°C.
(Note 2) 50% duty cycle, 1ms pulse width. Derate 1.6mA / °C above 70°C.
(Note 3) Pulse width 1μs, 300pps.
(Note 4) Derate 0.9mW / °C above 70°C.
(Note 5) Derate 1mW / °C above 70°C.

**2mm below seating plane.

Recommended Operating Conditions

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	0	—	12	V
Forward current, each channel	I_F	—	16	25	mA
Operating temperature	T_{opr}	−25	—	85	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Electrical Characteristics
Over Recommended Temperature (Ta = 0°C~70°C, unless otherwise noted)

Characteristic		Symbol	Test Condition	Min.	Typ.**	Max.	Unit
Current transfer ratio (each channel)	TLP2530	CTR	I_F = 16mA, V_O = 0.4V V_{CC} = 4.5V, Ta = 25°C (Note 6)	7	30	—	%
	TLP2531			19	30	—	
	TLP2530	CTR	I_F = 16mA, V_O = 0.5V V_{CC} = 4.5V (Note 6)	5	—	—	%
	TLP2531			15	—	—	
Logic low output voltage (each channel)	TLP2530	V_{OL}	I_F = 16mA, I_O = 1.1mA V_{CC} = 4.5V	—	0.1	0.4	V
	TLP2531		I_F = 16mA, I_O = 2.4mA V_{CC} = 4.5V	—	0.1	0.4	V
Logic high output current (each channel)		I_{OH}	I_F = 0mA, V_O = V_{CC} = 5.5V Ta = 25℃	—	3	500	nA
			I_F = 0mA, V_O = V_{CC} = 15V	—	—	50	μA
Logic low supply current		I_{CCL}	I_{F1} = I_{F2} = 16mA V_{O1} = V_{O2} = Open V_{CC} = 15V	—	160	—	μA
Logic high supply current		I_{CCH}	I_{F1} = I_{F2} = 0mA V_{O1} = V_{O2} = Open V_{CC} = 15V	—	0.05	4	μA
Input forward voltage (each channel)		V_F	I_F = 16mA, Ta = 25°C	—	1.65	1.7	V
Temperature coefficent of forward voltage(each channel)		$\Delta V_F / \Delta Ta$	I_F = 16mA	—	–2	—	mV/°C
Input reverse breakdown voltage(each channel)		BV_R	IR = 10μA, Ta = 25°C	5	—	—	V
Input capacitance (each channel)		C_{IN}	f = 1MHz, V_F = 0	—	60	—	pF
Input-output insulation leakage current		I_{I-O}	Relative humidity = 45% t = 5s, V_{I-O} = 3000V_{dc} Ta = 25°C (Note 7)	—	—	1.0	μA
Resistance (input–output)		R_{I-O}	V_{I-O} = 500V_{dc} (Note 7)	—	10^{12}	—	Ω
Capacitance (input–output)		C_{I-O}	f = 1MHz (Note 7)	—	0.6	—	pF
Input-input leakage current		I_{I-I}	Relative humidity = 45% t = 5s, V_{I-I} = 500V (Note 8)	—	0.005	—	μA
Resistance (input–input)		R_{I-I}	V_{I-I} = 500V_{dc} (Note 8)	—	10^{11}	—	Ω
Capacitance (input–iutput)		C_{I-I}	f = 1MHz (Note 8)	—	0.25	—	pF

**All typicals at Ta = 25°C.

Switching Characteristics (unless otherwise specified, Ta = 25°C, V_{CC} = 5V, I_F = 16mA)

Characteristic		Symbol	Test Cir–cuit	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time to logic low at output (each channel)	TLP2530	t_{pHL}	1	R_L = 4.1kΩ	—	0.3	1.5	μs
	TLP2531			R_L = 1.9kΩ	—	0.2	0.8	
Propagation delay time to logic high at output (each channel)	TLP2530	t_{pLH}	1	R_L = 4.1kΩ	—	0.5	1.5	μs
	TLP2531			R_L = 1.9kΩ	—	0.3	0.8	
Common mode transient immunity at logic high level output (each channel, Note 9)	TLP2530	CM_H	2	I_F = 0mA, V_{CM} = 400V_{p-p} R_L = 4.1kΩ	—	1500	—	V / μs
	TLP2531			I_F = 0mA, V_{CM} = 400V_{p-p} R_L = 1.9kΩ	—	1500	—	
Common mode transient immunity at logic low level output (each channel, Note 9)	TLP2530	CM_L	2	V_{CM} = 400V_{p-p} R_L = 4.1kΩ, I_F = 16mA	—	−1500	—	V / μs
	TLP2531			V_{CM} = 400_{p-p} R_L = 1.9kΩ, I_F = 16mA	—	−1500	—	
Bandwidth (each channel, Note 10)		BW	3	R_L = 100Ω	—	2	—	MH_Z

(Note 6) DC current transfer ratio is defined as the ratio of output collector current, $I_{O,}$ to the forward LED input current, $I_{F,}$ times 100%.

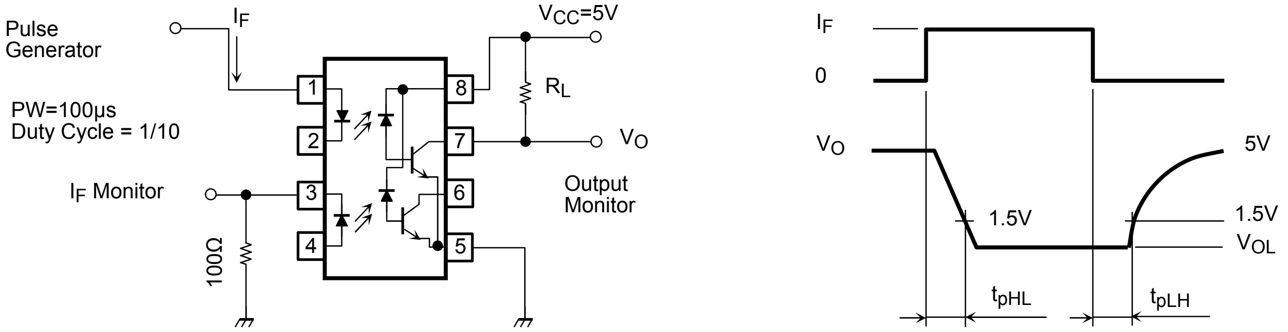
(Note 7) Device considered a two−terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7, and 8 shorted together.

(Note 8) Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

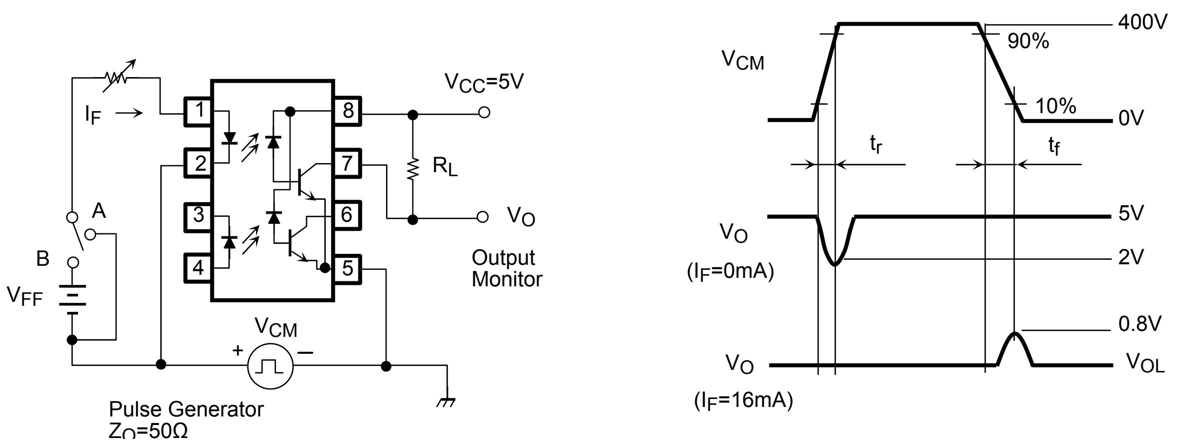
(Note 9) Common mode transient immunity in logic high level is the maximum tolerable (positive) dVcm / dt on the leading egde of the common mode pulse, Vcm, to assure that the output will remain in a logic high state(i.e., V_O > 2.0V).
Common mode transient immunity in logic low Level is the maximum tolerable (negative) dVcm / dt on the trailing edge of the common mode pulse signal, Vcm, to assure that the output will remain in logic low state(i.e., V_O > 0.8V).

(Note 10) The frequency at which the ac output voltage is 3dB below the low frequency asymptote.

Test Circuit 1: Switching Time, t_pHL, t_pLH

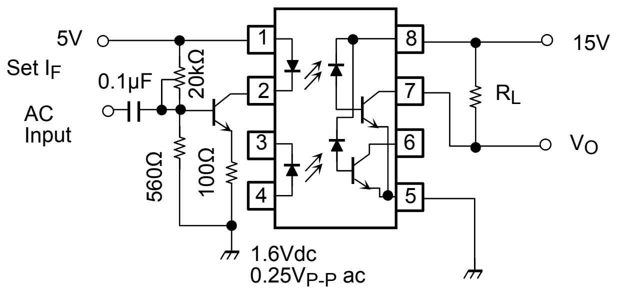


Test Circuit 2: Transient Immunity And Typical Waveform

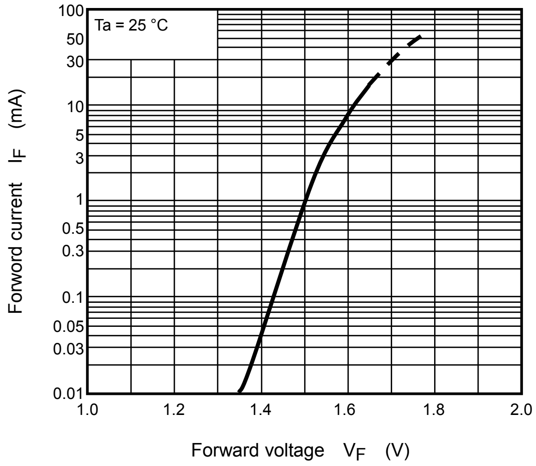


$$CM_H = \frac{320(V)}{t_r(\mu s)},\ CM_L = \frac{320(V)}{t_f(\mu s)}$$

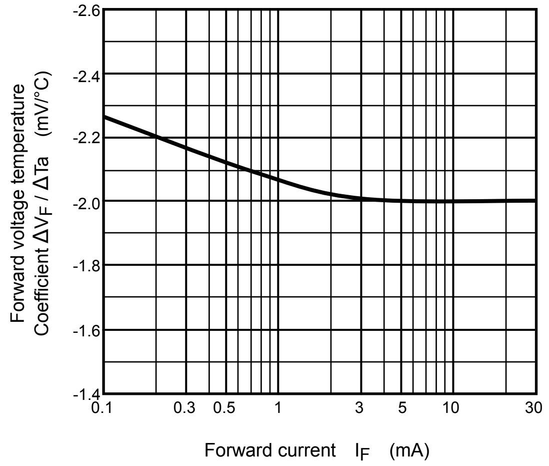
Test Circuit 3: Frequency Response



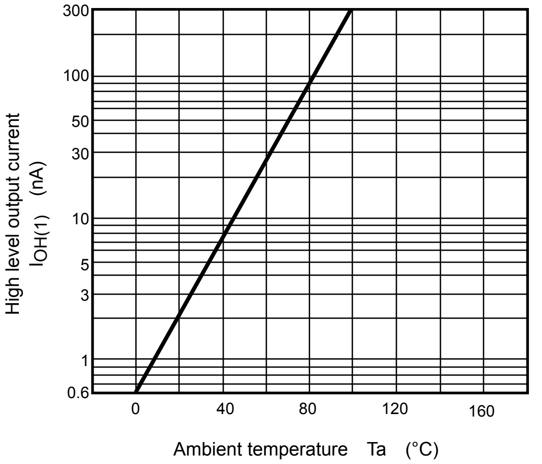
$I_F – V_F$



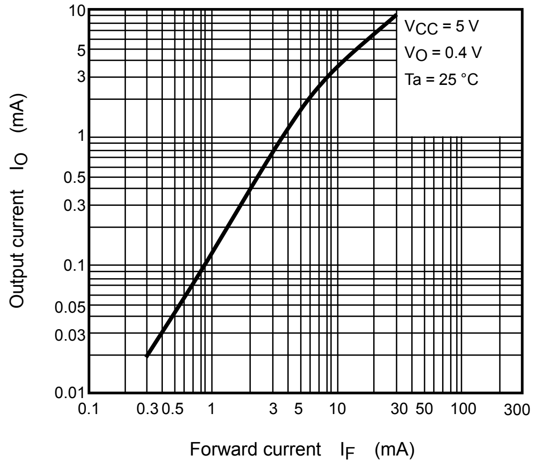
ΔVF /ΔTa - I_F



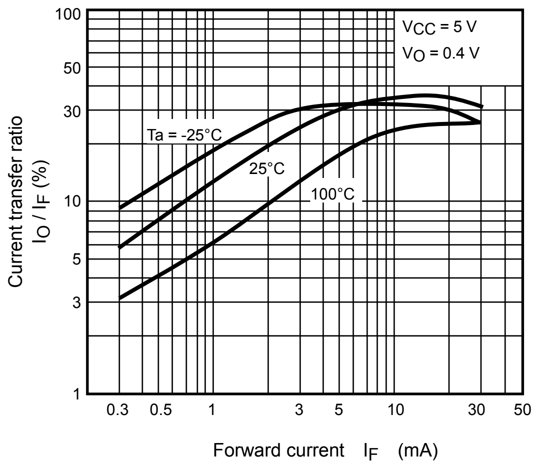
$I_{OH(1)}$ – Ta



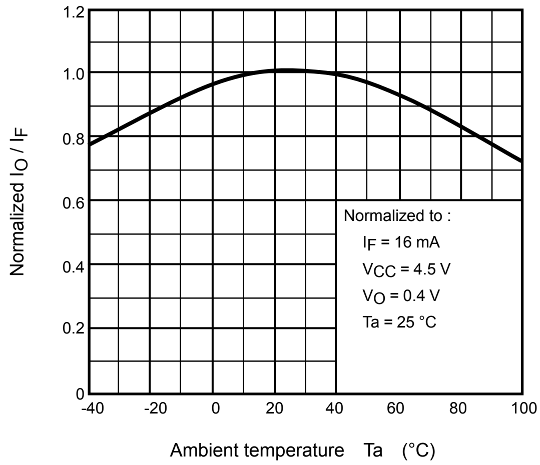
$I_O – I_F$

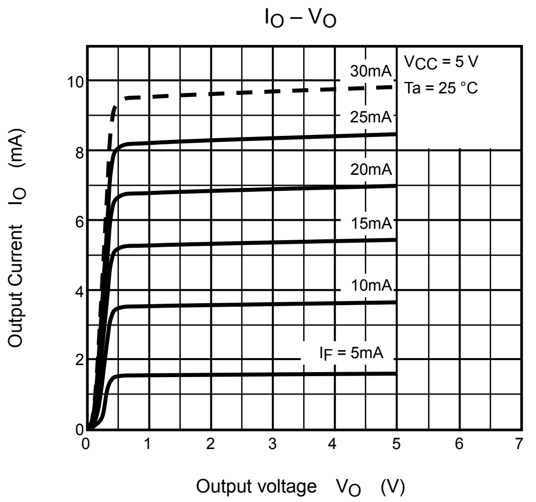


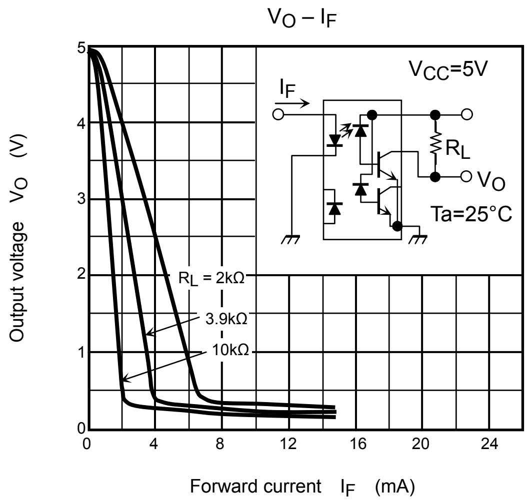
$I_O / I_F – I_F$

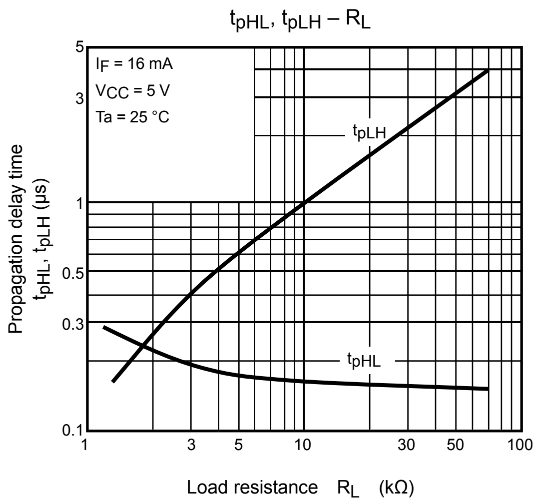


I_O / I_F – Ta




IO – VO
VCC = 5 V
Ta = 25 °C
30mA
25mA
20mA
15mA
10mA
IF = 5mA
Output Current IO (mA)
Output voltage VO (V)
0
2
4
6
8
10
0
1
2
3
4
5
6
7


VO – IF
VCC=5V
IF
RL
VO
Ta=25°C
RL = 2kΩ
3.9kΩ
10kΩ
Output voltage VO (V)
Forward current IF (mA)
0
1
2
3
4
5
0
4
8
12
16
20
24


tpHL, tpLH – RL
IF = 16 mA
VCC = 5 V
Ta = 25 °C
tpLH
tpHL
Propagation delay time tpHL, tpLH (μs)
Load resistance RL (kΩ)
0.1
0.3
0.5
1
3
5
1
3
5
10
30
50
100

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