

HIGH-EFFICIENCY, SOT23 STEP-DOWN, DC-DC CONVERTER

FEATURES

- High Efficiency Synchronous Step-Down Converter With up to 95% Efficiency
- 2.5-V to 6-V Input Voltage Range
- Adjustable Output Voltage Range From 0.7 V to V_I
- Fixed Output Voltage Options Available
- Up to 300 mA Output Current
- 1-MHz Fixed Frequency PWM Operation
- Highest Efficiency Over Wide Load Current Range Due to Power Save Mode
- 15- μ A Typical Quiescent Current
- Soft Start
- 100% Duty Cycle Low-Dropout Operation
- Dynamic Output-Voltage Positioning
- Available in a 5-Pin SOT23 Package

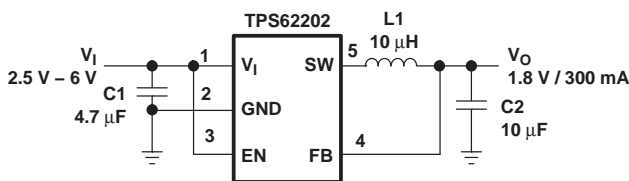
APPLICATIONS

- PDAs and Pocket PC
- Cellular Phones, Smart Phones
- Low Power DSP Supply
- Digital Cameras
- Portable Media Players
- Portable Equipment

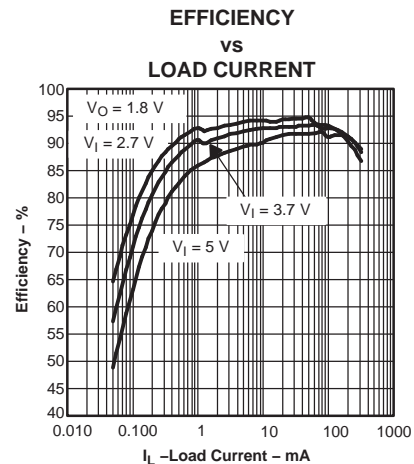
DESCRIPTION

The TPS6220x devices are a family of high-efficiency synchronous step-down converters ideally suited for portable systems powered by 1-cell Li-Ion or 3-cell NiMH/NiCd batteries. The devices are also suitable to operate from a standard 3.3-V or 5-V voltage rail.

With an output voltage range of 6 V down to 0.7 V and up to 300 mA output current, the devices are ideal to power low voltage DSPs and processors used in PDAs, pocket PCs, and smart phones. Under nominal load current, the devices operate with a fixed switching frequency of typically 1 MHz. At light load currents, the part enters the power save mode operation; the switching frequency is reduced and the quiescent current is typically only 15 μ A; therefore, it achieves the highest efficiency over the entire load current range. The TPS6220x needs only three small external components. Together with the SOT23 package, a minimum system solution size is achieved. An advanced fast response voltage mode control scheme achieves superior line and load regulation with small ceramic input and output capacitors.



**Figure 1. Typical Application
(Fixed Output Voltage Version)**



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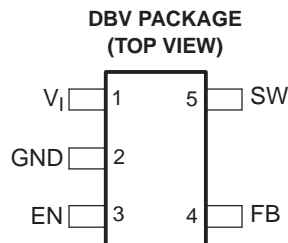
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION ⁽¹⁾

| T _A | OUTPUT VOLTAGE | SOT23 PACKAGE | SYMBOL |
|----------------|----------------|---------------|--------|
| -40°C to 85°C | Adjustable | TPS62200DBV | PHKI |
| | 1.2 V | TPS62207DBV | PJGI |
| | 1.5 V | TPS62201DBV | PHLI |
| | 1.6 V | TPS62204DBV | PHSI |
| | 1.8 V | TPS62202DBV | PHMI |
| | 1.875 V | TPS62208DBV | ALW |
| | 2.5 V | TPS62205DBV | PHTI |
| | 3.3 V | TPS62203DBV | PHNI |

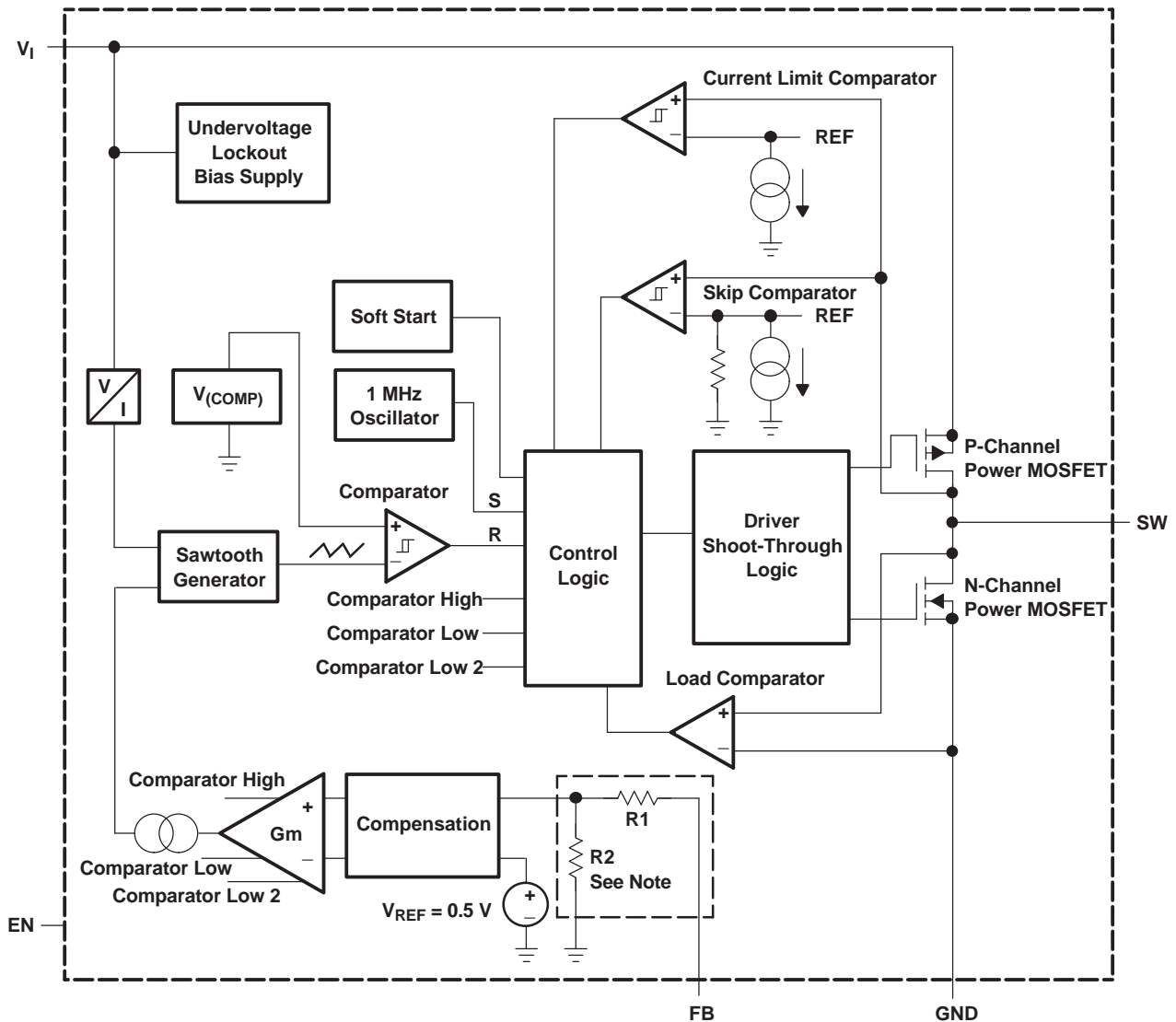
- (1) The DBV package is available in tape and reel. Add R suffix (DBVR) to order quantities of 3000 parts. Add T suffix (DBVT) to order quantities of 250 parts



Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|----------------|-----|-----|---|
| EN | 3 | I | This is the enable pin of the device. Pulling this pin to ground forces the device into shutdown mode. Pulling this pin to V _I enables the device. This pin must not be left floating and must be terminated. |
| FB | 4 | I | This is the feedback pin of the device. Connect this pin directly to the output if the fixed output voltage version is used. For the adjustable version an external resistor divider is connected to this pin. The internal voltage divider is disabled for the adjustable version. |
| GND | 2 | | Ground |
| SW | 5 | I/O | Connect the inductor to this pin. This pin is the switch pin and is connected to the internal MOSFET switches. |
| V _I | 1 | I | Supply voltage pin |

FUNCTIONAL BLOCK DIAGRAM



For the adjustable version (TPS62200) the internal feedback divider is disabled and the FB pin is directly connected to the internal GM amplifier

DETAILED DESCRIPTION

OPERATION

The TPS6220x is a synchronous step-down converter operating with typically 1-MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents and in power save mode operating with pulse frequency modulation (PFM) at light load currents.

During PWM operation the converter uses a unique fast response, voltage mode, controller scheme with input voltage feed forward. This achieves good line and load regulation and allows the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal (S), the P-channel MOSFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel switch is exceeded. Then the N-channel rectifier switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again turning off the N-channel rectifier and turning on the P-channel switch.

DETAILED DESCRIPTION (continued)

The GM amplifier and input voltage determines the rise time of the Sawtooth generator; therefore any change in input voltage or output voltage directly controls the duty cycle of the converter. This gives a very good line and load transient regulation.

POWER SAVE MODE OPERATION

As the load current decreases, the converter enters the power save mode operation. During power save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency.

Two conditions allow the converter to enter the power save mode operation. One is when the converter detects the discontinuous conduction mode. The other is when the peak switch current in the P-channel switch goes below the skip current limit. The typical skip current limit can be calculated as

$$I_{\text{skip}} \leq 66 \text{ mA} + \frac{V_{\text{in}}}{160 \Omega}$$

During the power save mode the output voltage is monitored with the comparator by the thresholds comp low and comp high. As the output voltage falls below the comp low threshold set to typically 0.8% above V_{out} nominal, the P-channel switch turns on. The P-channel switch is turned off as the peak switch current is reached. The typical peak switch current can be calculated:

$$I_{\text{peak}} = 66 \text{ mA} + \frac{V_{\text{in}}}{80 \Omega}$$

The N-channel rectifier is turned on and the inductor current ramps down. As the inductor current approaches zero the N-channel rectifier is turned off and the P-channel switch is turned on again, starting the next pulse. The converter continues these pulses until the comp high threshold (set to typically 1.6% above V_{out} nominal) is reached. The converter enters a sleep mode, reducing the quiescent current to a minimum. The converter wakes up again as the output voltage falls below the comp low threshold again. This control method reduces the quiescent current typically to 15 μA and reduces the switching frequency to a minimum, thereby achieving the high converter efficiency. Setting the skip current thresholds to typically 0.8% and 1.6% above the nominal output voltage at light load current results in a dynamic output voltage achieving lower absolute voltage drops during heavy load transient changes. This allows the converter to operate with a small output capacitor of just 10 μF and still have a low absolute voltage drop during heavy load transient changes. Refer to [Figure 2](#) for detailed operation of the power save mode.

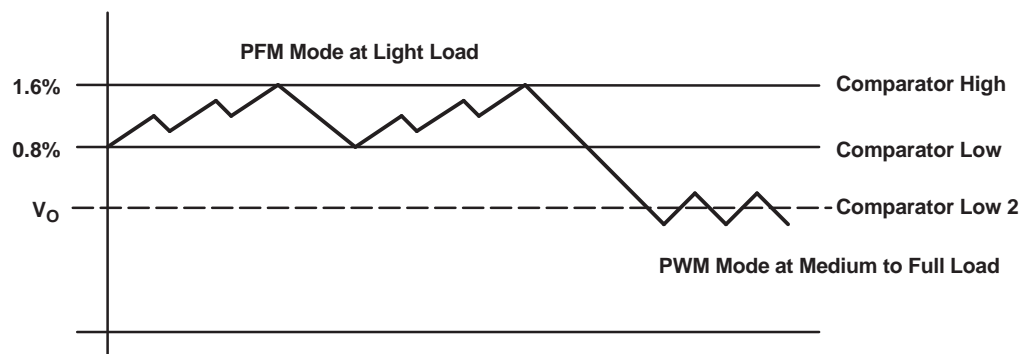


Figure 2. Power Save Mode Thresholds and Dynamic Voltage Positioning

The converter enters the fixed frequency PWM mode again as soon as the output voltage falls below the comp low 2 threshold.

DETAILED DESCRIPTION (continued)

DYNAMIC VOLTAGE POSITIONING

As described in the power save mode operation sections and as detailed in [Figure 2](#), the output voltage is typically 0.8% above the nominal output voltage at light load currents, as the device is in power save mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. During a load transient from full load to light load, the voltage overshoot is also minimized due to active regulation turning on the N-channel rectifier switch.

SOFT START

The TPS6220x has an internal soft start circuit that limits the inrush current during start-up. This prevents possible voltage drops of the input voltage in case a battery or a high impedance power source is connected to the input of the TPS6220x.

The soft start is implemented as a digital circuit increasing the switch current in steps of typically 60 mA, 120 mA, 240 mA and then the typical switch current limit of 480 mA. Therefore the start-up time mainly depends on the output capacitor and load current. Typical start-up time with 10 μ F output capacitor and 200 mA load current is 800 μ s.

LOW DROPOUT OPERATION 100% DUTY CYCLE

The TPS6220x offers a low input to output voltage difference, while still maintaining operation with the 100% duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation, depending on the load current and output voltage, can be calculated as

$$V_{in_{min}} = V_{out_{max}} + I_{out_{max}} \times (r_{ds(ON)_{max}} + R_L)$$

$I_{out_{max}}$ = maximum output current plus inductor ripple current
 $r_{ds(ON)_{max}}$ = maximum P-channel switch $r_{ds(ON)}$
 R_L = DC resistance of the inductor
 $V_{out_{max}}$ = nominal output voltage plus maximum output voltage tolerance

ENABLE

Pulling the enable low forces the part into shutdown, with a shutdown quiescent current of typically 0.1 μ A. In this mode, the P-channel switch and N-channel rectifier are turned off, the internal resistor feedback divider is disconnected, and the whole device is in shutdown mode. If an output voltage, which could be an external voltage source or super cap, is present during shutdown, the reverse leakage current is specified under electrical characteristics. For proper operation the enable pin must be terminated and must not be left floating.

Pulling the enable high starts up the TPS6220x with the soft start as previously described.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted) ⁽¹⁾

| | UNIT |
|---|------------------------------|
| Supply voltages, V_I ⁽²⁾ | -0.3 V to 7.0 V |
| Voltages on pins SW, EN, FB ⁽²⁾ | -0.3 V to $V_{CC} + 0.3$ V |
| Continuous power dissipation, P_D | See Dissipation Rating Table |
| Operating junction temperature range, T_J | -40°C to 150°C |
| Storage temperature, T_{stg} | -65°C to 150°C |
| Lead temperature (soldering, 10 sec) | 260°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | $R_{\theta JA}$ | $T_A \leq 25^\circ\text{C}$ POWER RATING | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|-----------------|---|--|--|
| DBV | 250°/W | 400 mW | 220 mW | 160 mW |

RECOMMENDED OPERATING CONDITIONS

| | MIN | NOM | MAX | UNIT |
|---|-----|-----|-------|---------------|
| Supply voltage, V_I | 2.5 | | 6.0 | V |
| Output voltage range for adjustable output voltage version, V_O | 0.7 | | V_I | V |
| Output current, I_O | | | 300 | mA |
| Inductor, L ⁽¹⁾ | 4.7 | 10 | | μH |
| Input capacitor, C_I ⁽¹⁾ | | 4.7 | | μF |
| Output capacitor, C_O ⁽¹⁾ | | 10 | | μF |
| Operating ambient temperature, T_A | 40 | | 85 | °C |
| Operating junction temperature, T_J | 40 | | 125 | °C |

(1) See the application section for further information.

ELECTRICAL CHARACTERISTICS

$V_I = 3.6$ V, $V_O = 1.8$ V, $I_O = 200$ mA, EN = VIN, $T_A = -40^\circ\text{C}$ to 85°C , typical values are at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------|---------------------------------------|-----|------|-----|------------------|
| SUPPLY CURRENT | | | | | | |
| V_I | Input voltage range | | 2.5 | | 6.0 | V |
| I_Q | Operating quiescent current | $I_O = 0$ mA, Device is not switching | | 15 | 30 | μA |
| | Shutdown supply current | EN = GND | | 0.1 | 1 | μA |
| | Undervoltage lockout threshold | | 1.5 | | 2.0 | V |
| ENABLE | | | | | | |
| $V_{I(EN)}$ | EN high level input voltage | | 1.3 | | | V |
| | EN low level input voltage | | | | 0.4 | V |
| $I_{I(EN)}$ | EN input bias current | EN = GND or VIN | | 0.01 | 0.1 | μA |
| POWER SWITCH | | | | | | |
| $r_{ds(ON)}$ | P-channel MOSFET on-resistance | $V_{IN} = V_{GS} = 3.6$ V | | 530 | 690 | $\text{m}\Omega$ |
| | | $V_{IN} = V_{GS} = 2.5$ V | | 670 | 850 | |
| | N-channel MOSFET on-resistance | $V_{IN} = V_{GS} = 3.6$ V | | 430 | 540 | $\text{m}\Omega$ |
| | | $V_{IN} = V_{GS} = 2.5$ V | | 530 | 660 | |
| $I_{lkg(P)}$ | P-channel leakage current | $V_{DS} = 6.0$ V | | 0.1 | 1 | μA |

ELECTRICAL CHARACTERISTICS (continued)

$V_I = 3.6\text{ V}$, $V_O = 1.8\text{ V}$, $I_O = 200\text{ mA}$, $EN = VIN$, $T_A = -40^\circ\text{C}$ to 85°C , typical values are at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------------------|--|--|--------|----------|---------------|
| $I_{IKG(N)}$ | N-channel leakage current | $V_{DS} = 6.0\text{ V}$ | | 0.1 | 1 | μA |
| $I_{(LIM)}$ | P-channel current limit | $2.5\text{ V} < V_{in} < 6.0\text{ V}$ | 380 | 480 | 670 | mA |
| OSCILLATOR | | | | | | |
| f_S | Switching frequency | | 650 | 1000 | 1500 | kHz |
| OUTPUT | | | | | | |
| V_O | Adjustable output voltage range | TPS62200 | 0.7 | | V_{IN} | V |
| V_{ref} | Reference voltage | | | 0.5 | | V |
| | Feedback voltage ⁽¹⁾ | TPS62200 | $V_I = 3.6\text{ V}$ to 6.0 V , $I_O = 0\text{ mA}$ | | 0% | 3% |
| | | Adjustable | $V_I = 3.6\text{ V}$ to 6.0 V , $0\text{ mA} \leq I_O \leq 300\text{ mA}$ | | -3% | 3% |
| V_O | Fixed output voltage ⁽¹⁾ | TPS62207 | $V_I = 2.5\text{ V}$ to 6.0 V , $I_O = 0\text{ mA}$ | | 0% | 3% |
| | | 1.2 V | $V_I = 2.5\text{ V}$ to 6.0 V , $0\text{ mA} \leq I_O \leq 300\text{ mA}$ | | -3% | 3% |
| | | TPS62201 | $V_I = 2.5\text{ V}$ to 6.0 V , $I_O = 0\text{ mA}$ | | 0% | 3% |
| | | 1.5 V | $V_I = 2.5\text{ V}$ to 6.0 V , $0\text{ mA} \leq I_O \leq 300\text{ mA}$ | | -3% | 3% |
| | | TPS62204 | $V_I = 2.5\text{ V}$ to 6.0 V , $I_O = 0\text{ mA}$ | | 0% | 3% |
| | | 1.6 V | $V_I = 2.5\text{ V}$ to 6.0 V , $0\text{ mA} \leq I_O \leq 300\text{ mA}$ | | -3% | 3% |
| | | TPS62202 | $V_I = 2.5\text{ V}$ to 6.0 V , $I_O = 0\text{ mA}$ | | 0% | 3% |
| | | 1.8 V | $V_I = 2.5\text{ V}$ to 6.0 V , $0\text{ mA} \leq I_O \leq 300\text{ mA}$ | | -3% | 3% |
| | | TPS62208 | $V_I = 2.5\text{ V}$ to 6.0 V , $I_O = 0\text{ mA}$ | | 0% | 3% |
| | | 1.875 V | $V_I = 2.5\text{ V}$ to 6.0 V , $0\text{ mA} \leq I_O \leq 300\text{ mA}$ | | -3% | 3% |
| | | TPS62205 | $V_I = 2.7\text{ V}$ to 6.0 V , $I_O = 0\text{ mA}$ | | 0% | 3% |
| | | 2.5 V | $V_I = 2.7\text{ V}$ to 6.0 V , $0\text{ mA} \leq I_O \leq 300\text{ mA}$ | | -3% | 3% |
| | | TPS62203 | $V_I = 3.6\text{ V}$ to 6.0 V , $I_O = 0\text{ mA}$ | | 0% | 3% |
| | | 3.3 V | $V_I = 3.6\text{ V}$ to 6.0 V , $0\text{ mA} \leq I_O \leq 300\text{ mA}$ | | -3% | 3% |
| Line regulation | | $V_I = 2.5\text{ V}$ to 6.0 V , $I_O = 10\text{ mA}$ | | 0.26 | | %/V |
| Load regulation | | $I_O = 100\text{ mA}$ to 300 mA | | 0.0014 | | %/mA |
| I_{IKG} | Leakage current into SW pin | $V_{in} > V_{out}$, $0\text{ V} \leq V_{sw} \leq V_{in}$ | | 0.1 | 1 | μA |
| $I_{IKG(Rev)}$ | Reverse leakage current into pin SW | $V_{in} = \text{open}$, $EN = \text{GND}$, $V_{SW} = 6.0\text{ V}$ | | 0.1 | 1 | μA |

(1) For output voltages $\leq 1.2\text{ V}$ a $22\text{ }\mu\text{F}$ output capacitor value is required to achieve a maximum output voltage accuracy of 3% while operating in power save mode (PFM mode)

TYPICAL CHARACTERISTICS

Table of Graphs

| | | | FIGURES |
|--------------|---|-------------------|---------|
| η | Efficiency | vs Load current | 3,4,5 |
| | | vs Input voltage | 6 |
| I_Q | No load quiescent current | vs Input voltage | 7 |
| f_s | Switching frequency | vs Temperature | 8 |
| V_o | Output voltage | vs Output current | 9 |
| $r_{ds(on)}$ | $r_{ds(on)}$ - P-channel switch, | vs Input voltage | 10 |
| | $r_{ds(on)}$ - N-Channel rectifier switch | vs Input voltage | 11 |
| | Line transient response | | 12 |
| | Load transient response | | 13 |
| | Power save mode operation | | 14 |
| | Start-up | | 15 |

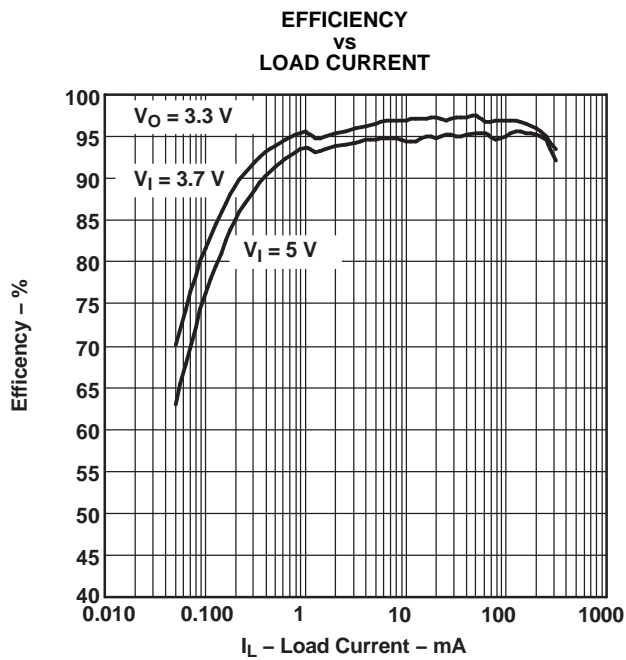


Figure 3.

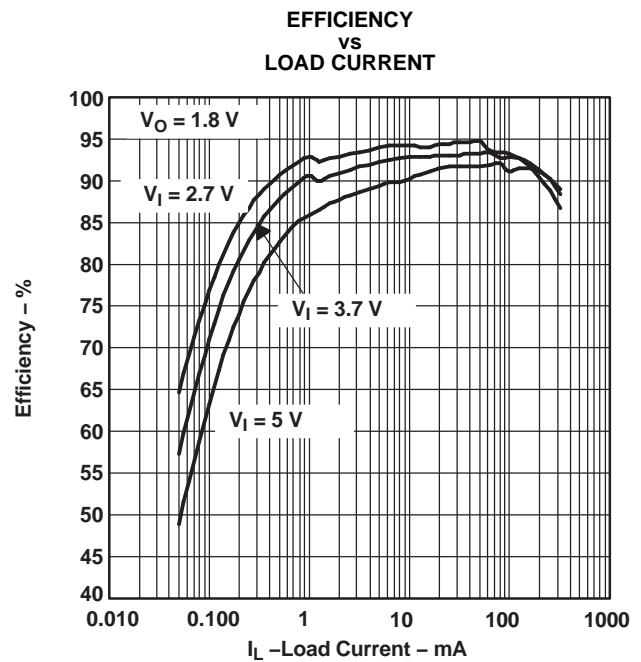


Figure 4.

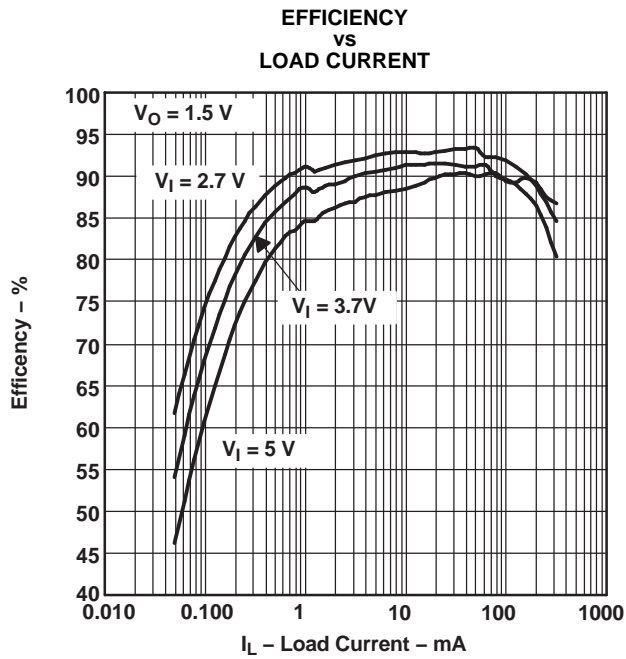


Figure 5.

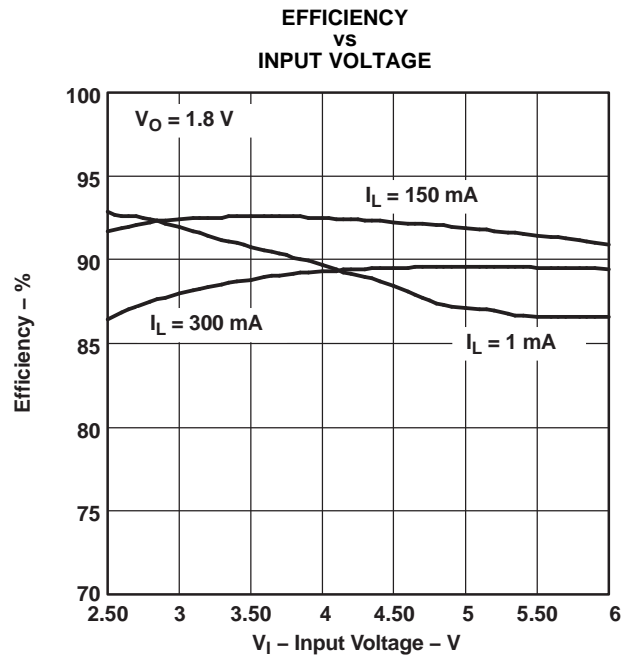


Figure 6.

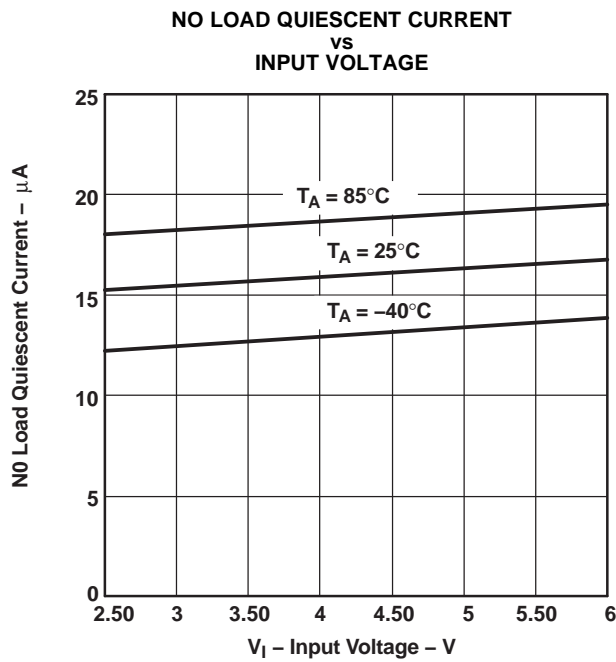


Figure 7.

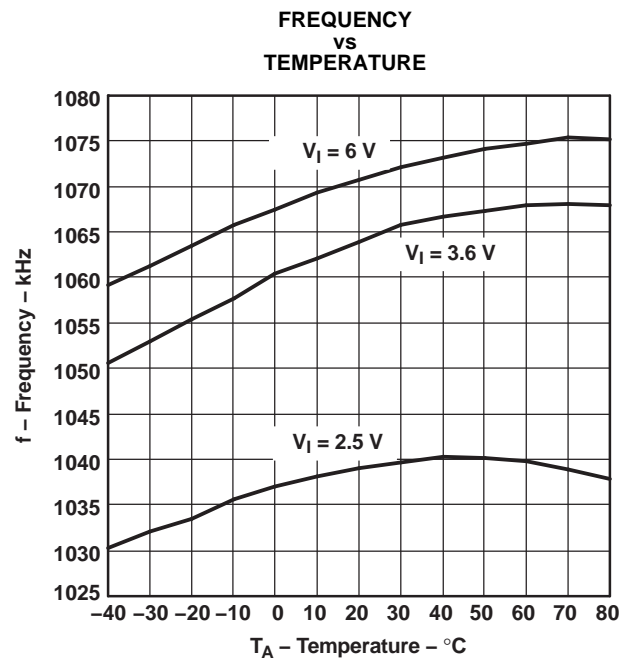


Figure 8.

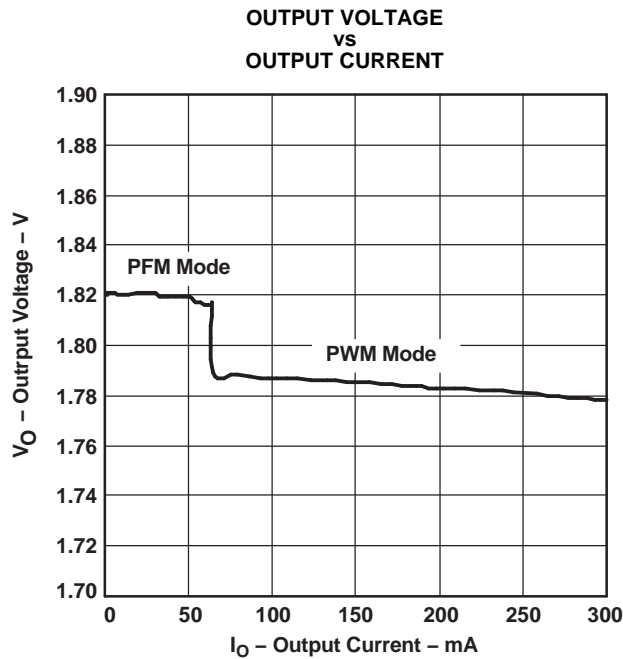


Figure 9.

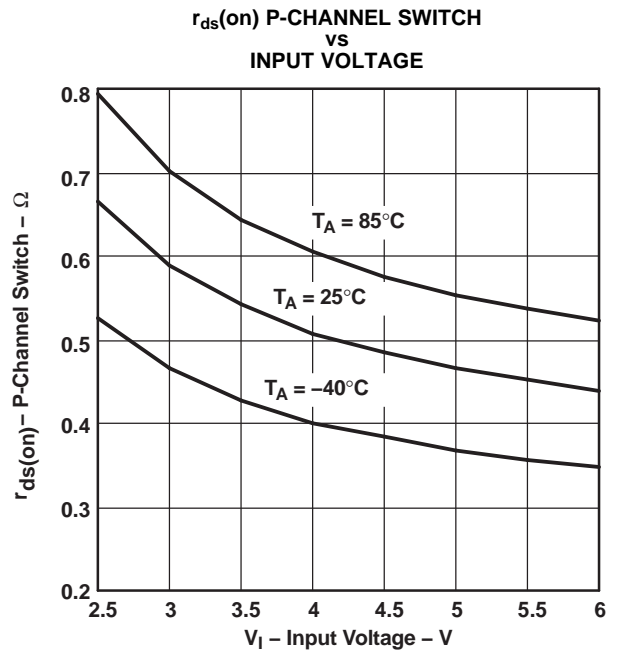


Figure 10.

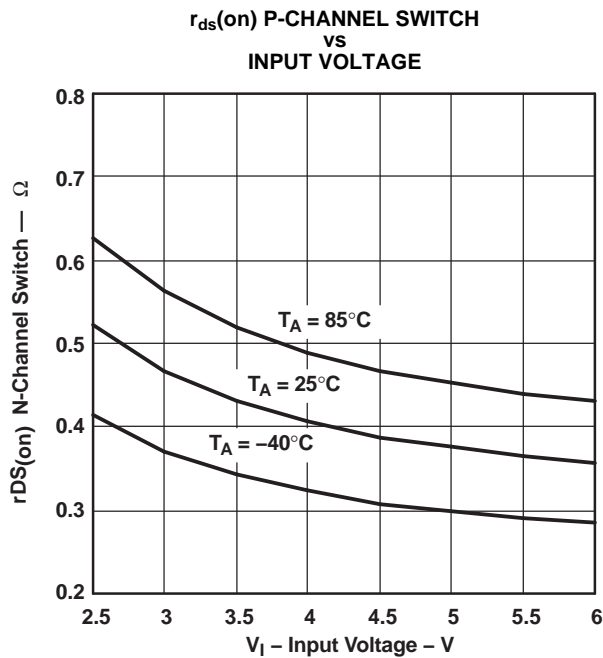


Figure 11.

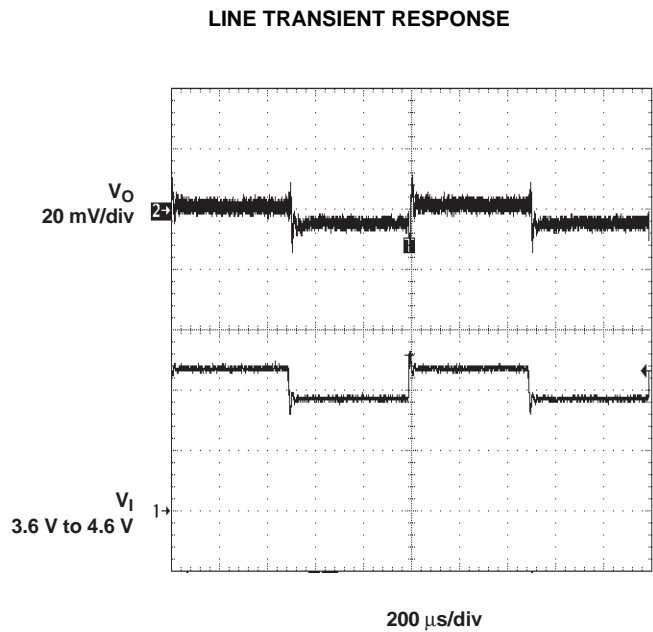


Figure 12.

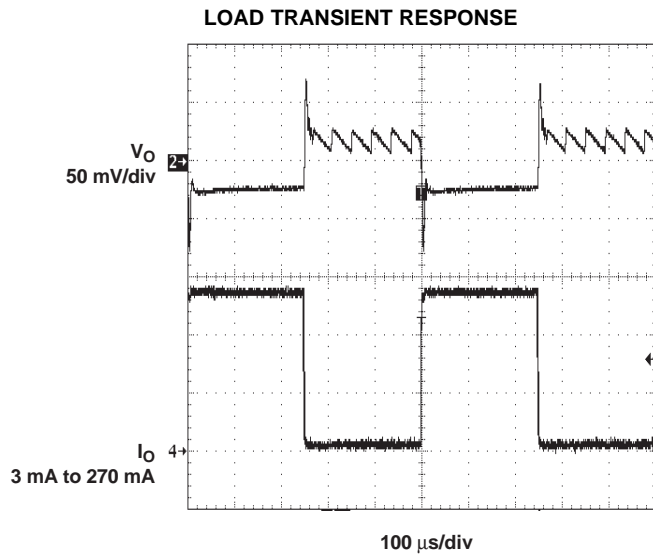


Figure 13.

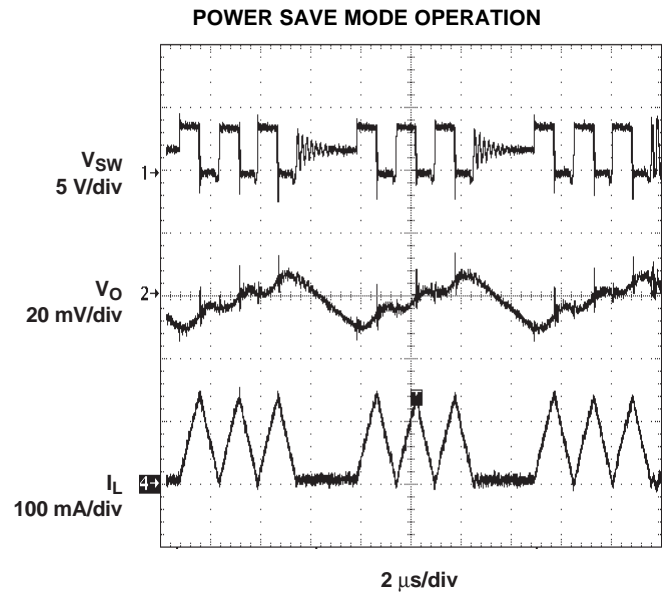


Figure 14.

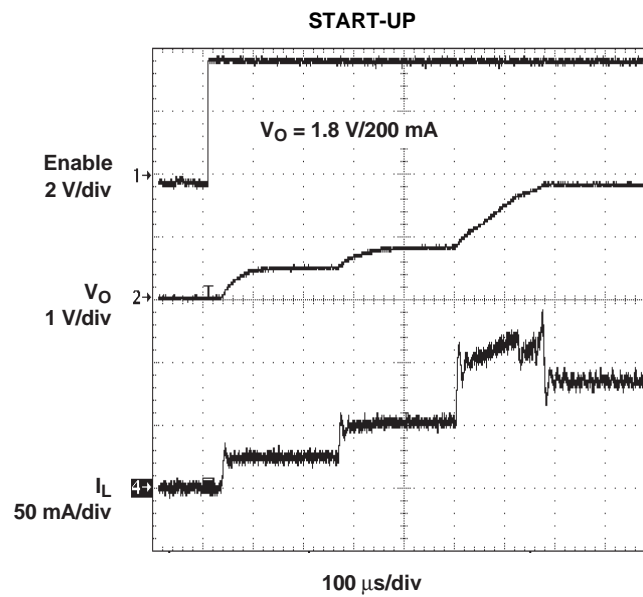


Figure 15.

APPLICATION INFORMATION

ADJUSTABLE OUTPUT VOLTAGE VERSION

When the adjustable output voltage version TPS62200 is used, the output voltage is set by the external resistor divider. See [Figure 16](#).

The output voltage is calculated as

$$V_{\text{out}} = 0.5 \text{ V} \times \left(1 + \frac{R1}{R2} \right)$$

- $R1 + R2 \leq 1 \text{ M}\Omega$ and internal reference voltage $V(\text{ref})_{\text{typ}} = 0.5 \text{ V}$

$R1 + R2$ should not be greater than $1 \text{ M}\Omega$ for reasons of stability. To keep the operating quiescent current to a minimum, the feedback resistor divider should have high impedance with $R1+R2 \leq 1 \text{ M}\Omega$. Because of the high impedance and the low reference voltage of $V_{\text{ref}} = 0.5 \text{ V}$, the noise on the feedback pin (FB) needs to be minimized. Using a capacitive divider $C1$ and $C2$ across the feedback resistors minimizes the noise at the feedback without degrading the line or load transient performance.

$C1$ and $C2$ should be selected as

$$C1 = \frac{1}{2 \times \pi \times 10 \text{ kHz} \times R1}$$

- $R1$ = upper resistor of voltage divider
- $C1$ = upper capacitor of voltage divider

For $C1$ a value should be chosen that comes closest to the calculated result.

$$C2 = \frac{R1}{R2} \times C1$$

- $R2$ = lower resistor of voltage divider
- $C2$ = lower capacitor of voltage divider

For $C2$ the selected capacitor value should always be selected larger than the calculated result. For example, in [Figure 16](#) for $C2$, 100 pF are selected for a calculated result of $C2 = 86.17 \text{ pF}$.

If quiescent current is not a key design parameter, $C1$ and $C2$ can be omitted, and a low-impedance feedback divider must be used with $R1+R2 < 100 \text{ k}\Omega$. This design reduces the noise available on the feedback pin (FB) as well, but increases the overall quiescent current during operation.

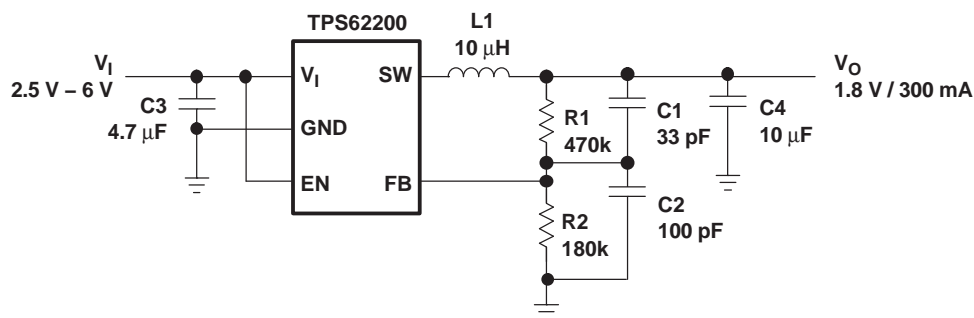


Figure 16. Typical Application Circuit for the Adjustable Output Voltage

INDUCTOR SELECTION

The TPS6220x device is optimized to operate with a typical inductor value of $10 \mu\text{H}$.

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Although the inductor core material has less effect on efficiency than its dc resistance, an appropriate inductor core material must be used.

APPLICATION INFORMATION (continued)

The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current, and the lower the conduction losses of the converter. On the other hand, larger inductor values cause a slower load transient response. Usually the inductor ripple current, as calculated below, is around 20% of the average output current.

In order to avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current that is calculated as

$$\Delta I_L = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \quad I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

f = switching frequency (1 MHz typical, 650 kHz minimal)

L = inductor value

ΔI_L = peak-to-peak inductor ripple current

I_{Lmax} = maximum inductor current

The highest inductor current occurs at maximum V_{in} .

A more conservative approach is to select the inductor current rating just for the maximum switch current of 670 mA. Refer to [Table 1](#) for inductor recommendations.

Table 1. Recommended Inductors

| INDUCTOR VALUE | COMPONENT SUPPLIER | COMMENTS |
|----------------|----------------------|-------------------|
| 10 μ H | Sumida CDRH5D28-100 | High efficiency |
| 10 μ H | Sumida CDRH5D18-100 | |
| 10 μ H | Sumida CDRH4D28-100 | |
| 10 μ H | Coilcraft DO1608-103 | |
| 6.8 μ H | Sumida CDRH3D16-6R8 | Smallest solution |
| 10 μ H | Sumida CDRH4D18-100 | |
| 10 μ H | Sumida CR32-100 | |
| 10 μ H | Sumida CR43-100 | |
| 10 μ H | Murata LQH4C100K04 | |

INPUT CAPACITOR SELECTION

Because the buck converter has a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. Also the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 4.7 μ F input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements.

Ceramic capacitors show a good performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors.

Place the input capacitor as close as possible to the input pin of the device for best performance (refer to [Table 2](#) for recommended components).

OUTPUT CAPACITOR SELECTION

The advanced fast response voltage mode control scheme of the TPS6220x allows the use of tiny ceramic capacitors with a value of 10 μ F without having large output voltage under and overshoots during heavy load transients.

Ceramic capacitors with low ESR values have the lowest output voltage ripple and are therefore recommended. If required, tantalum capacitors may be used as well (refer to [Table 2](#) for recommended components).

At nominal load current the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{out} = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \times \left(\frac{1}{8 \times C_{out} \times f} + ESR \right)$$

where the highest output voltage ripple occurs at the highest input voltage V_{in} .

At light load currents, the device operates in power save mode, and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds. The typical output voltage ripple is 1% of the output voltage V_o .

Table 2. Recommended Capacitors

| CAPACITOR VALUE | CASE SIZE | COMPONENT SUPPLIER | COMMENTS |
|-----------------|-----------|--|--------------------|
| 4.7 μ F | 0805 | Taiyo Yuden JMK212BY475MG | Ceramic |
| 10 μ F | 0805 | Taiyo Yuden JMK212BJ106MG TDK C12012X5ROJ106K | Ceramic Ceramic |
| 10 μ F | 1206 | Taiyo Yuden JMK316BJ106KL TDK C3216X5ROJ106M | Ceramic |
| 22 μ F | 1210 | Taiyo Yuden JMK325BJ226MM | Ceramic |

LAYOUT CONSIDERATIONS

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator shows stability problems as well as EMI problems.

Therefore use wide and short traces for the main current paths, as indicated in bold in [Figure 17](#). The input capacitor, as well as the inductor and output capacitor, should be placed as close as possible to the IC pins

The feedback resistor network must be routed away from the inductor and switch node to minimize noise and magnetic interference. To further minimize noise from coupling into the feedback network and feedback pin, the ground plane or ground traces must be used for shielding. This becomes very important especially at high switching frequencies of 1 MHz.

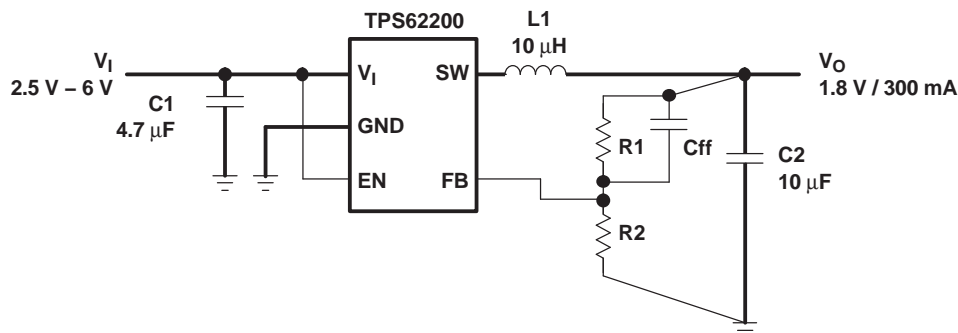


Figure 17. Layout Diagram

TYPICAL APPLICATIONS

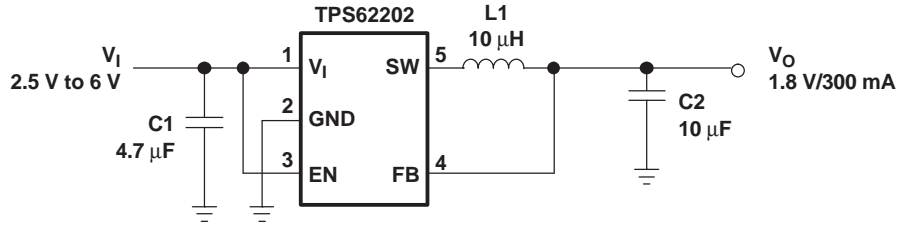


Figure 18. Li-Ion to 1.8 V Fixed Output Voltage Version

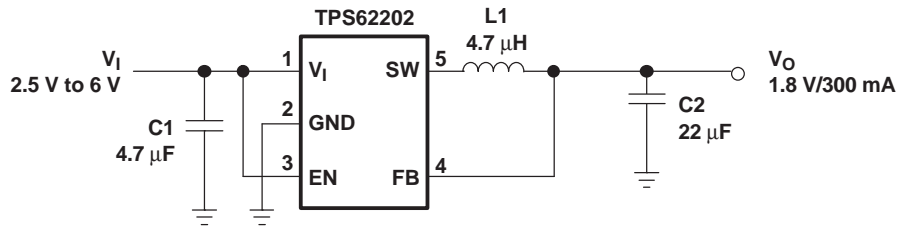


Figure 19. 1.8 V Fixed Output Voltage version Using 4.7 μH Inductor

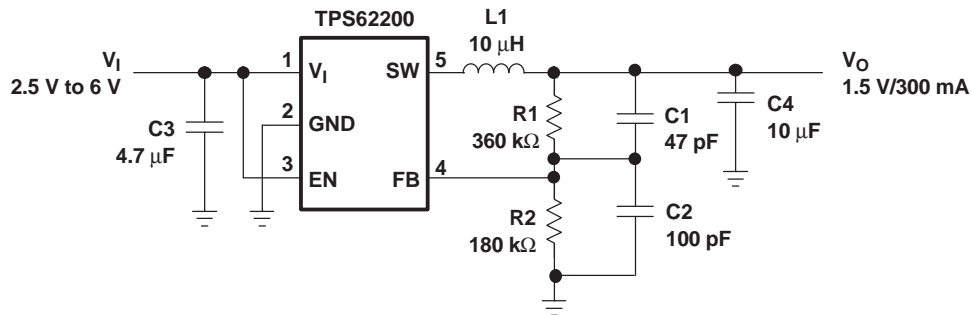


Figure 20. Adjustable Output Voltage Version Set to 1.5 V

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| TPS62200DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHKI | Samples |
| TPS62200DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHKI | Samples |
| TPS62200DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHKI | Samples |
| TPS62200DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHKI | Samples |
| TPS62201DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHLI | Samples |
| TPS62201DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHLI | Samples |
| TPS62201DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHLI | Samples |
| TPS62201DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHLI | Samples |
| TPS62202DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHMI | Samples |
| TPS62202DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHMI | Samples |
| TPS62202DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHMI | Samples |
| TPS62202DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHMI | Samples |
| TPS62203DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHNI | Samples |
| TPS62203DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHNI | Samples |
| TPS62203DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHNI | Samples |
| TPS62203DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHNI | Samples |
| TPS62204DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHSI | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| TPS62204DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHSI | Samples |
| TPS62204DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHSI | Samples |
| TPS62204DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHSI | Samples |
| TPS62205DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHTI | Samples |
| TPS62205DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHTI | Samples |
| TPS62205DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHTI | Samples |
| TPS62205DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHTI | Samples |
| TPS62207DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PJGI | Samples |
| TPS62207DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PJGI | Samples |
| TPS62207DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PJGI | Samples |
| TPS62207DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PJGI | Samples |
| TPS62208DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALW | Samples |
| TPS62208DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALW | Samples |
| TPS62208DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALW | Samples |
| TPS62208DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALW | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION



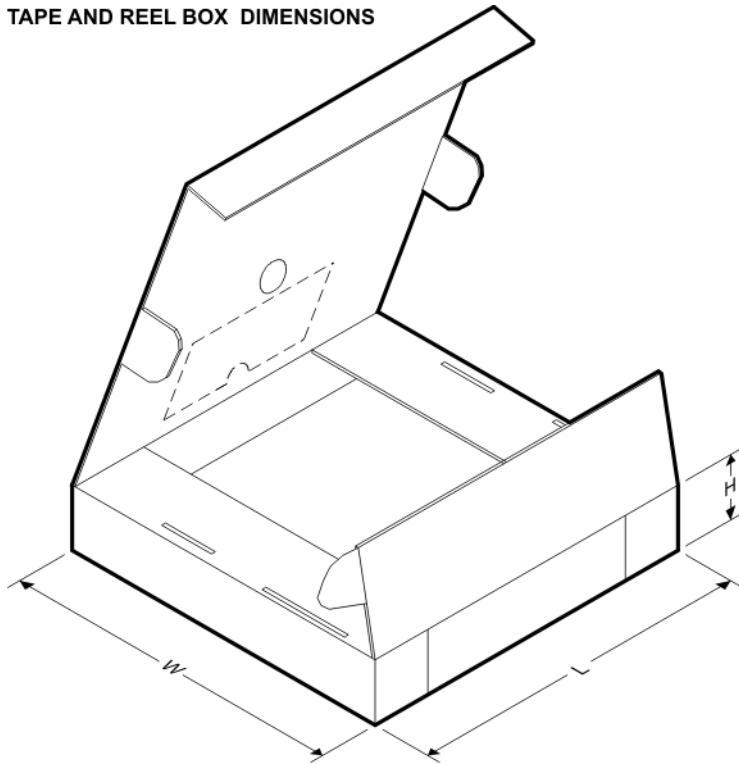
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS62200DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS62200DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS62201DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS62201DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS62202DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS62202DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS62203DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS62203DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS62204DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS62204DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS62205DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS62205DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS62207DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS62207DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS62208DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS62208DBVR | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS62208DBVT | SOT-23 | DBV | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS62208DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

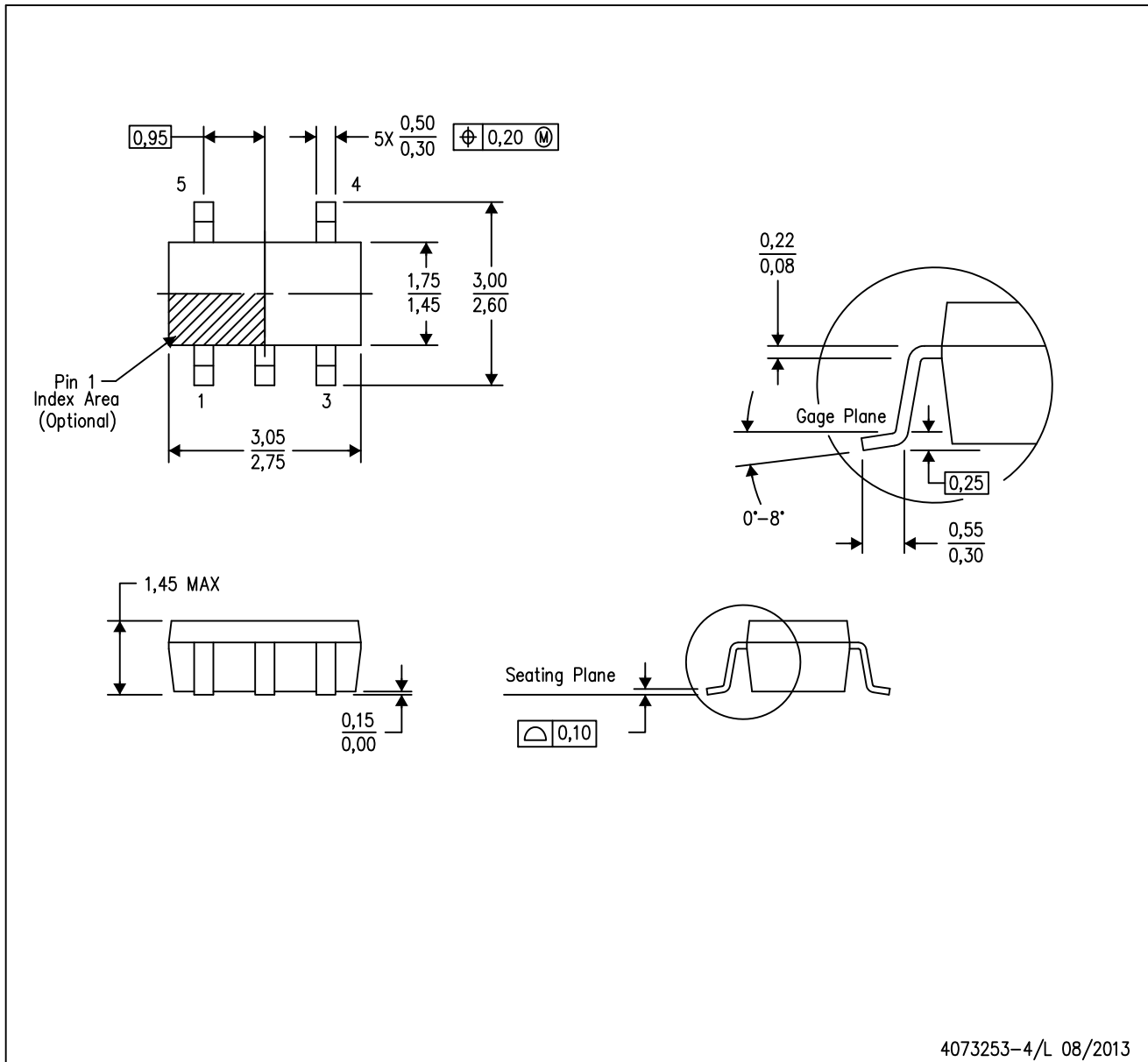
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS62200DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS62200DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS62201DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS62201DBVR | SOT-23 | DBV | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS62201DBVT | SOT-23 | DBV | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TPS62201DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS62202DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS62202DBVR | SOT-23 | DBV | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS62202DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS62203DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS62203DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS62204DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS62204DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS62205DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS62205DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS62207DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS62207DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS62208DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS62208DBVR | SOT-23 | DBV | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS62208DBVT | SOT-23 | DBV | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TPS62208DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |

MECHANICAL DATA

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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